```
1   // Eugene Ngo
2   // 5/3/23
3   // EE 469
4   // Lab 3
5
6   // alu_testbench tests a variety of different inputs and ouputs
7   // pulled from the alu.tv file.
8   module alu_testbench();
9      logic [31:0] a, b;
10     logic [1:0]  ALUControl;
11     logic [31:0] Result;
12     logic [3:0]  ALUFlags;
13     logic clk;
14     logic [103:0] testvectors [1000:0];
15
16     alu dut (.a,.b,.ALUControl,.Result,.ALUFlags);
17
18     parameter CLOCK_PERIOD=100;
19
20     initial clk = 1;
21     always begin
22        #(CLOCK_PERIOD/2);
23        clk <= ~clk;
24     end
25
26
27     initial begin
28        $readmemh("alu.tv", testvectors);
29        for (int i = 0; i < 20; i = i + 1) begin
30           {ALUControl,a,b,Result,ALUFlags} = testvectors[i]; @(posedge clk);
31        end
32     end
33  endmodule
```