```
1   // Eugene Ngo
2   // 4/7/2023
3   // CSE 469
4   // Lab 1 Task 3
5
6   // alu_testbench tests all expected, unexpected, and edgecase behaviors
7   module alu_testbench();
8      logic [31:0] a,b;
9      logic [1:0] ALUControl;
10     logic [31:0] Result;
11     logic [3:0] ALUFlags;
12     logic clk;
13     logic [103:0] testvectors [1000:0];
14
15     alu dut (.a(a), .b(b), .ALUControl(ALUControl), .Result(Result),
16              .ALUFlags(ALUFlags));
17
18     parameter CLOCK_PERIOD = 100;
19
20     initial clk = 1;
21
22     always begin
23           #(CLOCK_PERIOD/2);
24           clk = ~clk;
25     end
26
27     initial begin
28        $readmemh("alu.tv", testvectors);
29
30        for (int i = 0; i < 20; i = i + 1) begin
31           {ALUControl, a, b, Result, ALUFlags} = testvectors[i];
32           @(posedge clk);
33        end // end loop
34     end // end initial
35  endmodule
```