

Domain Specific Languages and Requirements (Engineering)



itemis

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What are Requirements?



... a requirement is a singular documented need of what a particular product or service should be or perform.

Wikipedia

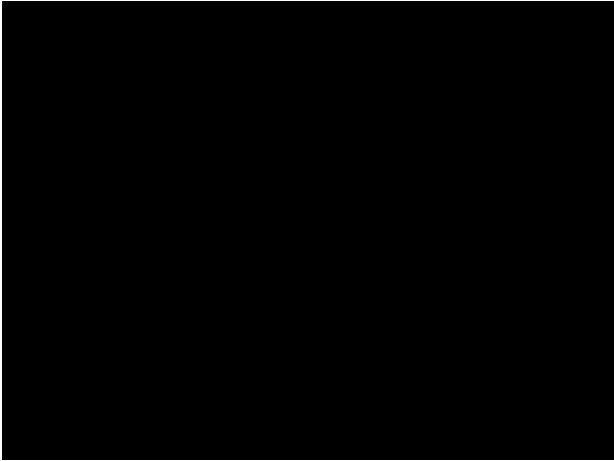
... specifies a verifiable constraint on an implementation that it shall undeniably meet or


- (a) be deemed unacceptable, or
- (b) result in implementation failure, or
- (c) result in system failure.

Wiktionary

... what a system should do, and with which quality attributes, without presupposing a specific implementation.

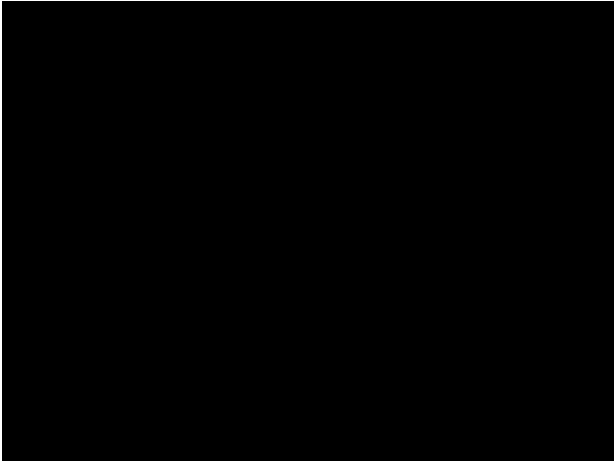
Mine.





Cohesive
Complete
Consistent
Atomic
Traceable
Current
Feasible
Unambiguous
Mandatory
Verifiable

Wikipedia



Brain [Domain Person]

Prose

Brain [Developer]

Code




Brain [Domain Person]

Prose

Brain [Developer]

Code



Brain [Domain Person]


-----lossy

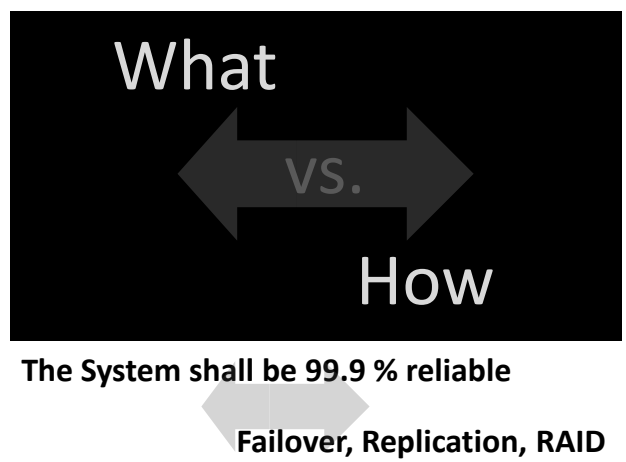
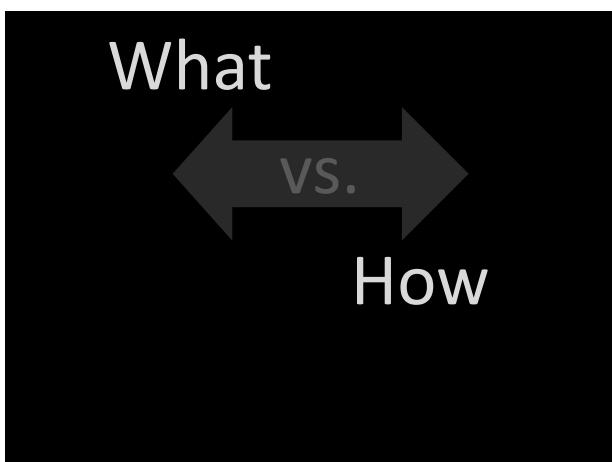
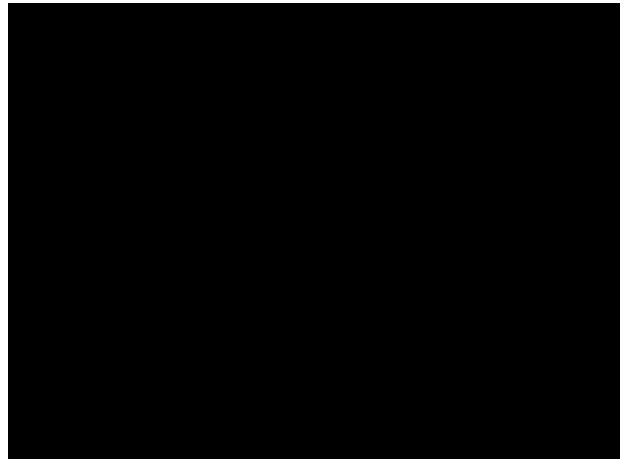
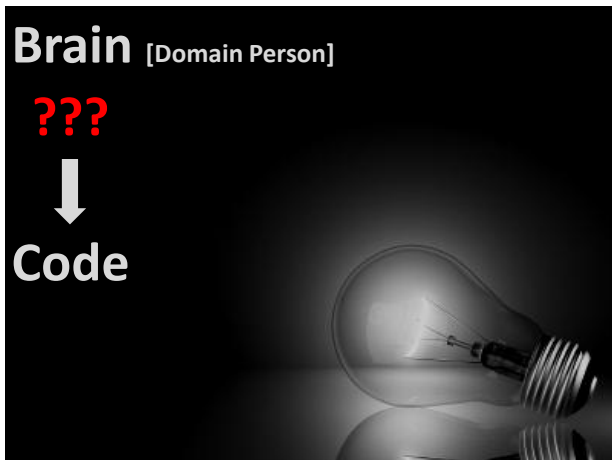
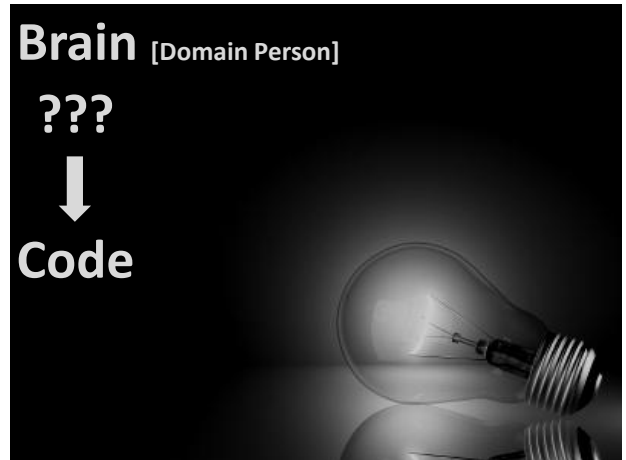
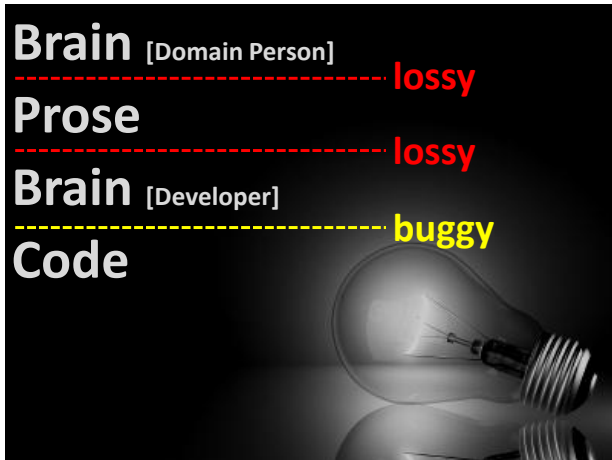
Prose

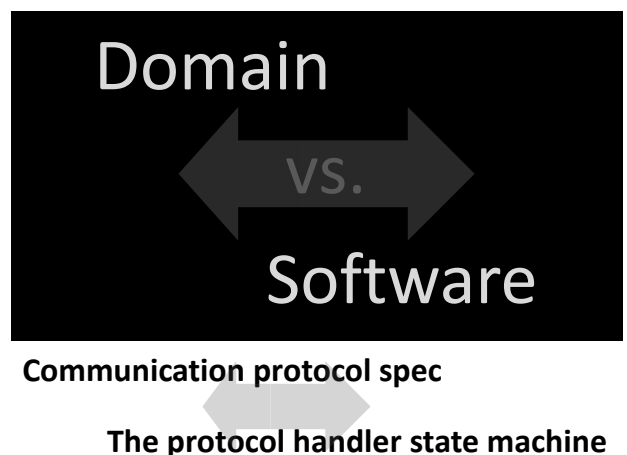
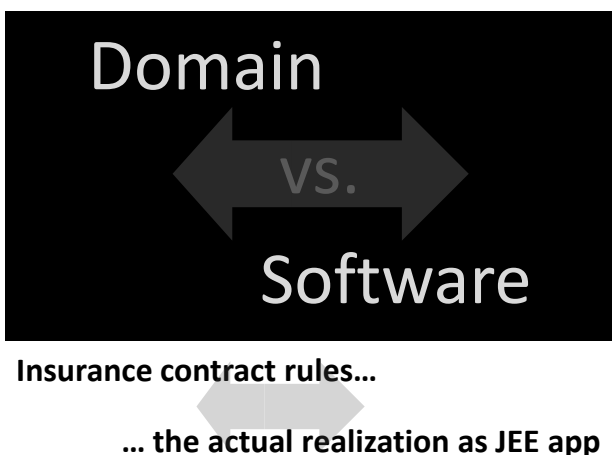
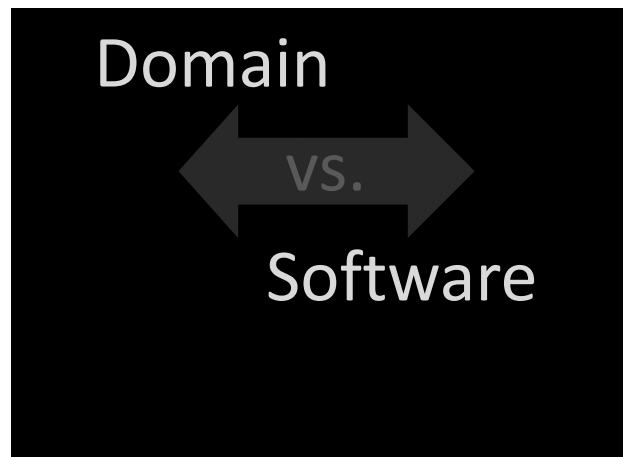
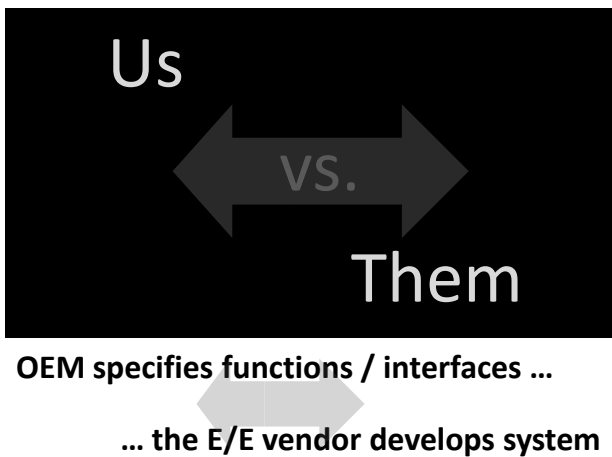
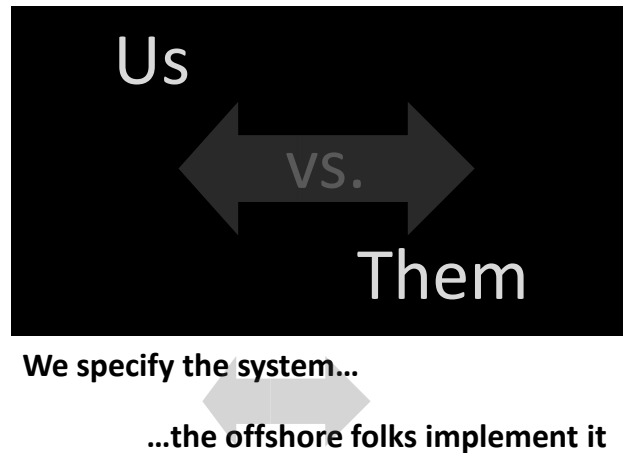
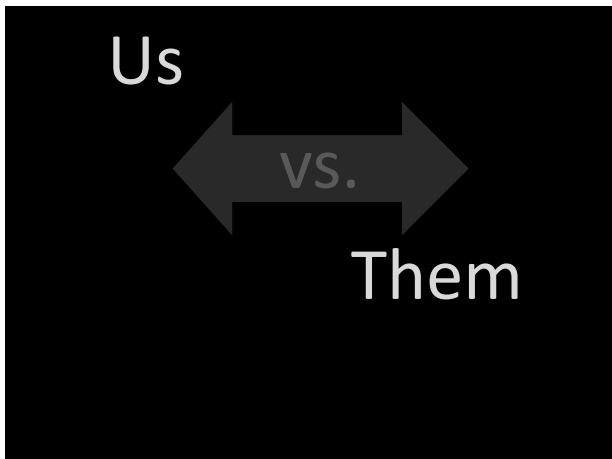
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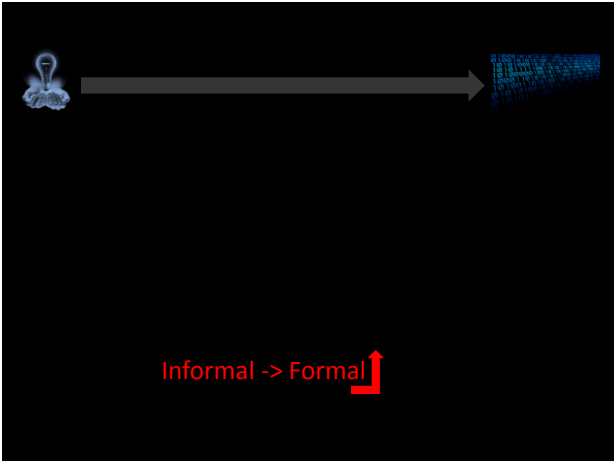
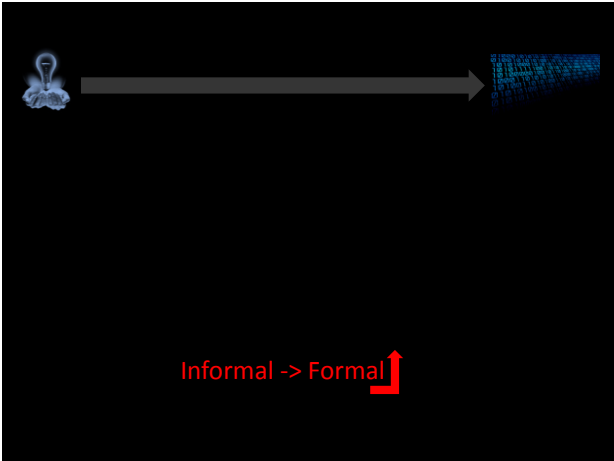
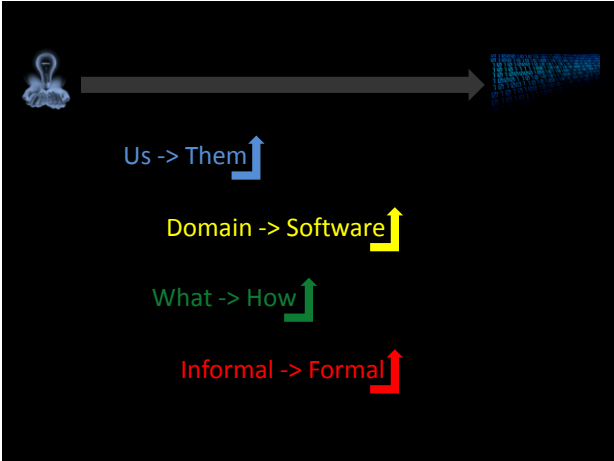
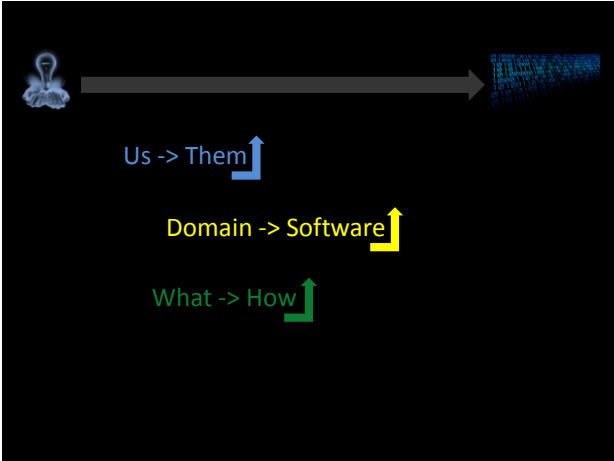
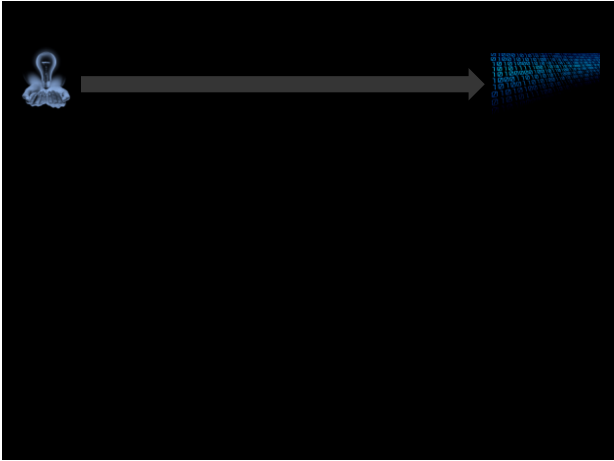
Brain [Developer]

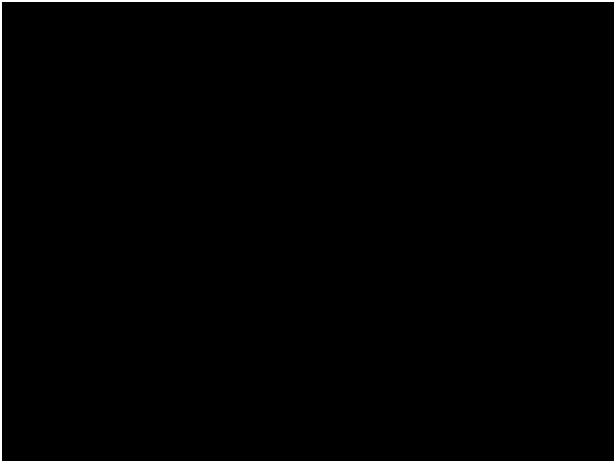
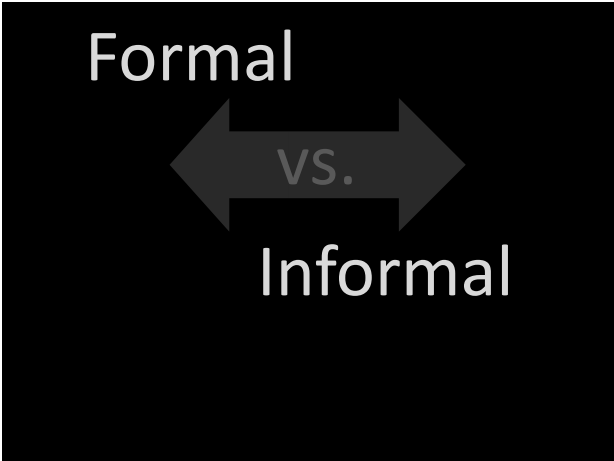
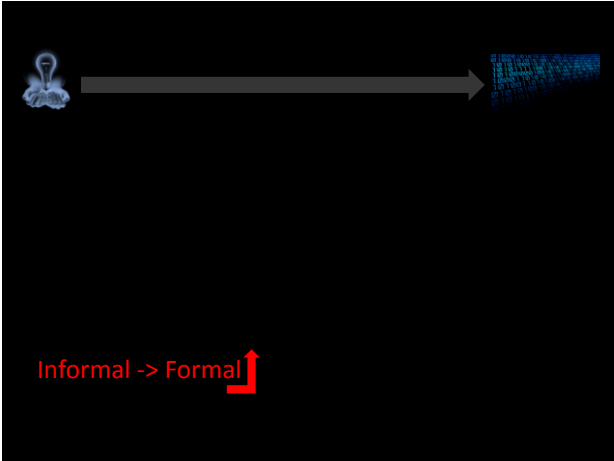
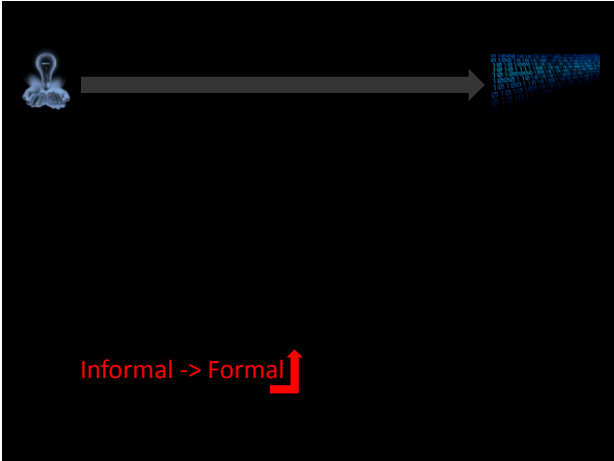
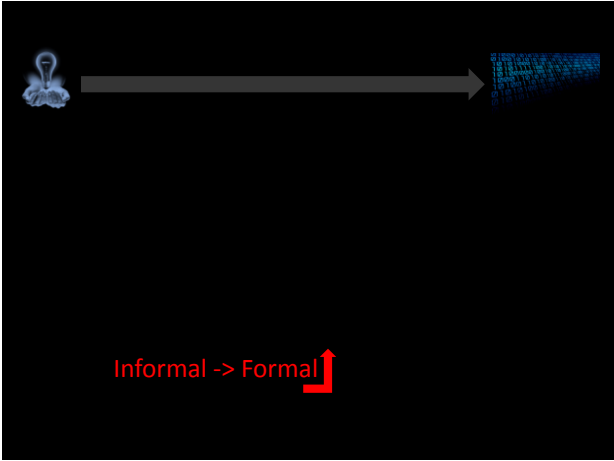
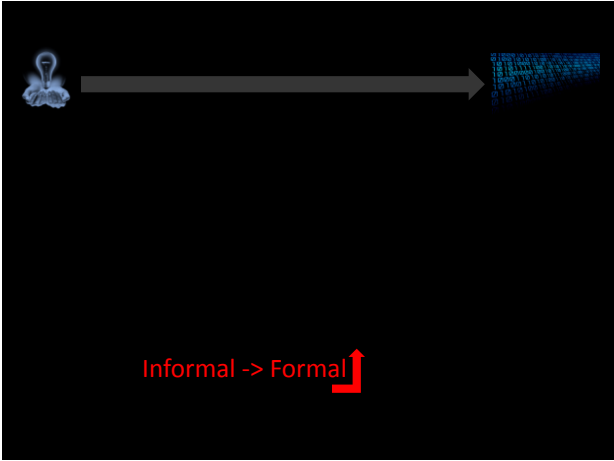
Code











Formal Requirements & Design



FORMAL

processable
by
tools

Cohesive
Complete
Consistent
Atomic
Traceable
Current
Feasible
Unambiguous
Mandatory
Verifiable

processable
by
tools

Cohesive
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processable
by
tools

→ implementation



Domain -> Software ↑

What -> How ↑

Informal -> Formal ↑

Requirements & Design

What
Requirements

Iteration 1

Requirements & Design

What
Requirements

Iteration 1

How
Design

Iteration 1

Requirements & Design

What
Requirements

Iteration 1

Iteration 2

How
Design

Iteration 1

Iteration 2

Level of Detail

Requirements & Design

What
Requirements

Iteration 1

Iteration 2

Iteration 3

How
Design

Iteration 1

Iteration 2

Iteration 3

Level of Detail

Requirements & Design

What
Requirements

Iteration 1

Iteration 2

Iteration 3

How
Design

Iteration 1

Iteration 2

Iteration 3

What -> How

Requirements & Design

What
Requirements

Iteration 1

Iteration 2

Iteration 3

How
Design

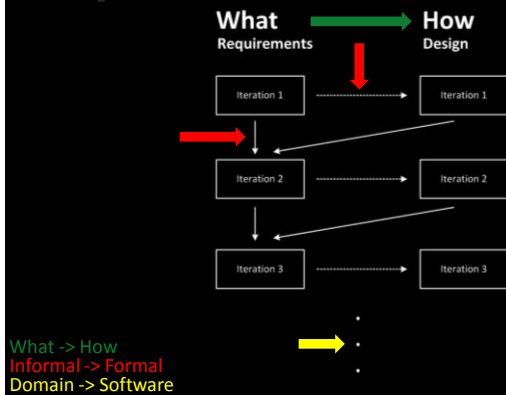
Iteration 1

Iteration 2

Iteration 3

What -> How
Informal -> Formal

Requirements & Design



Formal requirements specify **what** a system should do from a **domain** perspective, and with which quality attributes, without presupposing a specific software implementation, but **processable by tools**.

Mine++

Requirement/Informal:

It shall not be possible to get radiated when operating a microwave.

Requirement/Informal:

It shall not be possible to get radiated when operating a microwave.

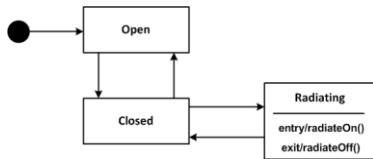
Design/Informal:

The radiator may only work iff the door of the microwave is closed.

- + door isolation
- + some quality requirements

Requirement/Informal:

It shall not be possible to get radiated when operating a microwave.

Design/Formal:

Domain Specific Languages

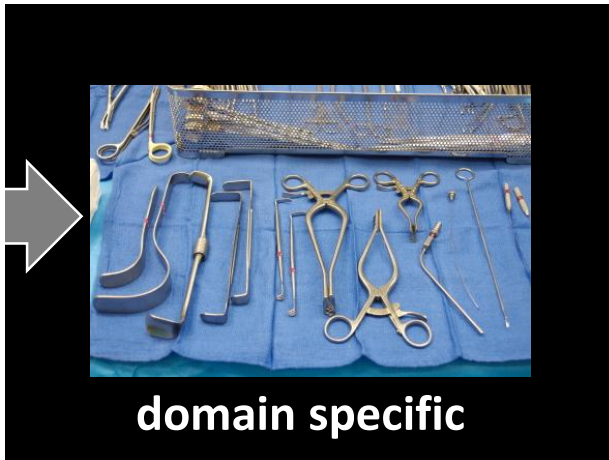


DSL

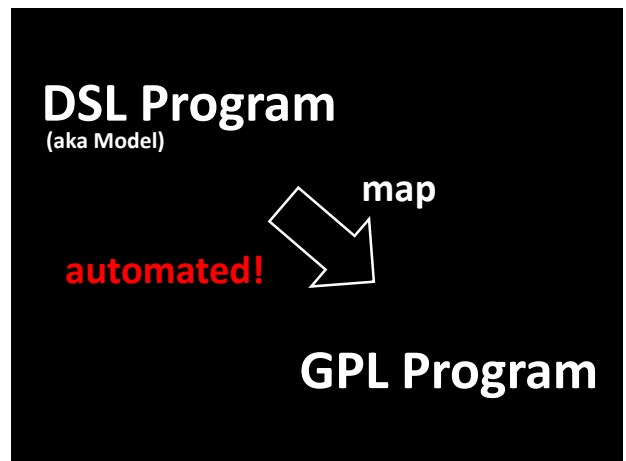
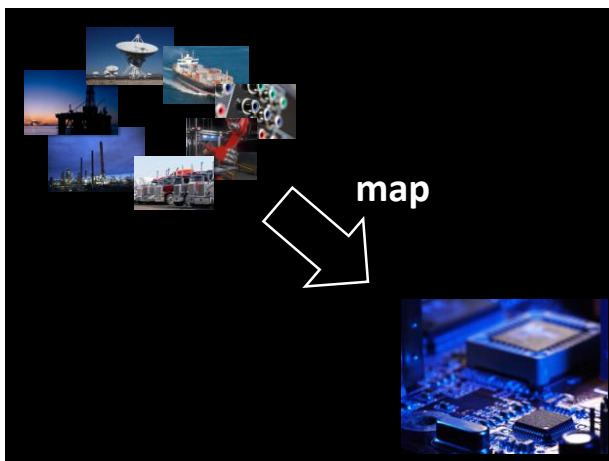
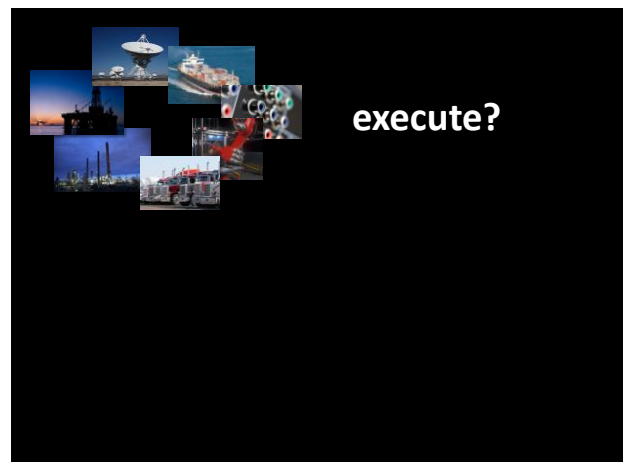
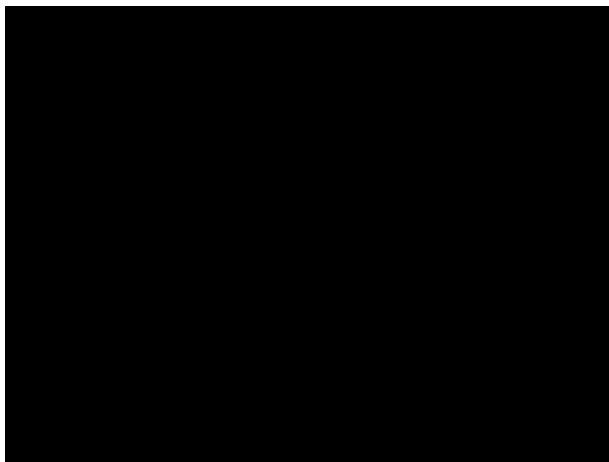
A DSL is a **focussed, processable language** for describing a specific **concern** when building a system in a specific **domain**. The **abstractions** and **notations** used are natural/suitable for the **stakeholders** who specify that particular concern.

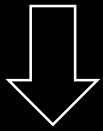


general purpose



tailor made
effective++
specialized, limited
used by experts
together with other
specialized tools





map

Generation

Transformation
Compilation

Interpretation

Example 1:

Embedded Protocol Handler



Factory Control System
Plug-in Cards
Componentized System

CONTEXT

PROBLEM

Cards have to communicate via predefined protocol

Protocol only specified as „plain text and pictures“

Verification tough, no automatic processing

Define DSL for describing the protocol, formally define protocol with it

Generate Handler

Express test cases

SOLUTION

Component Specification

```
processing DigitalIn "DI" moduleType OxD8 hal = DigitalInHAL (
  datatypes (
    SinglePointIndicationWithoutTime;
    SinglePointIndicationWithTime;
    DoublePointIndicationWithoutTime;
    DoublePointIndicationWithTime;
    BitStringType10BitWithoutTime;
    BitStringType10BitWithTime;
  )
)
parameterTypes (
  DataType default {
    subattr dso # intendedDataType == gdt SinglePointIndicationWithTime;
  };
  debounceFilterTime default {
    attr filterTimeInMs == 0x02;
    subattr dsl # DS == 0x00;
    subattr dsl # DS == 0x00;
  };
  maximumCollectingFrequency;
}
function READDATA () : ProcessData;
function WRITEDATA (input : ProcessData);
struct ProcessData {
  int8 channel;
  int8 fixdata[4];
}
struct Memory {
  int8 state;
  ProcessData data;
}
instance memory Memory ;
)
```

SOLUTION

Message Format Definition

```
procedure writeRegisterNumberI requestCode 0x29 (
  request: struct request1 {
    int8 acc pattern {
      2:b00;
    };
    6:parentRequestCode;
  };
  int8 registerAddress;
) ;
reply: struct dontCareReply {
  int8 statusByte patternref statusByte;
  int8 dontCare patternref defaultReturn;
} ;
request: struct request2 {
  int8 registerType pattern {
    4:is0000;
  };
  4:registerType;
} ;
int8 registerAddress;
int8 registerdata [2];
) ;
)
```

SOLUTION

Testing

```
procedure writeRegisterNumberI requestCode 0x29 (
  request: struct request1 {
    int8 acc pattern {
      2:b00;
    };
    6:parentRequestCode;
  };
  int8 registerAddress;
) ;
reply: struct dontCareReply {
  int8 statusByte patternref statusByte;
  int8 dontCare patternref defaultReturn;
} ;
request: struct request2 {
  int8 registerType pattern {
    4:is0000;
  };
  4:registerType;
} ;
int8 registerAddress;
int8 registerdata [2];
) ;
) ;

test writeRegisterNumberI for dip writeRegisterNumberI (
  send request1 {
    attr registerAddress == reg parameterInstructions;
  };
  expect dontCareReply {
    subattr statusByte # standardStatus == 2;
  };
  send request2 {
    subattr registerType # registerType == 3;
    attr registerAddress == reg parameterInstructions;
    attr registerdata == 0x77;
    subattr registerdata # channelNumber == 5;
  };
) ;

register parameterInstruction address 0x37 struct {
  int8 dsl pattern {
    2:b00;
  };
  6:channelNumber;
} ;
)
```

tests

refines

SOLUTION

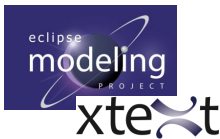
Testing could be simplified and automated

Handler could be generated

Mistakes in Spec could be found automatically

Second „version“ could be done trivially

BENEFITS



Eclipse Modeling
Eclipse Xtext

TOOLS

Example 2: Pension Fund Specification



CONTEXT

Insurance Company
Old-age Pension Funds
Lots of plans, based on how the laws change over time
Old plans must be kept around

PROBLEM

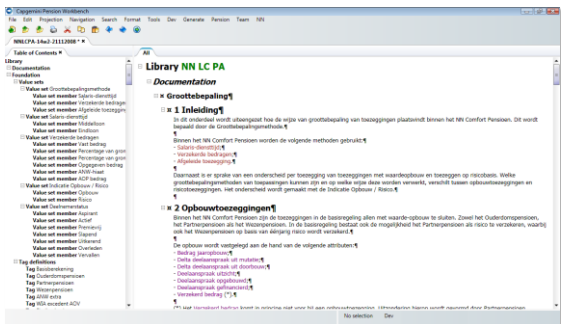
Time to implement/adapt new plans too long:
- Word documents,
- manual implementation

SOLUTION

Describe the complete plan and all calculation rules formally with a set of DSLs and then generate all of the calculation engine.

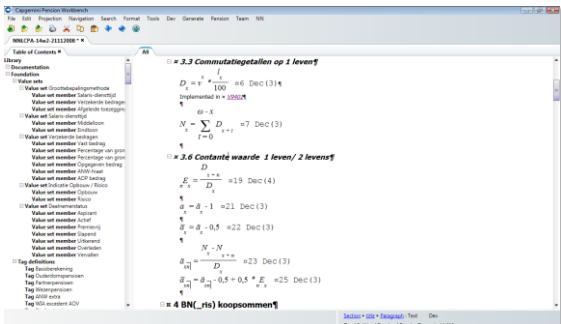
SOLUTION

Textual Documentation

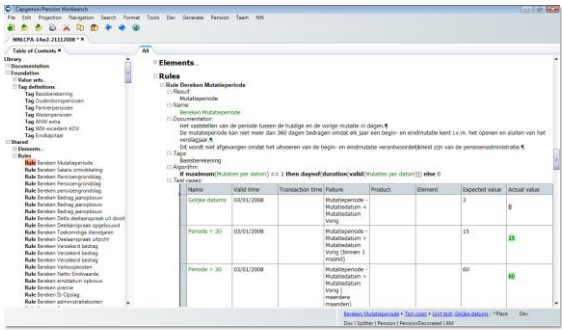


SOLUTION

Insurance Mathematics



Calculation Rules and Tests



Domain users could implement complete plans themselves

Time-to-implement from 30 days to 3 days per plan



Intentional Software's Domain Workbench

Example 3:
Radar Systems Engineering



Radar Systems for satellites need to be designed

Radar requirements influence sensor design influences satellite bus influences launch vehicle ... circular.

PROBLEM

Requirements cannot simply be written down because tradeoffs studies need to be performed

These need to be numerical.

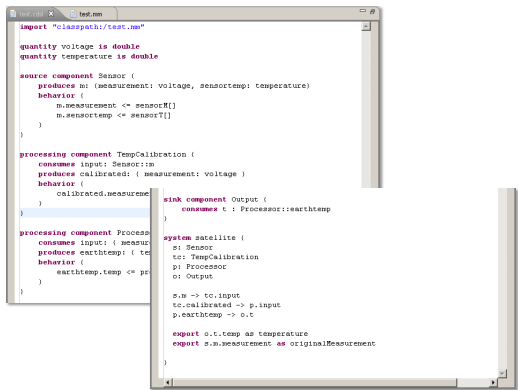
SOLUTION

Break system down into components

Use approximate numerical fomulae to how requirements and design effect other components

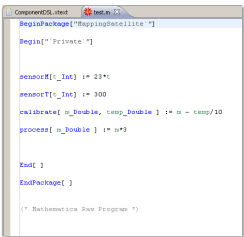
SOLUTION

Component Definition



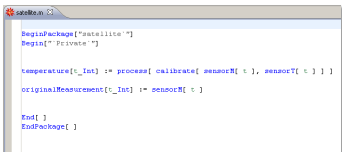
SOLUTION

Component Behavior Specification



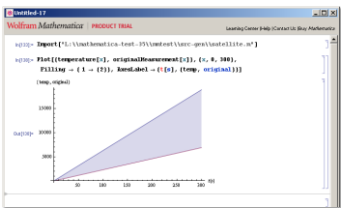
SOLUTION

Resulting System Behaviour



SOLUTION

Analysis



BENEFITS

Numerical approximate
requirements/design tradeoffs
can be performed

TOOLS

Eclipse Modeling
Eclipse Xtext
Wolfram Mathematica
Mathematica Workbench

Example 4:
Alarm System Menus

**CONTEXT**

Alarm Systems
Operator Panels

**PROBLEM**

The structure of the UI and
menus of the operator panel
was described in Word, and
then manually implemented.

Error prone, slow, ...

Use a DSL to describe menu structures directly, and generate various artifacts from it:

- flash simulator data
- C code for implementation
- i18n templates

Menu Structure

```
import "classpath:/units.xpt"
import "classpath:/software.xsw"

namespace si

uses units

condition locked
condition BlinkingLight

menu Normal label "Normal/Menu"
  item unlockNow eye(TurnOffAlarm) if locked
  submenu Normal label "Normal Settings"
    item alarmLevel eye(AlarmLevel)
    valueRange soundLevel restrict 10..80
    item testLight eye(TurnOffAlarm) if BlinkingLight
  end
  submenu autoLocking label "Automatic Locking"
    item startTime eye(TurnOnAlarm)
    valueRange time
    item endTime eye(TurnOffAlarm)
    template areaSettings [size=1, area=1, sv=eye(TurnOnAlarm)] areaSettings
    template areaSettings [size=1, area=1, sv=eye(TurnOffAlarm)] areaSettings
  end
  template [size=100, area=100, sv=eye(TurnOffAlarm)] areaSettings
  item testEye eye(TurnOffAlarm) labelEye "testEye" area="on/off"
  item testEye eye(AlarmLevel) label "test"
  item alarmLevel eye(AlarmLevel)
  valueRange soundLevel restrict size..80

menu Expert extends Normal
  item master eye(BlinkingLight) afterItem unlockNow
end
```

Software Components

```
message TurnOffAlarm
message TurnOnAlarm
message AlarmLevel
message UnlockNow

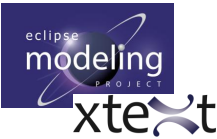
component AlarmManager {
  receives TurnOffAlarm
  receives TurnOnAlarm
  receives AlarmLevel
}

component MasterSwitch {
  receives UnlockNow
}
```

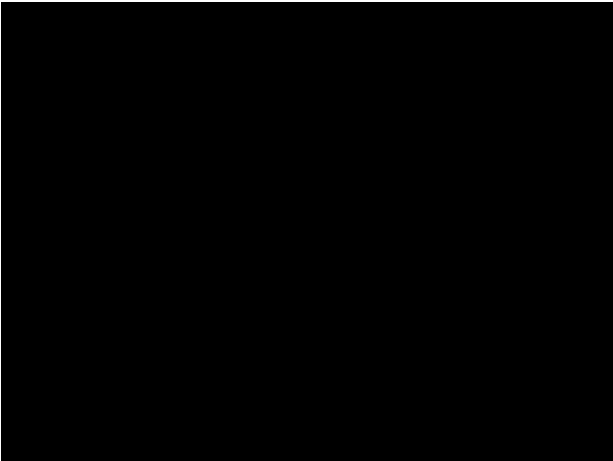
Various non-software artifacts could be generated

Integration with software structure simpler

Fewer errors, faster...



Eclipse Modeling
Eclipse Xtext



CONTEXT

PROBLEM

SOLUTION

SOLUTION

```

@ DummyRequirementsCollection -
DUMMY REQUIREMENTS (to be replaced by interface to real RE tool)
show trace true

Init           The system should start operating only after it has been initialized properly
refines TwoPhase
Efficient      The program should be as small regarding memory footprint as possible
refines Init refines MaxSpeed
Cyclic        the actual control of the device should be based on a cyclic task
Calibration   The black/white values should be easily calibrated
MaxSpeed      Speeds per motor can only be up to 80
OptionalOutput[k1][k2][k3] Display output should be optional
TwoPhase      Initialization should be separate from operation
ConsistentSetting Motor settings have to be updated consistently

```

SOLUTION

19

Selecting from the Requirements

```
task Cycle0
  desc This is the cycle task that is called every line to do the actual control of the
  task run cycle prio = 1 every = 2 {
    task
      state@Calibration: The black/white values should
      state@ConsistentSetting: Motor settings have to be upda
      init@Cycle0: The actual control of the devi
      bo@Efficient: The program should be as small
      if@Init: The system should start operat
      if@MaxSpeed: Speeds per motor can only be u
      if@OptionalOutput: Display output should be optio
      if@TestPhase: Initialization should be requir
    }
  }
  task Test
    init32 light = 0;
```

Find Usages of Requirements



SOLUTION



JetBrains MPS

TOOLS



What if I don't yet
have a language?



Actually, this is the
normal case!
Domain Specific Language

Building Languages



**As you
understand
the
domain...**

**...develop a language to
express it!**



**Language resembles
domain concepts**



**Then express the
design with
the language.**



**Clear understanding of
the domain from building
the language**



Iterate!



Understand Domain

Define Language

Use Language

Iterate!



Understand Domain

Domain Expert
Language Engineer

Define Language

Language Engineer

Use Language

Domain Expert
Domain User

Iterate!



Understand Domain

Domain Expert
Language Engineer

Define Language

FORMAL!

Use Language

FORMAL!

Like

Analysis!



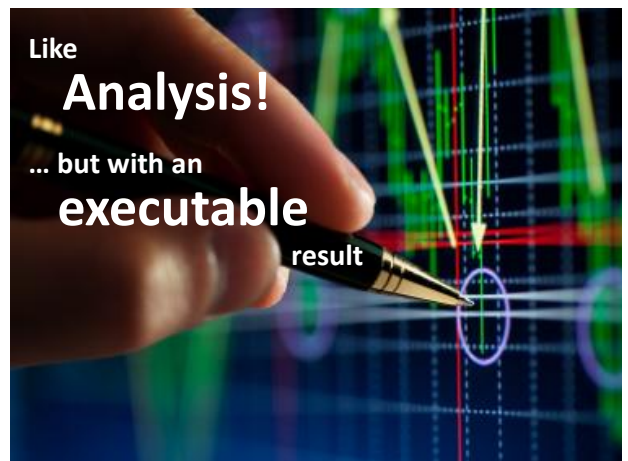
Like

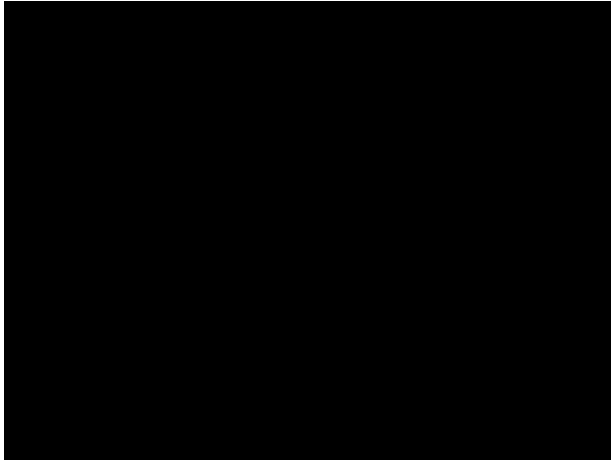
Analysis!

... but with an

executable

result





DSL Engineering Tools



Notations



Notations Editors



Notations Editors Multi-Languages



Notations Editors Multi-Languages Debugger



Notations
Editors
Multi-Languages
Debugger
Testing



Notations
Editors
Multi-Languages
Debugger
Testing

Groupware



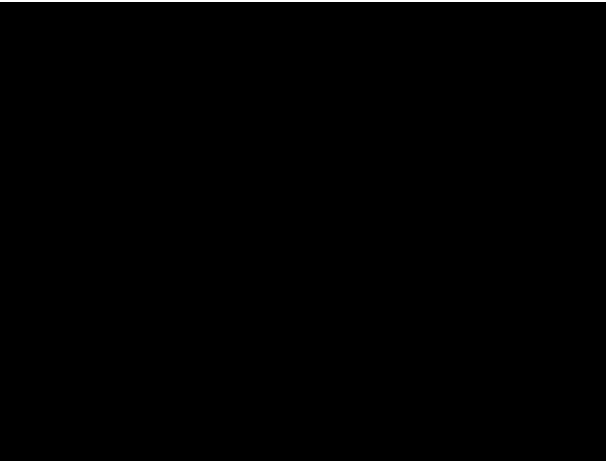
Notations
Editors
Multi-Languages
Debugger
Testing

Groupware
Scalable



Notations
Editors
Multi-Languages
Debugger
Testing

Groupware
Scalable
Integrated



Open Source
Eclipse Public License



**Large world wide
community**



**graphical, textual and
form-based DSLs**



**Developed by JetBrains
Open Source
Apache 2.0**



**Projectional Editor
all kinds of notations,
mainly textual**

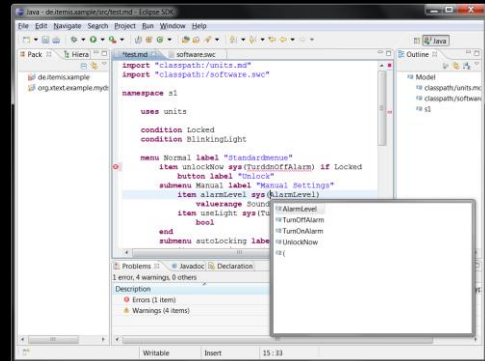


**Commercial Product
Projectional Editor
Most flexible notations**

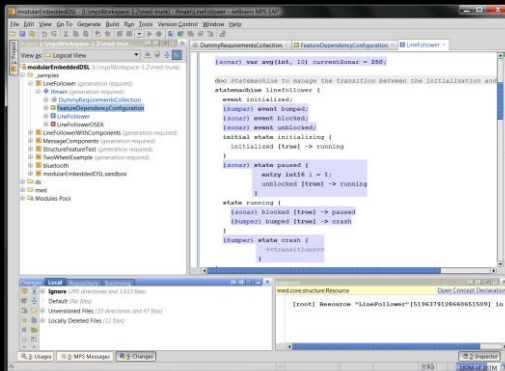
Notational Flexibility?



Textual Rich IDEs



Textual Rich IDEs

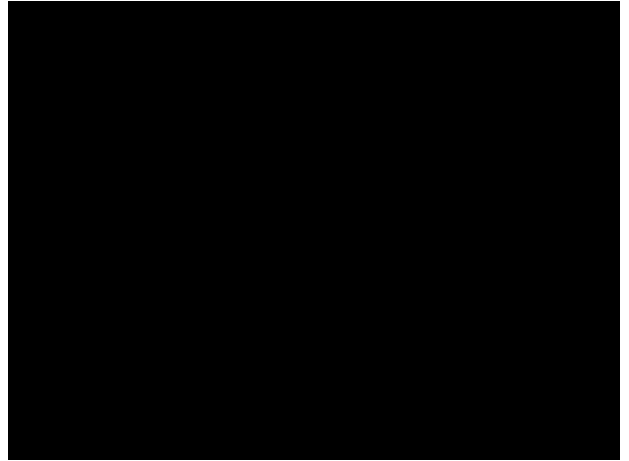


Textual Languages and Editors are easier to build

Textual Languages and Editors are easier to build

Evolve Language and simple editor as you understand and discuss the architecture, in real time!

Textual Integrates easily with current infrastructure: CVS/SVN diff/merge



Standards & UML



You can model
everything
with **UML**

You can model
everything
with **UML**
somehow!

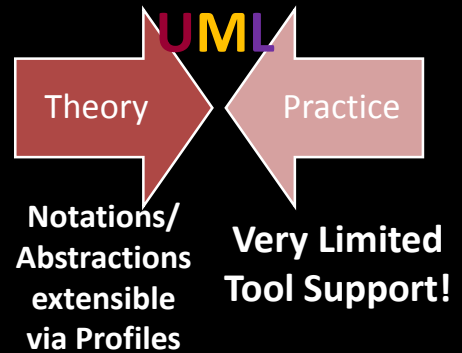
Problem

Shoehorning domain
abstractions into the
generic language

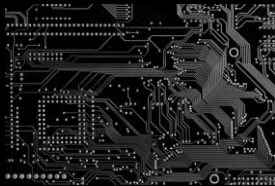
Problem

Sidetracked
by existing
abstractions
and notations

Problem



Problem



Meta Model
Complexity!

But!

But don't
reinvent
the wheel
either.



Where are
standards
useful?



People have
to learn
underlying
concepts
anyway



Is UML with
a profile
still a
**standard
language?**



On which
meta level do
I want to
standardize?
M2 (UML),
M3 (MOF)?



Isn't a **DSL**
based on **MOF**
as „standard“
as a profile
based on
UML?

Similar statements can be
made relative to

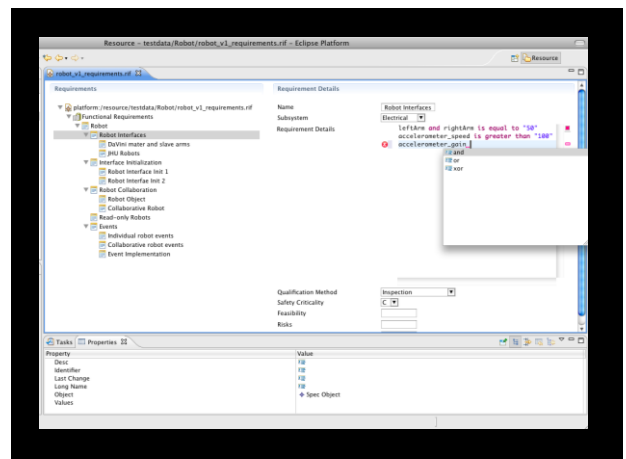
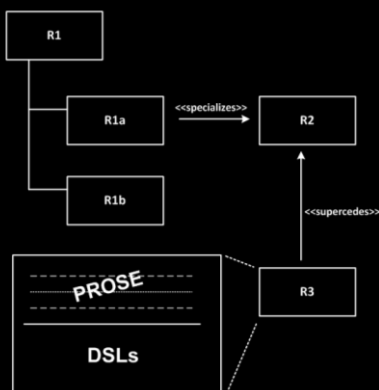
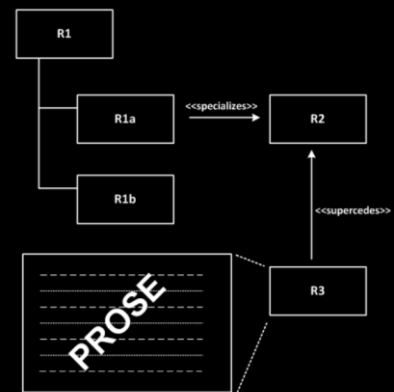
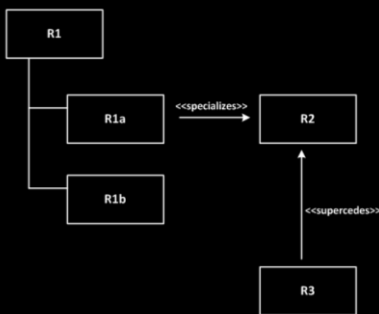
BPMN

Textual Requirements?



Textual Requirements

still necessary.



Tracing

```

@ DummyRequirementsCollection
@ Linelollower

trace Cyclic
do { This is the cyclic task that is called every line to do the actual control of the
task run cyclic prio = 1 every = 2 {
  trace Twiddle
  state switch linefollower
  state running
  int8 bump = 0;
  bump = ecrobot_get_touch_sensor(SENSOR_PORT_T: NXT_PORT_S3);
  if ( bump == 1 ) {
    event linefollower:bumped
    terminate;
  }
  trace Init
  int32 light = 0;
  light = ecrobot_get_light_sensor(SENSOR_PORT_T: NXT_PORT_S1);
  if ( light < ( WHITE + BLACK ) / 2 ) {
    trace ConsistentSetting
    updateMotorSettings(SLOW, FAST)
  } else {
    trace ConsistentSetting
    updateMotorSettings(FAST, SLOW)
  }
  state crash
  updateMotorSettings(0, 0);
  default
  <noop>;
}
}

```

Tracing

```

@ DummyRequirementsCollection
@ Linelollower

trace Cyclic
do { This is the cyclic task that is called every line to do the actual control of the
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    updateMotorSettings(FAST, SLOW)
  }
  state crash
  updateMotorSettings(0, 0);
  default
  <noop>;
}
}

```

state@ConsistentSetting: The black/white values should	*requirements (ifmain.null)
state@Cyclic: The actual control of the dev	*requirements (ifmain.null)
if { bump == 1 }	*requirements (ifmain.null)
event linefollower:bumped	*requirements (ifmain.null)
terminate	*requirements (ifmain.null)
trace Init	*requirements (ifmain.null)
int32 light = 0;	
light = ecrobot_get_light_sensor(SENSOR_PORT_T: NXT_PORT_S1);	
if (light < (WHITE + BLACK) / 2) {	
trace ConsistentSetting	
updateMotorSettings(SLOW, FAST)	
} else {	
trace ConsistentSetting	
updateMotorSettings(FAST, SLOW)	
}	
state crash	
updateMotorSettings(0, 0);	
default	
<noop>;	

Things to keep in mind



Limit Expressiveness



Notation is important!

$$\begin{aligned}\frac{\partial}{\partial \theta} M T(\xi) &= \frac{\partial}{\partial \theta} \int_{\mathbb{R}^n} T(x) f(x, \theta) dx = \int_{\mathbb{R}^n} \frac{\partial}{\partial \theta} T(x) f(x, \theta) dx \\ \frac{\partial}{\partial a} \ln f_{a, \sigma^2}(\xi_1) &= \left(\frac{\xi_1 - a}{\sigma^2} \right) f_{a, \sigma^2}(\xi_1) = \frac{1}{\sqrt{2\pi\sigma^2}} \left(\frac{\xi_1 - a}{\sigma^2} \right) e^{-\frac{(\xi_1 - a)^2}{2\sigma^2}} \\ \int_{\mathbb{R}^n} T(x) \cdot \frac{\partial}{\partial \theta} f(x, \theta) dx &= M \left(T(x) \cdot \frac{\partial}{\partial \theta} \ln f(x, \theta) \right) \int_{\mathbb{R}^n} f(x, \theta) dx \\ \int_{\mathbb{R}^n} T(x) \cdot \left(\frac{\partial}{\partial \theta} \ln f(x, \theta) \right) \cdot f(x, \theta) dx &= \int_{\mathbb{R}^n} \frac{\partial}{\partial \theta} T(x) f(x, \theta) dx \\ \frac{\partial}{\partial \theta} M T(\xi) &= \frac{\partial}{\partial \theta} \int_{\mathbb{R}^n} T(x) f(x, \theta) dx = \int_{\mathbb{R}^n} \frac{\partial}{\partial \theta} T(x) f(x, \theta) dx\end{aligned}$$

Graphical vs. Textual



Invest in good constraints



Testing may be an important benefit of your DSL



Simulations („play around“ with the models)



Who are 1st Class Citizens?



**Learn from - but don't copy –
programming languages**



**Support for Reuse
and Variations**



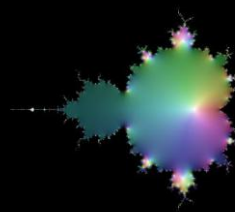
Tooling Matters!



**Annotation Models
to add technical details**



**Develop the language
iteratively!**



**Co-Evolve Language
and Concepts**



Can domain users actually „program“?



Domain Users vs. Experts



Summary



Cohesive
 Complete
 Consistent
 Atomic
 Traceable
 Current
 Feasible
 Unambiguous
 Mandatory
 Verifiable

Wikipedia

Cohesive
 Complete
Consistent
 Atomic
 Traceable
 Current
 Feasible
 Unambiguous
 Mandatory
 Verifiable

Validation
 Checking
 Simulation

Wikipedia

Cohesive
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 Verifiable

Everything is a model
tracing links simple

Wikipedia

Cohesive
 Complete
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 Traceable
 Current
 Feasible
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 Mandatory
 Verifiable

Described Formally

Wikipedia

Cohesive
 Complete
 Consistent
 Atomic
 Traceable
 Current
 Feasible
 Unambiguous
 Mandatory
Verifiable

Domain Expert involved
in Definition and Review

Wikipedia

Cohesive
 Complete
 Consistent
 Atomic
 Traceable
 Current
 Feasible
 Unambiguous
 Mandatory
 Verifiable
Executable

Automatic Refinement
downstream, Code Gen.

Cohesive
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Reward
for the
additional effort
of formalization!

And Developers???



And Developers???

- ... Languages
- ... Technology Evaluation
- ... Generators
- ... Testing
- ... Operations

... what they want to do anyway!



Brain [Domain Person]

???



Code



Brain [Domain Person]

DSL



Brain [Developer]

Code



One more thing:

One more thing:
Why all these pictures?



I like airplanes.



„Build a research airplane for
high AoA and thrust vector control“



„Build a research airplane for
high AoA and thrust vector control“



Not enough!

„Build a research airplane for
high AoA and thrust vector control“



Not enough!

Systems Engineering

„Build a research airplane for
high AoA and thrust vector control“



Not enough!

Systems Engineering

Requirements ... Design ... continuous.
Early Formalization of many aspects.



And:
The airplane is custom-built for the task.
One size does not fit all.

THE END.



.coordinates

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itemis