Design, Analysis and Simulation of an I/O Link

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I. System Level Analysis

A. *Impulse response/Pulse response*

The impulse response was calculated and plotted using the s-parameter file provided:

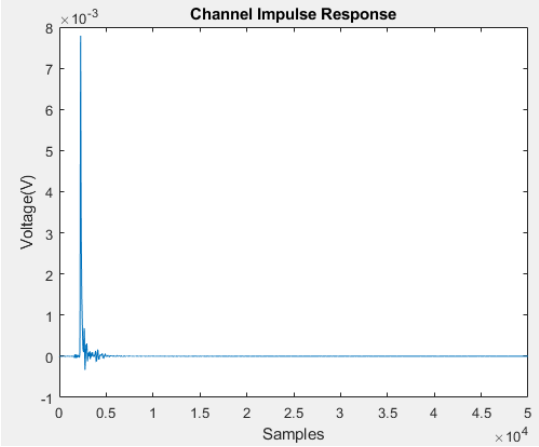

Fig. 1. Channel Impulse Response

Then, a 1V pulse was used as in input, the corresponding pulse response is shown below:

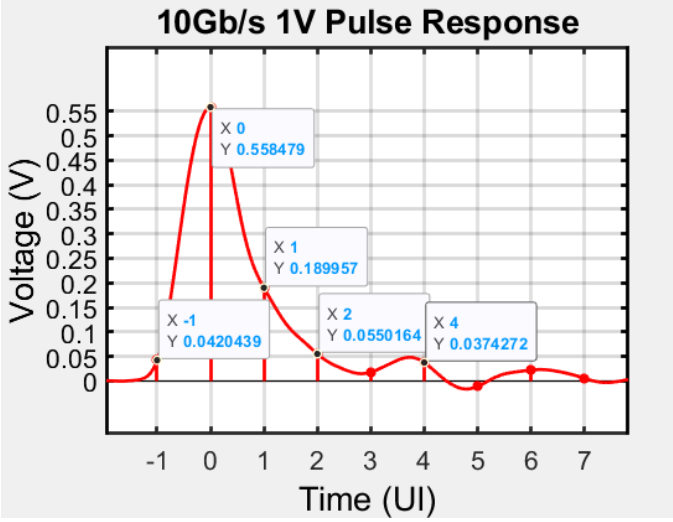

Fig. 2. Channel Pulse Response – with magnitude of 5 most important cursors

B. *Worst case pattern*

Using the pulse response shown in Fig. 2., worst case pattern 1 and worst-case pattern 0 were obtained.
Worst case pattern 1 (where positive ISI corresponds to bit 1 and negative ISI corresponds to bit 0):

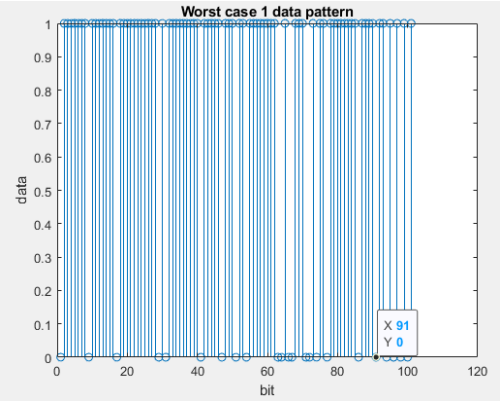

Fig. 3. Worst case 1 data pattern

The worst-case bit 1 occurs at bit 91.

Worst case pattern 0 (where positive ISI corresponds to bit 0 and negative ISI corresponds to bit 1):

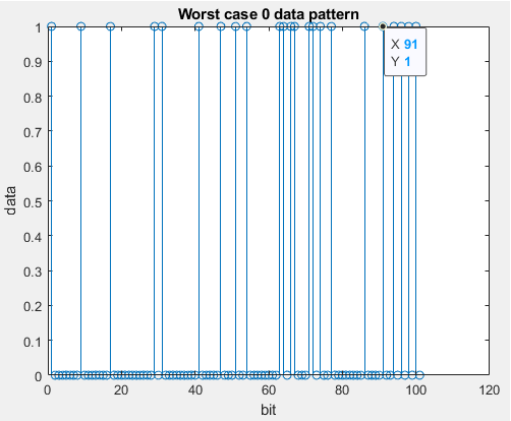

Fig. 4. Worst case 0 data pattern

The worst-case bit 0 occurs at bit 91.

C. *Eye diagram*

Using the channel impulse response and random data (1, -1) as input, the eye diagram was generated:

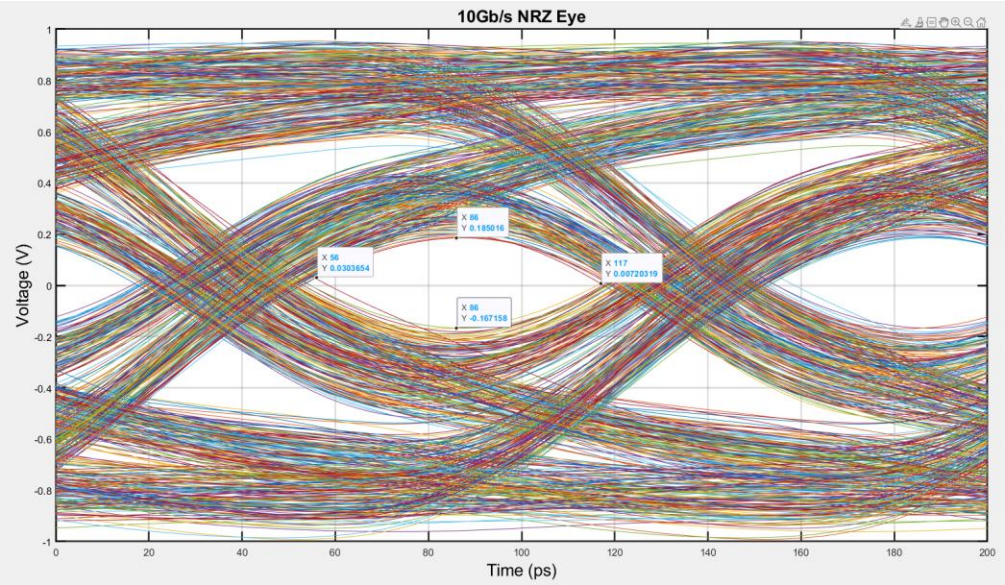

Fig. 5. Eye diagram of I/O link

The eye height is about 0.2017V and the eye width is about 61ps.

D. Equalizers

Using the impulse response, we generated a 3-tap TX FIR with 1 precursor tap, the coefficients are:

```
taps =

   -0.0492
    0.7177
   -0.2330
```

Fig. 6. Tap coefficients for 3-tap TX FIR

The pulse response with the equalizer was also plotted:

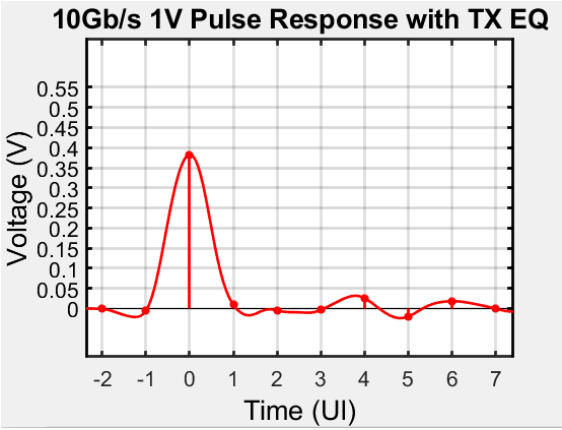

Fig. 7. Pulse response with 3-tap TX FIR

We can clearly see the improvements in ISI compared to the pulse response without an equalizer.

Next, we generated a RX DFE, the coefficients are:

```
dfe_taps =

    0.0950    0.0275    0.0089
```

Fig. 8. Tap coefficients for 3-tap DFE

The pulse response was also plotted:

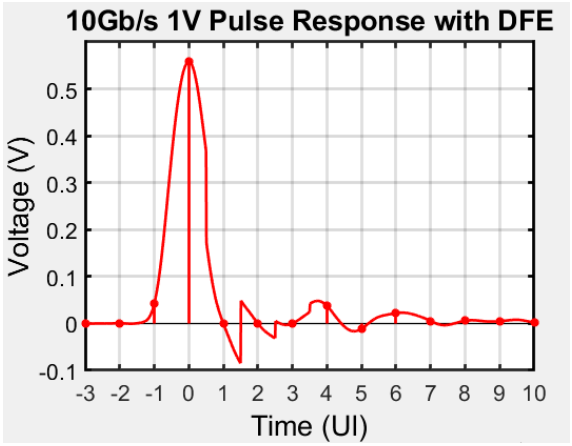

Fig. 9. Pulse response with 3-tap DFE

The pulse response improved its ISI compared to the vanilla channel and has less attenuation compared to TX FIR equalizer.

E. Source code

MATLAB code for worst case pattern calculation:

```
%Worst case 1
wc1 = zeros(101,1);
for i=1:101
    if sample_values(102-i) >= 0
       wc1(i) = 1;
    else
       wc1(i) = 0;
    end
        wc1(91) = 0;
end

figure;
stem(wc1);
title('Worst case 1 data pattern');
xlabel('bit');
ylabel('data')

%Worst case 0
wc0 = zeros(101,1);
for i=1:101
    if sample_values(102 - i) >= 0
       wc0(i) = 0;
    else
       wc0(i) = 1;
    end
    wc0(91) = 1;
end
figure;
stem(wc0);
title('Worst case 0 data pattern');
xlabel('bit');
ylabel('data')
```

Fig. 10. MATLAB code for worst case data sequence

II. TX DESIGN JUSTIFICATION

A. *Equalization choice*

To decide what kind of equalization to use, we generated the pulse response of the channel:

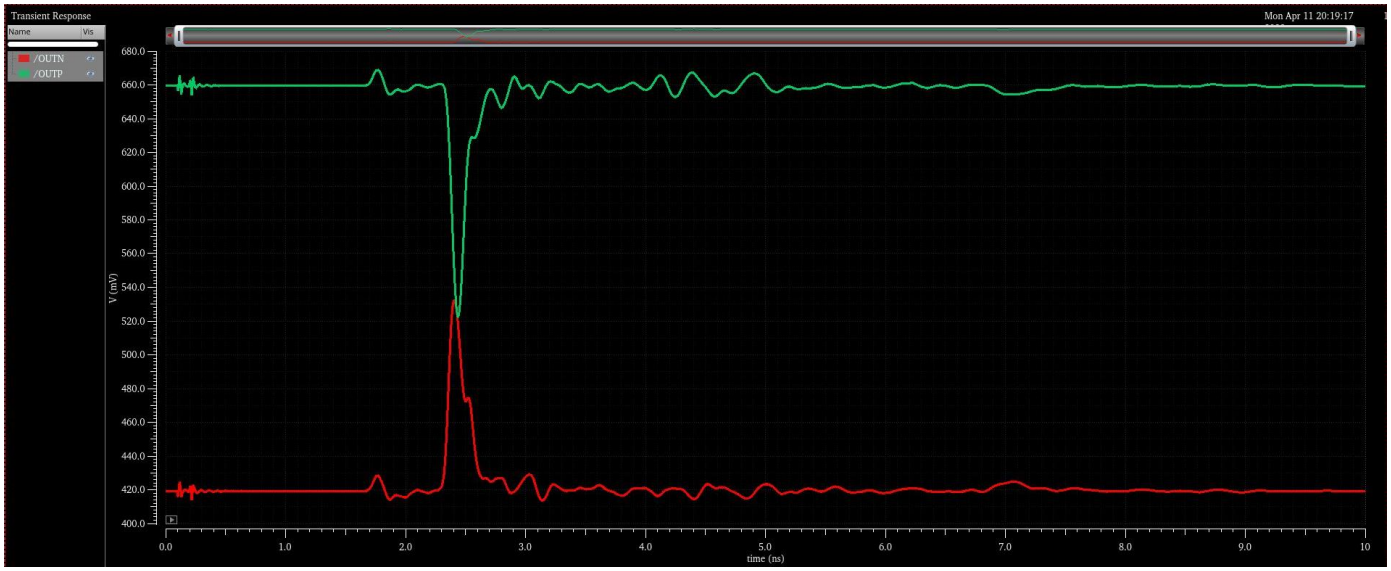

Fig. 11. Channel pulse Response

We can see that the first post cursor is larger than other cursors. We choose to use a 2-tap equalizer TXPE because of following reasons:

1. Implementing EQ with TXPE side is easier since we can use flip flops to obtain a delayed signal. To implement DFE, we must deal with analog signals which requires more complicated circuits.
2. DFE could exacerbate ISI when bit-errors occur.
3. A simple 2-tap EQ was chosen because a large amount of EQ would amplify noise.
4. We might want to equalize pre-cursors later in the design process, TXPE could be modified to do that while DFE can only equalize post cursors.

B. *Circuit topologies and clock-rate*

- Voltage mode driver + equalization

  As mentioned in the above section, a 2-tap TXPE was chosen. Since we had a fixed EQ coefficient $\alpha = 0.25$, making α independent of the number of slices was not necessary. However, to make it easier to tune the output impedance of the VM driver, we designed each slice to have 1000Ω impedance so that ideally, we would need 20 slices to get 50Ω. This helps with impedance tuning because we can achieve $\alpha = 0.25$ with 12,16,24 and 28 slices which gives us a large range for tuning.

- Serializer + clock rate

  To design a 4:1 serializer, we have two choices – full rate or half rate. Full rate design has the downside of having to deal with setup time of the last DFF while half rate design has an output eye that is sensitive to clock duty cycle. In this case, we chose the half rate design because we are using ideal clock sources so that clock duty cycle isn't a problem. The clock rate for our serializer: 5GHz.

- Multiplexer and DFF selection

  The multiplexer we chose to use in our serializer uses transfer gates instead of CMOS (in appendix). Transfer gate multiplexer doesn't have regeneration properties but is faster compared to other multiplexer designs. Since we don't have much loss on the serializer path, the transfer gate design is preferable.

  The DFF design we chose to use a high-speed design (in appendix). This design has lower dynamic power consumption compared to the conventional NAND gate DFF design because it uses less transistors and has less internal switching, the speed is also faster because the input to output path is shorter.

III. TX CIRCUITS

A. *Voltage mode driver with EQ*

- VM driver segment (Fig. 12)

  Each VM driver segment is tuned to have an output impedance of 1000Ω. NAND and NOR circuits used in this schematic is included in the Appendix.

  Testbench circuit and results for impedance matching is shown in Fig. 13 and 14.

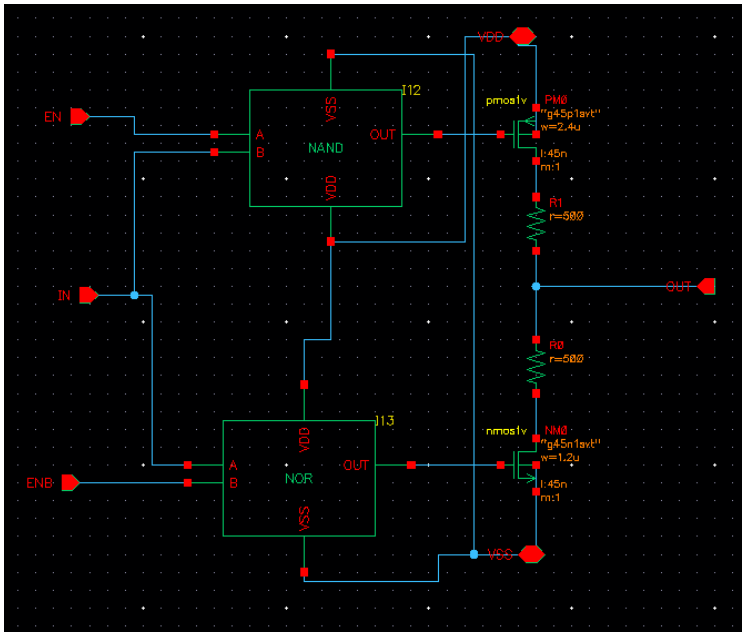

Fig. 12. VM driver segment schematic

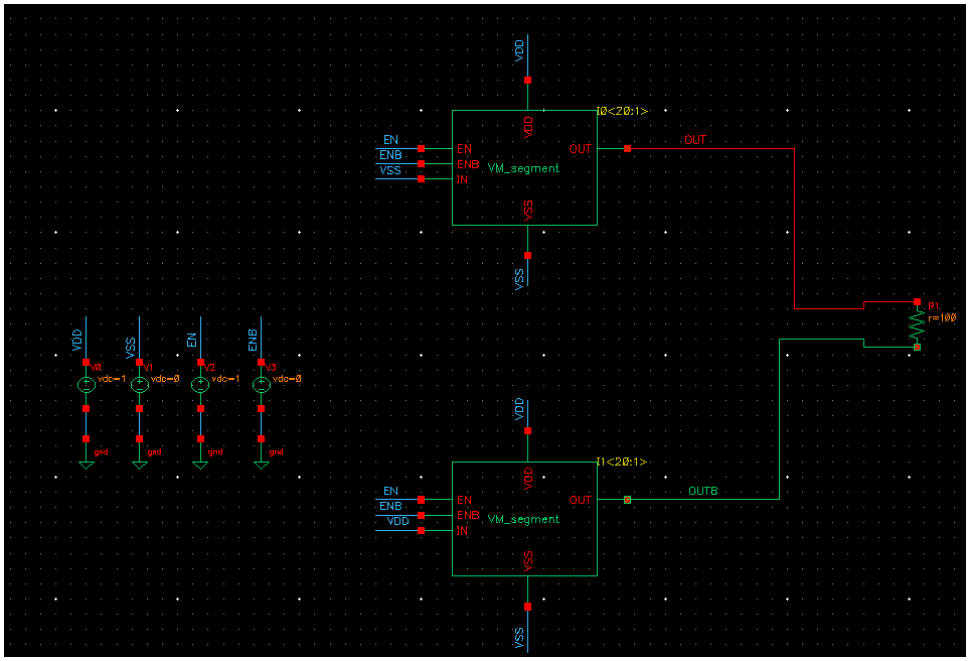

Fig. 13. VM driver segment testbench

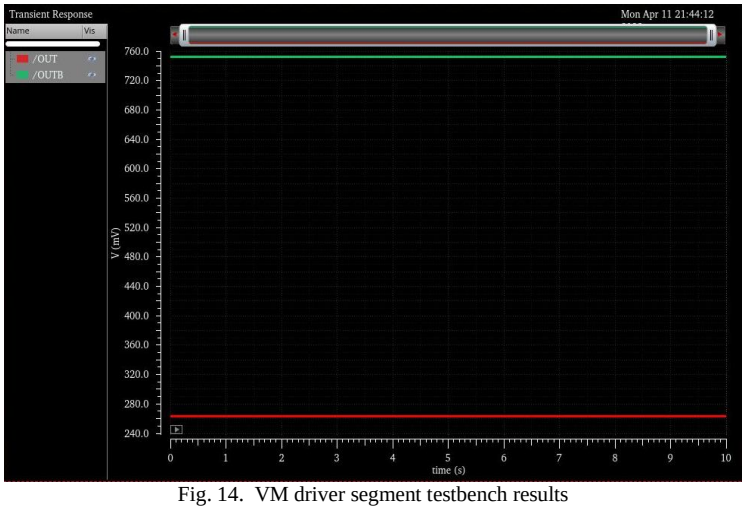

Fig. 14. VM driver segment testbench results

- VM driver (Fig. 15)

  The VM driver ideally uses 20 slices, they were separated into 15/5 to implement an equalizer with $\alpha = 0.25$. An additional 10 slices were added for impedance tuning.

  A pulse input testbench is shown in Fig. 16 and the results in Fig. 17.

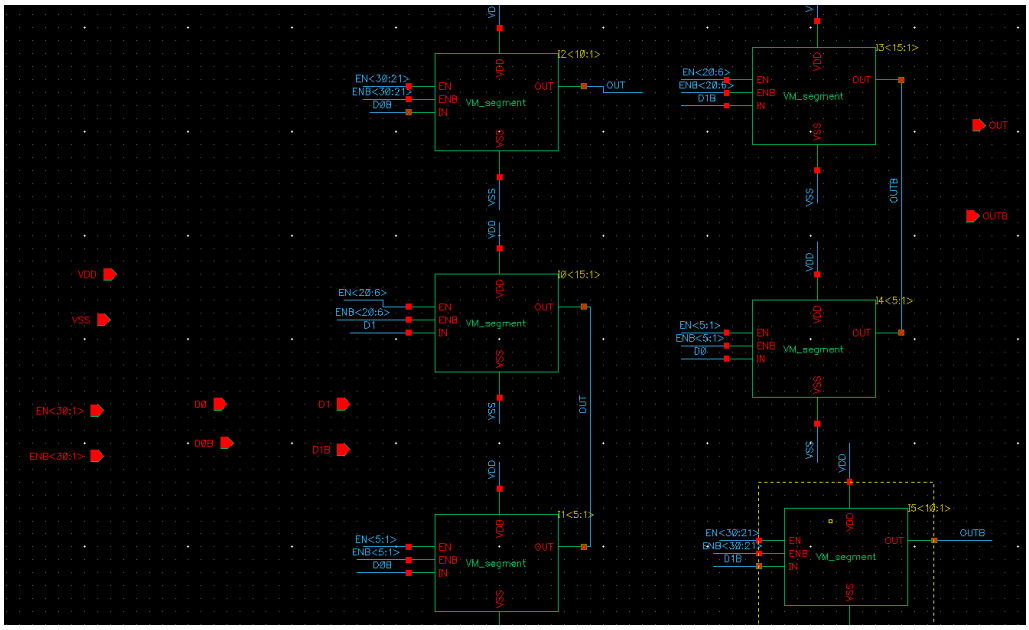

Fig. 15. VM driver

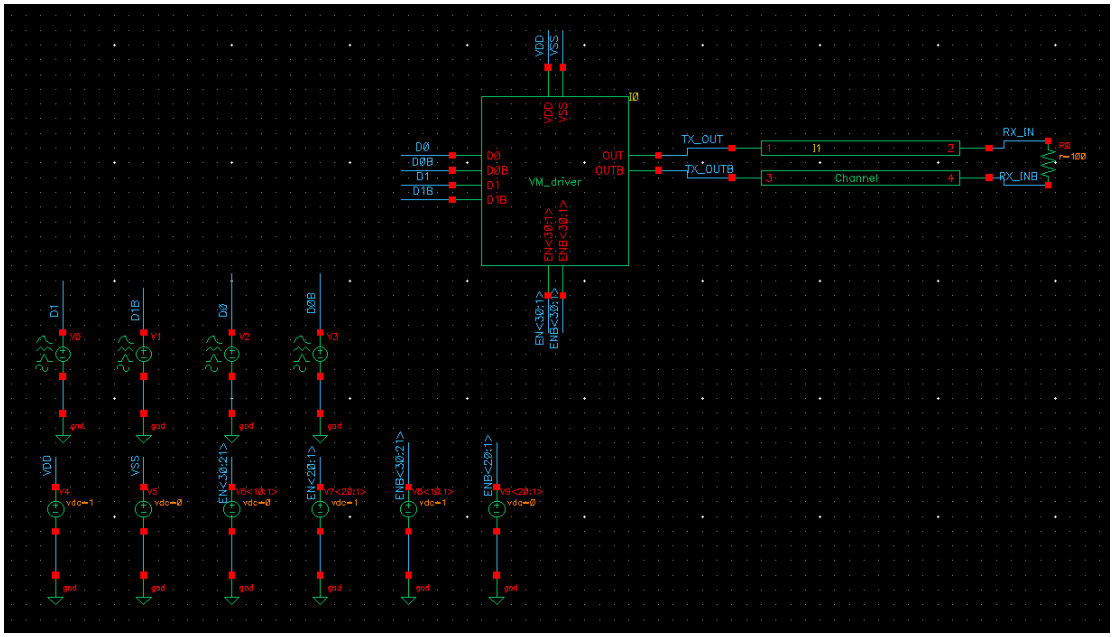

Fig. 16. VM driver pulse input testbench

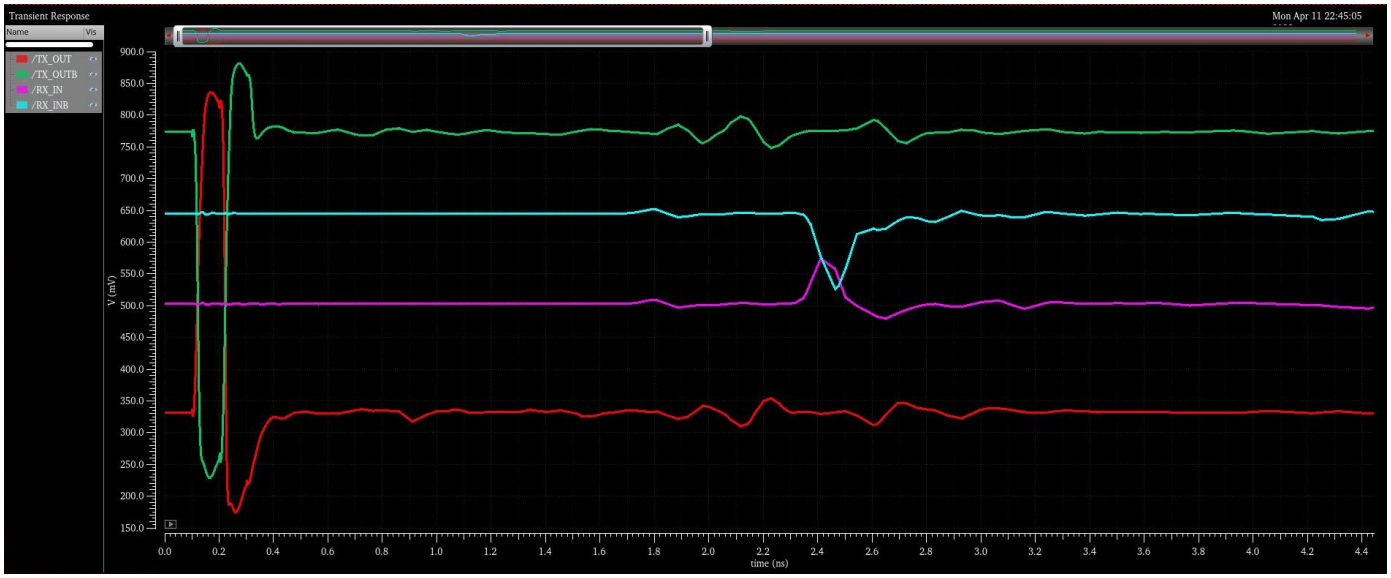

Fig. 17. VM driver testbench results

B. Serializer

A half-rate 4:1 serializer was implemented along with a delayed signal output for EQ.

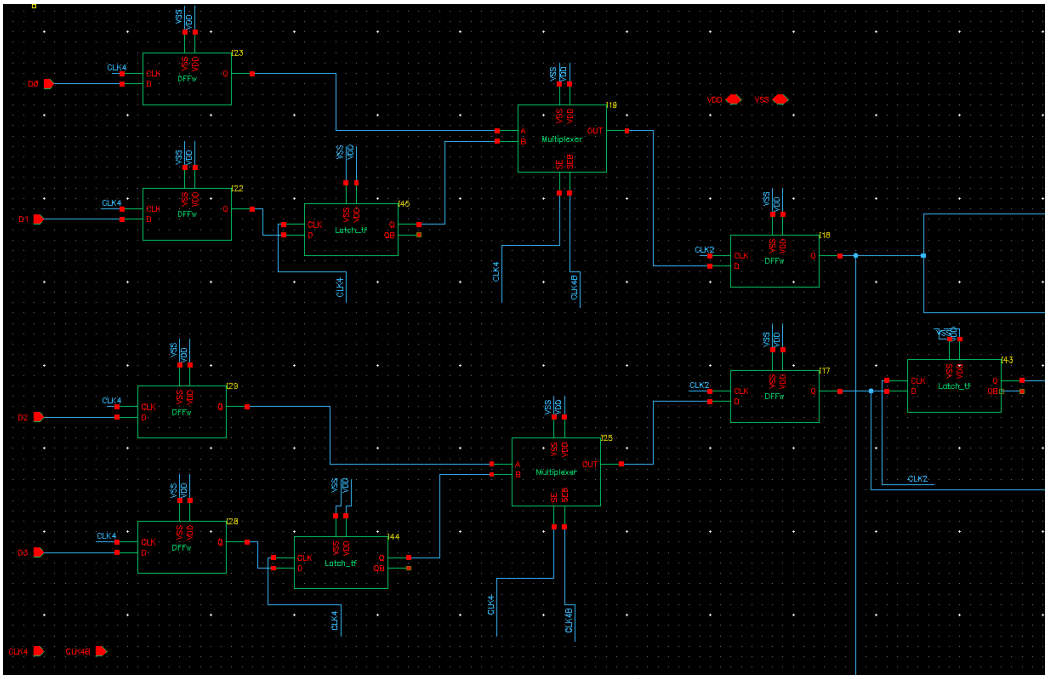

Fig. 18. Serializer schematic (left part)

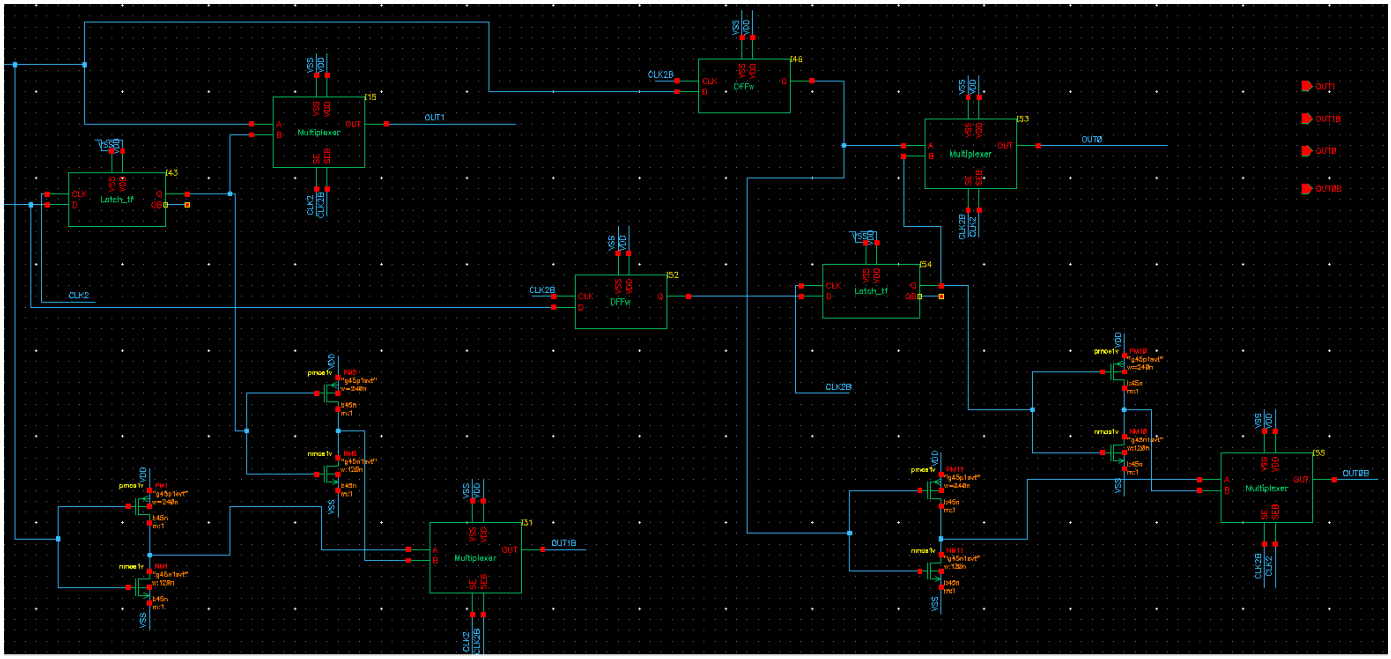

Fig. 19. Serializer schematic (right part)

DFF, latches and multiplexer components were custom made, all circuits are included in the Appendix. For testing, we sent a DC input D0 = 1, D1 = 1, D2 = 1, D3 = 0 and Fig. 12 shows the output results.

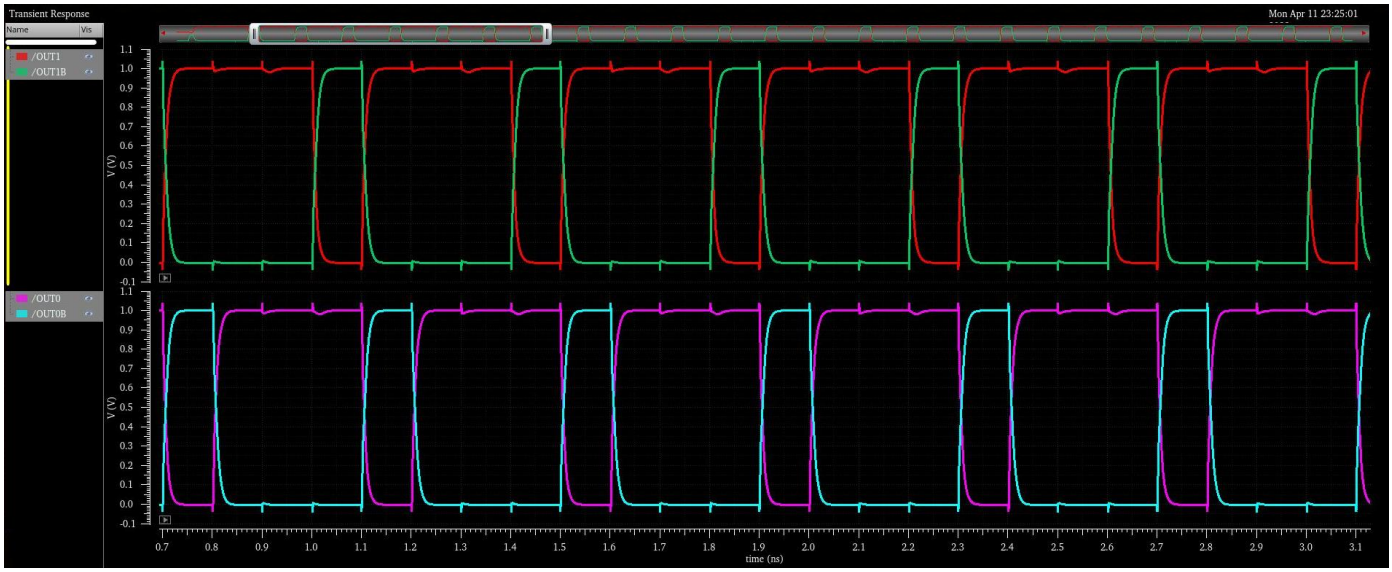

Fig. 20. Serializer output results

C. *Predrivers*

The predrivers are simple CMOS buffers using two inverters.

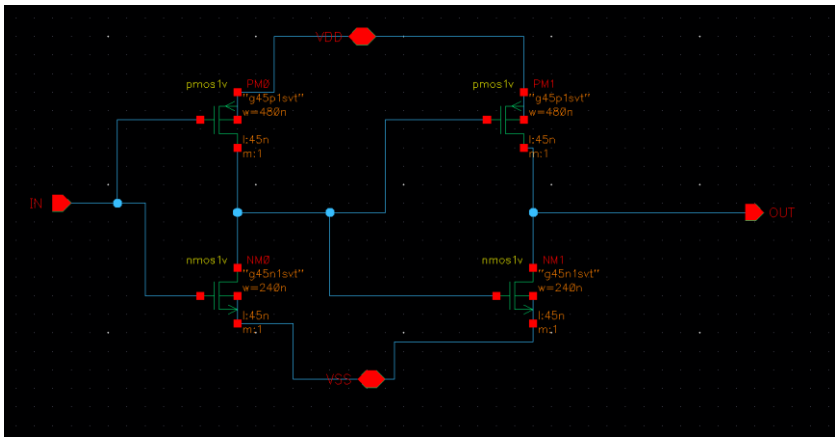

Fig. 21. Predriver buffer schematic

D. *Clock buffers*

The maximum capacitance load for each clock in our TX design was 6.24fF, which is lower than the constraint of 20fF. Because of that, custom design wasn't needed. The clock buffers are the same CMOS buffers as the pre-drivers.

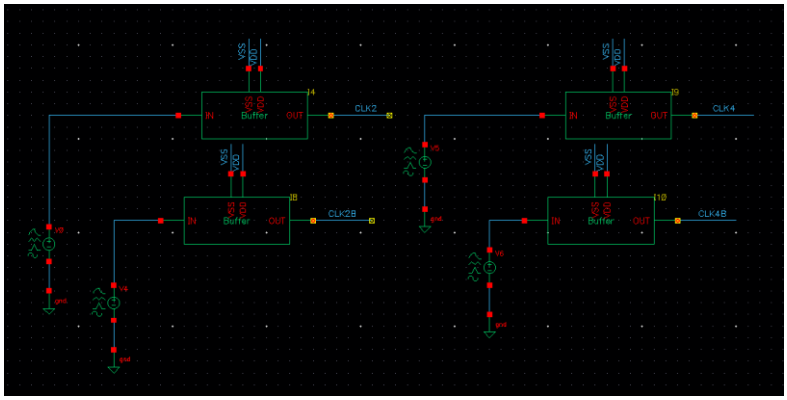

Fig. 22. TX Clock buffer schematic

IV. TX ANALYSIS

A. *Transient waveform for data alternating transition*

PRBS is used for input data sequence.

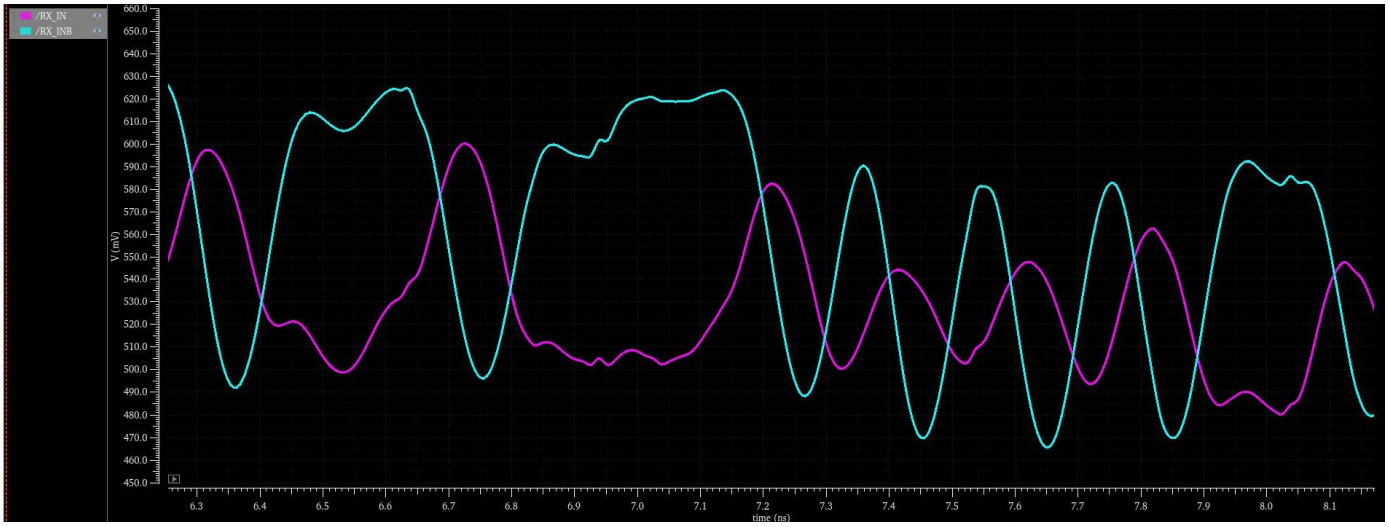

Fig. 23. 6UI Transient waveform showing alternating data transition at TX output (after channel)

B. *10000UI eye diagram with PRBS7 input*

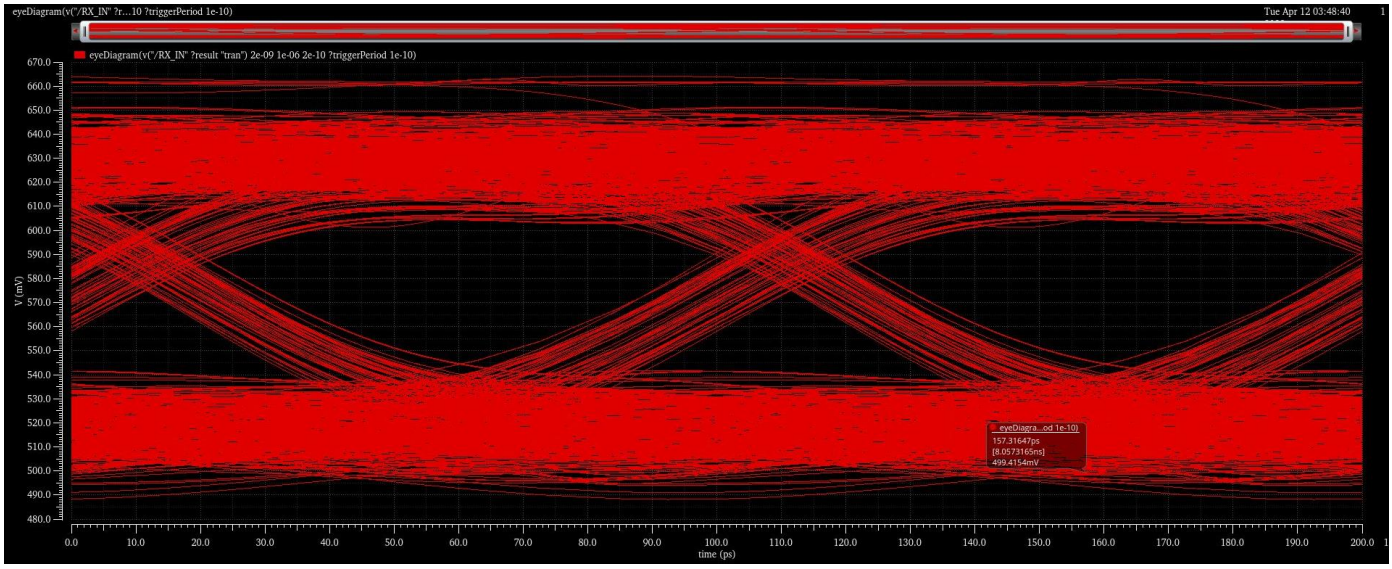

Fig. 24. 10000UI eye diagram with PRBS7 input

Eye width = 79ps, eye height = 68mV.

C. Worst case 0 eye diagram

Using the worst-case 0 pattern as input, we got the following eye diagram. (Fig. 25)

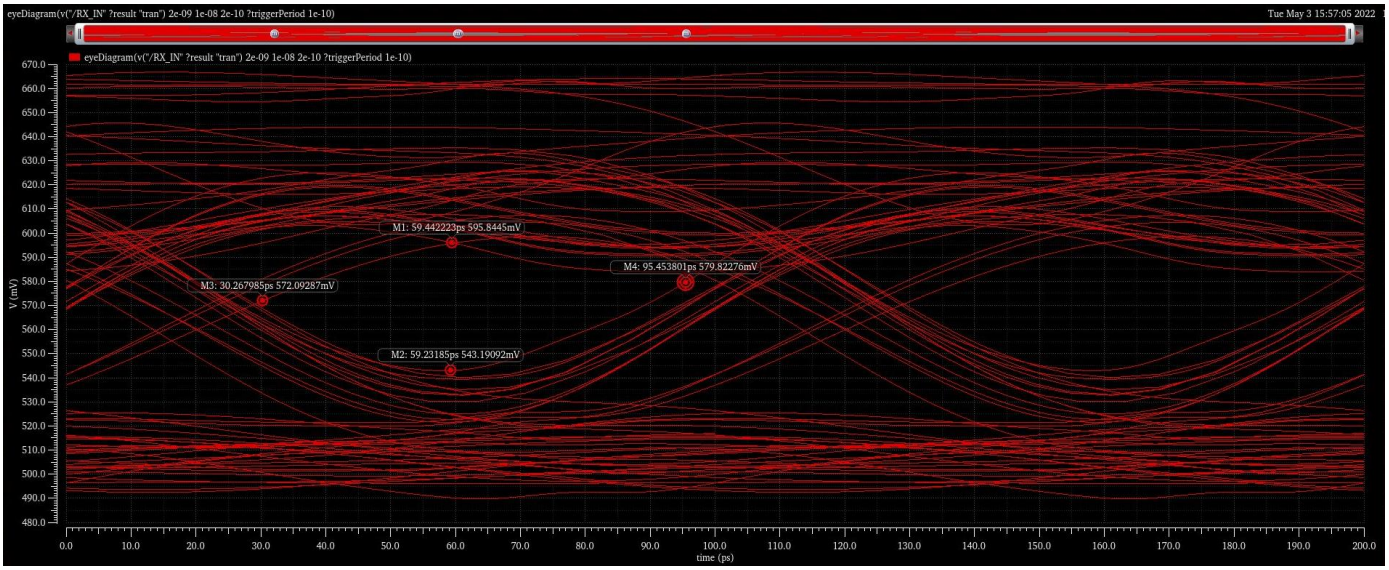

Fig. 25. Worst case 0 pattern eye diagram

Eye width = 65ps, eye height = 52mV.

D. Worst case 1 eye diagram

Using the worst-case 1 pattern as input, we got the following eye diagram. (Fig. 26)

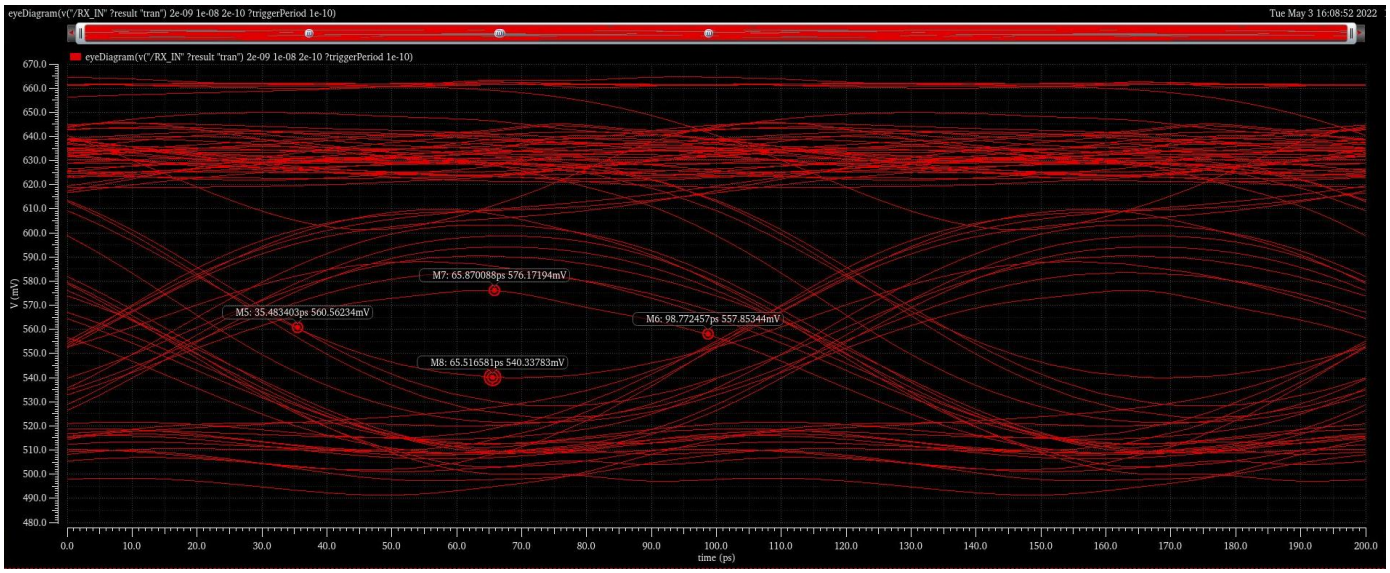

Fig. 26. Worst case 1 pattern eye diagram

Eye width = 63ps, eye height = 36mV.

E. Output impedance tuning range

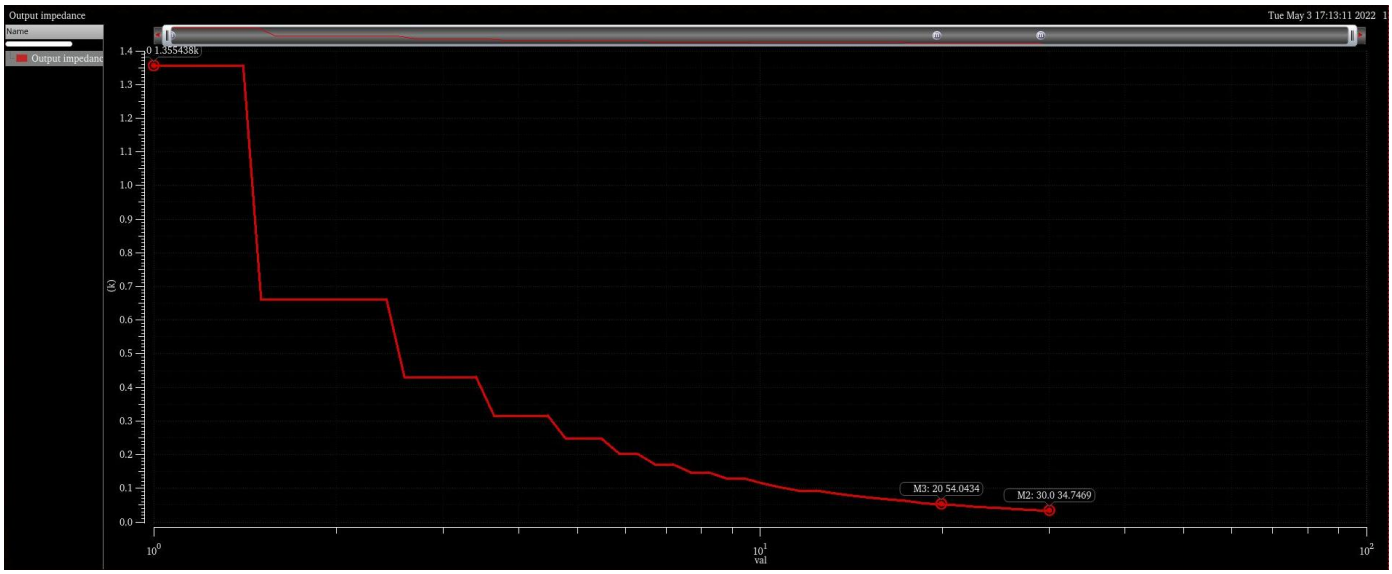

Fig. 27. TX output impedance tuning range

When only one segment is enabled, we have an output impedance of 1.35k Ohms. When 20 segments are enabled, we have about 50 Ohms, which is the ideal number of segments. When we have all 30 segments enabled, the impedance drops to 34.7 Ohms, giving us a range for tuning.

V. RX CLOCK RATE JUSTIFICATION

To implement the 1:4 deserializer, we need 4 clocks to deserialize 10GHz serial data. This means that the clock period should be 400ps, corresponding to a frequency of 2.5GHz, and the phase shift between each clock should be 100ps.

VI. RX CIRCUITS

A. Resistor bank/DC biasing

To have a tunable termination at the RX side, we designed a resistor bank which contains 15 segments that can be enabled/disabled.

Figure 28 shows the design of the resistor segment. IN corresponds to RX_IN signal and the TERM corresponds to ground, EN is the enable signal, which uses 2V for logic high instead of 1V. This is to make sure the NMOS stays in the linear region even after adding DC offset to RX_IN.

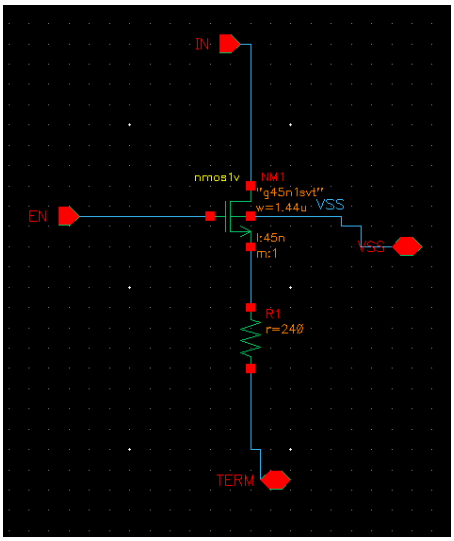

Fig. 28. Resistor bank segment schematic

Figure 29 shows the resistor bank along with adding DC offset. Two resistor banks were used for RX_IN and RX_INB.

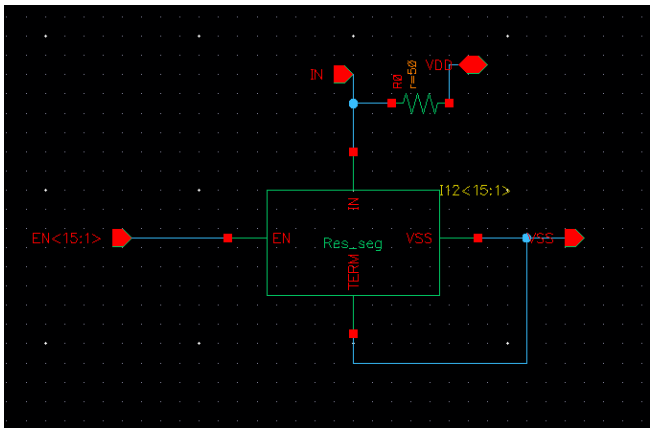

Fig. 29. Resistor bank schematic

B. Strongarm latch, T/H switch

Figure 30 shows the strongarm latch design, outputs are pre-charged to VDD during reset phase.

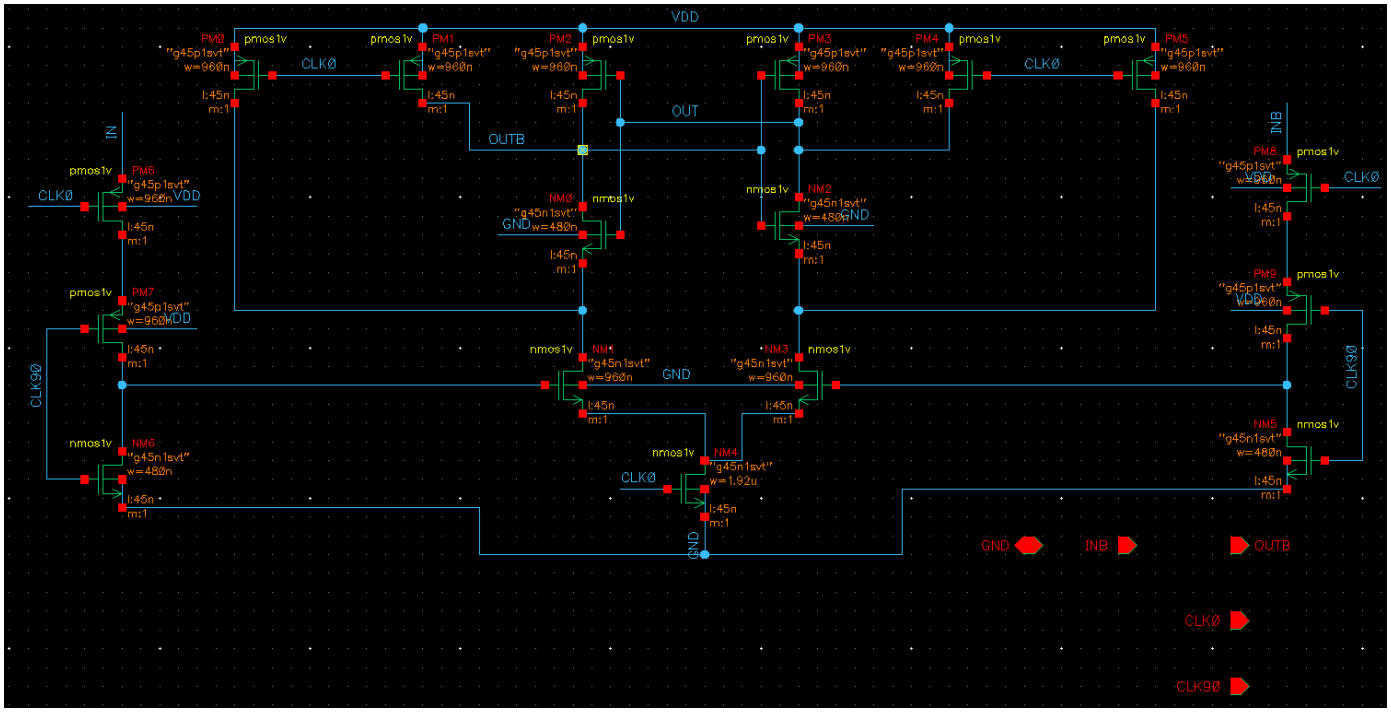

Fig. 30. Strongarm latch schematic

The T/H switch schematic is shown in Figure 31. SR latch was implemented using 2 NAND gates. NAND gate design can be found in appendix (same design as TX).

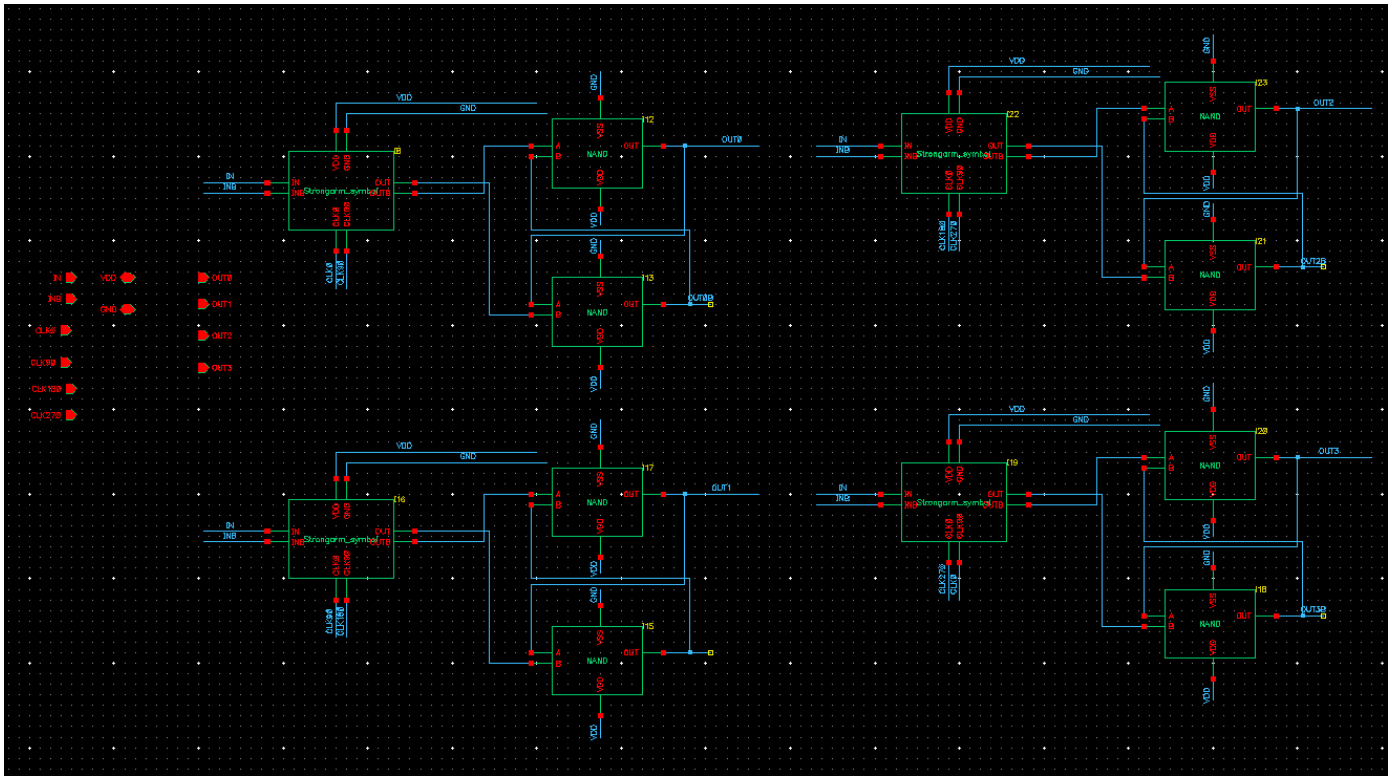

Fig. 31. Slicer circuit schematic

C. *Synchronizer*

Figure 32 shows the synchronizer. D0 and D1 are first synchronized with CLK0 then D0, D1, D2 and D3 are synchronized to CLK180. DFF design can be found in appendix (same design as TX).

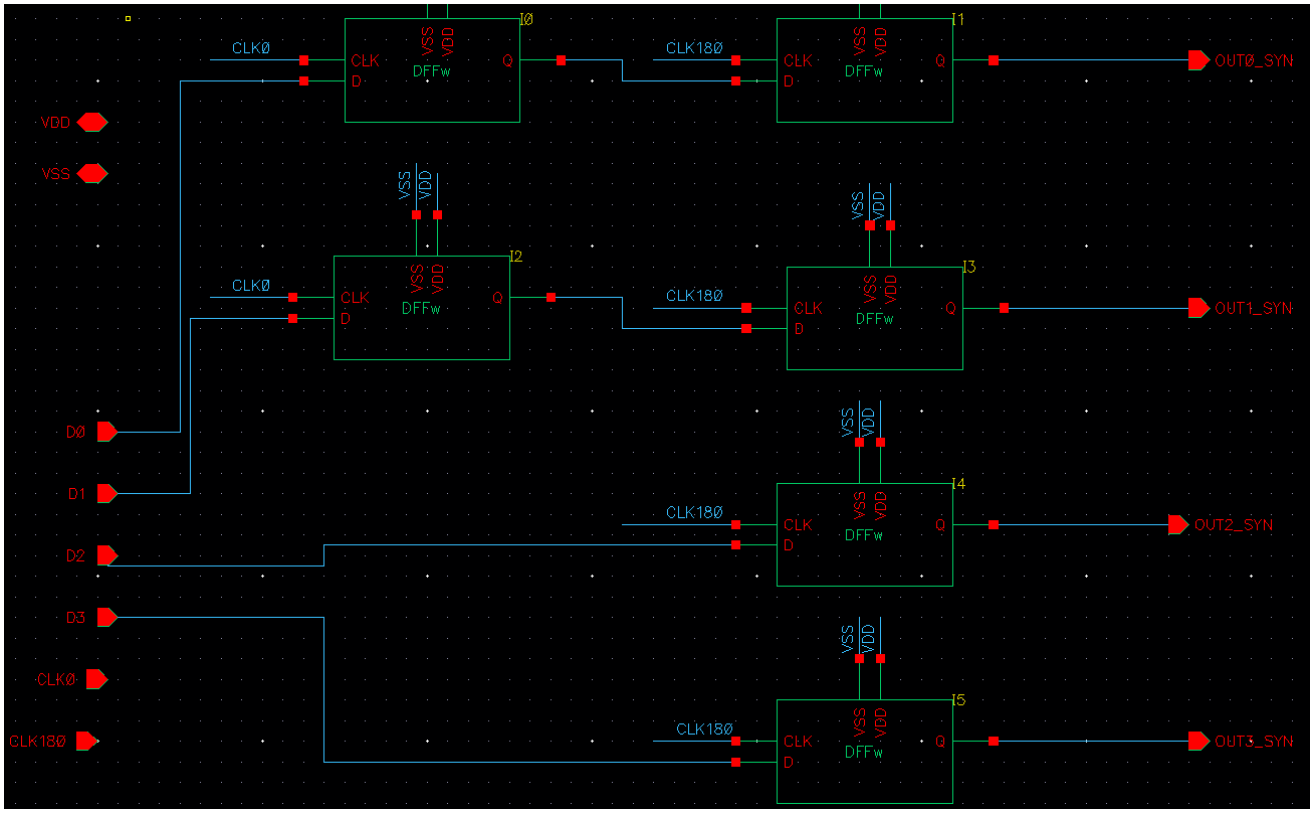

Fig. 32. Synchronizer circuit schematic

D. Clock buffers

The maximum capacitance load for each clock in our RX design was 14.83fF, which is lower than the constraint of 20fF. Because of that, custom design wasn't needed. The clock buffers are simple CMOS buffers (same design as TX pre-driver).

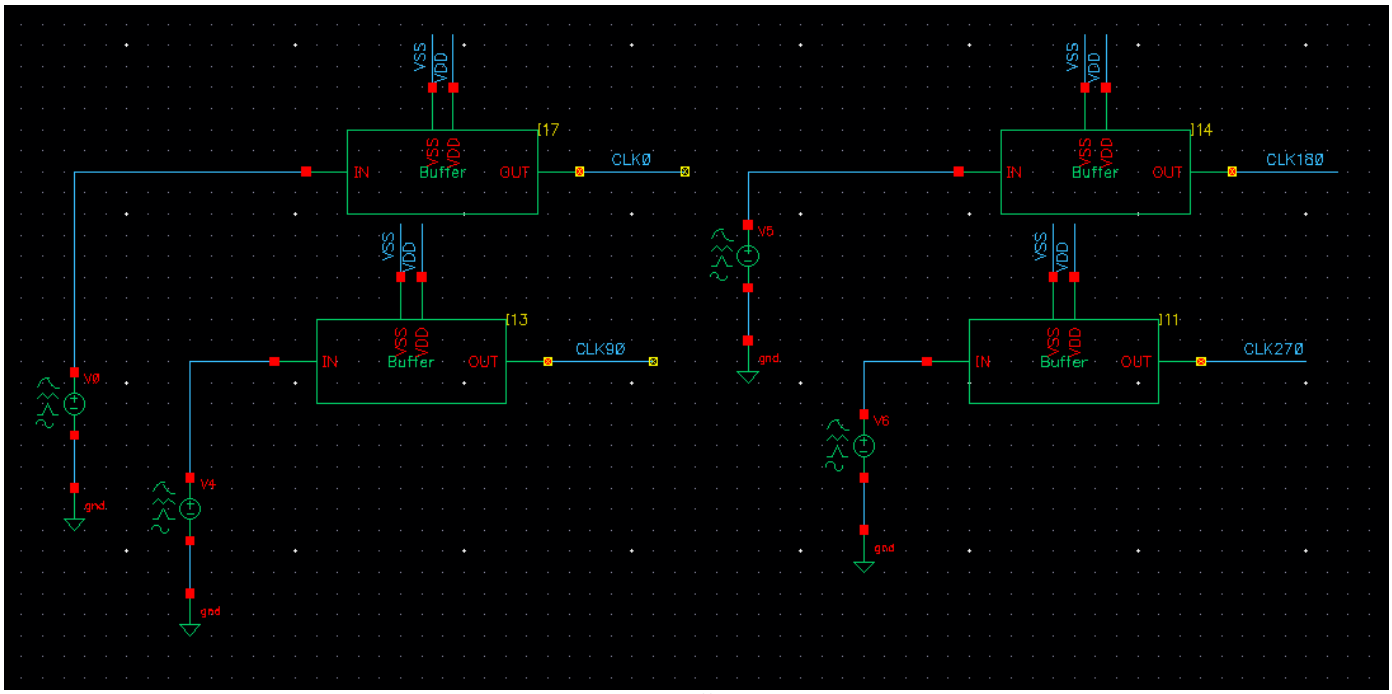

Fig. 33. RX clock buffer circuit schematic

VII. RX ANALYSIS

A. Transient waveform for data alternating transition

Figure 34 shows the RX output for data alternating transition. OUT0-4 is the unsynchronized output and OUT0-4_syn is the synchronized output.

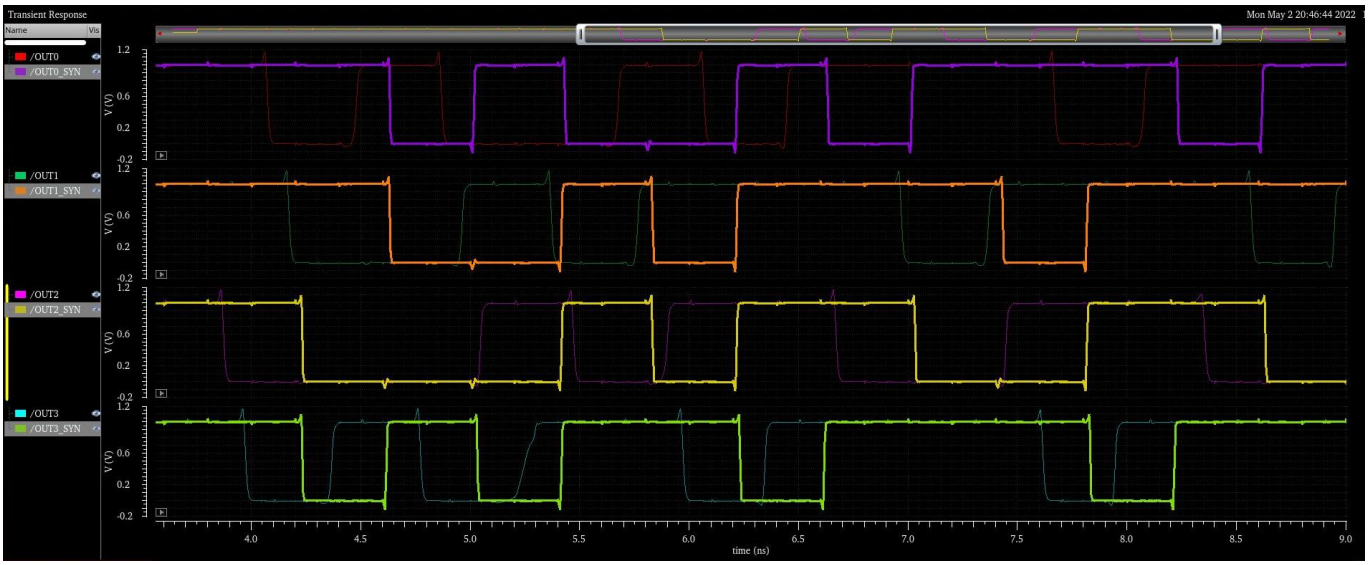

Fig. 34. 6UI RX data alternating transition output

B. Worst case data sequence recovery

Figure 35 shows the worst case 0 data sequence recovery.
The worst case 0 data sequence (found in Figure 4):
1000000010000000100000000000010100000000010000010001001000000000110110001101001000000000110000100101010 1

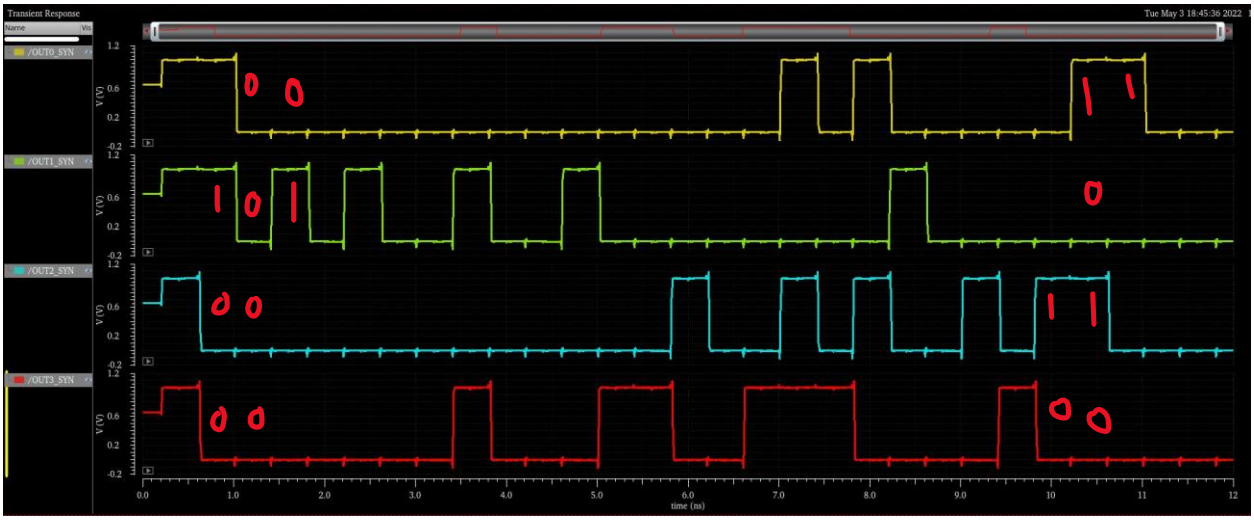

Fig. 35. Worst case 0 data sequence recovery

Figure 36 shows the worst case 1 data sequence recovery.
The worst case 1 data sequence (found in Figure 3):
0111111101111111011111111111010111111111011111011101101111111100100111001011011111111001111011010101 0

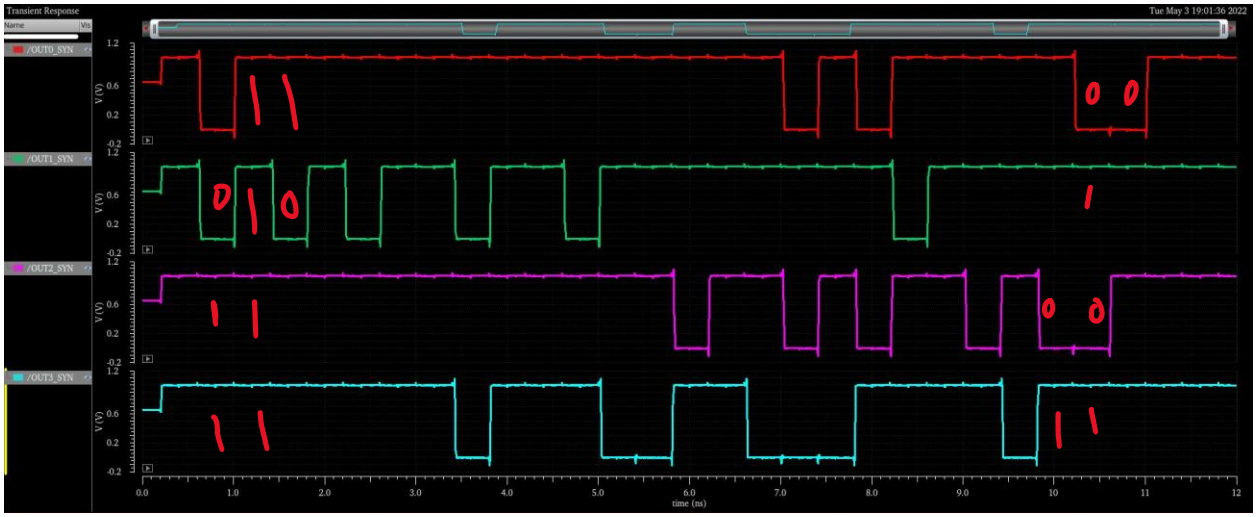

Fig. 36. Worst case 1 data sequence recovery

C. PRBS7 error checker output

Figure 37 shows the error checker output when four PRBS7 data sequences are used as input.

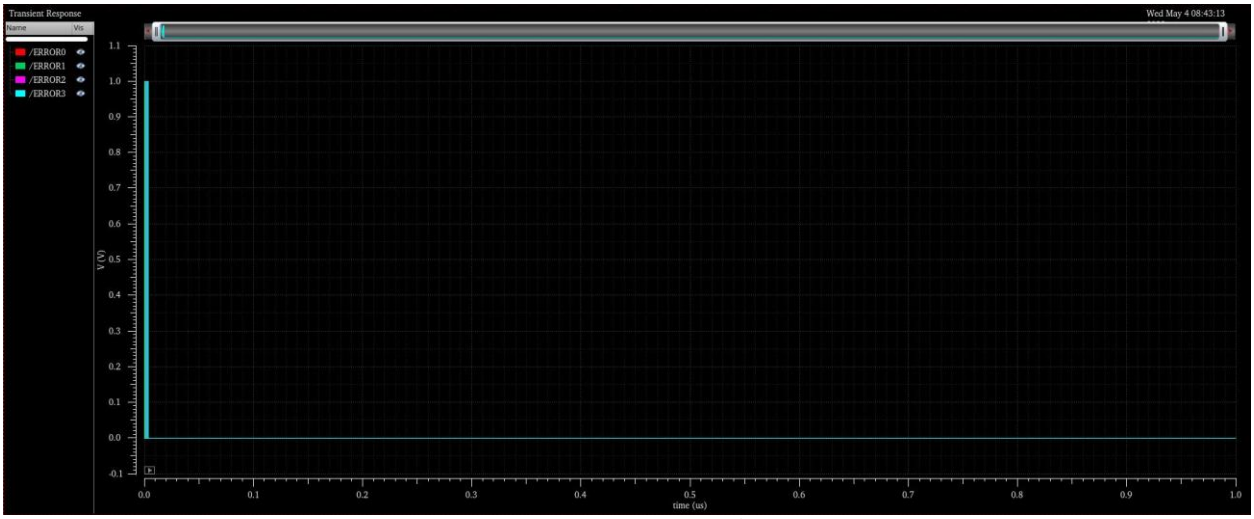

Fig. 37. PRBS7 error checker output for 10000UI

D. *Input impedance tuning range*

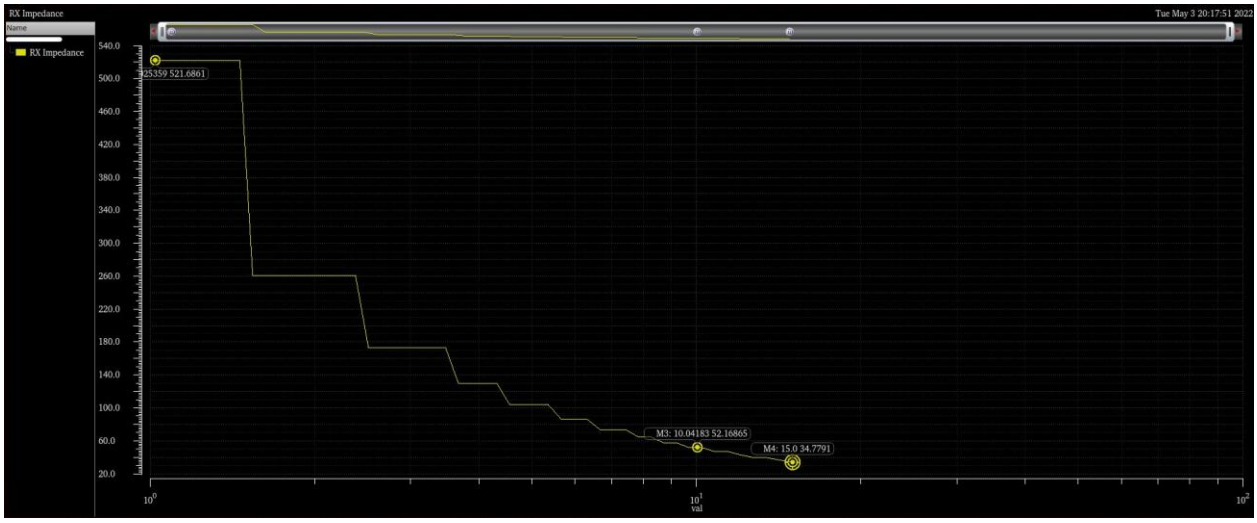

Fig. 38. RX Input impedance tuning range

When only 1 resistor segment is enabled, we have an input impedance of 521 Ohms. When we enable 10 segments, we get impedance around 50 Ohms, which is the ideal number of segments. When we enable all 15 segments, we get impedance of 34.7 Ohms, giving us a good amount of tuning range.

VIII. POWER BREAKDOWN/SPECIFICATIONS

A. *TX power breakdown*

Average power was calculated by averaging power consumption of a 100n transient simulation using PRBS inputs.

	Serializer	Pre-driver	VM driver + EQ	Clock buffers	Total
Average power	58.32µW	54.39µW	6.21mW	68.42µW	6.39mW
Energy/bit	5.832e-15J/bit	5.439e-15J/bit	6.21e-13J/bit	68.42e-15J/bit	6.39e-13J/bit

Table 1. TX average power

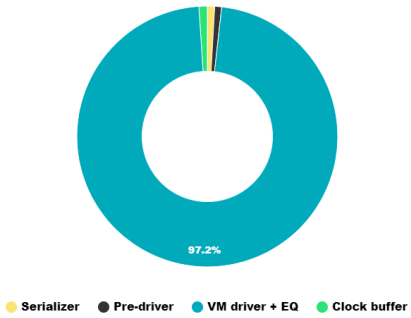

Figure 39. TX power breakdown

B. RX power breakdown

	Resistor bank + DC bias	T/H switch	Synchronizer	Clock buffers	Total
Average power	1.84mW	103.4µW	11.98µW	42.1 µW	1.998mW
Energy/bit	1.84e-13J/bit	1.03e-14J/bit	1.2e-15J/bit	4.21e-15J/bit	1.998e-13J/bit

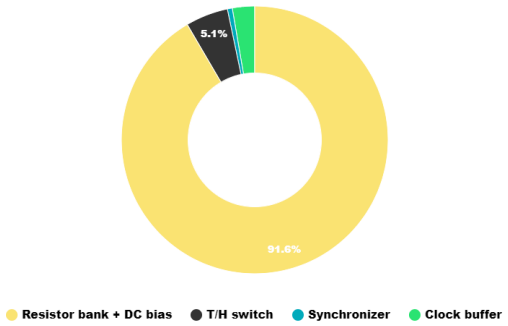

Figure 40. RX power breakdown

C. Specifications

Voltage/Current sources

	Frequency	Magnitude
CLK2 (serializer)	5Hz	0V, 1V
CLK2B (serializer)	5Hz	0V, 1V
CLK4 (serializer)	2.5Hz	0V, 1V
CLK4B (serializer)	2.5Hz	0V, 1V
VDD (used for all circuit VDD supplies and DC bias)	DC	1V
VDD2 (used for RX resistor bank enable)	DC	2V
CLK0	2.5Hz	0V, 1V
CLK90	2.5Hz	0V, 1V
CLK180	2.5Hz	0V, 1V
CLK270	2.5Hz	0V, 1V
VSS (used for all circuit VSS supplies)	DC	0V

Specifications

Overall power consumption	Overall energy/bit	TX impedance tuning range	RX impedance tuning range	MOSFET technology
8.39mW	8.39e-13J/bit	34.7Ω - 1.35kΩ	34.7Ω - 521.6Ω	gpdk45nm

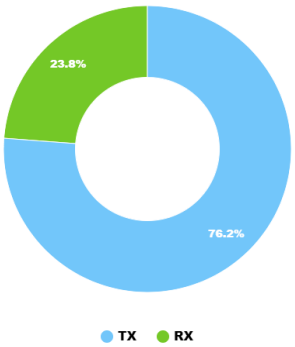

Figure 41. Overall power breakdown

Transistor size

	Min	Max
PMOS	W = 120nm, L = 45nm	W = 2.4µm, L = 45nm
NMOS	W = 120n, L = 45nm	W = 1.92µm, L = 45nm

IX. Appendix

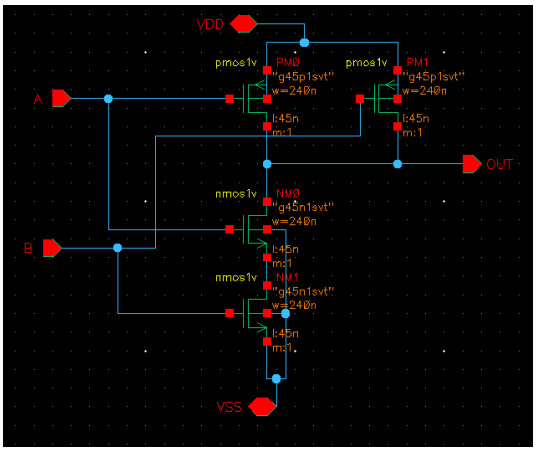

Fig. 42. NAND gate schematic

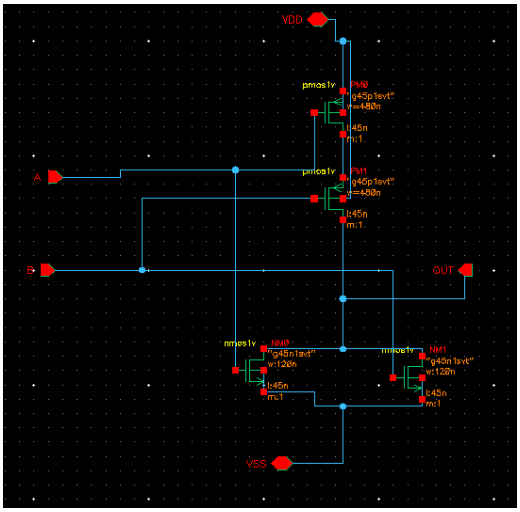

Fig. 43. NOR gate schematic

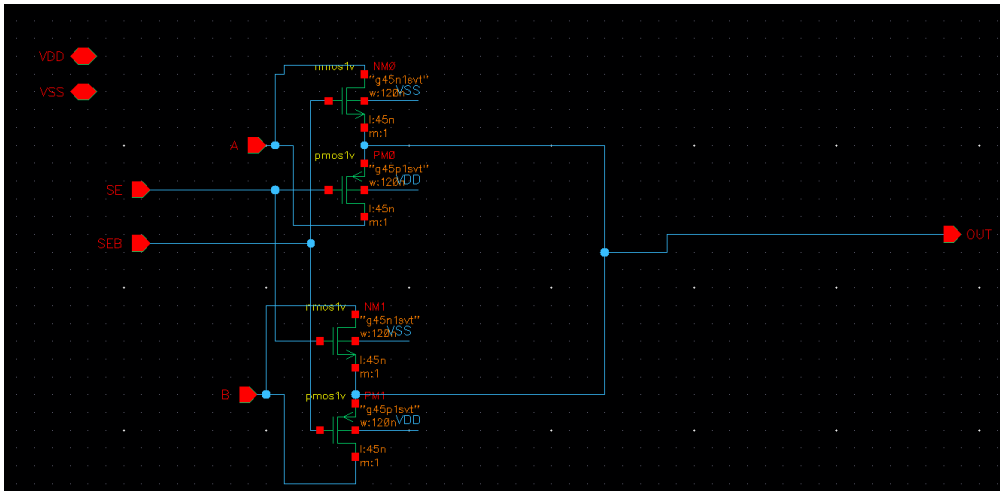

Fig. 44. Multiplexer schematic

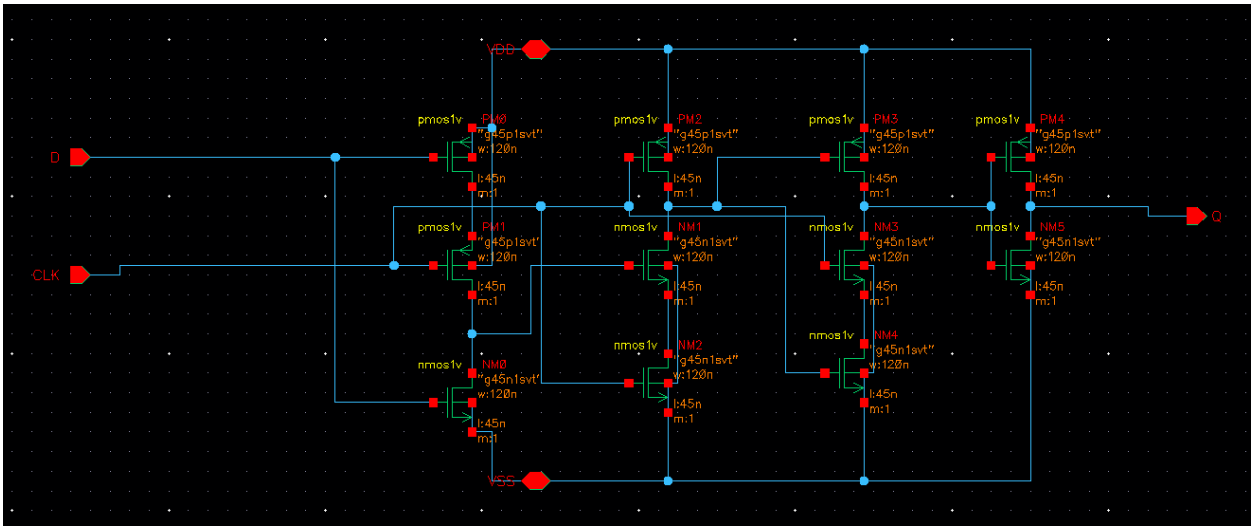

Fig. 45. DFF schematic [1]

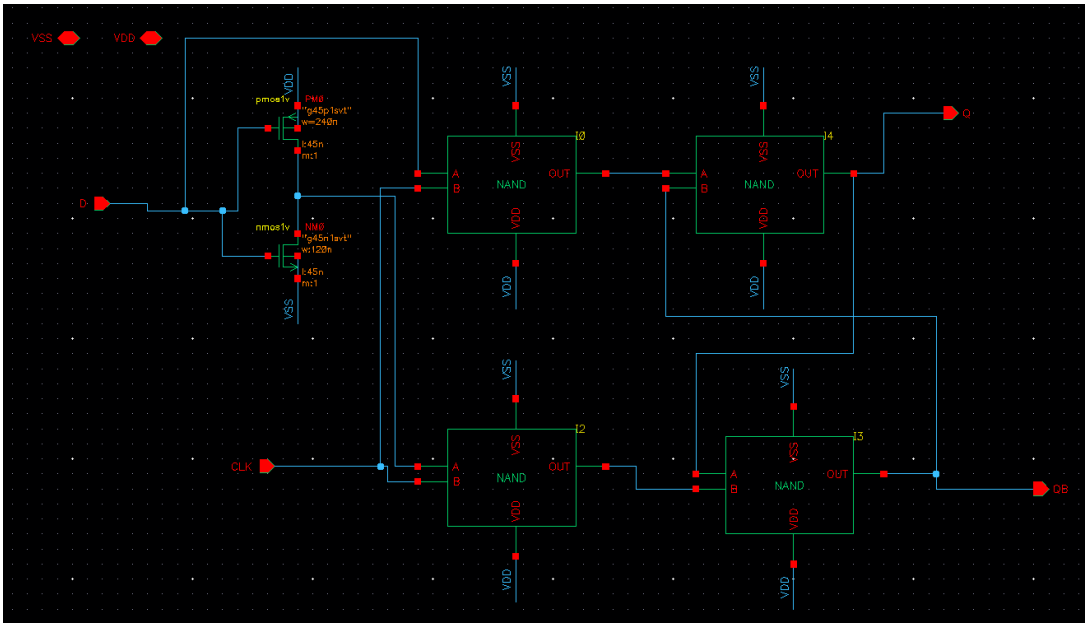

Fig. 46. Latch schematic

X. REFERENCES

[1] Prathamesh G. Dhoble, Avinash D. Kale, and Maharashtra P. R. Patil. Design high speed conventional d flip-flop using 32nm cmos technology. International Journal for Innovative Research in Science and Technology, 1:178–184, 2015.