

ELEC402 Assignment4 – NAND3 Simulation and Layout

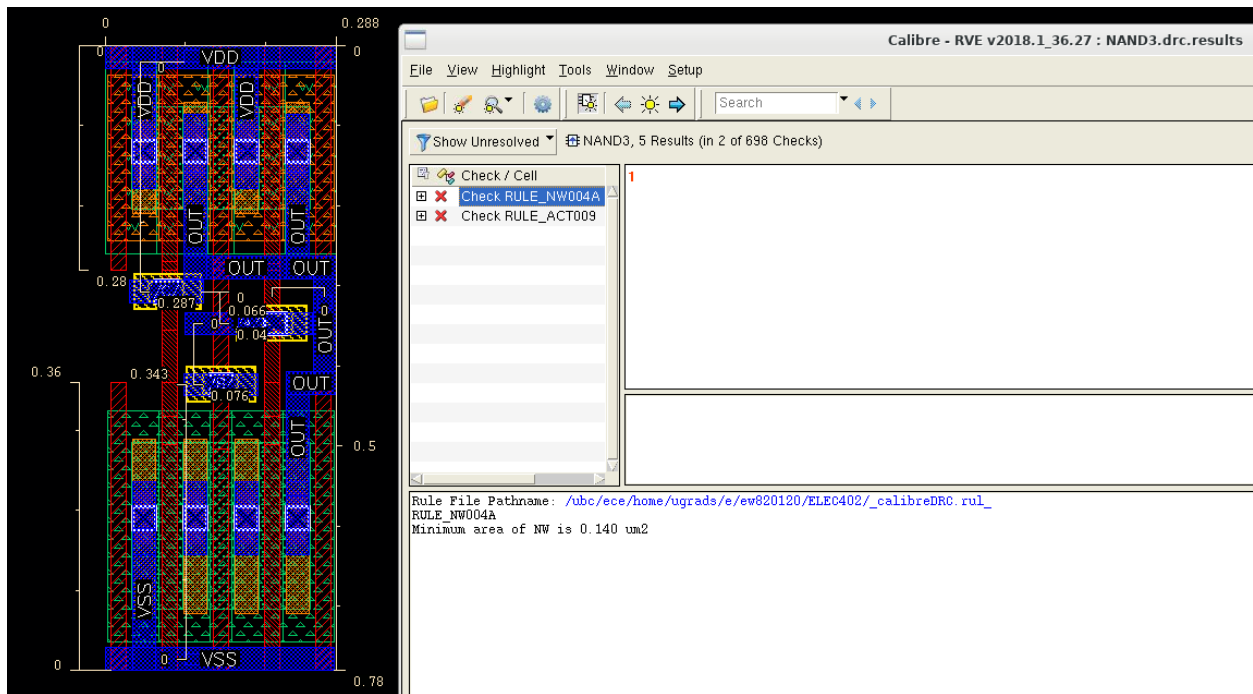
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1. NAND3 Simulation & Layout

Area/delay:

Area	Delay (tphl)	Delay (tplh)	Area x Delay(ave)
$0.22464\mu m^2$	17.036ps	13.71ps	$3.453\mu m^2ps$

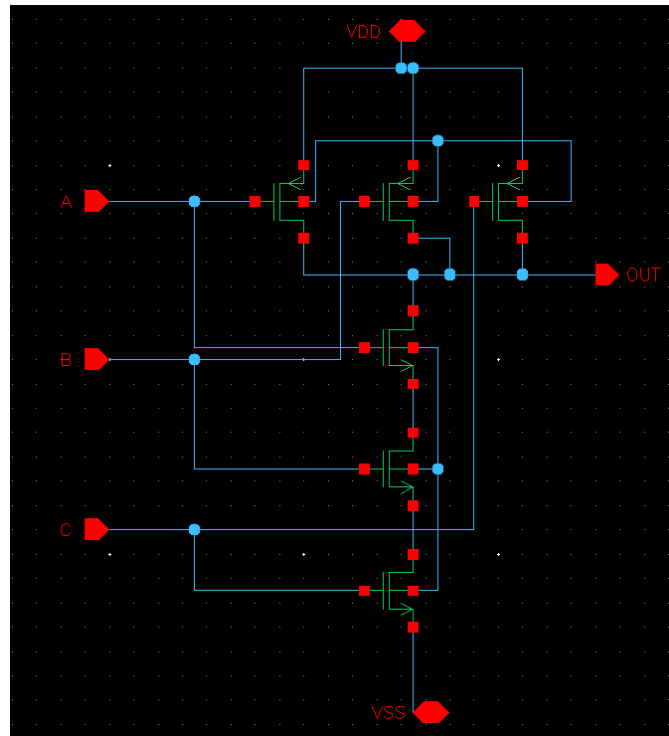
Layout + DRC results:



To get equal tphl and tplh, PMOS fins were set to 4 and NMOS fins were set to 6.

The width was $0.28\mu m$ and $0.36\mu m$ respectively.

Schematic for LVS:



LVS results:

Calibre - RVE v2018.1_36.27 : svdb NAND3

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- LVS Report

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Extraction Results

Layout Cell / Type	Source Cell	Nets	Instances	Ports
NAND3	NAND3	8L, 8S	1L, 1S	6L, 6S

Cell NAND3 Summary (Clean)

```
#####  
#          #          #          #          #  
#          #          #          #          #  
#          #          #          #          #  
#          #          #          #          #  
#          #          #          #          #  
#####
```

LAYOUT CELL NAME: NAND3
SOURCE CELL NAME: NAND3

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	6	6	
Nets:	10	10	
Instances:	3	3	NI (4 pins)
	3	3	MP (4 pins)
Total Inst:	6	6	

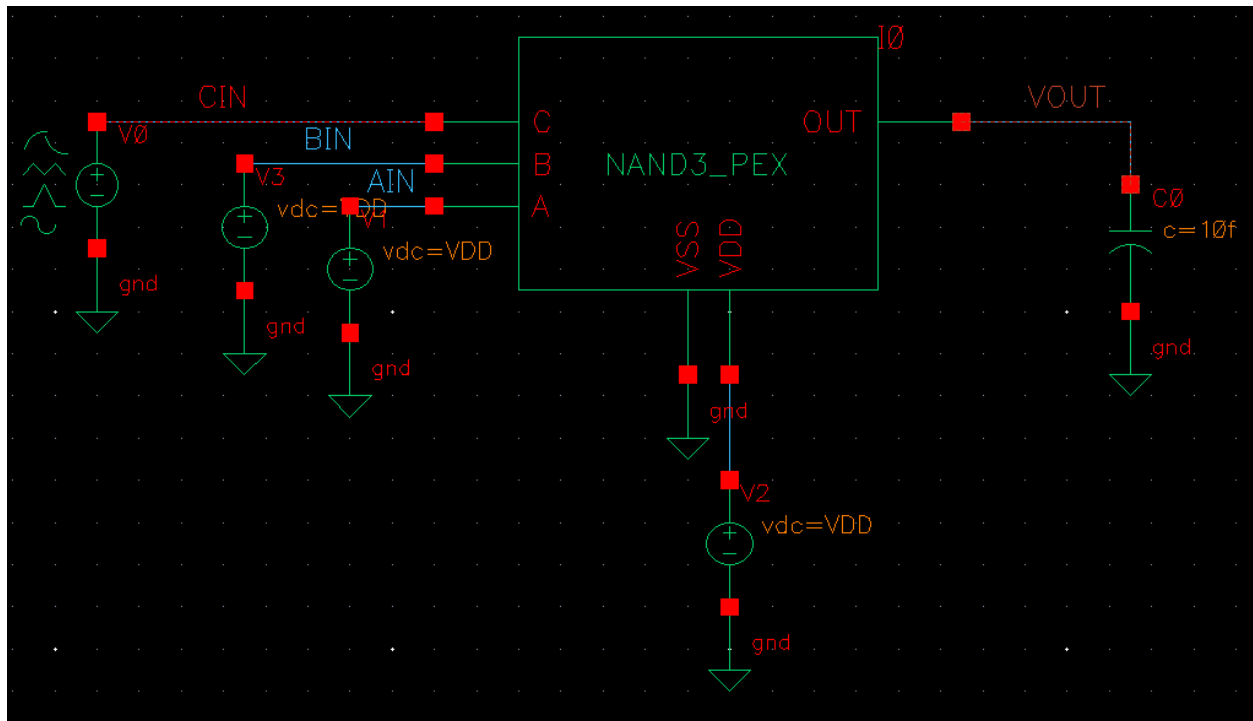
PEX Netlist File - NAND3.pex.netlist

```
PEX Netlist File - NAND3.pex.netlist
File Edit Options Windows

* VDD VDD
* A A
* B B
* VSS VSS
* C C

NM4 NET1 B NET2 NET6 NETET L=2e-08 W=2.08e-07 NFIN=6 ADEJ=2.112e-15
+ ASEJ=2.112e-15 PDEJ=5.76e-07 PSEJ=5.76e-07
NM5 NET2 C N VSS NM5+ NET6 NETET L=2e-08 W=2.08e-07 NFIN=6 ADEJ=1.056e-15
+ ASEJ=9.12e-16 PDEJ=2.64e-07 PSEJ=2.28e-07
NM3 N OUT NM3 d A NET1 NET6 NETET L=2e-08 W=2.08e-07 NFIN=6 ADEJ=1.824e-15
+ ASEJ=1.056e-15 PDEJ=5.04e-07 PSEJ=2.64e-07
NM1 N OUT MM2 d B N VDD MM1+ NET3 PEET L=2e-08 W=1.28e-07 NFIN=4 ADEJ=1.408e-15
+ ASEJ=1.408e-15 PDEJ=3.84e-07 PSEJ=3.84e-07
NM2 N OUT MM2 d C N VDD MM1+ NET3 PEET L=2e-08 W=1.28e-07 NFIN=4 ADEJ=7.04e-16
+ ASEJ=7.04e-16 PDEJ=3.36e-07 PSEJ=1.76e-07
MM0 N OUT MM0 d A N VDD MM1+ NET3 PEET L=2e-08 W=1.28e-07 NFIN=4 ADEJ=2.112e-15
+ ASEJ=7.04e-16 PDEJ=3.36e-07 PSEJ=1.76e-07
C 8 C VSS O 0219681f
C 17 NET2 VSS O 023649f
C 22 B VSS O 0266234f
C 29 A VSS O 0203244f
C 34 NET1 VSS O 023643f
*
#include "NAND3.pex.netlist NAND3.pxi"
*
.ends
*
```

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466	467	468	469	470	471	472	473	474	475	476	477	478	479	480	481	482	483	484	485	486	487	488	489	490	491	492	493	494	495	496	497	498	499	500	501	502	503	504	505	506	507	508	509	510	511	512	513	514	515	516	517	518	519	520	521	522	523	524	5
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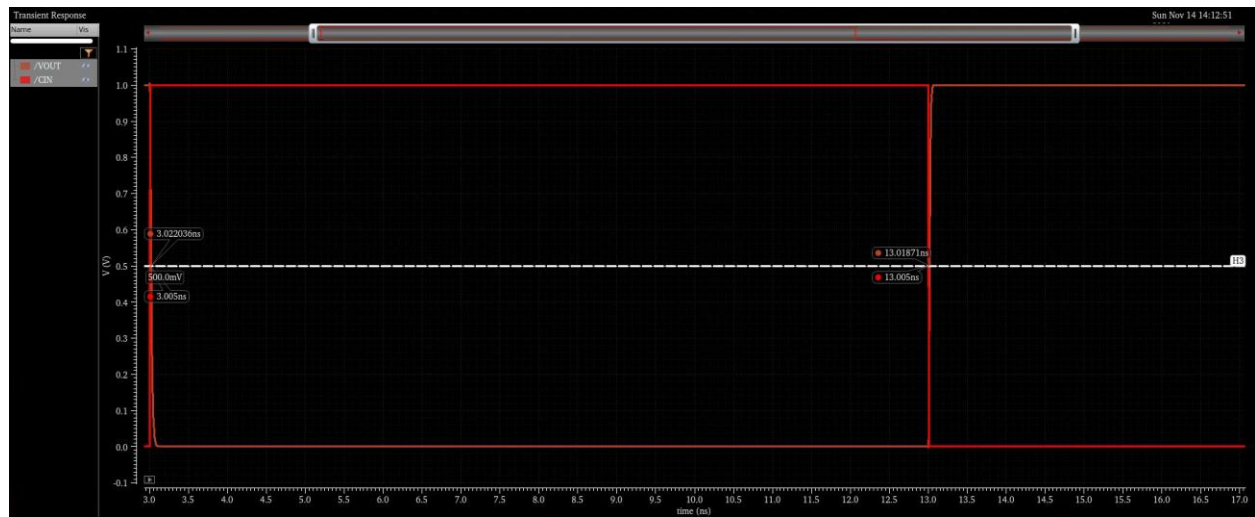


For the pull up network, this transition would only connect one path giving us the WC tpb

For the pull down network, the capacitance in A, B would be charged before the transition and

We will measure `tpll` and `tplh` using the above testbench (toggling `C` between high and low)

WV:



$t_{phl} = 17.036\text{ps}$, $t_{plh} = 13.71\text{ps}$.

The difference is $= 3.326\text{ps}$, which fulfills the requirement $< 5\text{ps}$ difference.

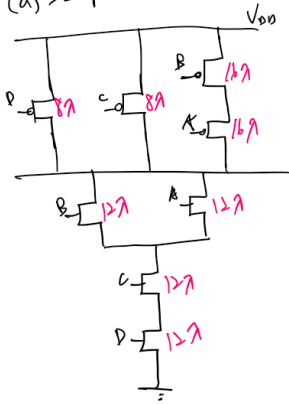
2.

2.

logic function

$$\overline{Y} = (A+B)CD, Y = (\overline{A}\overline{B}) + \overline{C} + \overline{D}$$

(a) sizing



WC_{pu} = only AB branch

WC_{pd} = ACD or BCD

(b)

Worst case t_{PHL}:

WC transition would be when parallel transistors only have one path that's conducting.

⇒ ABCD → ABCD would be the WC transition because if D was originally 0110 → 0111

opp, all the other nodes would have to discharge after the transition.

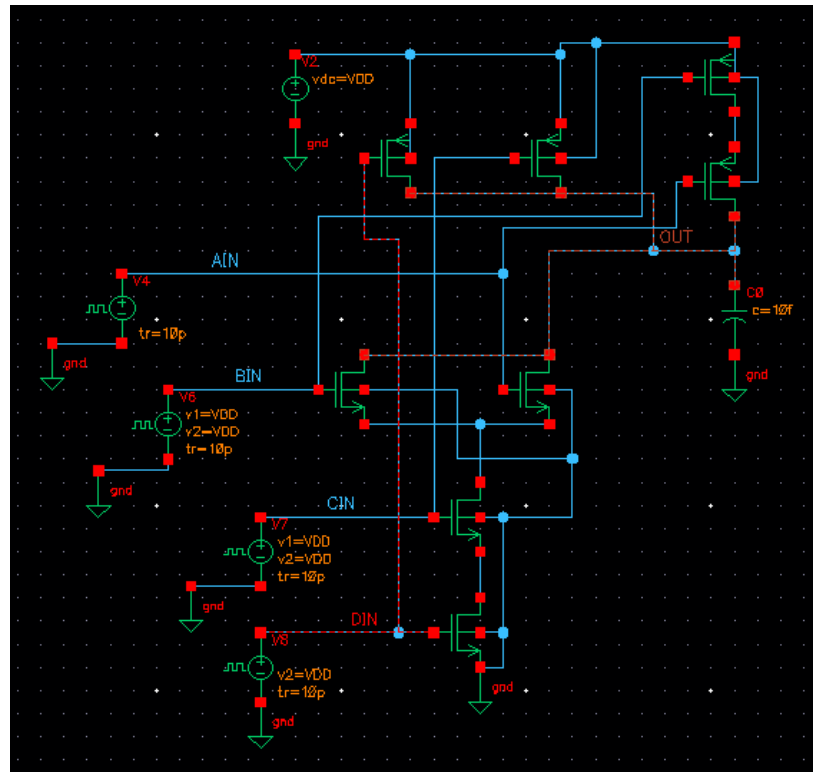
Worst case t_{PLH}:

Using the same logic as above:

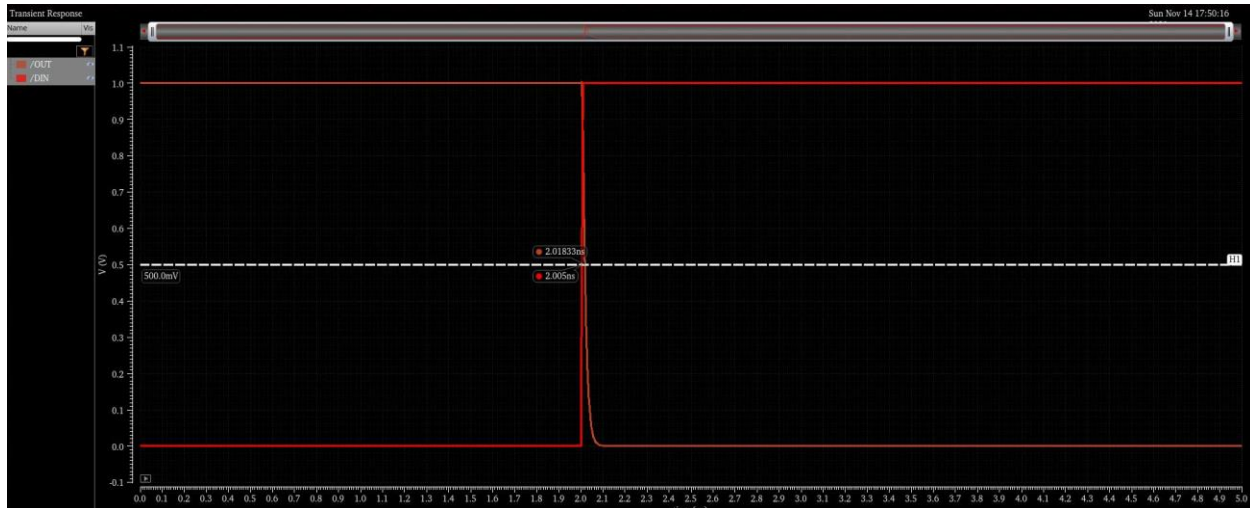
WC transition: ABCD → 0011

This is the case that the most nodes will have to charge.

Tphl test bench schematic (sizing was achieved using $2\lambda = 1 \text{ fin}$):

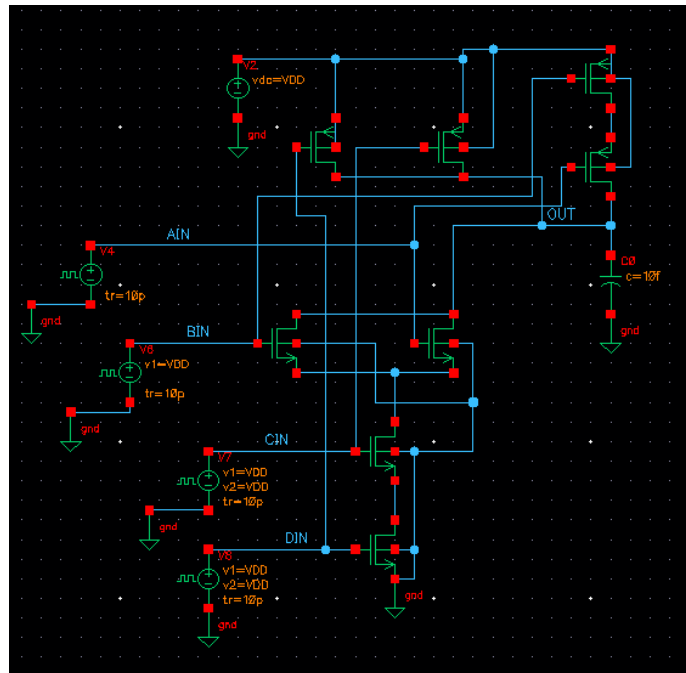


Tphl WV results:

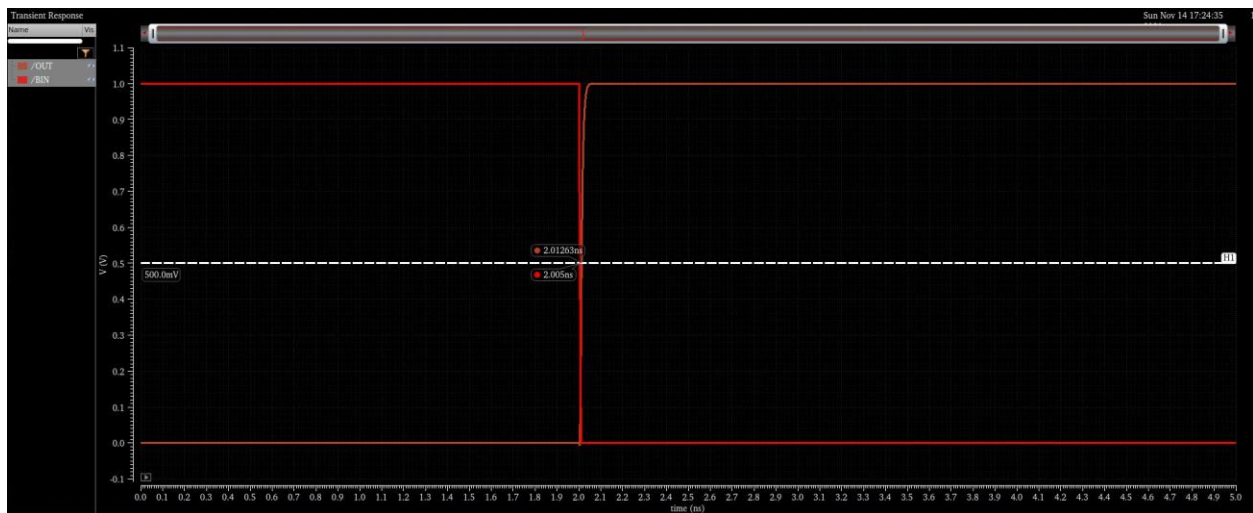


From the results waveform, we can see that the tphl is 13.33ps.

Tplh testbench schematics (sizing was achieved using $2\lambda = 1 \text{ fin}$):



Tplh WV results:



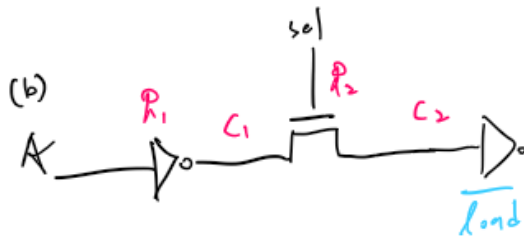
From the results waveform, we can see that the tplh is 7.63ps.

3.

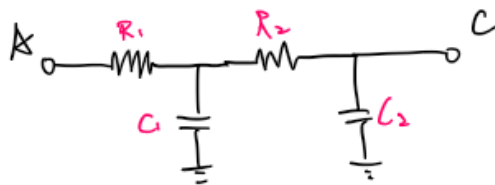
3(a)

$$\overline{OUT} = C = \overline{A}(sel + sel\overline{B}) + \overline{B}(sel + sel\overline{A})$$

$$OUT = \overline{\overline{A}(sel + sel\overline{B}) \overline{B}(sel + sel\overline{A})} = (A + (\overline{sel} \overline{sel\overline{B}})) (B + (sel \overline{sel\overline{A}}))$$



↓ eq circuit



$$R_1 = R_{eqn} \times \frac{L}{W} = 12.5k \times \frac{1}{2} = 6.25k \Omega$$

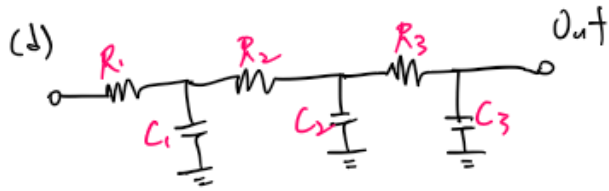
$$R_2 = R_{eqn} \times \frac{L}{W} = 6.25k \Omega$$

$$C_1 = 12n \times C_{eff} + \underbrace{2 \times 4n \times C_{eff} + 4n \times C_g}_{\text{MOS ON (sel = high)}} = 2.4 fF$$

$$C_2 = \underbrace{8n \times C_{eff} + 4n \times C_g}_{\text{MOS ON}} + 12n \times C_g \times f = 1.6 fF + 2.4 fF$$

(c)

$$\tau = R_1 C_1 + (R_1 + R_2) C_2 = 35ps + 30ps$$



$$R_3 = \frac{6.25k}{f}, \quad C_3 = 1.2f \text{ fF} + \underbrace{50 \text{ fF}}_{\text{load}}$$

$$RC \text{ delay} : (R_1 C_1 + R_2 C_2 + R_3 C_3)$$

$$= (15 \text{ ps} + (10 \text{ ps} + 15f \text{ ps})) + (1.5 \text{ ps} + \frac{312.5}{f} \text{ ps})$$

$$= 32.5 \text{ ps} + (15f + \frac{312.5}{f}) \text{ ps}$$

(e) To get smallest delay: minimize $(15f + \frac{312.5}{f})$

$$\frac{d(15f + \frac{312.5}{f})}{df} = 0 \Rightarrow \underline{\underline{f \approx 4.56}}$$

$$\left. \frac{d(15f + \frac{312.5}{f})}{df^2} \right|_{f=4.56} > 0 \Rightarrow \text{local min}$$