ELEC402 Assignment4 – NAND3 Simulation and Layout

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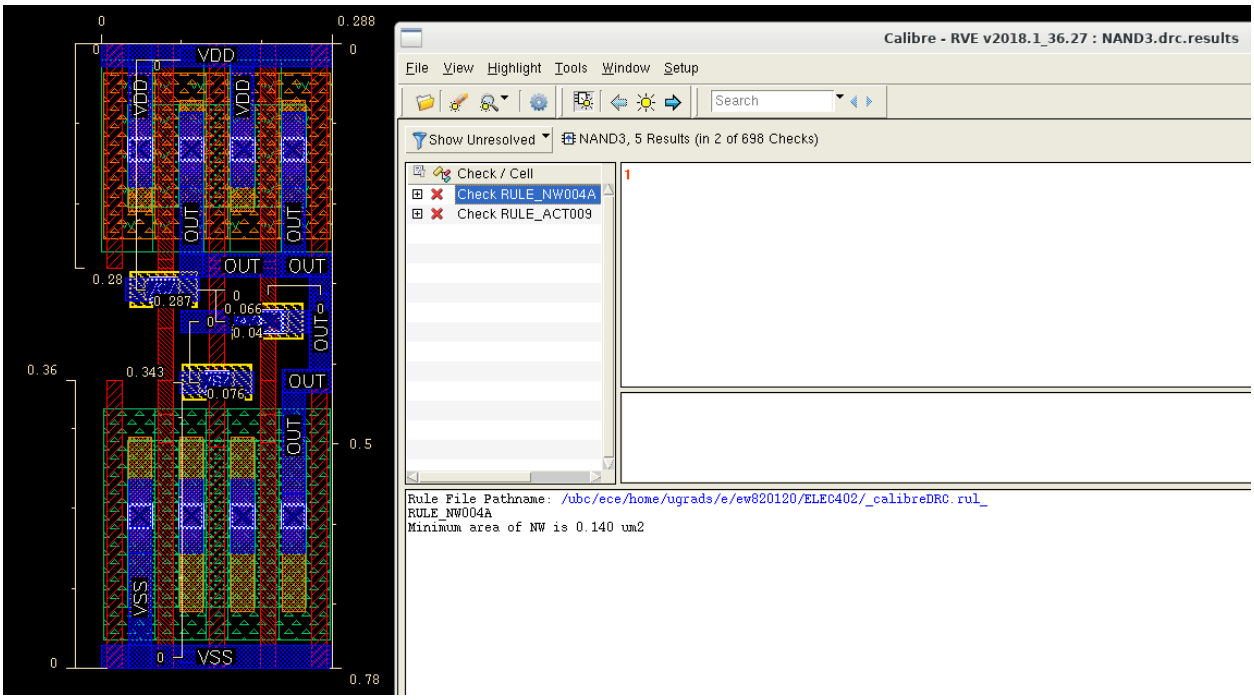
1. NAND3 Simulation & Layout

Area/delay:

Area	Delay (tphl)	Delay (tplh)	Area x Delay(ave)
$0.22464\mu m^2$	17.036ps	13.71ps	$3.453\mu m^2 ps$

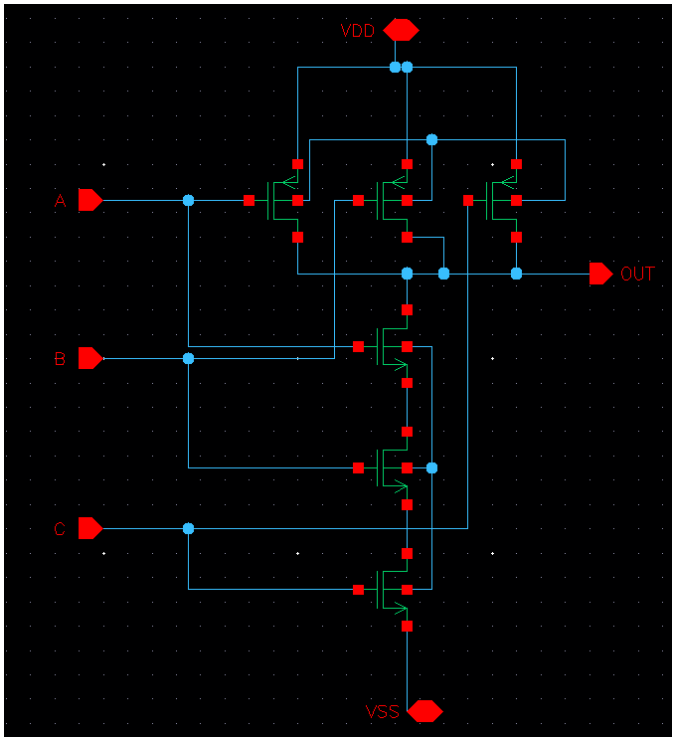
Layout + DRC results:



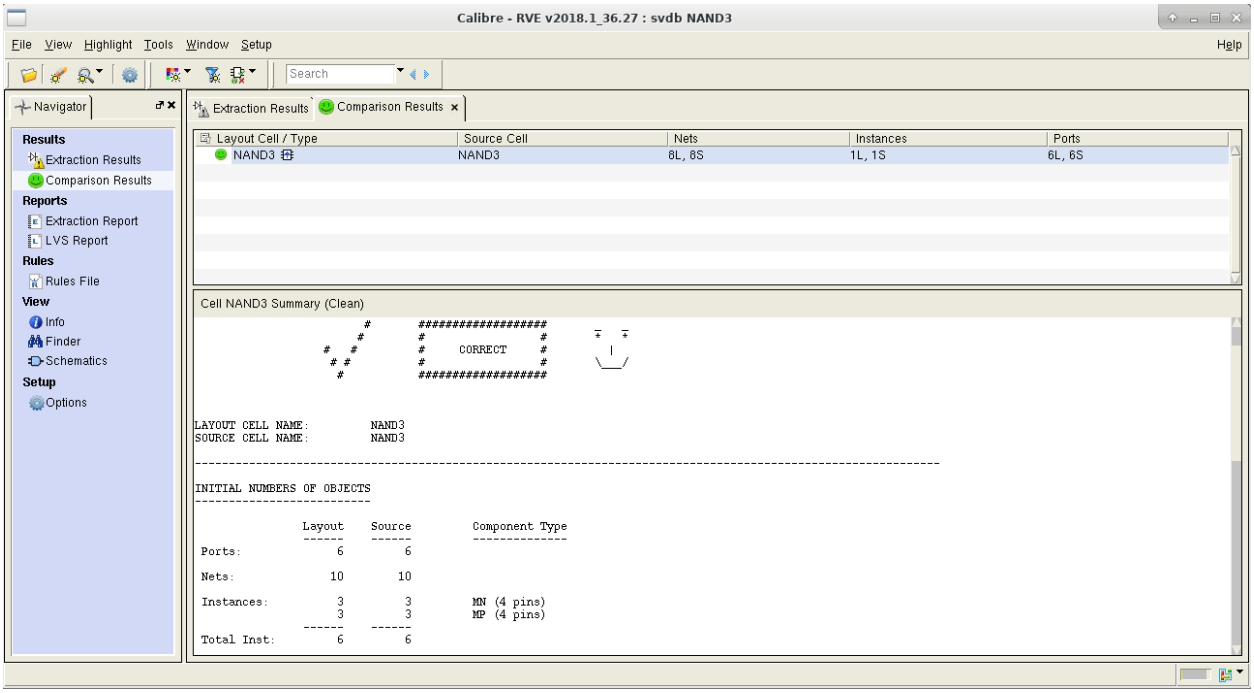
To get equal tphl and tplh, PMOS fins were set to 4 and NMOS fins were set to 6.

The width was $0.28\mu m$ and $0.36\mu m$ respectively.

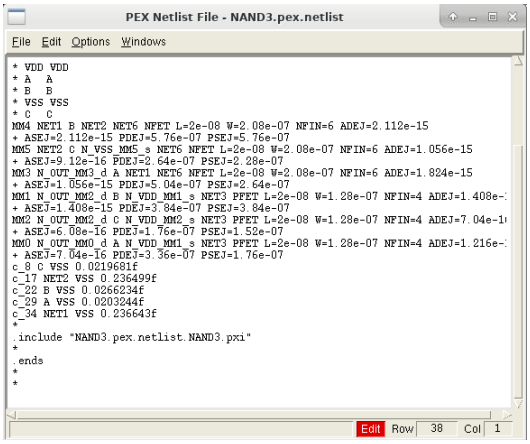
Schematic for LVS:



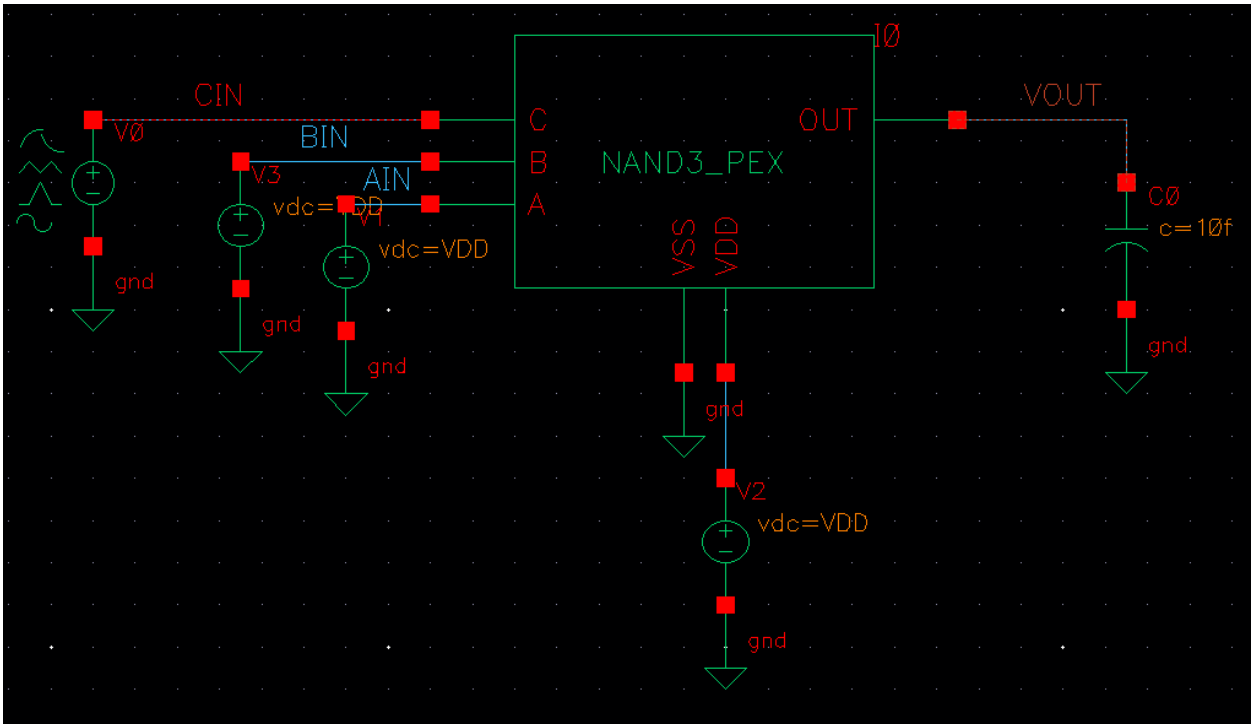
LVS results:



PEX netlist:



Testbench schematic:



The worst-case for tplh would-be A, B = high and C switches from high and low.

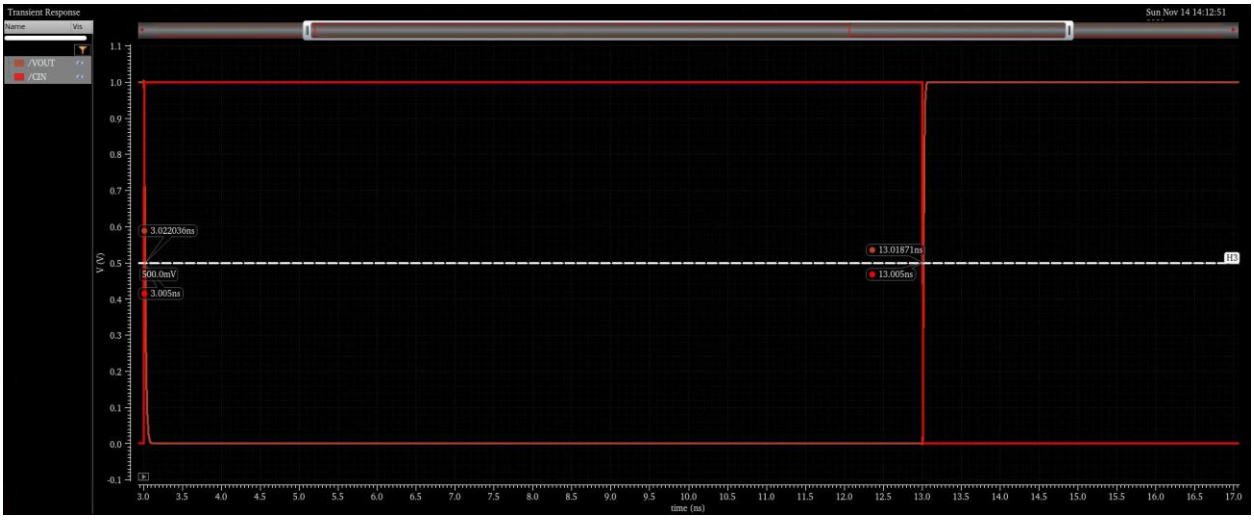
For the pull-up network, this transition would only connect one path giving us the WC tplh.

The worst-case for tplh would-be A, B = high and C switches from low and high.

For the pull-down network, the capacitance in A, B would be charged before the transition and they must discharge after C switches to high, giving us the WC tphl.

We will measure tphl and tplh using the above testbench (toggling C between high and low).

WV:



tphl = 17.036ps, tplh = 13.71ps.

The difference is = 3.326ps, which fulfills the requirement <5ps difference.

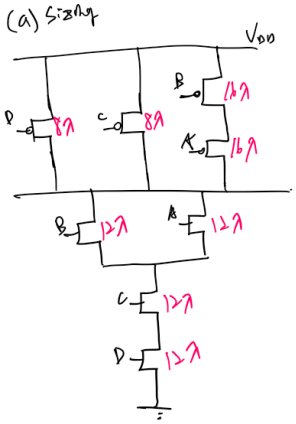
2.

2.

Logic function

$\overline{Y} = (A+B)CD$, $Y = (\overline{A}\,\overline{B}) + \overline{C} + \overline{D}$

(a) Sizing



WC_{pu} = only AB branch

WC_{pd} = ACD or BCD

(b)

Worst case t_{phl}:

WC transition would be when parallel transistors only have one path that's conducting.

⇒ ABCD 0110 → ABCD 0111 would be the WC transition because if D was originally 0PP, all the other nodes would have to discharge after the transition.

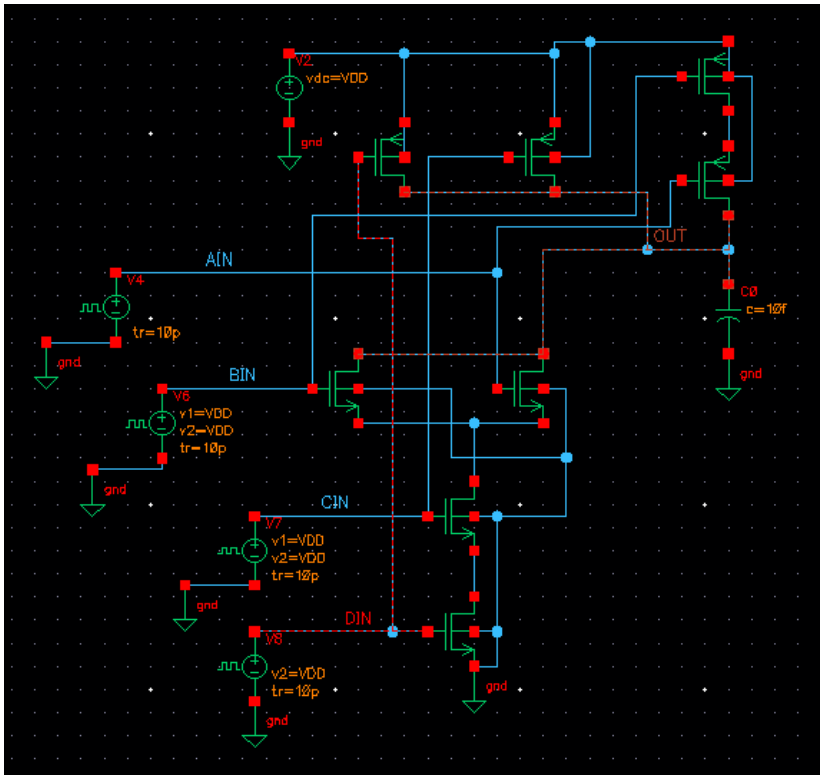
Worst case t_{plh}:

Using the same logic as above:

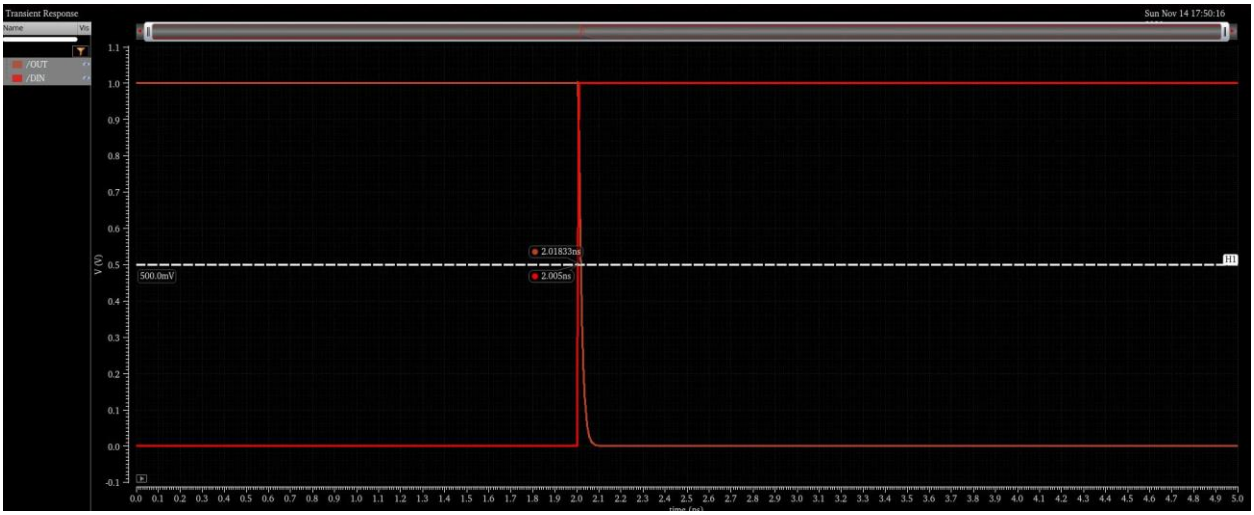
WC transition: ABCD 0111 → ABCD 0011

This is the case that the most nodes will have to charge.

Tphl test bench schematic (sizing was achieved using 2λ = 1 fin):

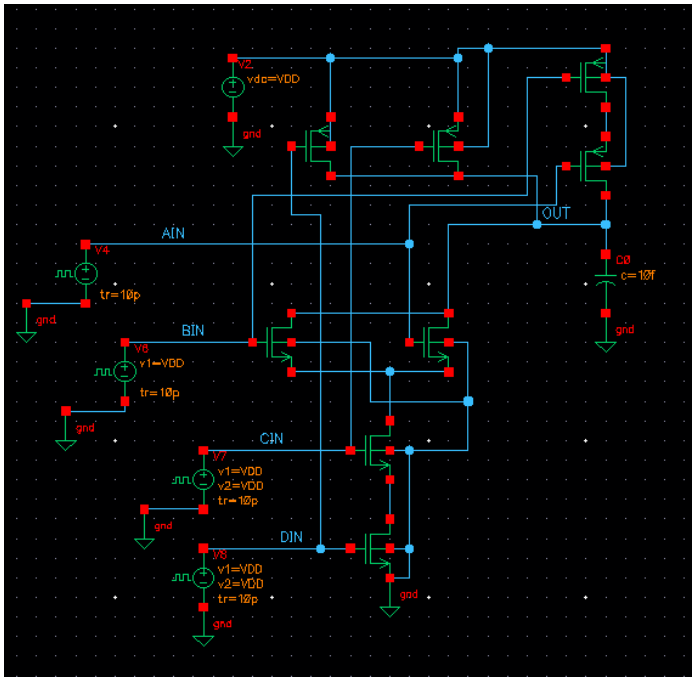


Tphl WV results:

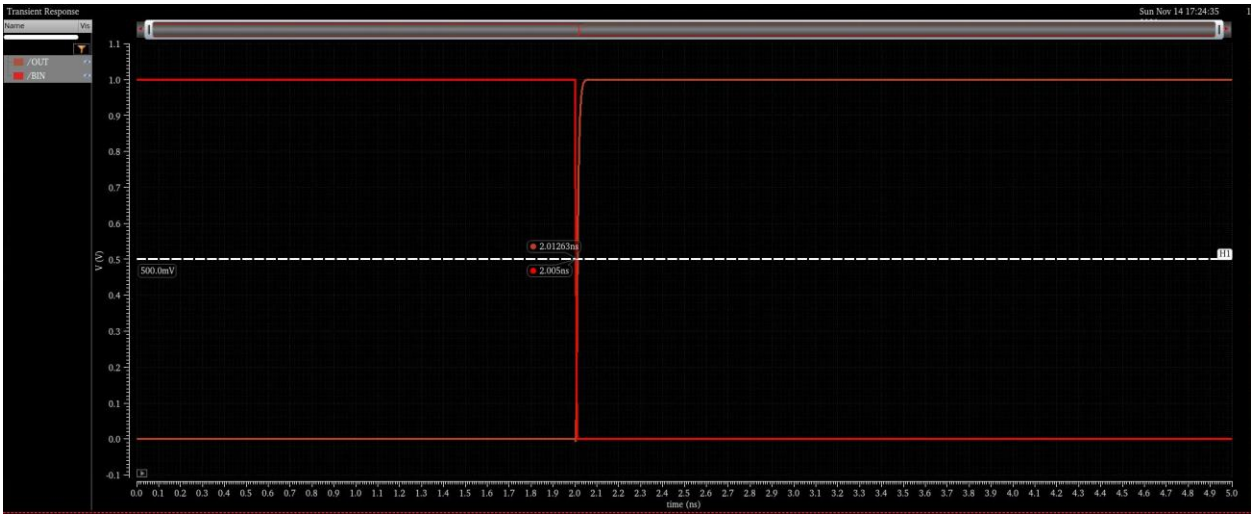


From the results wavefrom, we can see that the tphl is 13.33ps.

Tplh testbench schematics (sizing was achieved using 2λ = 1 fin):



Tphl WV results:



From the results wavefrom, we can see that the tplh is 7.63ps.

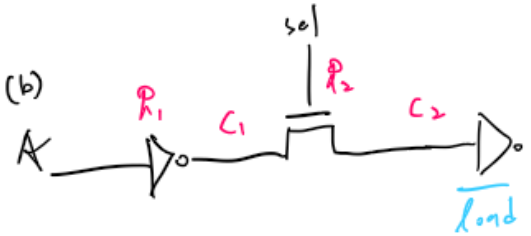
3.

3.(a)

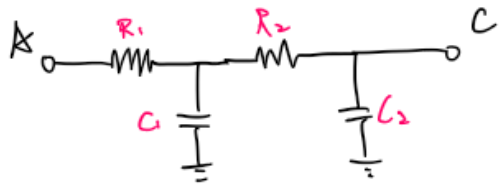
$\overline{OUT} = C = \overline{A}(sel + \overline{sel}\,\overline{B}) + \overline{B}(\overline{sel} + sel\,B)$

$OUT = \overline{\overline{A}(sel + \overline{sel}\,\overline{B})}\;\overline{\overline{B}(\overline{sel} + sel\,B)} = (A + (\overline{sel}\,sel\,B))(B + (sel\,\overline{sel}\,\overline{B}))$

(b)



↓ eq circuit



$R_1 = R_{eqn} \times \frac{L}{W} = 12.5k\Omega \times \frac{1}{2} = 6.25k\Omega$

$R_2 = R_{eqn} \frac{L}{W} = 6.25k\Omega$

$C_1 = 12\lambda \times C_{eff} + \underbrace{2 \times 4\lambda \times C_{eff} + 4\lambda \times C_g}_{\text{Mos ON (sel = high)}}$

$= 2.4fF$

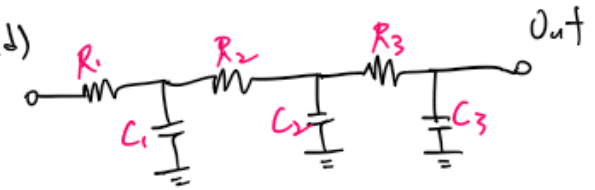
$C_2 = \underbrace{8\lambda \times C_{eff} + 4\lambda \times C_g}_{\text{Mos ON}} + 12\lambda \times C_g \times f$

$= 1.6fF + 2.4f\,fF$

(c)

$\tau = R_1 C_1 + (R_1 + R_2) C_2 = 35ps + 30f\,ps$

(d)



$R_3 = \frac{6.25k}{f}$, $C_3 = 1.2f\,fF + \underbrace{50fF}_{load}$

RC delay: $(R_1C_1 + R_2C_2 + R_3C_3)$

$= (15ps + (10ps + 15f(ps) + (4.5ps + \frac{312.5}{f}ps))$

$= 32.5ps + (15f + \frac{312.5}{f})ps$

(e)

To get smallest delay: minimize $(15f + \frac{312.5}{f})$

$\frac{d(15f + \frac{312.5}{f})}{df} = 0 \Rightarrow f \approx 4.56$

$\left.\frac{d(15f + \frac{312.5}{f})}{df^2}\right|_{f=4.56} > 0 \Rightarrow$ local min