

PIXEL CMOS PROJECT

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MIMOSA26 PROTOTYPE

Technical Documentation Version 0.4

JTAG SOFTWARE

GETTING STARTED

Support:

Web address: <http://www.iphc.cnrs.fr/-CMOS-ILC-.html>

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Important Information

Warranty:

The MIMOSA26 test board is warranted against defects in material and workmanship for a period of one year from the date of shipment, as evidence by receipts or other documentation. IPHC laboratory will, at its option, repair or replace equipment that proves to be defective during the warranty period. This warranty includes parts and labor.

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About this manual

This is a short description for initiation of using the JTAG software for MIMOSA26 device.

Modifications Chronology

VERSION	MODIFICATIONS	CHAPTERS
0.1	Creation of the document.	All
0.2	Changes in graphical user interface (GUI)	All
0.3	Power pulsing	All
0.4	Power pulsing detailed	All

1. Getting Started

This document is a short description for initiation of using the JTAG software for a MIMOSA26 prototype test system. All the necessary hardware installation should be done before starting with this document.

The software is archived with the WinZip program.

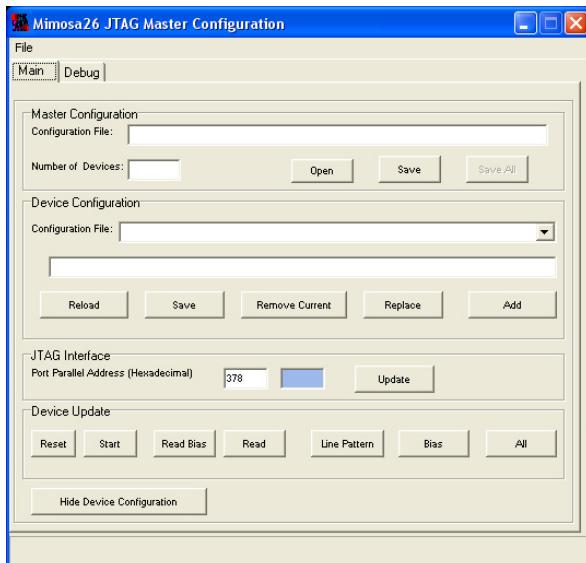
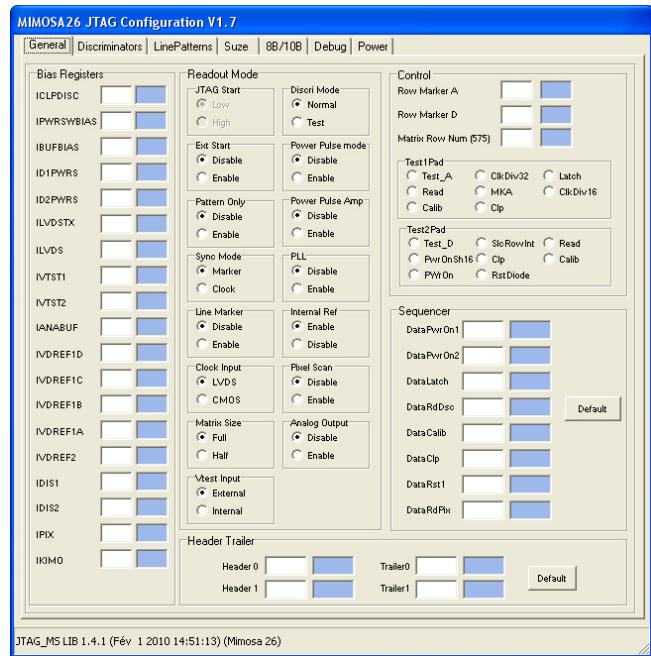
MINIMUM SYSTEM REQUIREMENTS FOR PC

- Pentium IV, 2 GHz or faster
- Microsoft Windows XP
- 256 MB RAM min. (512 MB recommended)
- CD-ROM driver
- 100 MB free hard disk place for software installation
- AGP video card with 64MB video RAM

To use this software, the MIMOSA26 prototype test system should be connected to PC's parallel port and all the necessary power supplies should be connected and powered.

2. Software installation

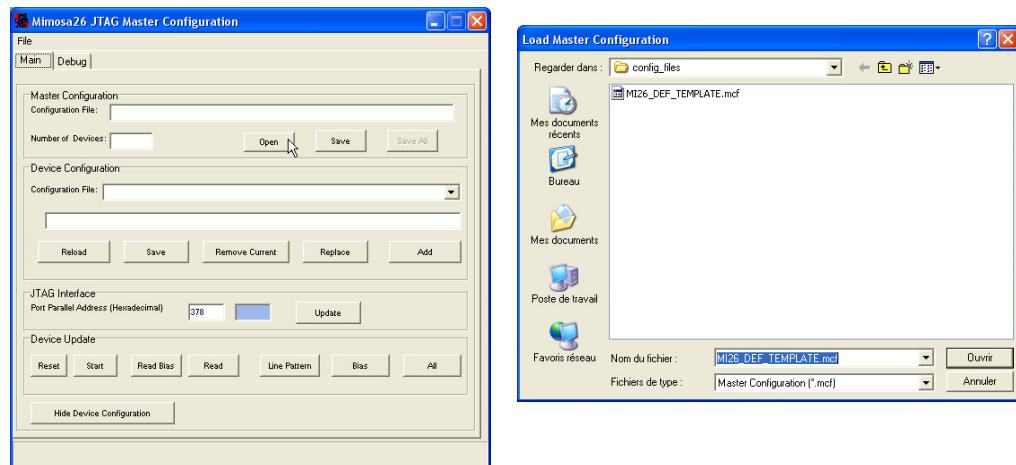
1. All the files for the MIMOSA26 JTAG SOFTWARE are packed in a file **MIMOSA26_MULTI_JTAG.zip**. To start, create a directory C:\CCMOS_SCTRL\ and copy the file **MIMOSA26_MULTI_JTAG.zip** to the directory C:\CCMOS_SCTRL\. Unzip **MIMOSA26_MULTI_JTAG.zip** file to this directory.
2. To start the MIMOSA26 JTAG SOFTWARE, double click the file **C:\CCMOS_SCTRL\MIMOSA26_JTAG\MI26.exe**. Following two windows should be shown on the screen.



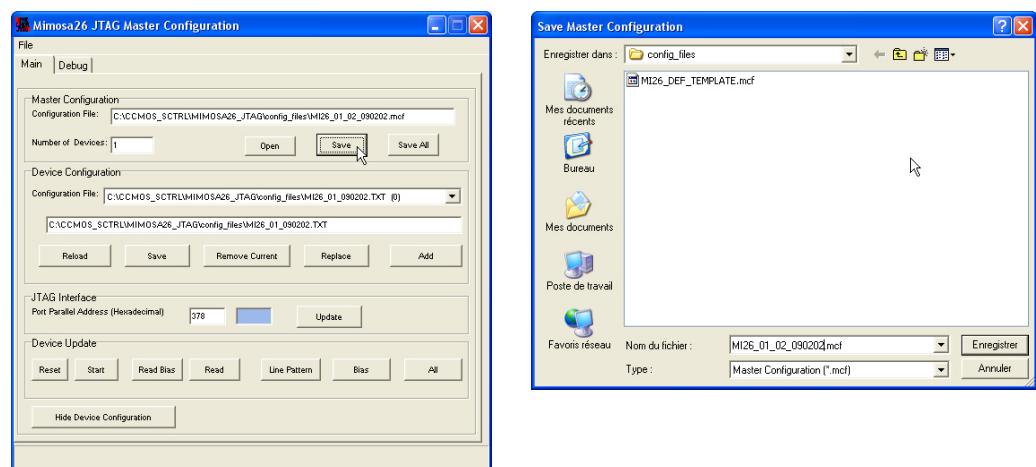
3. Using the software

In this example, the MIMOSA26 JTAG software is configured for 2 MIMOSA26 devices.

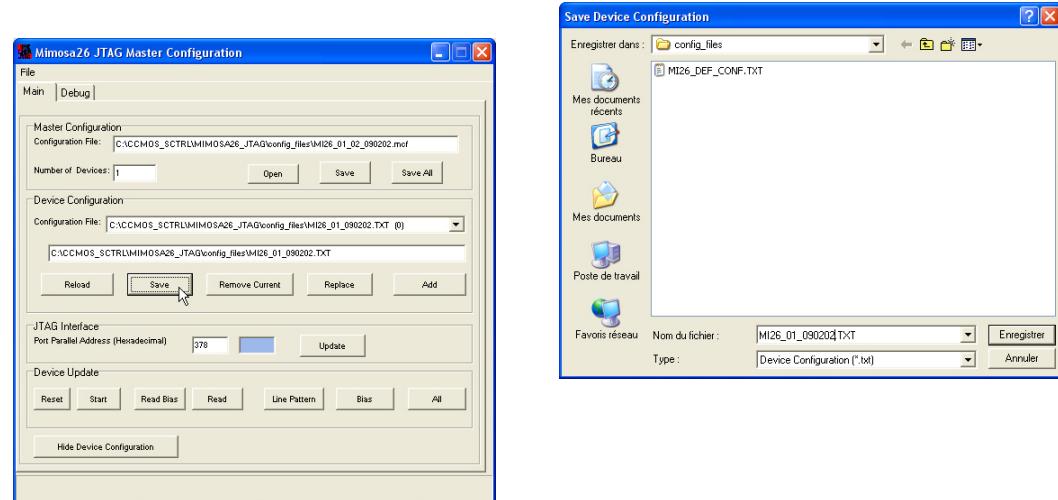
1. To start the MIMOSA26 JTAG SOFTWARE, double click the file **C:\CCMOS_SCTRL\MIMOSA26_JTAG\MIMOSA26_JTAG.bat** as it was explained in previous chapter.
2. To start using the software, the environment of MIMOSA26 devices has to be defined. This definition is stored in a Master Configuration file that includes information of number of MIMOSA26 devices in JTAG chain and name of a Device Configuration file for each device in chain. Press Button “Open” on window titled “MIMOSA26 JTAG Master Configuration”. Please select file “MI26_DEF_TEMPLATE.mcf” (see the image below). This is a simple template (read-only) file that can be used as a start point for the environment definition. The Master Configuration files are in directory “C:\CCMOS_SCTRL\MIMOSA26_JTAG\config_files”.



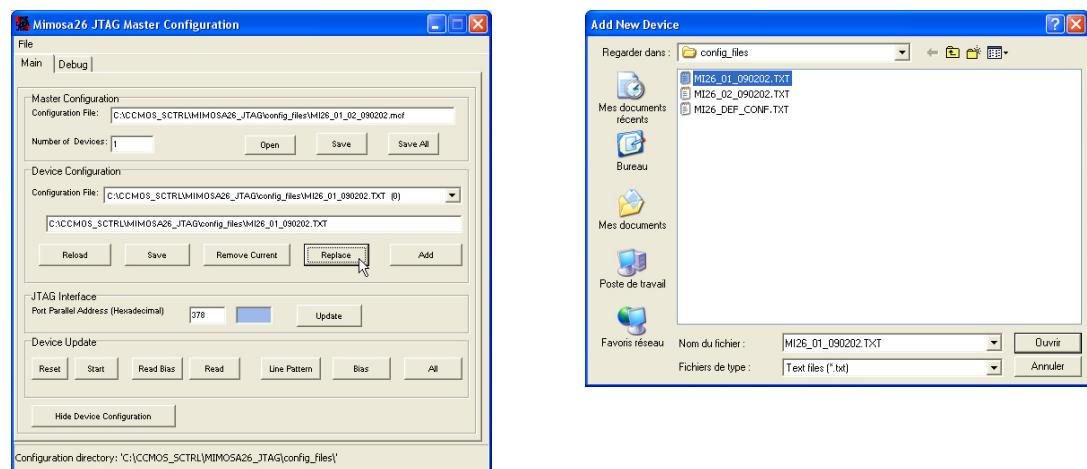
3. Save this template file with a suitable name for the configuration, e.g. “MI26_01_02_090202.mcf” by clicking “Save” button on “MIMOSA26 JTAG Master Configuration” window (see the image below).



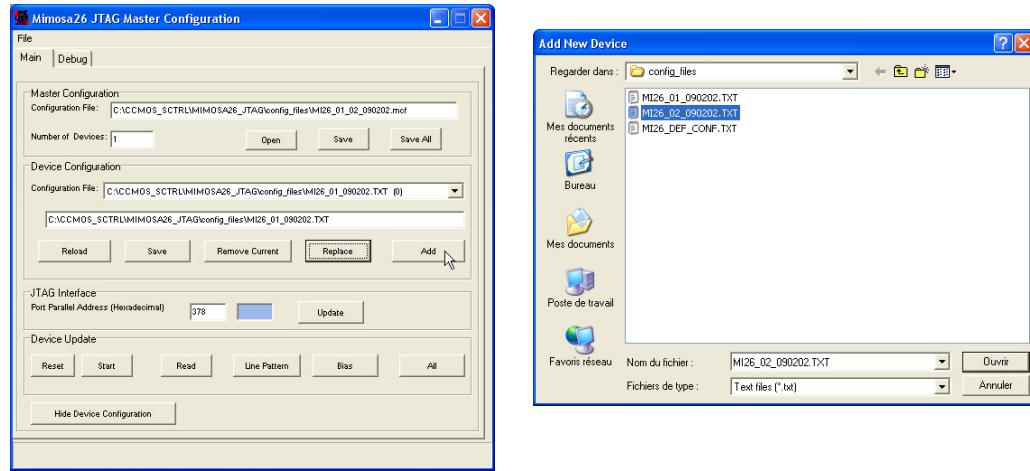
4. Load the Master Configuration file “MI26_01_02_090202.mcf” by clicking button “Open” (See the chapter 3.2.).
5. As the Master Configuration template file uses a Device Configuration template file the default configuration file has to be replaced by a Device Configuration files dedicated to this environment (There are 2 devices in this configuration example). Please select “Save” button on Device Configuration section. Set the file as “MI26_01_090202.txt” and save it. Please save this Device Configuration file again with a name as “MI26_02_090202.txt”.



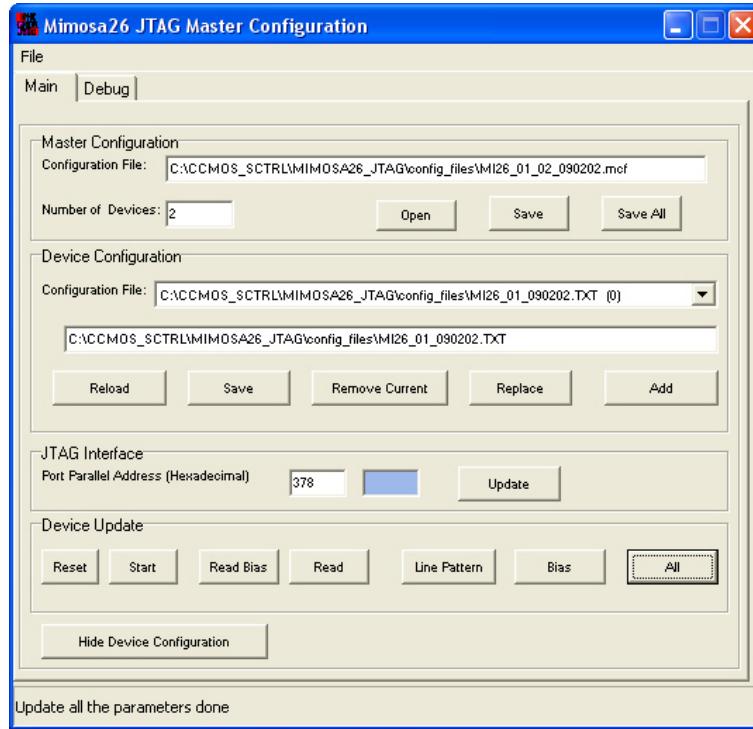
6. Replace the Device Configuration template file on Master Configuration by clicking the button “Replace” on Device Configuration section. Select the file “MI26_01_090202.txt”.



7. Add the other two devices to the MIMOSA26 JTAG environment. Click the button “Add” on Device Configuration section. Select the file “MI26_02_090202.txt” (see the image below).



8. If the definition of MIMOSA26 JTAG environment was successfully performed the number of device in Master Configuration section should be 2 (see the image below). Save the Master Configuration to file by clicking “Save” on Master Configuration section.



At this moment, the MIMOSA26 JTAG environment is defined. The MIMOSA26 JTAG chain can be updated and read back the status of devices.

9. To reset the MIMOSA26 devices, click the button “Reset” (see the image below).



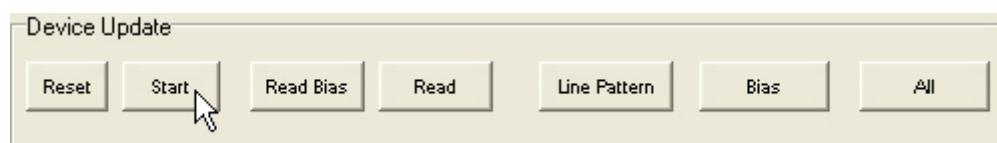
10. To update the parameters to the devices, please select a button “All” from the “Device Update” section (see the image below).



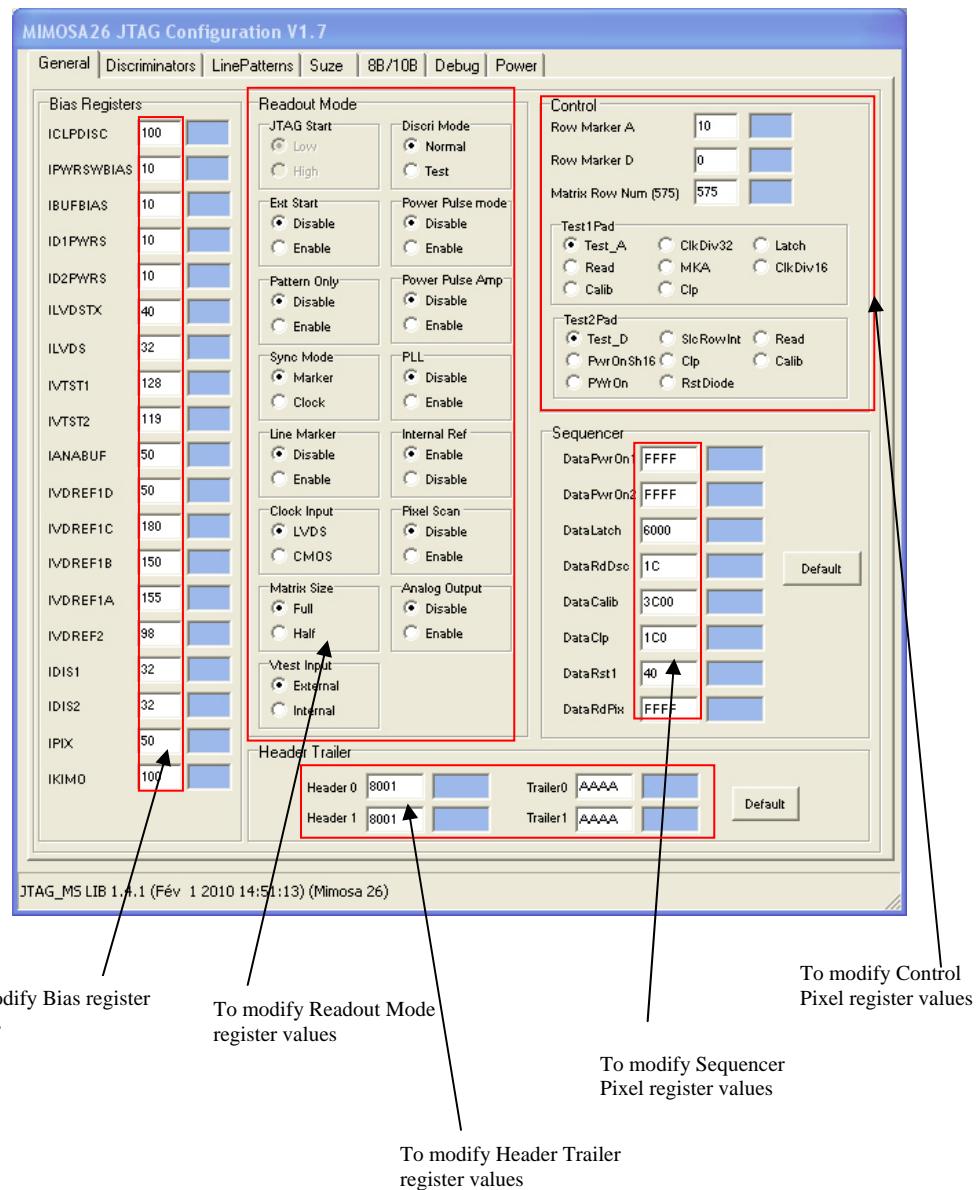
11. To read back the parameters from MIMOSA26 devices, click the button “Read” (see the image below).



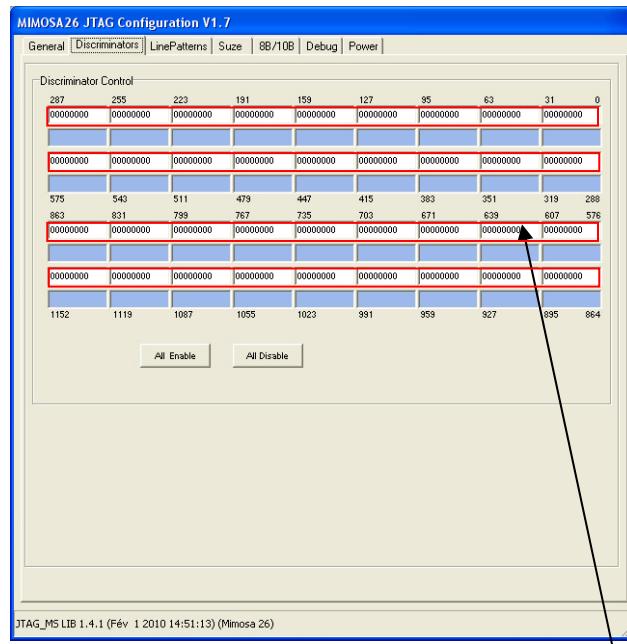
12. To perform a start-up sequence for the MIMOSA26 devices, click the button “Start” (see the image below).



13. In the following image is shown a Device Configuration window for the general device parameter settings. If this window is not visible please click “Show Device Configuration” or click two times “Hide Device Configuration”. See the Chapter 4 for the overview of functionalities of the Device Configuration window. There are five zones that user can modify the device parameters: Bias (BIAS_DAC) Register, Readout mode (RO_MODE) Register, Control (CTRL_PIXEL) Register, Sequencer (SEQ_PIXEL) Register and Header/Trailer (HEADER_TRAILER) Register. **Please save the parameters after the modifications by clicking button “Save” on Device Configuration, otherwise the modifications will be lost.**

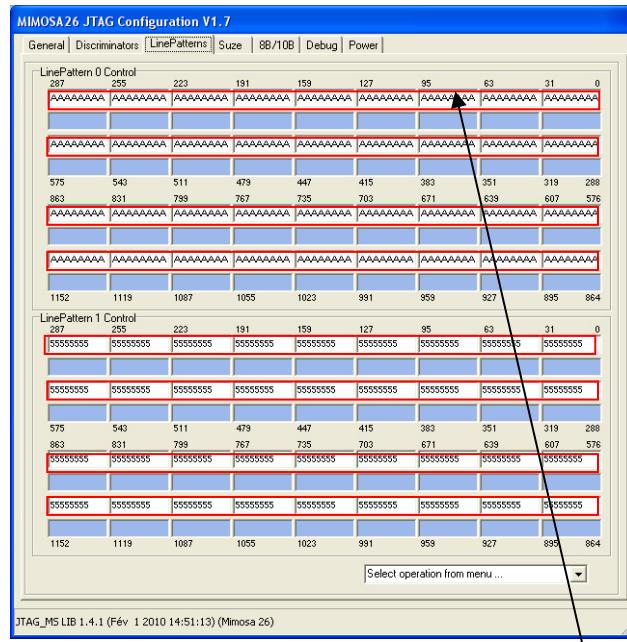


14. In the following image is shown a Device Configuration window for the device Column Discriminator parameter settings.



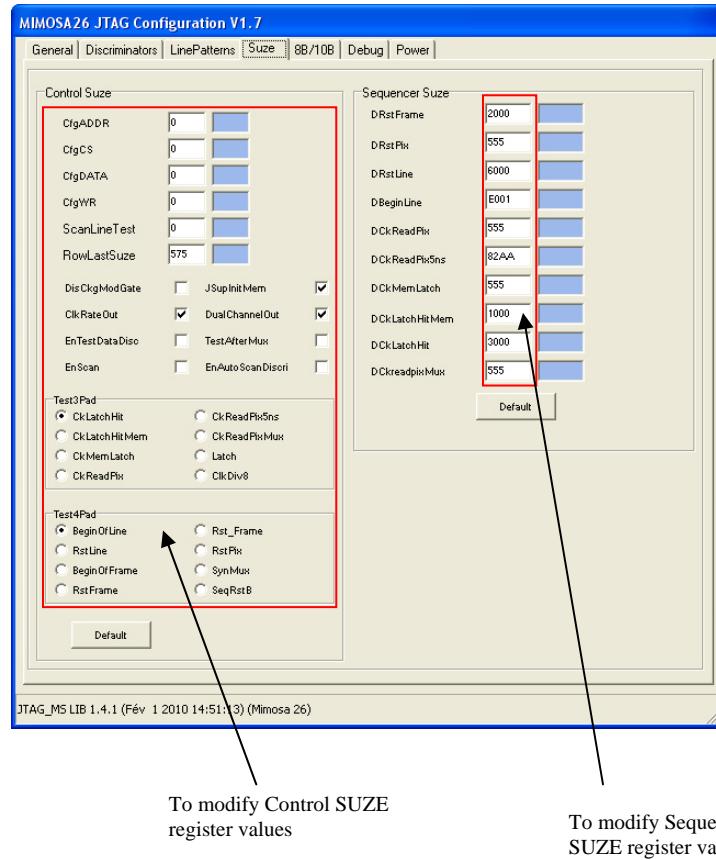
To modify Discriminator Control register values

15. In the following image is shown a Device Configuration window for the device Line Patterns parameter settings.



To modify Line Pattern register values

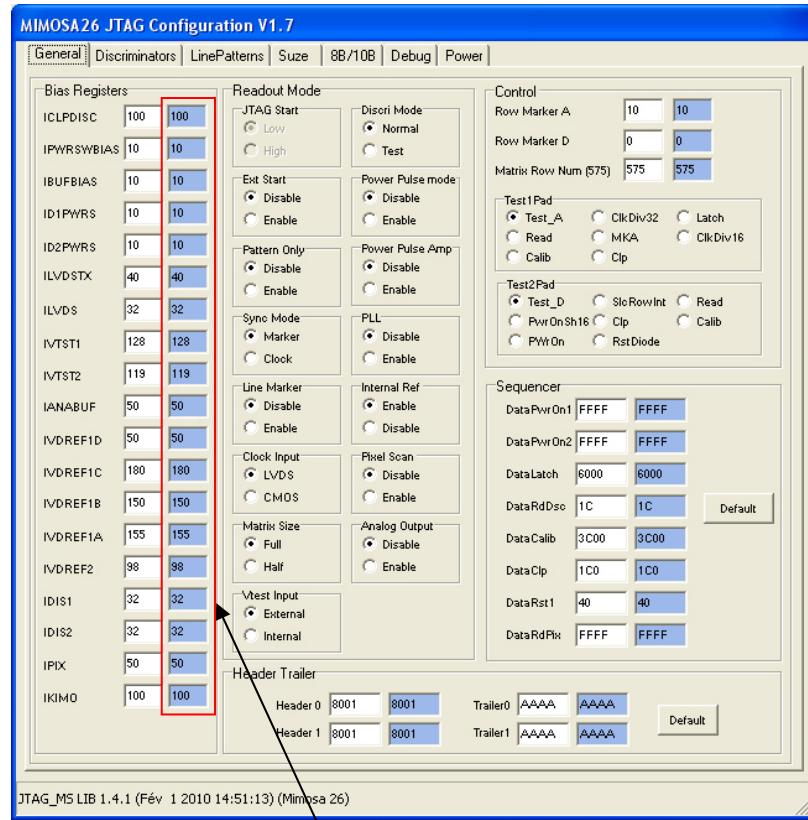
16. In the following image is shown a Device Configuration window for the SUZE (Zero Suppression engine) parameter settings.



To modify Control SUZE
register values

To modify Sequencer
SUZE register values

17. If the device configuration was successfully finished the read back values for DACs should be shown at the right-side of each parameter (see the image below).

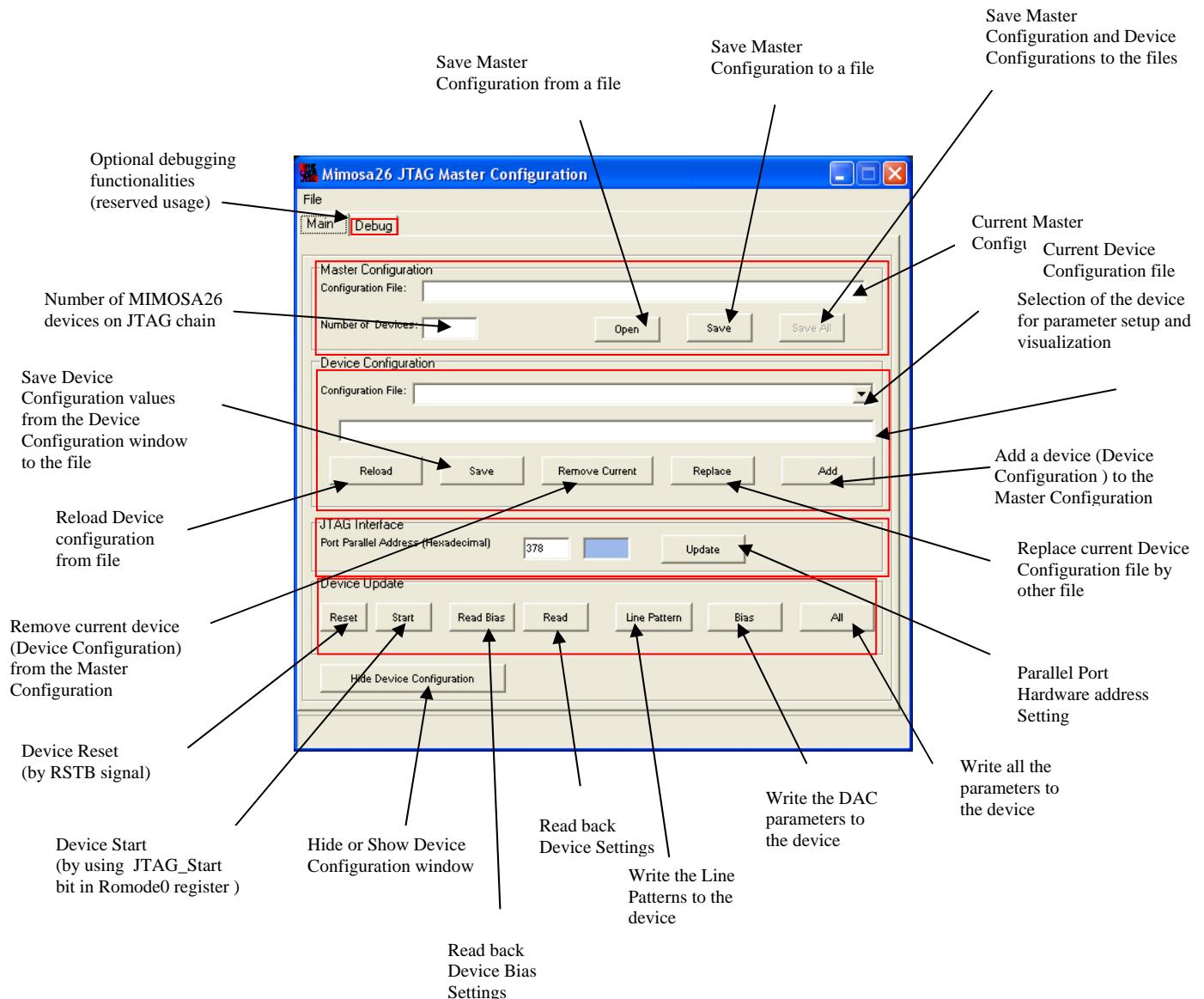


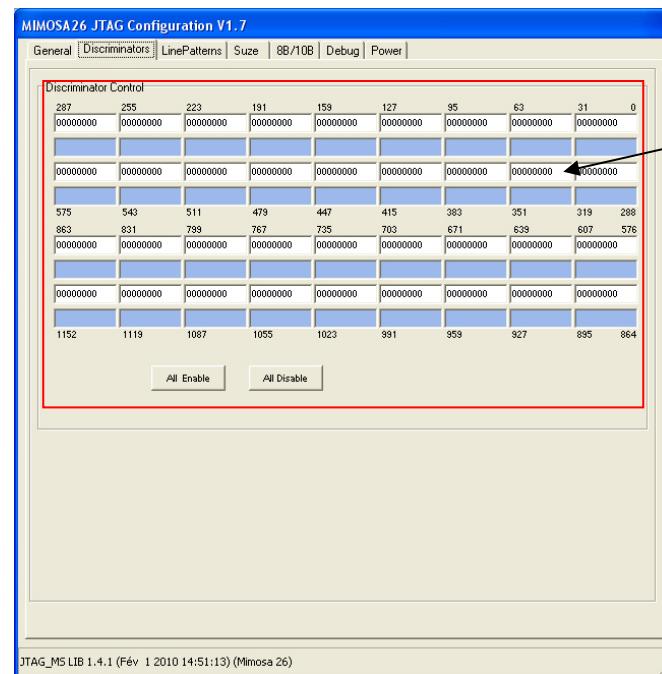
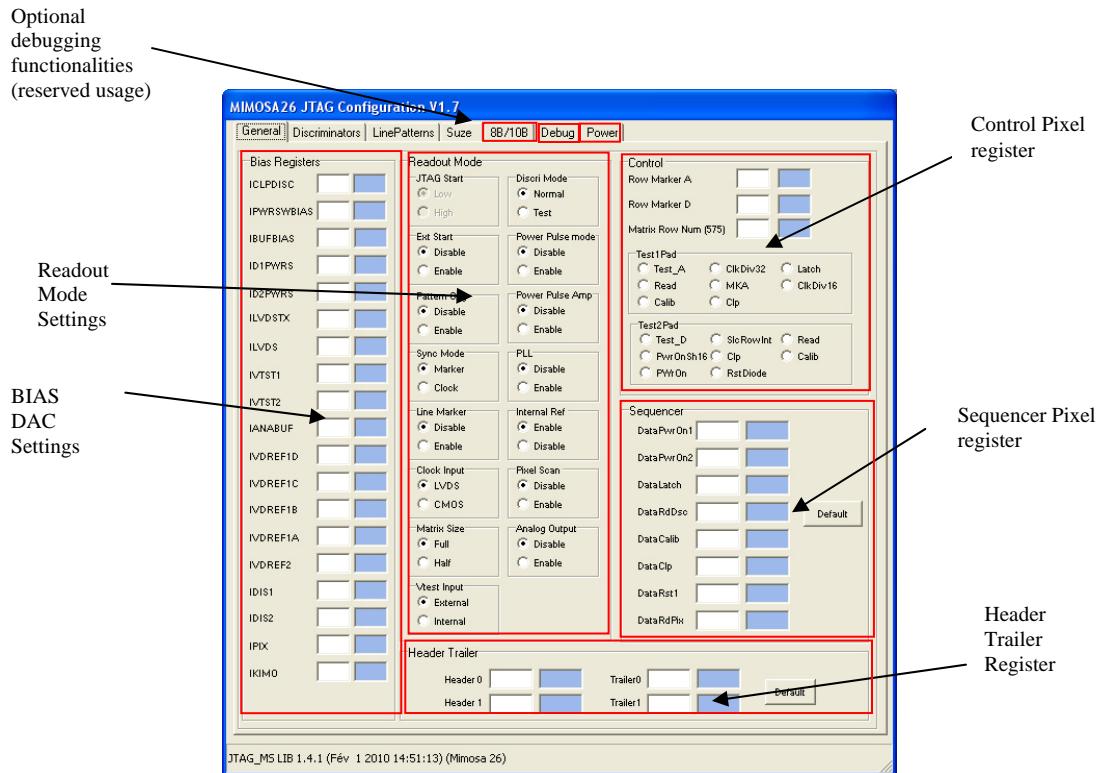
Read back value from
MIMOSA26 device

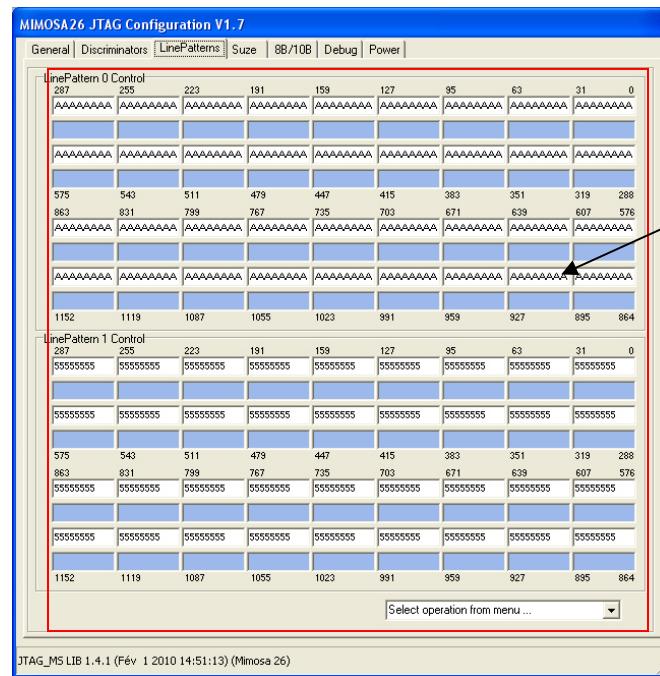
18. As a default, the Port Parallel Hardware address is set to a default value of 0x378. In most cases there is no need to modify this value. In case that this address is not valid, the port address can be changed by typing a new value to “Port Parallel Address” field in hexadecimal form. Please click the button “Update” to take account the modification of the address of port parallel. After this please reload the Master Configuration.

JTAG Interface	Port Parallel Address (Hexadecimal)	378	<input type="button" value="Update"/>
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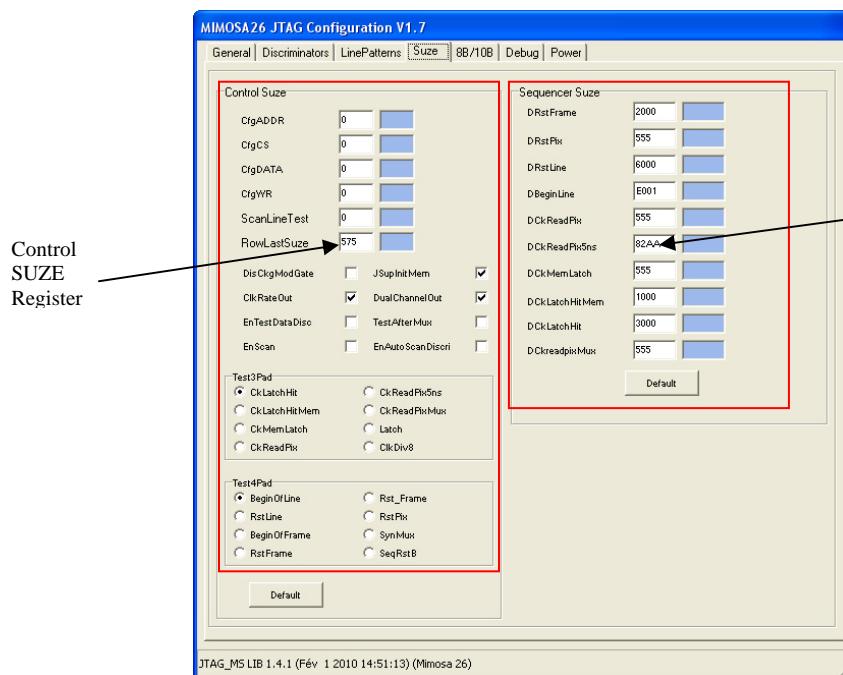
4. Overview of the functions







Line Pattern Registers

Control
SUZE
RegisterSequencer
SUZE
Register

5. Appendix A: Power consumption reduction by JTAG software

A new power pulsing functionality has been added to MIMOSA26 JTAG Version 1.8 to alternate MIMOSA26 JTAG register settings during a period of inactivity of device to reduce the power consumption. The alternation for the JTAG register settings is controlled by an external signal furnished via the PC port parallel. For the moment, the following JTAG registers values can be alternated:

Register	Bit or Bit Field
BIAS_DAC	All the values (Bit[151:0])
ROMODE1	ENDISCRIPWRSAVE (Bit1) ENDSICRIAOP (Bit2)
SEQUENCER_PIX_REG	DATAPWRON1 (Bit[31:0]) DATAPWRON2 (Bit[63:32]) DATARDPIX (Bit[127:112])

JTAG power pulsing interface is implemented by using 2 signals on the PC parallel port. When the JTAG power pulsing external control is enabled, the MIMOSA26 JTAG software monitors state of a “POWER PULSING REQUEST IN” signal on the PC parallel port. In case of a transition of ‘0’ to ‘1’ on the signal “POWER PULSING REQUEST IN” is detected by JTAG software, the alternate JTAG register settings is charged to the MIMOSA26 device(s). After the loading the alternate register values, a “POWER PULSING STATUS OUT” signal is enabled on the PC parallel port.

The “POWER PULSING REQUEST IN” signal has to remain active during the all period of the power pulsing. When the transition of ‘1’ to ‘0’ on the signal “POWER PULSING REQUEST IN” is detected , the JTAG software charges the normal operation values to the device(s) registers. The end of the update of the register values is signaled by disabling the “POWER PULSING STATUS OUT” signal (Fig. A1).

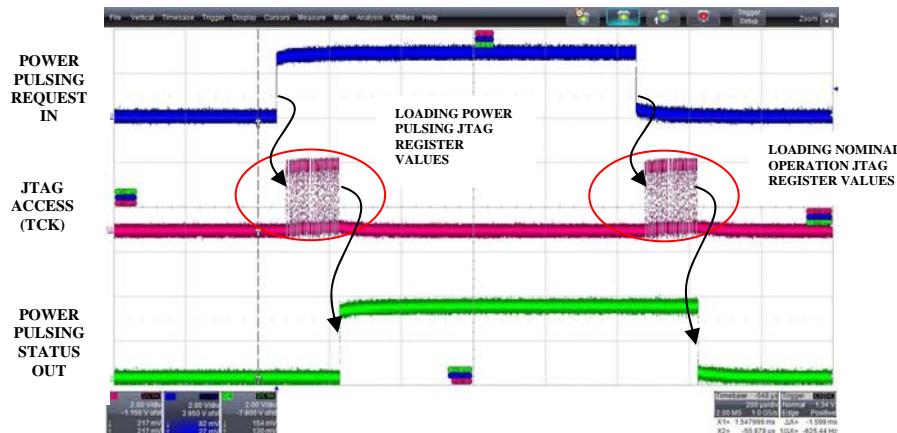
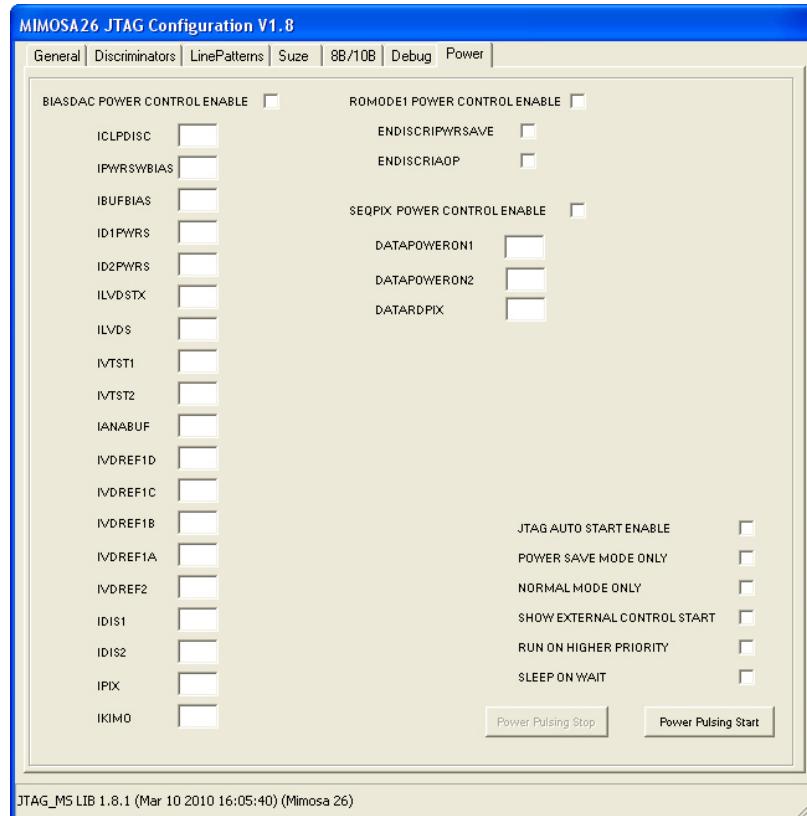


Figure A1. A screen capture of the JTAG power pulsing.

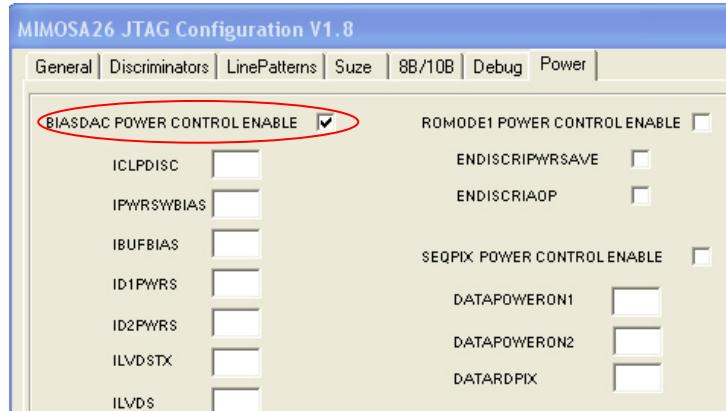
In following table is shown the usage of the PC parallel port signal for the power pulsing.

SIGNAL	PARALLEL PORT PIN (DB25)
TCK	4
TMS	5
TDI	3
TDO	10
RSTB	2
POWER PULSING REQUEST IN	12
POWER PULSING STATUS OUT	7
GND	18,19,20,21

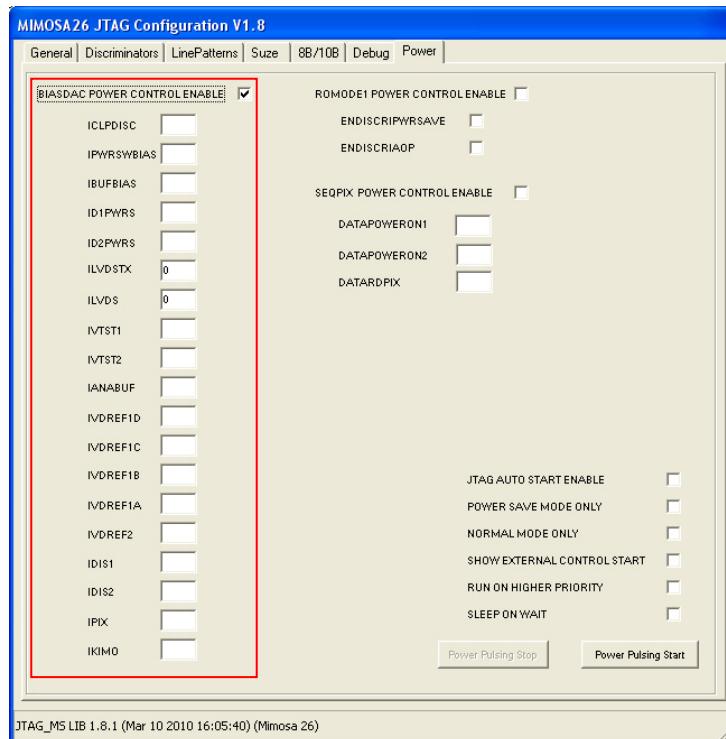
In following Figure is shown the GUI of JTAG power pulsing for Mimosa 26 device at the initial state.



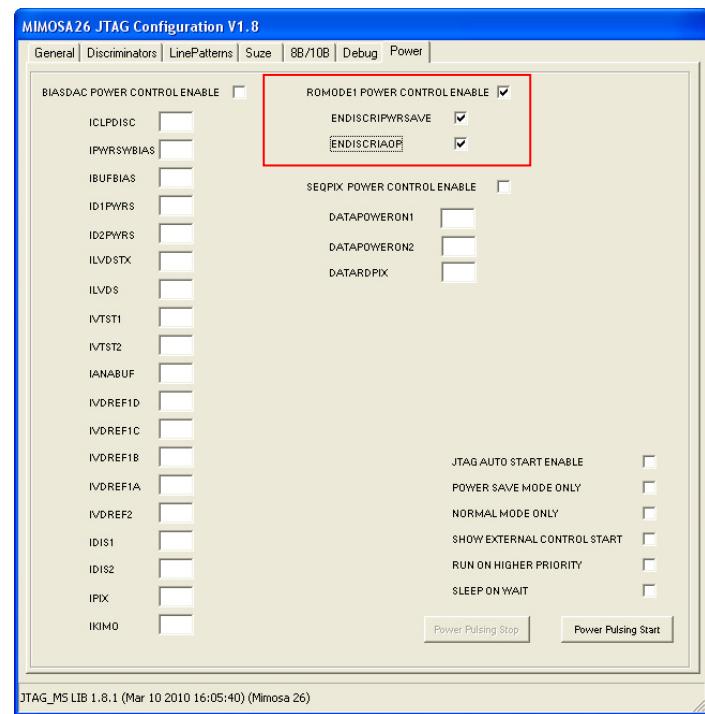
The access to the each of 3 JTAG register during the power pulsing cycle is validated by a corresponding checkbox. The “BIAS_DAC POWER CONTROL ENABLE” checkbutton validates the JTAG access to the BIAS_DAC register during the power pulsing cycle. In a following Figure the access to the BIAS_DAC register is validated.



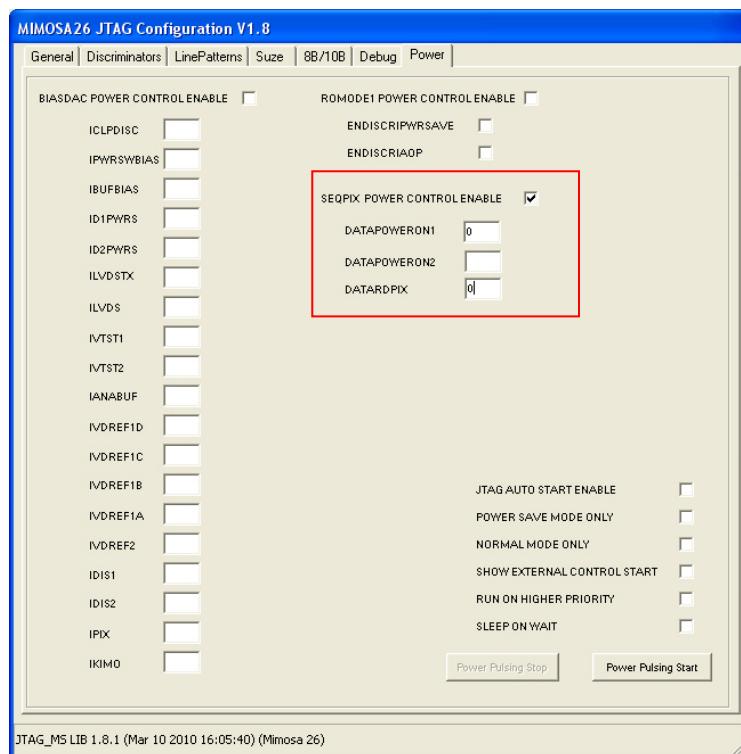
The DAC values can be modified for power pulsing mode by setting a value to the corresponding entry at the GUI. In following Figure, the ILVDSTX DAC register and ILVDS DAC register are set to value of 0. If the BIAS_DAC entry is empty, the nominal operation value of DAC register found on “General” TabSheet is used (Please see the page 12).



In a following Figure the access to the ROMODE1 register is validated by a checkbox “ROMODE1 POWER CONTROL ENABLE”. The selection of the state of the bit fields of “ENDISCRIPWRSAVE” and “ENDISCRIAOP” are available at the GUI.



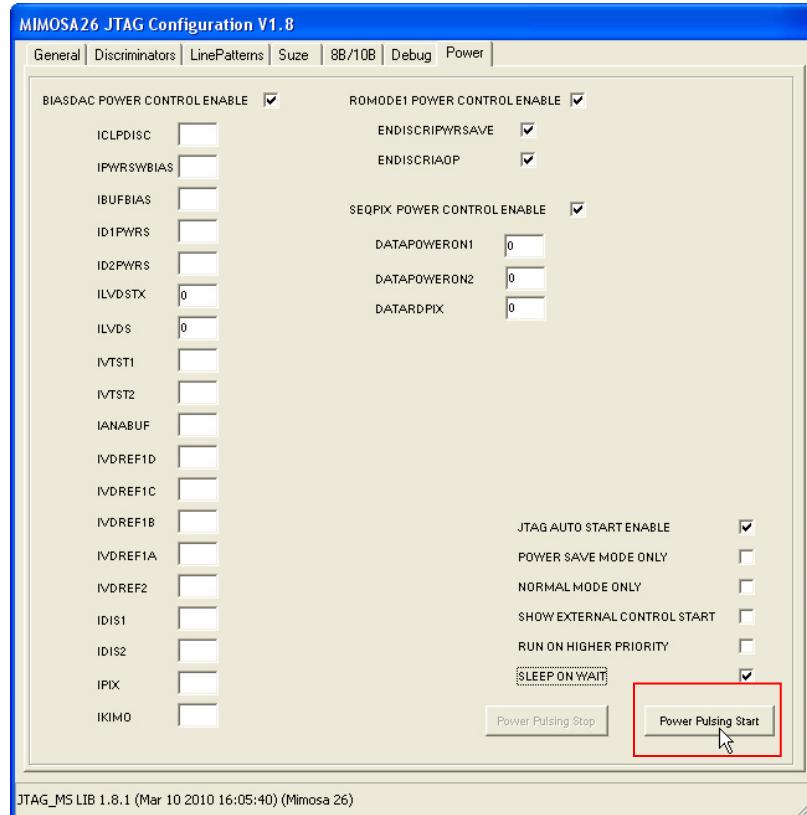
In a following Figure the access to the SEQPIX register is validated by a checkbox “SEQPIX POWER CONTROL ENABLE”. The JTAG register values for “DATAPOWERON1”, “DATAPOWERON2” and DATARDPIX can be adjusted for the power pulsing mode. If the value entry is left empty, the nominal operation value of SEQPIX register found on “General” TabSheet is used (Please see the page 12).



Some additional features are added for debugging and to adapt system responsiveness. These functionalities are explained in following Table.

FEATURE	FUNCTION
JTAG AUTO START ENABLE	The MIMOSA26 device is started by “JTAG_Start” bit founded on ROMODE0 Register. This function is normally required if the SEQPIX Register values are modified during the power pulsing to validate register value modifications.
POWER SAVE MODE ONLY	For Debugging purposes: Only power pulsing mode values are loaded to the device(s).
NORMAL MODE ONLY	For Debugging purposes: Only normal operation mode values are loaded to the device(s).
SHOW EXTERNAL CONTROL START	For Debugging purposes: The detection of the change of states of “POWER PULSING REQUEST IN” is shown on signal “POWER PULSING STATUS OUT” as a form short pulse.
RUN ON HIGHER PRIORITY	For the system Responsiveness control: JTAG software will execute parallel port monitoring at the higher priority level than the normal program execution priority level. This feature will increase system charge.
SLEEP ON WAIT	For the system Responsiveness control: JTAG software will decrease system charge during the monitoring the port parallel. This features decrease the system responsiveness.

The JTAG power pulsing mode can be started by the button “POWER PULSING START”



and stopped by the button “POWER PULSING STOP”.

