UNIVERSITY OF CALIFORNIA AT BERKELEY
College of Engineering
Department of Electrical Engineering and Computer Sciences

EE105 Lab Experiments

Experiment 8: Multi-stage Amplifiers

1 Objective

Often, a single stage transistor amplifier may not provide enough gain or the proper input/output impedances for a desired application. To remedy this, we can cascade amplifier stages to form a multi-stage amplifier with the desirable gain or impedance properties. In this lab, we will examine the cascode amplifier and another multi-stage amplifier formed by cascading a common-emitter and common-collector amplifier.

2 Materials

Component	Quantity
2N4401 NPN BJT	4
2N4403 PNP BJT	2
51 kΩ resistor	2
20 kΩ resistor	1
100 Ω resistor	2
51 Ω resistor	1
10 kΩ potentiometer	1
10 µF capacitor	1
100 µF capacitor	1

Table 1: Components used in this lab

3 Procedure

3.1 Cascode Amplifier

1. Construct the cascode amplifier (Q_1 and Q_2) with current mirror bias (Q_3 and Q_4) as shown in Figure 1(a). Use two 51 kΩ resistor in parallel to make a 25.5 kΩ resistor for R_{REF} and a 51 Ω resistor for R_S. Set V_{BIAS2} to 1.5 V.
2. Use the function generator to generate a 1 kHz, 20 mV peak-to-peak sinusoidal signal with a DC offset of around 580 mV to 650 mV (you may have to adjust the offset after connecting the signal to the amplifier to ensure you get a clean output signal). Use this signal as v_{IN}.
3. Measure I_{BIAS} and the DC voltage at v_{OUT}.
4. Using the oscilloscope, plot both the input v_{IN} and the output v_{OUT}. Sketch the waveforms you observe.
5. Why is v_{OUT} not sinusoidal?
6. Now add a 10 µF capacitor to the node v_{OUT} and a 20 kΩ resistor from the capacitor to ground as shown in Figure 1(b). This resistor will act as a load to the amplifier.

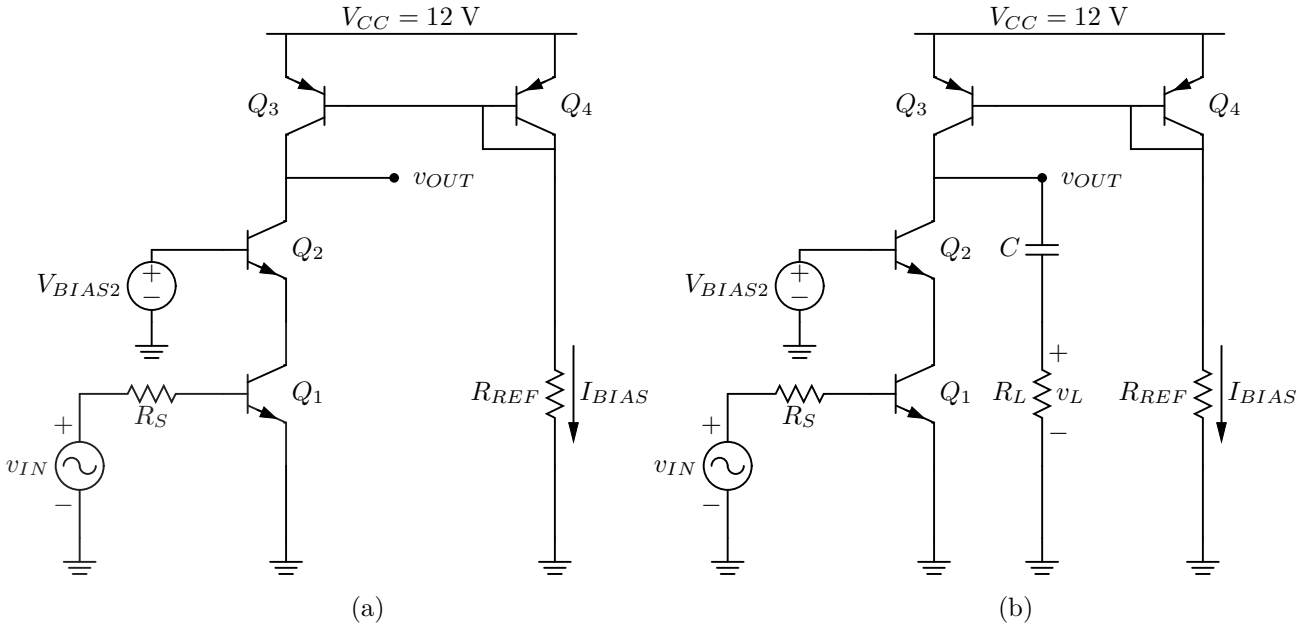

Figure 1: (a) Cascode amplifier test setup (b) Cascode amplifier test setup with load resistance

7. What is the peak-to-peak voltage of the output waveform (at v_L) with the load resistor? What is the gain of the amplifier with the resistive load?

3.2 Common Emitter-Common Collector Multi-stage Amplifer

From the previous lab exercises, you tried using a speaker as a load to a common emitter amplifier. However, the common emitter amplifier delivers very little voltage gain to the speaker because of the huge impedance mismatch between the amplifier and speaker. In this section of the lab, you will cascade a low output impedance common collector amplifier to the output of a common emitter amplifier as a voltage buffer to drive a low impedance speaker.

1. Before you begin, use the function generator to apply a sinusoidal signal with peak-to-peak voltage of 40 mV and a frequency of 1 kHz directly to the speaker. Can you hear anything?

2. Construct the cascaded amplifiers as shown in Figure 2. Set the potentiometer to around 8 kΩ for R_C. For the rest of the circuit, let $R_S = 51\ \Omega$, $R_{REF} = 200\ \Omega$ (use two 100 Ω resistors in series), and $C = 100\ \mu$F.

3. Use the function generator to generate a 40 mV peak-to-peak, 1 kHz frequency sine wave with a DC offset of around 540 mV to 600 mV. Use this signal as v_{IN}. Now, try to maximize the gain of the amplifier by increasing the resistance of the potentiometer for R_C. Can you hear anything now? Feel free to try out other frequencies to observe how the speaker responds to various frequencies.

4. Measure I_{BIAS1}, I_{BIAS2}, and the DC voltages at v_{OUT1} and v_{OUT2}.

5. Measure V_{BE} of Q_2. Is the DC voltage at v_{OUT1} enough to bias Q_2 in the forward active region?

6. Using the oscilloscope, plot both the input v_{IN} and the output v_{OUT2}. Sketch these waveforms.

7. Measure the gain v_{out2}/v_{in}.

8. Now increase the DC offset of the input waveform to 620 mV. What happens to the waveform at v_{OUT2}?

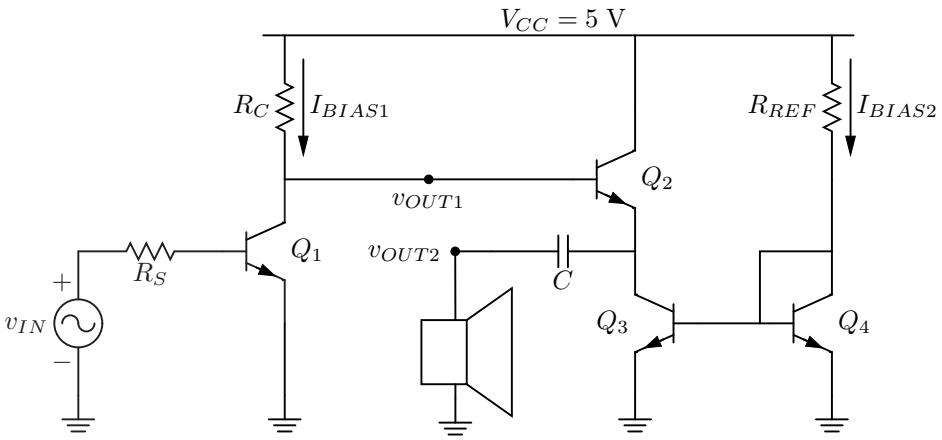

Figure 2: Multi-stage amplifier test setup