Integrated Systems Architectures

Lab 1: design and implementation of a digital filter Assignment

Read the Lab 1 description and address the following points.

1 Reference model development

(a) Design the filter with Matlab/Octave and represent the coefficients with the number of bits which have been assigned to your group. Put in the report a figure showing the frequency response for both floating point and fixed point coefficients. Comment it.

(b) Develop the fixed point model as a C program and reduce the precision of the multiplications reaching a maximum THD of -30 dB.

(c) Compare and comment the results.

2 VLSI implementation

- Develop the architecture of the filter (direct-form for FIR filters and direct-form-II/canonical-direct-form for IIR filters) by placing the proper number of registers, adders, multipliers and logic. Draw the timing diagram of the architecture showing it is compliant with the specifications (use https://wavedrom.com for the timing diagram).

- Develop the VHDL model of the filter and verify it against the fixed point C model with a proper testbench.
  The results given by the VHDL model must be equal to the ones obtained with the C model.
  Show that the results of the VHDL model are correct (equal to the results of the C model) even when VIN moves from '1' to '0' and then back to '1'.
  Be sure that the interface of your architecture is exactly

equal to the one shown in *es1v3.0_description.pdf* as an automatic tool will be used to check your design.

- Measure the amount of time required to complete the simulation (from the first rising edge of the clock sampling VOUT='1' to the last rising edge of the clock sampling VOUT='1').
- Peform the logic synthesis and find the maximum clock frequency at which the design can correctly run (minimum period giving slack *met* and equal to zero). Then, find the area.
- Set $f_{clk} = f_M/4$, find the area, verify the design, measure the amount of time required to complete the simulation and estimate the power consumption.
- Place & Route the design at $f_{clk} = f_M/4$, find the area, verify the design, measure the amount of time required to complete the simulation and estimate the power consumption.

Remember to put in appendix of your report all the reports showing post-synthesis and post-place-and-route results: area, timing (slack) and power consumption.

3 Advanced architecture development

- Develop a new C model to take into account the modifications required by the advanced architecture.
- Verify that the THD requirement is still satisfied.
- Change the interface of your filter according with the description given in *es1v3.0_description.pdf*.
- Repeat all the steps in 2.