

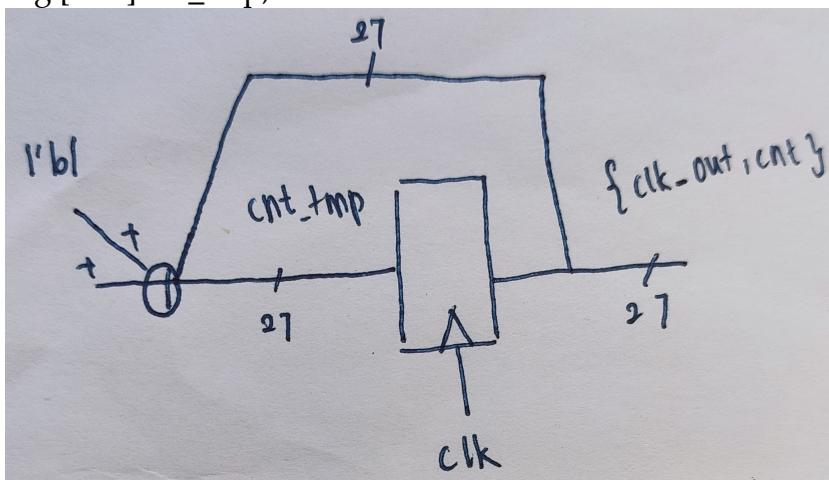
Report Lab 3

Design Specification

Lab3_1

```
output clk_out;  
input clk;  
input rst_n;
```

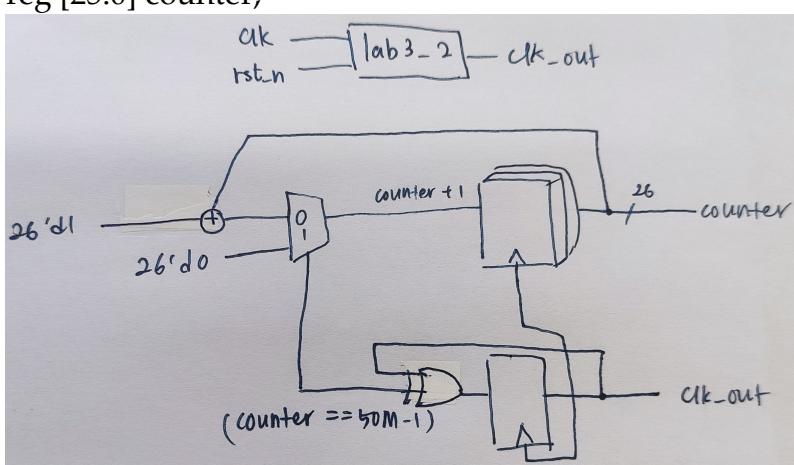
```
reg clk_out;  
reg [25:0] cnt;  
reg [26:0] cnt_tmp;
```



Lab3_2

```
input clk;  
input rst_n;  
output clk_out;
```

```
reg clk_out;  
reg [25:0] counter;
```

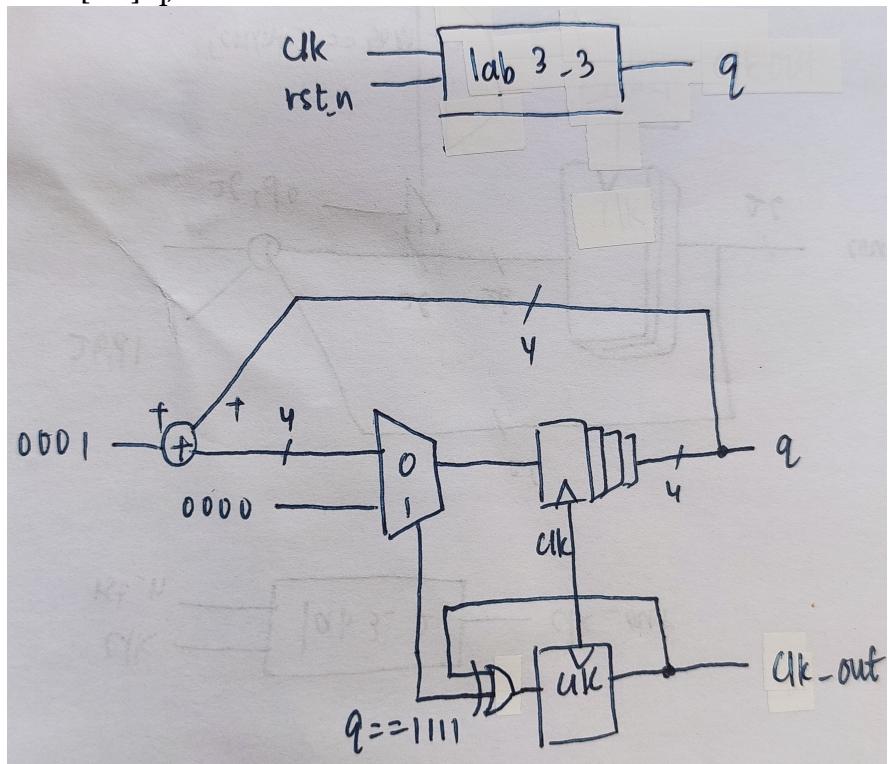


Lab3_3

Top Module:

```
output [3:0] q;  
input clk;  
input rst_n;
```

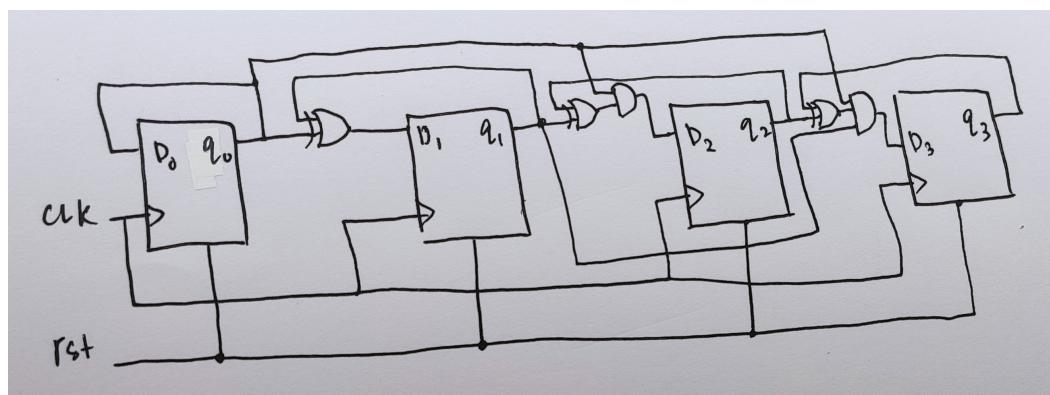
```
wire clk_d;  
wire [3:0] q;
```



Counter from Prelab3_1:

```
output [3:0] q;  
input clk;  
input rst_n;
```

```
reg [3:0] q;
```



Lab3_4

Top Module:

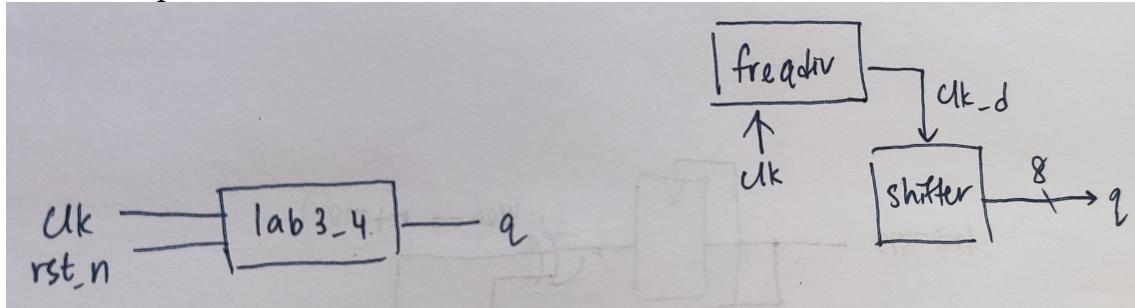
output [7:0] q;

input clk;

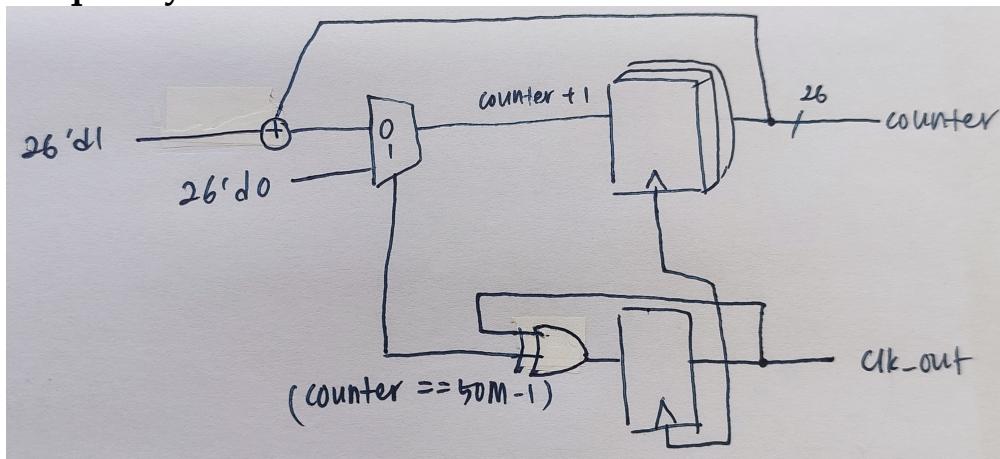
input rst_n;

wire clk_d;

wire [7:0] q;



Frequency divider:



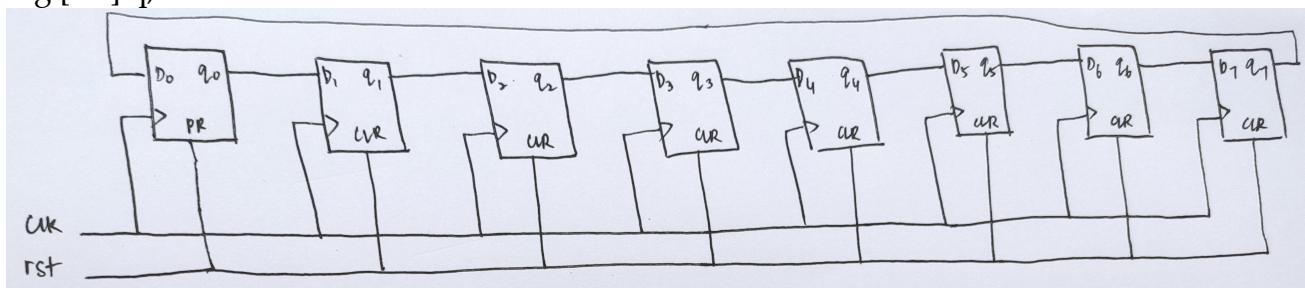
Shifter from Prelab3_2:

output [7:0] q;

input clk;

input rst_n;

reg [7:0] q;



Design Implementation

Lab3_1:

[25:0] cnt as a remainder of the counter and [26:0] cnt_tmp as input to the d flip-flop.

Lab3_2:

[25:0] counter as a counter, when the clk input is 50M then, the clk_out will invert the clk_out result at the next clk input. This make the 1Hz clock frequency divider.

Lab3_3:

The top module combine the counter from prelab3_1 and the 1Hz frequency divider to make a 1Hz binary up counter. The result is shown by the 4 Leds.

Lab3_4:

The top module combine the shifter from prelab3_2 and the 1Hz frequency divider to make a 1Hz shifter register, which shift the last bit of d flip flop, to the fist bit of d flip flop, with value of 10010110. The result is shown by 8 Leds.

Discussion

The idea for combination of the counter and the frequency divider are more clearly. The ability to code for a 1Hz of frequency divider, and use it for the other lab. The problem faced is the Basys 3 board still there, but seems like the board is functioning well, but the problem is the computer. And it cannot be solved until now.

Conclusion

From this experiment, I had learn about how to combine the modules in a top module by connecting the input and output correctly. Other than that, I had learn also the ability to code the 1Hz frequency divider, and combine it with the shift register and the counter done in the prelab. The frequency divider can be constructed with different clock frequency by the different number of counter.

References

<https://www.fpga4student.com/2017/08/verilog-code-for-clock-divider-on-fpga.html#:~:text=The%20Verilog%20clock%20divider%20is,parameter%20in%20the%20Verilog%20code.&text=To%20change%20the%20clock%20frequency,just%20modify%20the%20DIVISOR%20parameter>

The idea learn from this URL is the number of counter can be changed according to the clock frequency required.