Report Prelab 3

Design Specification

Prelab3_1:

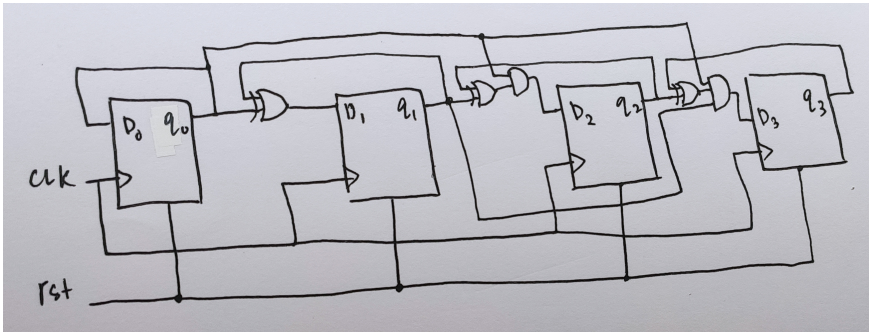
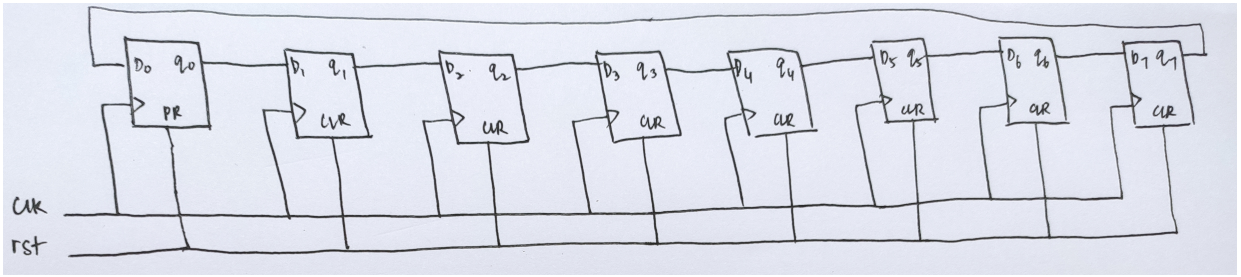


Figure 1: 4 bit binary up counter

output [3:0] q
input clk
input rst_n

The counter will start counting when the clock is positive edge or the reset is negative edge.

Prelab3_2:



output [7:0] q;
input clk;
input rst_n;

The shifter will start shifting when the positive edge of clock is triggered or the reset is negative edge.

Design Implementation

Prelab3_1:

The binary up counter is design when the positive edge is triggered, then the counter will add for 1. The reset signal is a low active reset. So, when the reset is 0, the counter will be reset to 0.

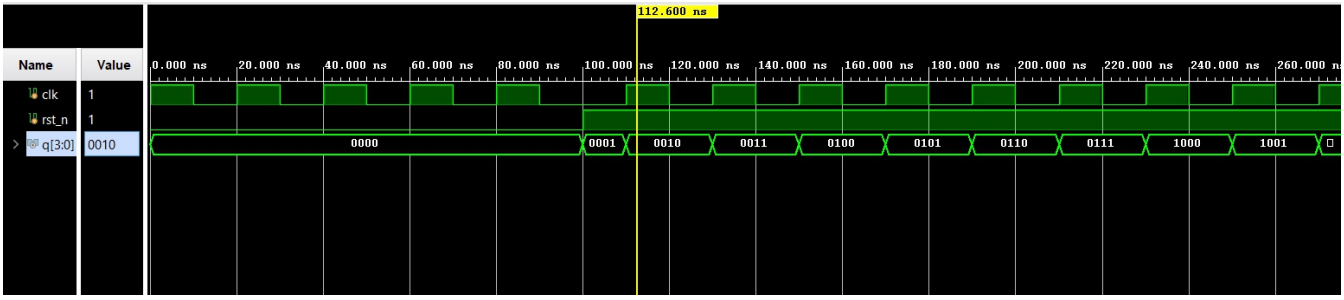


Figure 2: The results of the simulation

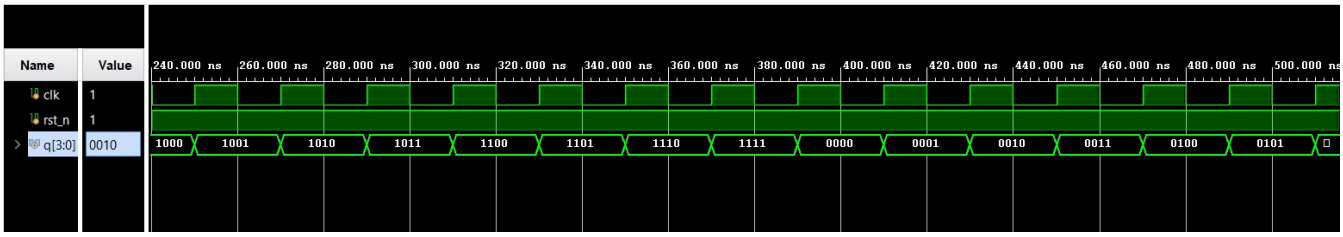


Figure 3: The results of the simulation

The results shown that when rst_n is 0, then the counter is reset, and when the rst_n is 1, the counter will start to counting up.
The testbench of this binary up counter is designed to change the value of reset after 100 nanoseconds, as shown in the figure above.

Prelab3_2:

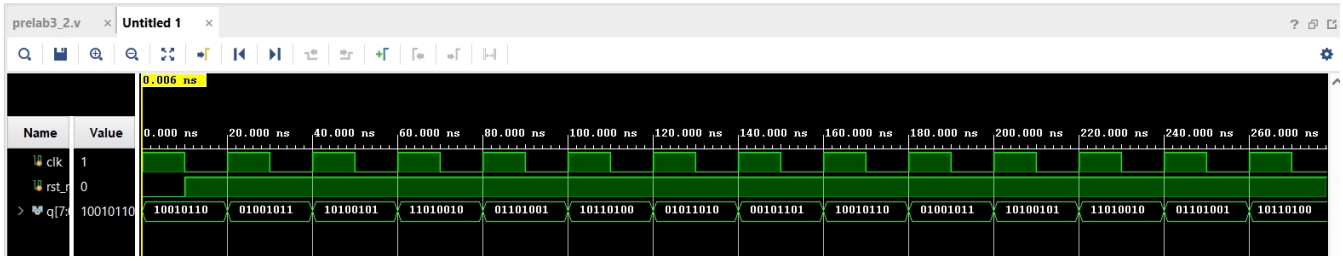


Figure 4: The result of the simulation

rst_n is set to 0 first, as it is designed as a low active reset signal, as the flip flops reset, it get the value of 10010110 as required. The last value will be shifted to the first flip flop when the positive edge of clock is triggered.

Discussion

The mistake I made is that wrong shifting the value in question 2. from this mistake, I had a

better understanding of the flip flop and how the <= used when doing the design of the flip flop. I had learned how to do the simple counter as in question 1.

Conclusion

More details about the flip flop and the counter with the register.

References

Digital Design With An Introduction To The Verilog HDL, Fifth Edition by M.Morris Mano and Micheal D. Ciletti, page 234