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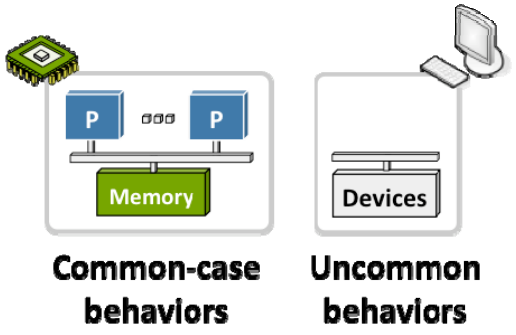
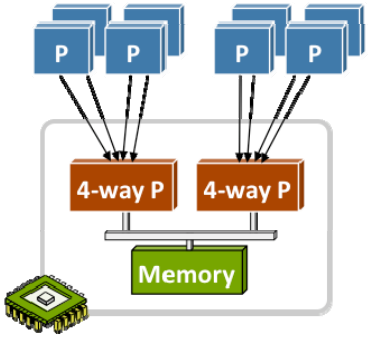
- with equipment, tools and answers from Xilinx, Intel and Bluespec
- with interactions and advising from the RAMP colleagues

The ProtoFlex Simulator

- **History**
  - Project started (circa 2007) to build scalable, full-system multiprocessor simulators using FPGAs
- **Key Features**
  - Functional simulator for N-way UltraSPARC III server (~50-90 MIPS)
  - Using hybrid simulation, runs real server apps + Solaris OS
  - Employs multithreading to virtualize # CPUs per FPGA core



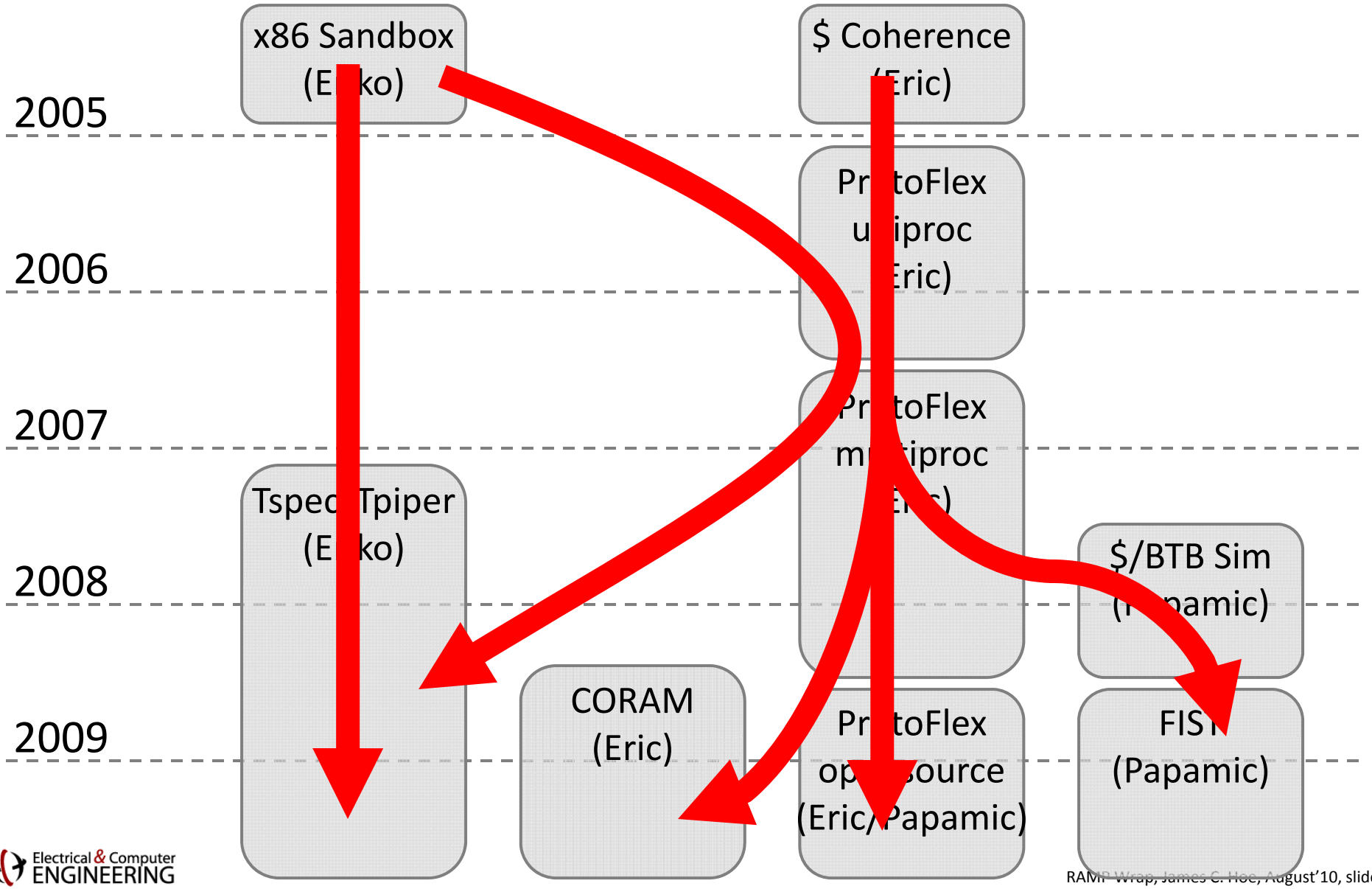
Hybrid Simulation



Virtualization

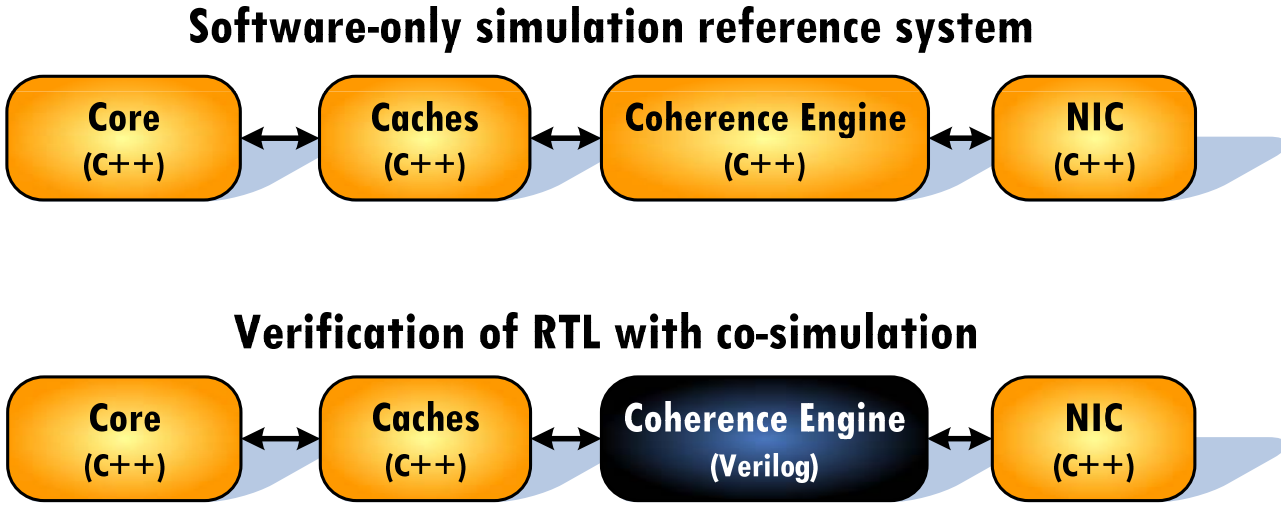
SINGLE-SLIDE REVIEW

The Road Travelled



PROTOFLEX

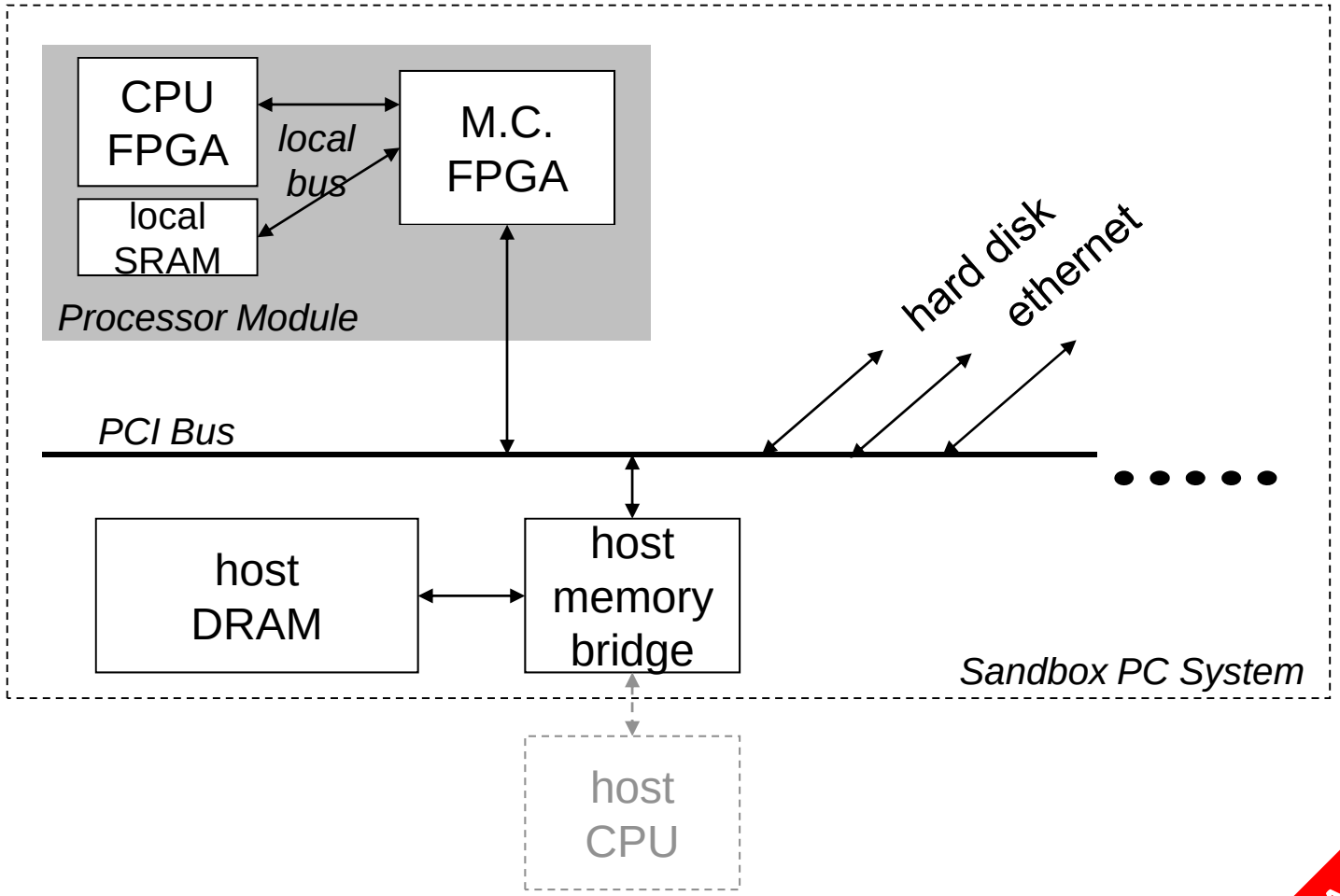
- **Systematic methodology for FPGA emulator development**
  - Rely on validated component-based simulators for reference
  - Create equivalent RTL piece-wise—validate with co-simulation



- **Advantages**
  - Gradual SW to HW transition
  - Concurrent RTL development of agreed reference model
  - Subsystem characterization

WARFP 2006
Eric

Sandbox Platform

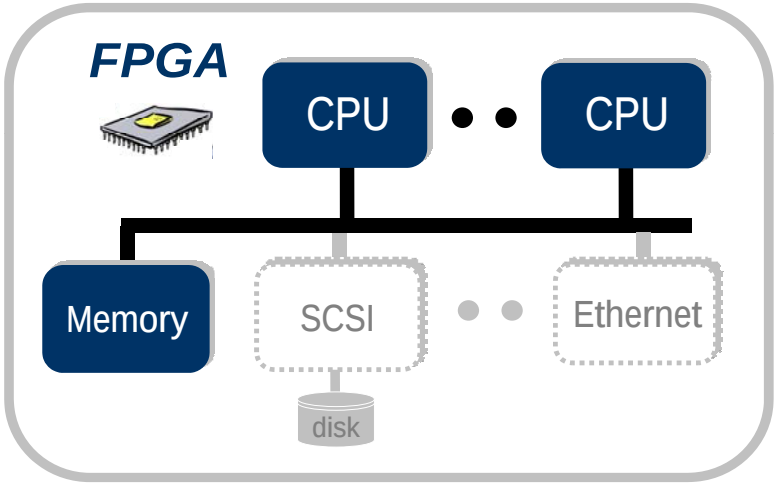


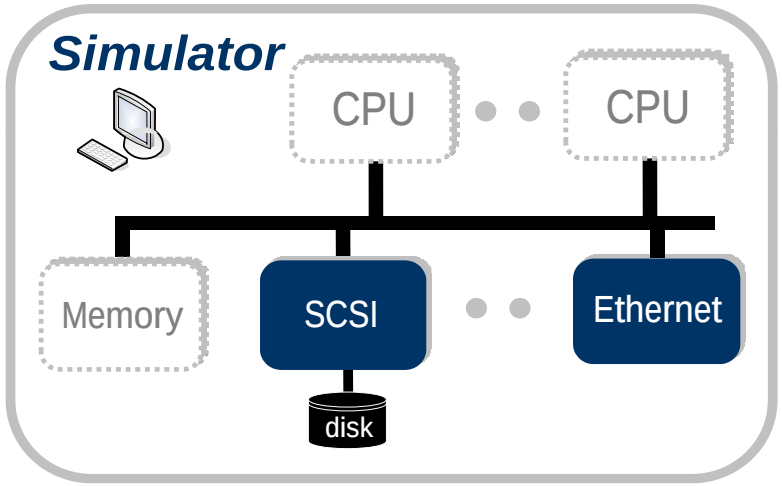
WARFP 2005
Eriko

Combining simulators & FPGAs

- **Simulators already provide full-system**

  ➔ why not simulate infrequent behaviors (e.g., I/O devices)?

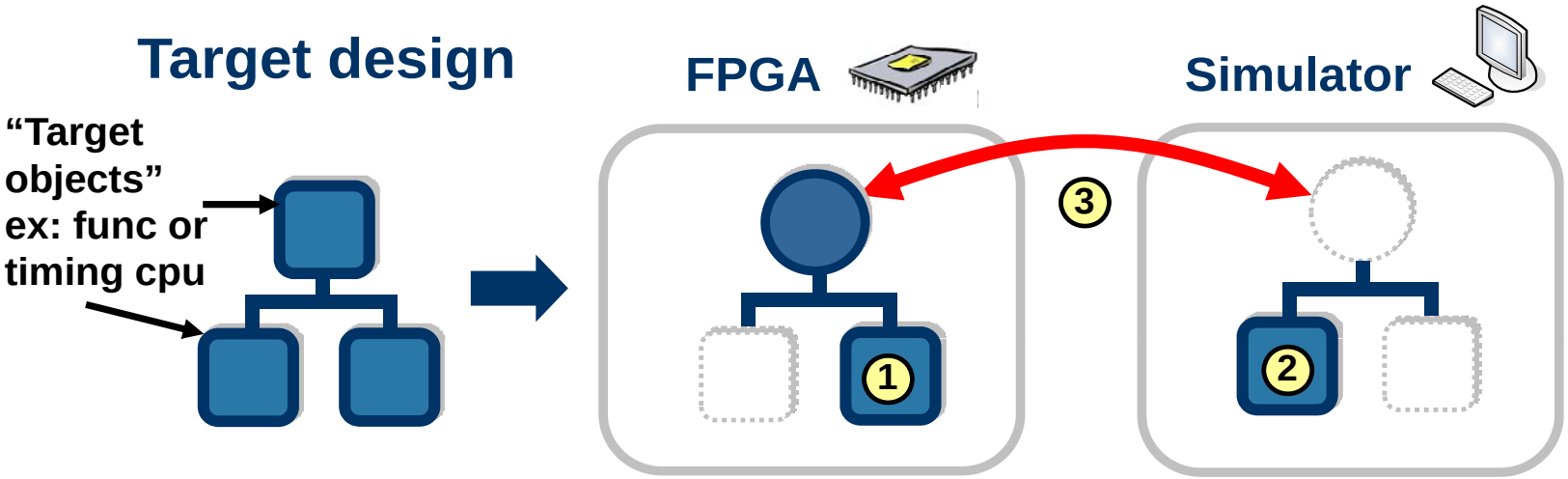




- **Advantages**
  - avoid impl. infreq. behaviors ➔ lowers full-system development
  - low impact on scalability & perf. on FPGA

RAMP Summer 2006, Eric

Migration



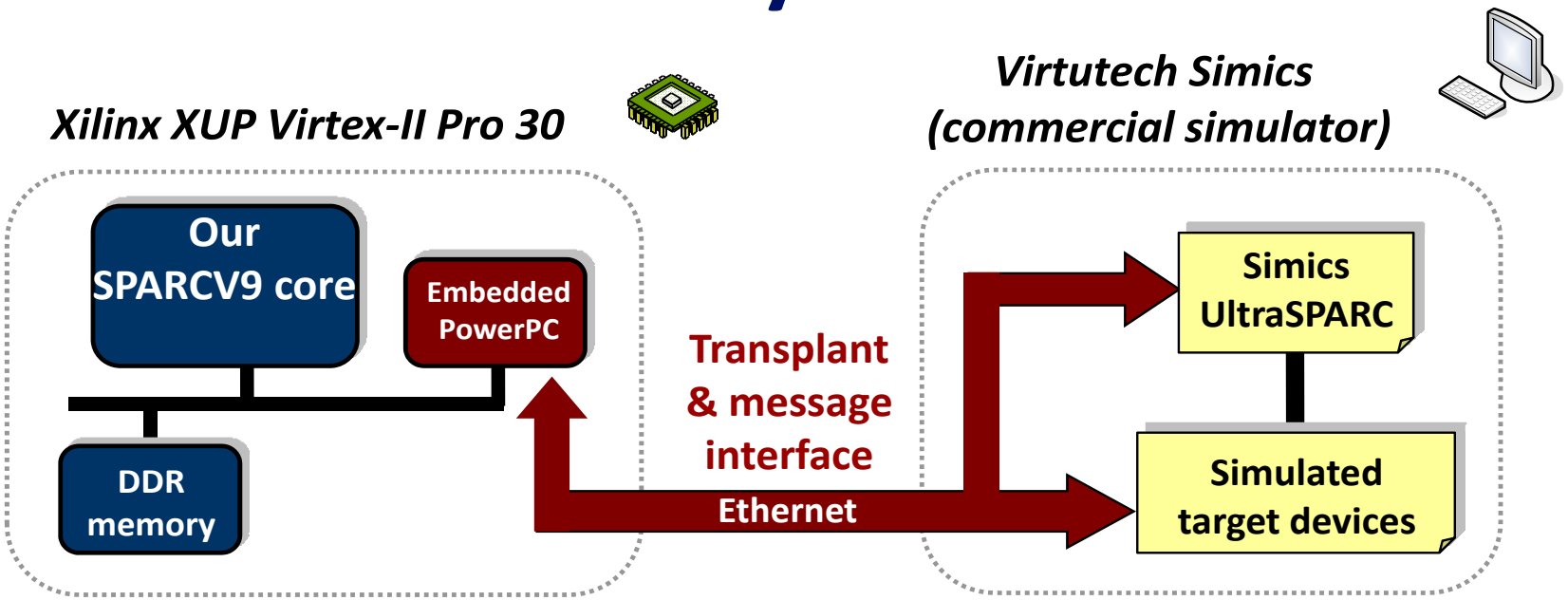
- **3 ways to map target object to host**

  FPGA-only ① Simulation-only ② Migratable ③

- **Migratable objects**
  - switch modes between FPGA & simulator hosts
  - *target behavior* need not be 100% in FPGA mode

    e.g., impl. 80% target behavior in FPGA, 100% in simulator

It Really Works



+

= "SUN 3800 Server"
(1x UltraSPARC III,
Solaris 8)

developed in 6 m

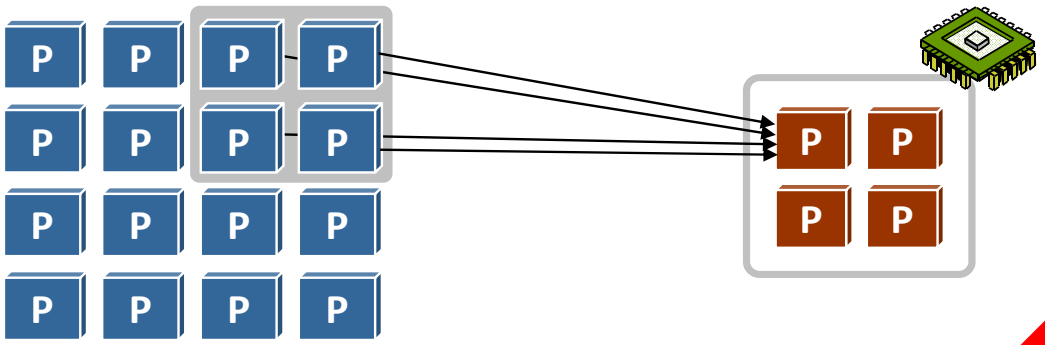
WARP 2007, Eric

Multiprocessor Host Interleaving

Advantages:

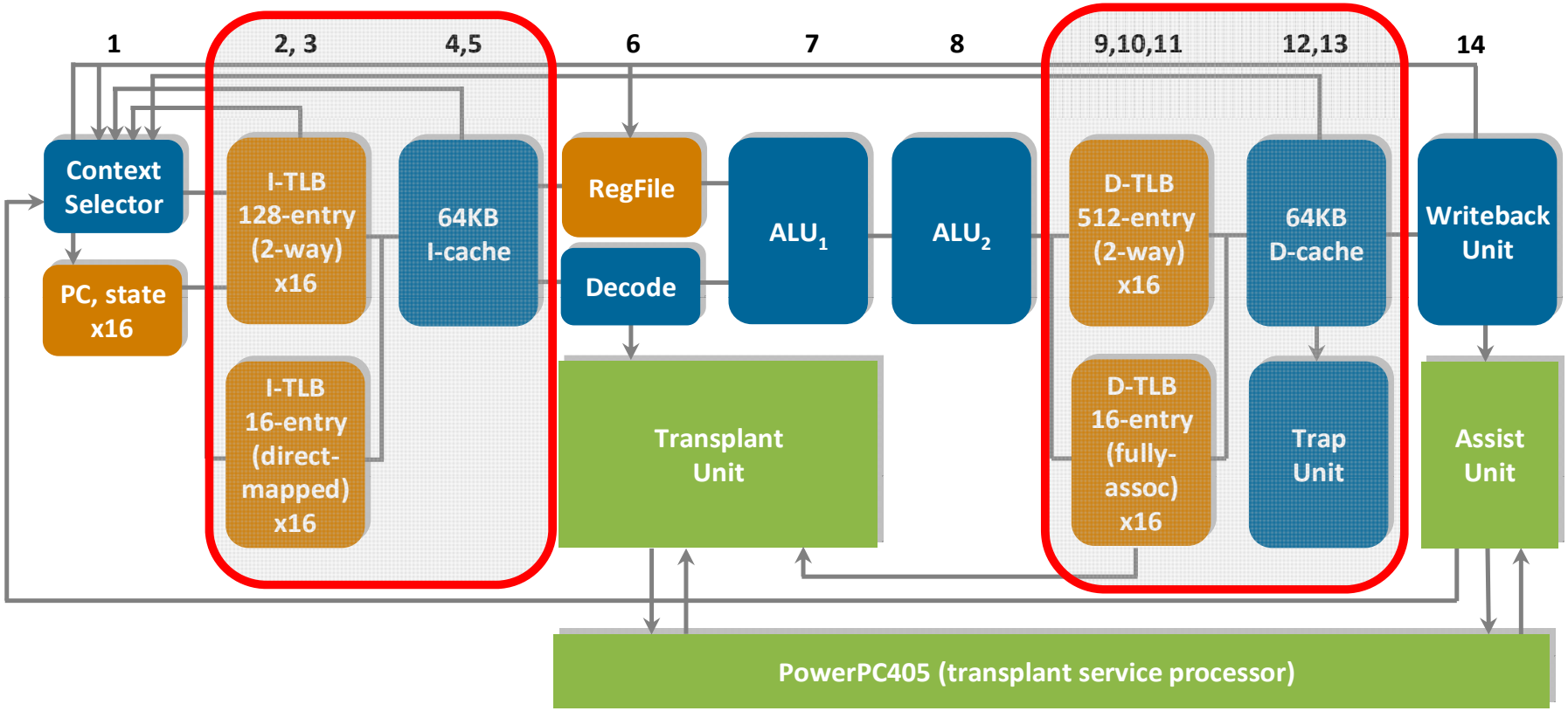
- Trade away FPGA throughput for smaller implementation
- Decouple logical simulated size from FPGA host size
- Host processor in FPGA can be made very simple

4-to-1 host interleaving



ISFPGA 2008 Eric

BlueSPARC host microarchitecture

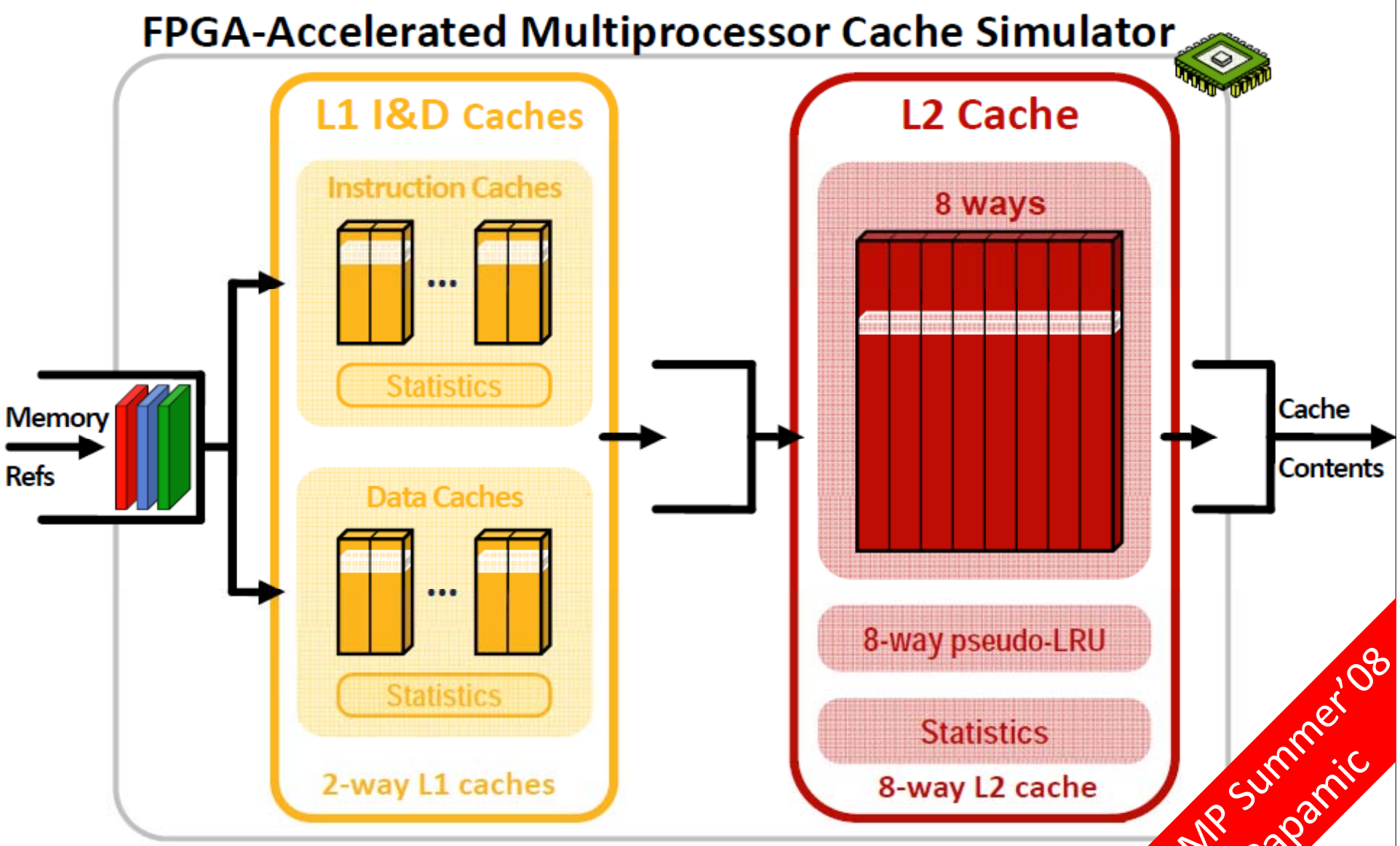


64-bit ISA, SW-visible MMU, complex memory

➔ high # of pipeline stages

ISFPGA 2008 Eric

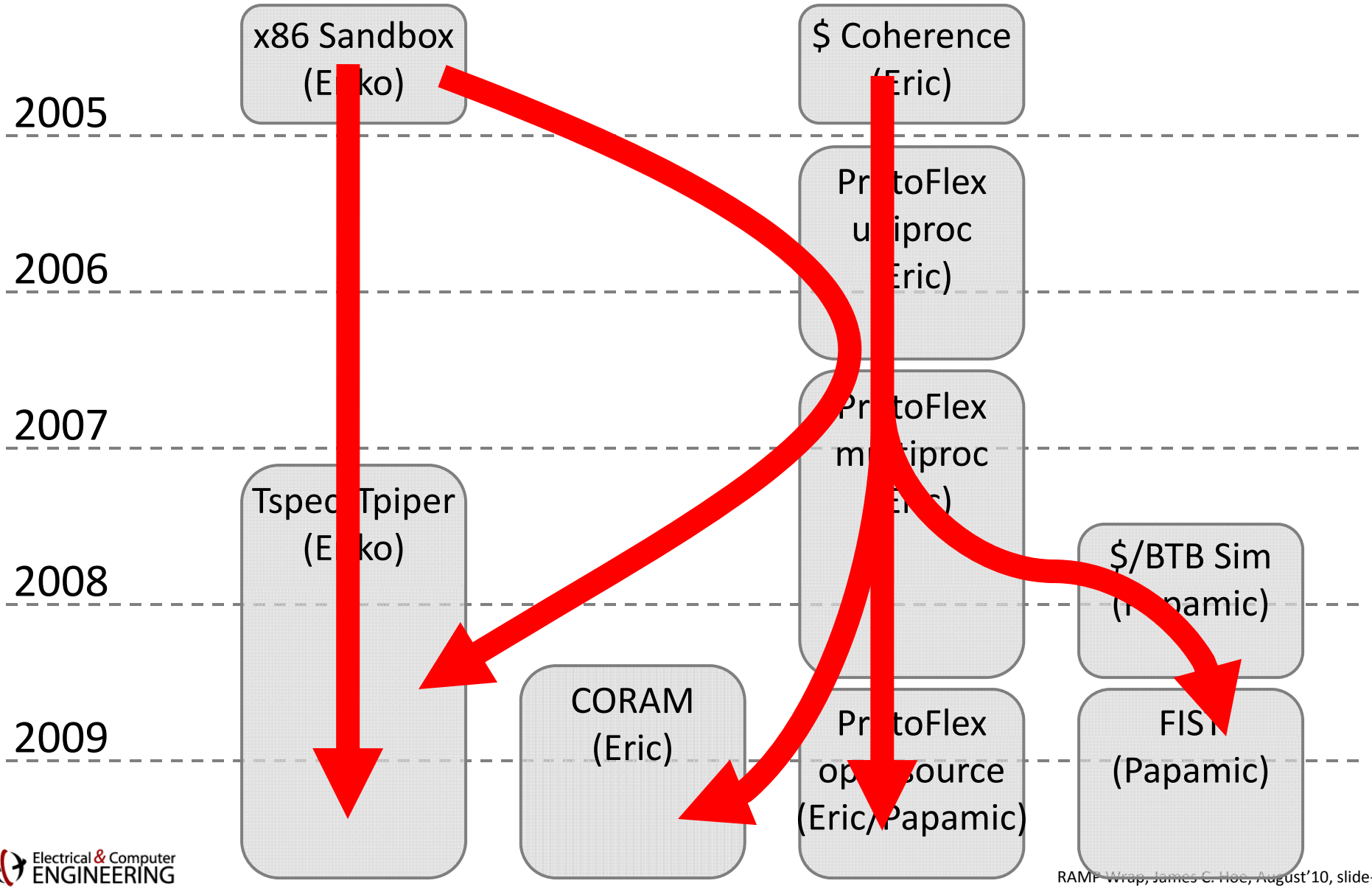
ProtoFlex Instrumentation



Open Sourcing ProtoFlex

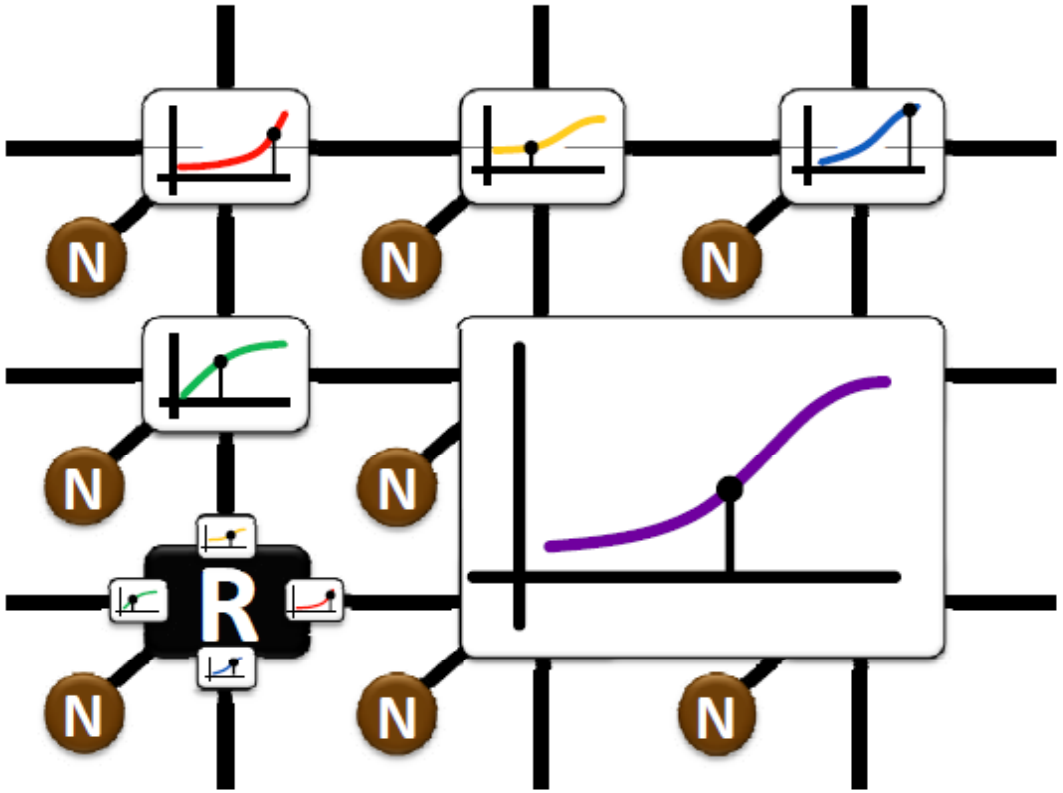
- **Why open source?**
  - Demonstration of FPGAs as viable architecture research vehicle
  - Facilitate adoption of **hybrid simulation** & **host multithreading**
  - Encourage building on top of our work
- **What are we releasing?**
  - Bluespec source HDL, Verilog and pre-generated netlists for SPARCV9 CPU model + interfaces
  - XUPV5 Reference Design for EDK 10.1
  - Virtutech Simics plug-ins for hybrid simulation
  - Top-level SW controller, user command-line interface
  - Documentation through online wiki

The Road Travelled



FIST Approach

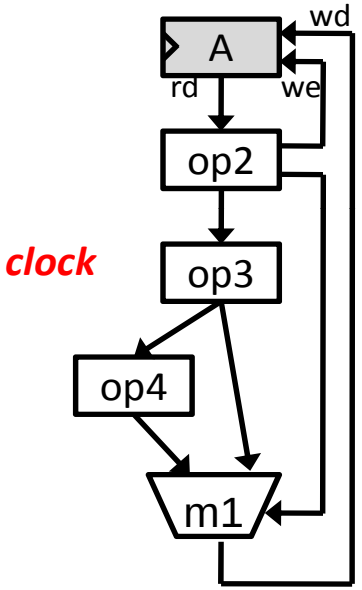
- **Treat each hop as a delay vs. load curve**
  - Trade-off between model complexity and fidelity
- **Keep track of load at each node**



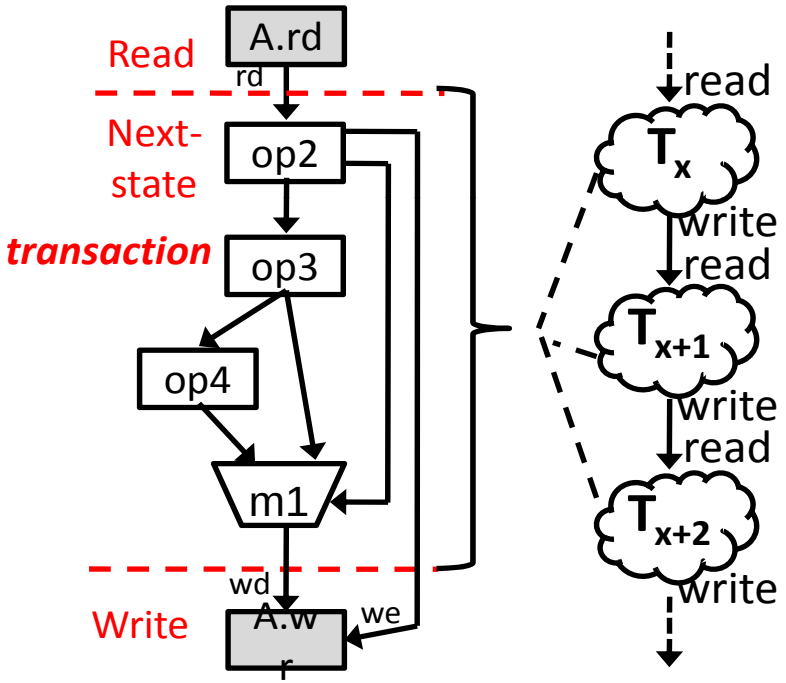
RAMP Winter'10
Papamic

Transactional Datapath Specification (T-spec)

Unpipelined RTL Datapath



T-spec: captures transaction abstraction



A clean way to reason about execution

Any implementation preserving transactional semantics i

Free from pipelining complexity (as simple as non-pipel L)

RAMP Winter'10 Eriko

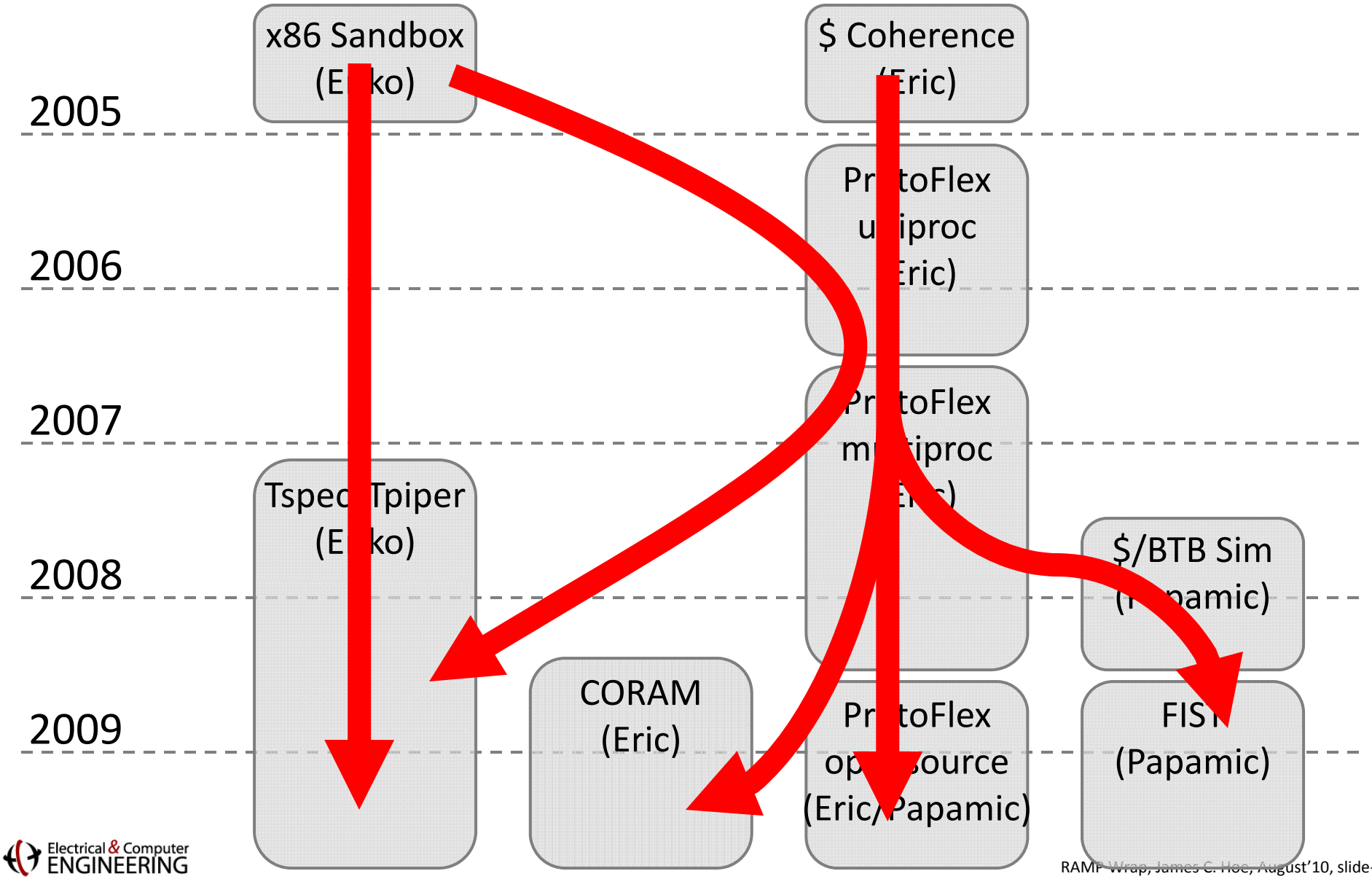
CORAM: FPGAs for Computing

- **Problems with programming today's FPGAs**
  - FPGAs today are meant to be ASIC-replacements (not compute)
  - RTL development effort requires more time
  - A major fraction of development effort goes into optimizing off- and on-chip interfaces to **bring data to where it needs to be**
  - Lack of portability of designs (interfaces usually must be respun)

- **Our observation**
  - *For any application running on any computing architecture---how memory is **organized**, **optimized**, and **delivered** is nearly as important as optimizing for the compute logic*

RAMP Summer'10 Eric

The Road Travelled



CARL'2010 Workshop

http://www.ece.cmu.edu/calcm/carl2010

- Workshop on the Intersections of Computer Archtecture and Reconfigurable Logic (CARL)
- Bring reconfigurable logic and reconfigurable computing to the computer architecture audience
  - 4~6 pages on any topic computer architects should care about
  - it is okay if the paper has been published in non-computer architecture forums
  - paper submission on October 1st
- Co-located with MICRO-43, Atlanta, December 5
- Organized by Derek, Joel and James; many familiar names on the TPC