Ramp Wrap

Kees Vissers
Xilinx

Contents

- Historic perspective
- Achievements and impact on Research and Xilinx
- High Level Synthesis
- Next step: ARM processors + FPGA
- Virtex7 , 28nm, power and compute
- Conclusion

Historic Perspective

- Kick-off around Hot Chips 2005, NSF proposal
- Donation of Chips, Project and boards, first work on Bee2
- Excellent cooperation, basically still an ‘unfunded’ project of the interested PIs
- First set of microblaze based implementations on XUPV2pro and racks of Bee2 systems
- Good cooperative spirit, very high quality teams and contributions
- Sparc emulations, strong influence on XUPV5.
- Chuck Thacker joins, professional Bee3 development, start of Beecube
- Many good basic systems: blue, white, red, gold …..
- Excellent work on Target and Host cycle decoupling
- Excellent work on combining Software and Hardware architecture simulation

Impact on Xilinx

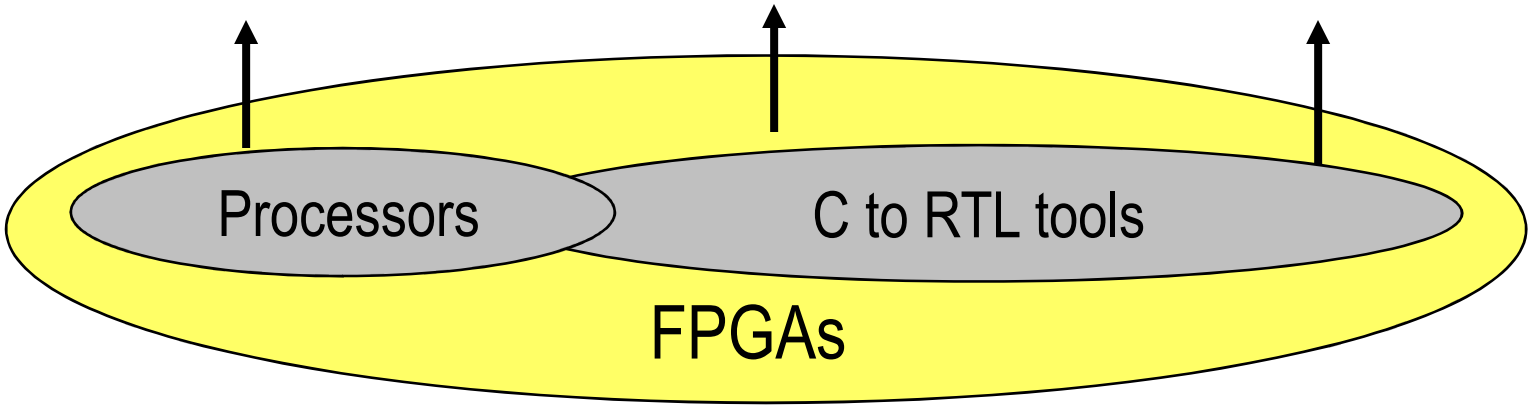
- Early work on XUPV2pro: Microblaze with MMU that now boots a full OS
- Work using V2, V5 and V6 (Bee4)
- Importance of using BRAM in emulating: even more BRAM on our FPGAs
- No avoidance for the memory wall and the power wall: More high speed I/Os, focus on Low Power in V7 for complete family
- Contribute to the importance of multicore and complete systems: Multicore Arm Product, with FPGA
- Programming remains too Hard: first High-level Synthesis, second models with a memory model.

Next

- Parlab: programming models
- XUP based systems in education
- Cloud FPGA supercomputer center
- Beecube off the ground
- Startup for architecture simulation?
- ARM + FPGA based programming views, open invitation
- NetFPGA 10G
- Microsoft back in Computer Architecture……..
- Xilinx will continue to look for good cooperation with top Universities and Industrial Research

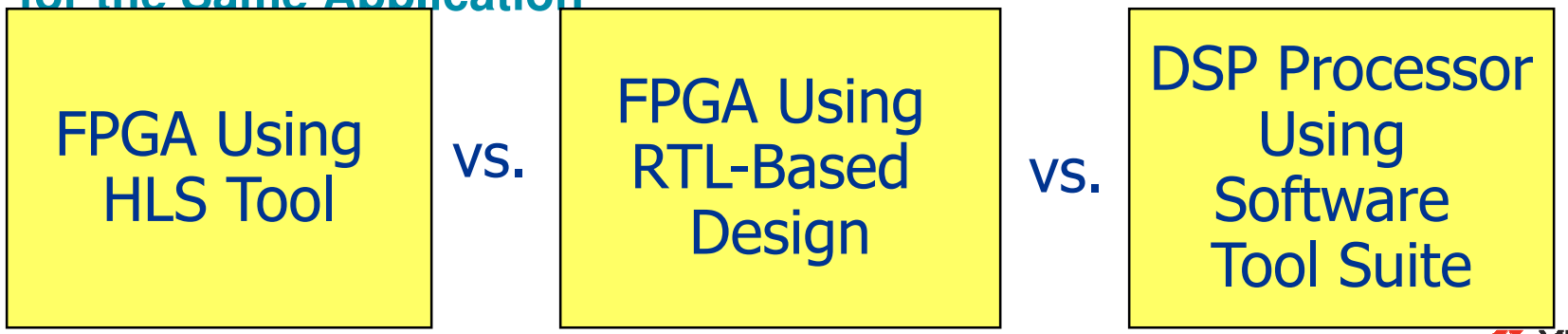
Processors and Pipelines

Design approach	RISC Proc.	Proc. w/ accels.	Folded datapath	Pipelined datapath	Replicated datapath
clock:sample	1000:1	100:1	10:1	1:1	1:10
Data Rate (200MHz clock)	200Ks/s	2Ms/s	20Ms/s	200Ms/s	2 Gs/s
Applications	control → audio → mobile video → HDTV → comms → networking				



BDTI High-Level Synthesis Tool Certification Program

- **The certification program was developed through a collaboration between BDTI and Xilinx**
  - The two companies jointly developed a robust methodology for evaluating HLS tools
  - The program incorporates two realistic example applications, one in wireless and one in video
- **The program currently evaluates HLS tools targeting Xilinx FPGAs**
- **The first two vendors to participate are AutoESL and Synfora, now Synopsys**
- **The Program Compares FPGA & DSP Implementation Approaches for the Same Application**



BDTI and the Xilinx Video Starter Kit

Use the video starter kit, and the given video files on the provided box.

- **Board contains a Spartan3 3400A**
  126 DSP48,
  126 BRAMs (18Kb),
  47,744 (4-input) LUTs

Optical flow:

- **Two operating points:**
  - real-time 60fps, 1280 x 720p (75Msps)
  - Maximum performance using all resources.

DQPSK: fixed workload 18.75Msps running with an implementation at 75MHz (initiation interval = 4).

Video Starter Kit

Video Source 'DVIco box'

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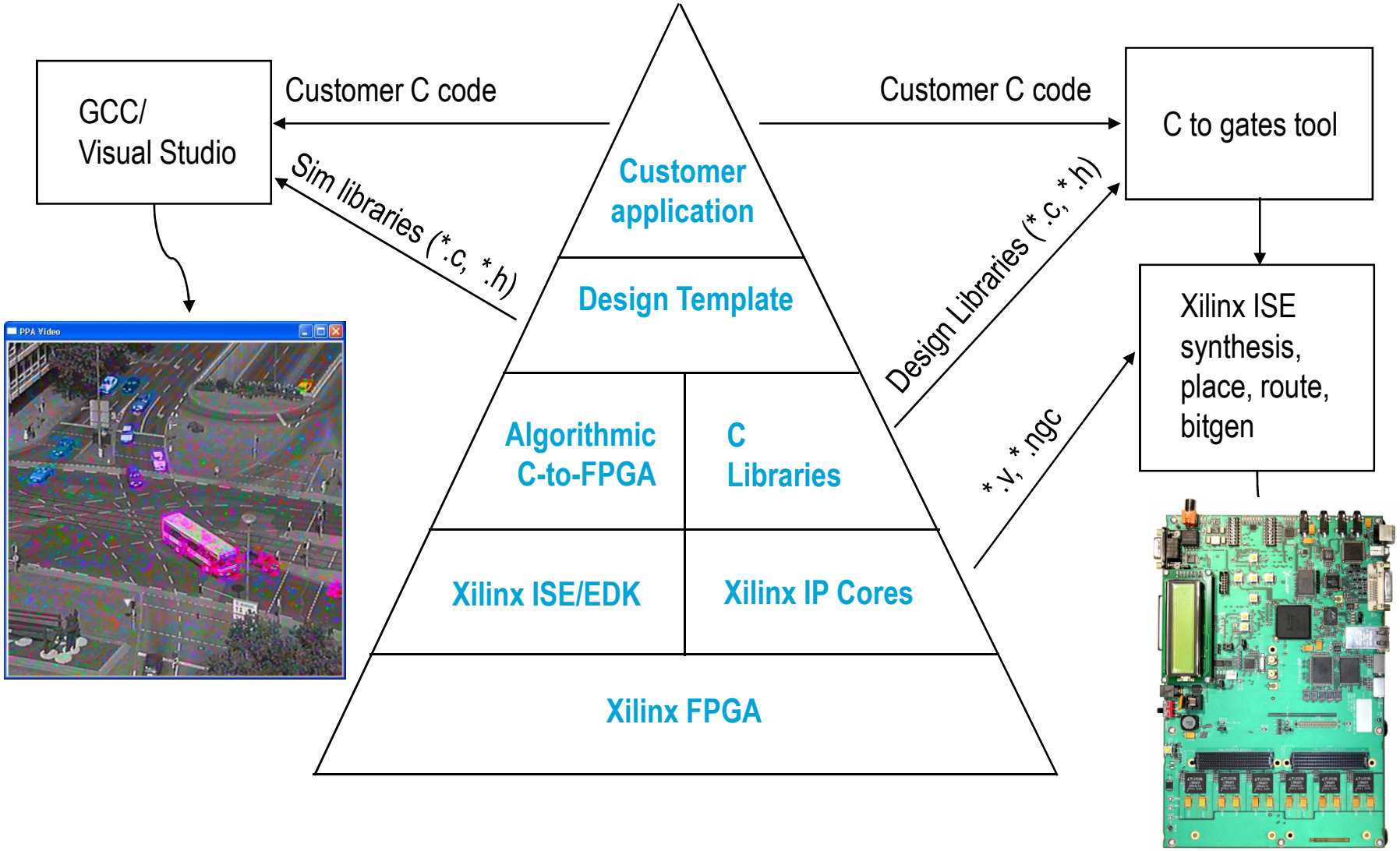
Design Flow



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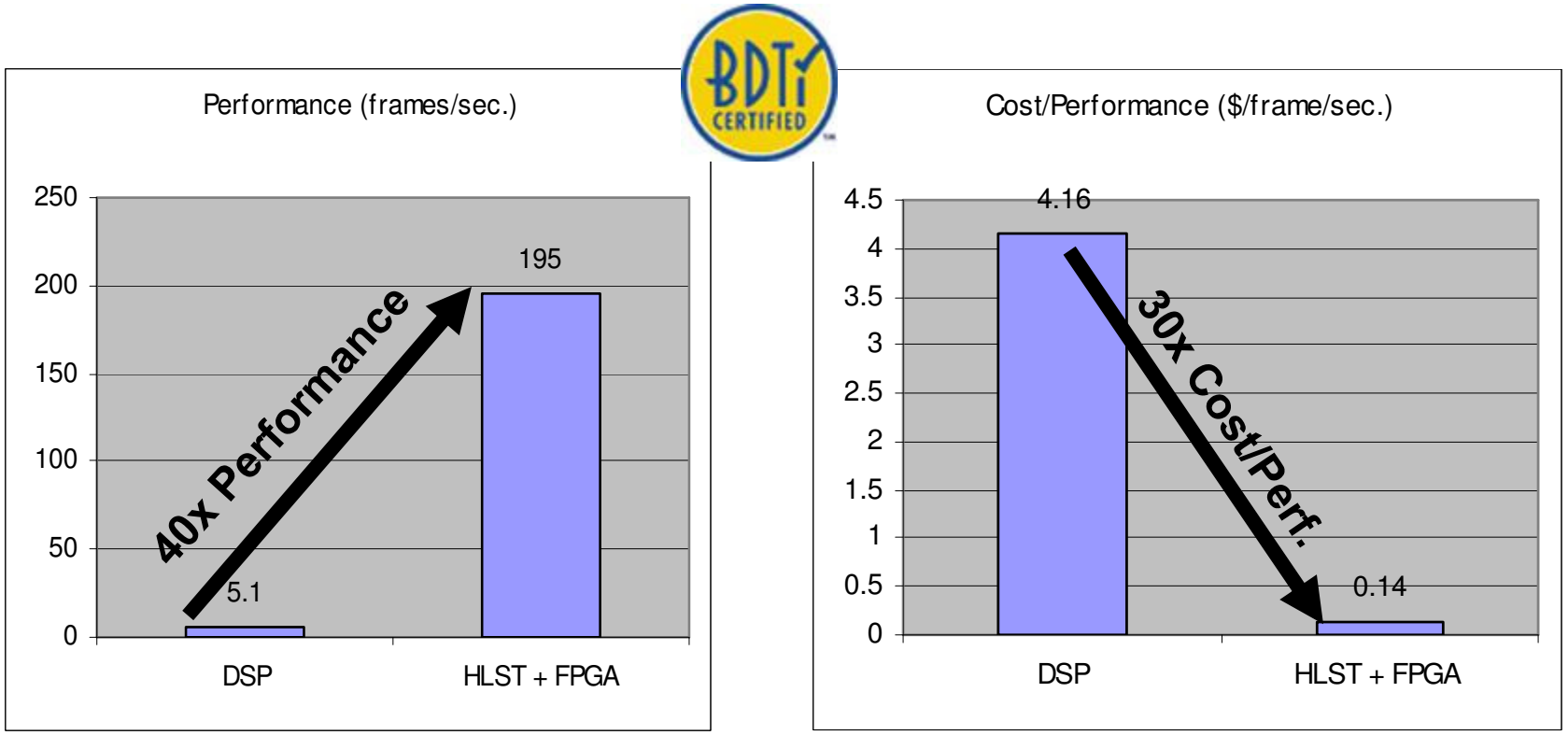
Very good results compared to a DSP for the Video Application

Certified results for the BDTI Optical Flow Workload, Operating Point 2: maximum frame rate achievable at 720p resolution



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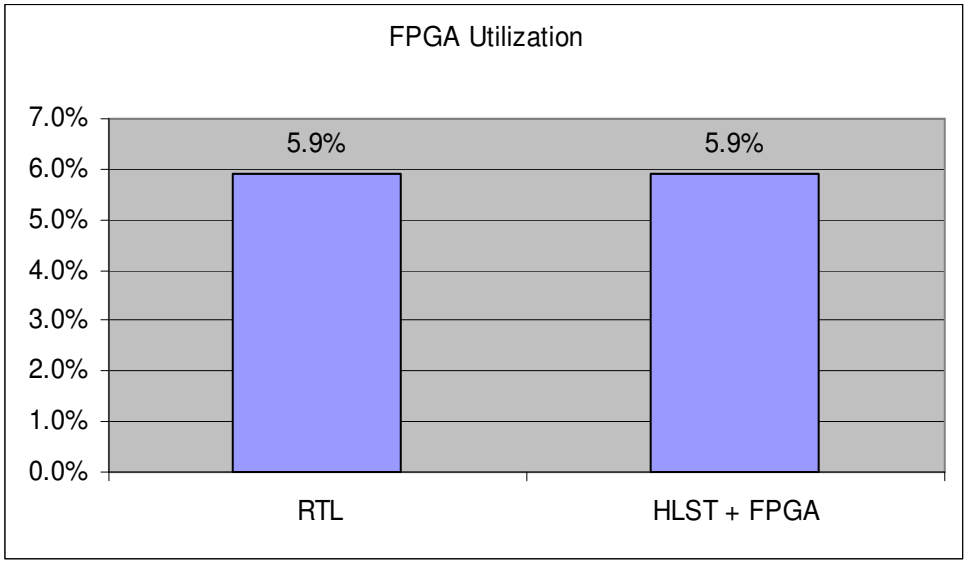
Synthesized results from C program as good as manual RTL

Results for the BDTI DQPSK Receiver Workload, 18.75 Msamples/second input data with a 75 MHz clock



These results are consistent with those reported by HLST users interviewed by BDTI

Usability Metrics (1 of 2) Representative Results based on the BDTI Optical Flow™ Workload

Metric	Out-of-Box Experience	Ease of Use	Completeness of Capabilities	Quality of Documentation and Support)
Combined HLST + Xilinx RTL tools (HLST rating / Xilinx rating)	**Fair** (Very Good / Poor)	**Good** (Good / Fair)	**Good** (Good / Good)	**Good** (Good / Very Good)
Texas Instruments DM6437 DSP processor and tool suite	**Good**	**Very Good**	**Very Good**	**Very Good**

The above table provides qualitative usability metric scores. Note that HLS tools + Xilinx tools targeting an FPGA include a combined overall score (in bold) followed in parenthesis by:

- The score for the HLS tool only (the first score in parenthesis)
- The score for the Xilinx RTL tools only (the second score in parenthesis)

Usability Metrics (2 of 2) Representative Results based on the BDTI Optical Flow™ Workload

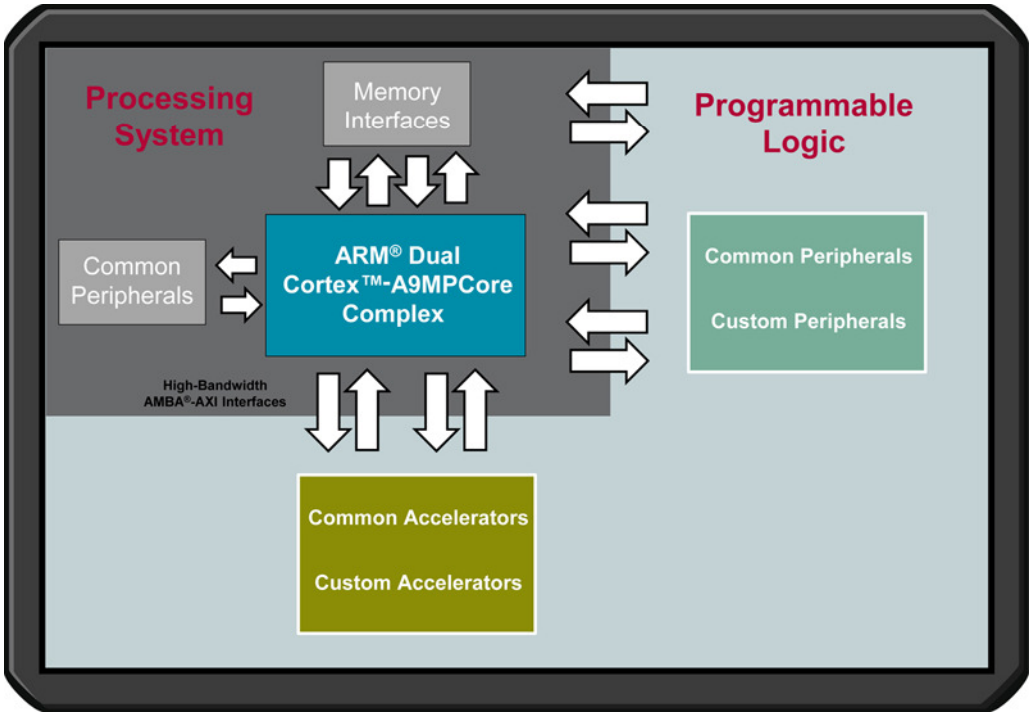
Metric	Efficiency of Design Methodology				
	Learning to use the Tool	Design & Implementation (first compiling version)	Design & Implementation (final optimized version)	Platform Infrastructure Development	Extent of Modifications to Reference Code)
Combined HLST + Xilinx RTL tools (HLST rating / Xilinx rating)	**Good** (Good / N.A.)	**Very Good** (Very Good / N.A.)	**Good** (Good / Good)	**Good** (Good / Good)	**Good** (Good / Good)
Texas Instruments DM6437 DSP processor and tool suite	**N.A.**	**Excellent**	**Good**	**Good**	**Fair**

The above table provides qualitative usability metric scores. Note that HLS tools + Xilinx tools targeting a Xilinx FPGA include a combined overall score (in bold) followed in parenthesis by:

- The score for the HLS tool only (the first score in parenthesis)
- The score for the Xilinx RTL tools only (the second score in parenthesis)

Next Generation Extensible Platform

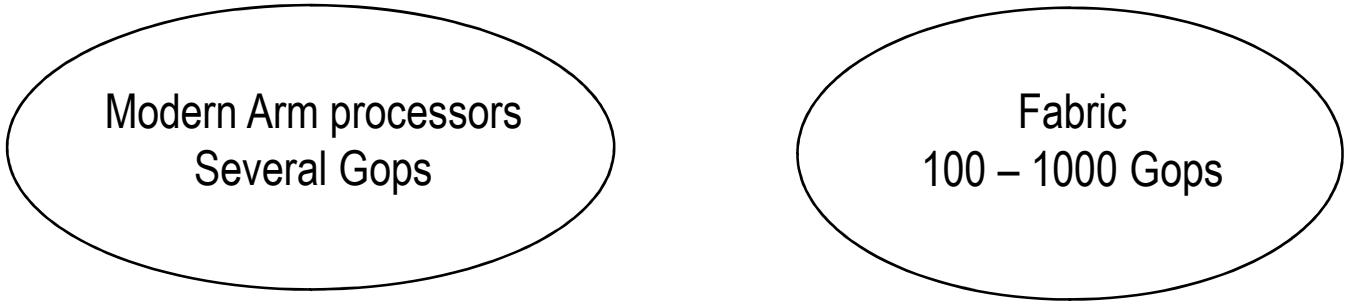
- Arm A9 Processors
- FPGA fabric
- Several mechanisms for interconnect



Next generation Products in context

Design approach	RISC Proc.	Proc. w/ accels.	Folded datapath	Pipelined datapath	Replicated datapath
clock:sample	1000:1	100:1	10:1	1:1	1:10
Data Rate (200MHz clock)	200Ks/s	2Ms/s	20Ms/s	200Ms/s	2 Gs/s

Applications control → audio → mobile video → HDTV → comms → networking



Introducing the Xilinx 7 Series FPGAs

Industry's First Unified Architecture

- **Industry's Lowest Power and First Unified Architecture**
  - Spanning Low-Cost to Ultra High-End applications
- **Three new device families with breakthrough innovations in power efficiency, performance-capacity and price-performance**

	ARTIX-7	KINTEX-7	VIRTEX-7
	Lowest Power & Cost	Industry's Best Price/Performance	Industry's Highest System Performance
Logic Cells	20K – 355K	30K – 410K	285K – 2,000K
DSP Slices	40 – 700	120 – 1540	700 – 3,960
Max. Transceivers	4	16	80
Transceiver Performance	3.75Gbps	6.6Gbps 10.3Gbps	10.3Gbps 13.1Gbps 28Gbps
Memory Performance	800Mbps	2133Mbps	2133Mbps
Max. SelectIO™	450	500	1200
SelectIO™ Voltages	3.3V and below	3.3V and below 1.8V and below	3.3V and below 1.8V and below

Note: Information on 28Gbps serial transceiver support to be disclosed later this year

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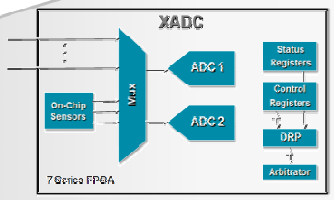
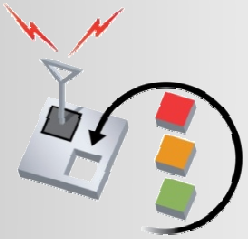
Xilinx Focused on Power Efficiency from Every Angle

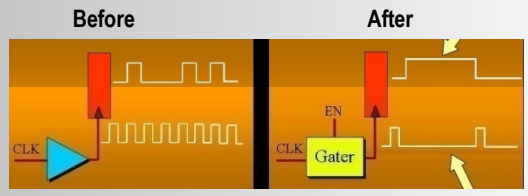
Additional Power Savings



Integrated Analog Front End



5th gen. partial reconfiguration



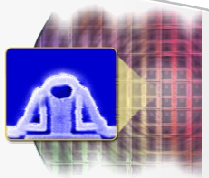
Fine grain clock and logic gating

-1 L Xilinx 7 Series FPGAs

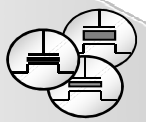
Lower device core voltage

***Low Power* by Xilinx**

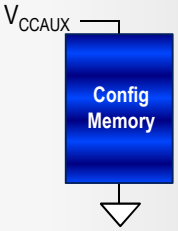
Reducing Static Power



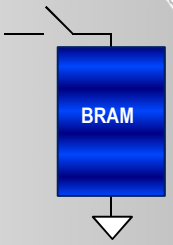
High performance, low power process



Transistor choice optimization

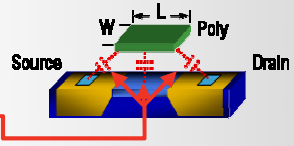


Reduced from 2.5V to 1.8V



Unused BRAM Power Savings

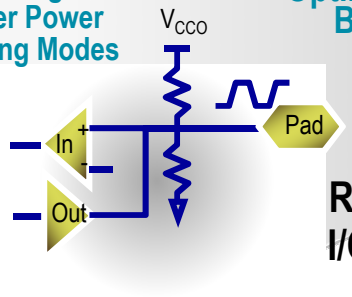
Process Shrink



Reducing Dynamic Power

IO Design & User Power Saving Modes

Optimized Hard Blocks



Reducing I/O Power

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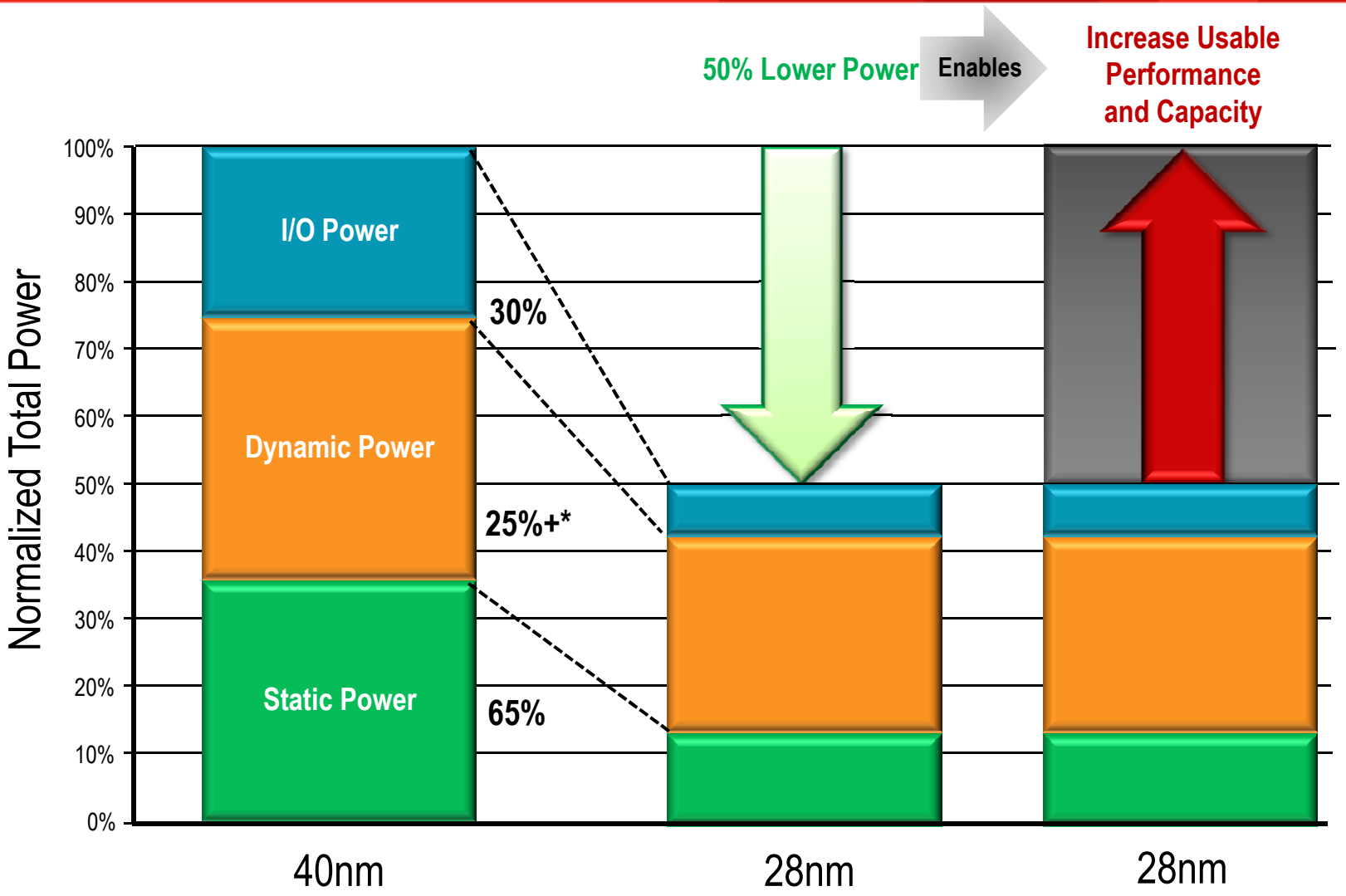
The Power Payoff: Capacity and Capability



* Additional savings beyond 25% from optimized hardened blocks

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7 Series Families Comparison

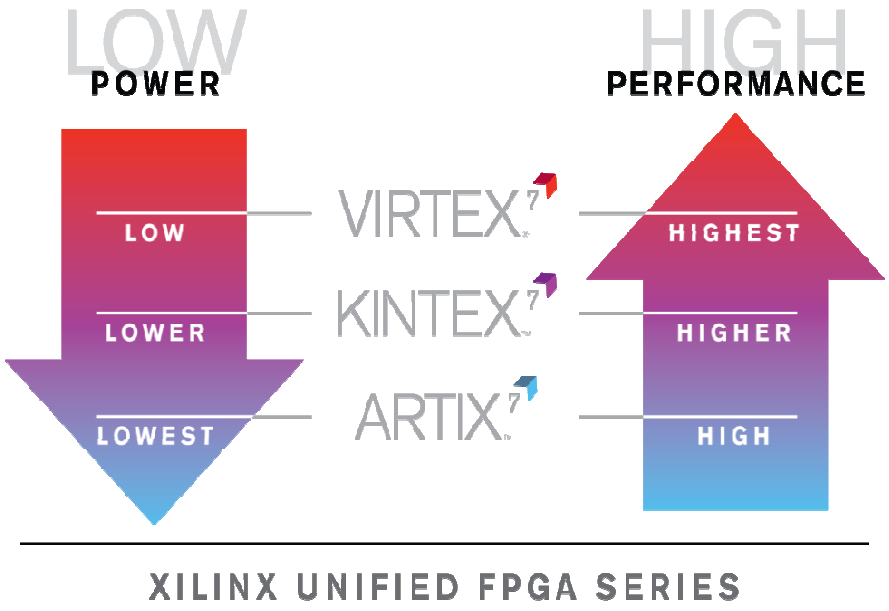
- **Unified architecture, scalable across all families from high-volume to ultra high-end applications**
  - Each family optimized for power, performance and price meeting specific application needs

Maximum Capability	Artix-7 Family	Kintex-7 Family	Virtex-7 Family
Logic Cells	352K	407K	1,955K
Block RAM	12Mb	29Mb	65Mb
DSP Slices	700	1,540	3,960
Peak DSP Performance (symmetric FIR)	504 GMACS	1,848 GMACS	4,752 GMACS
Transceiver Count	4	16	80
Peak Transceiver Speed	3.75Gbps	10.3125Gbps	13.1Gbps+
Peak Serial Bandwidth (full duplex)	30Gbps	330Gbps	1,886Gbps
PCI Express Interface	Gen1 x4	Gen2 x8	Gen3 x8*
Memory Interface	800Mbps	2,133Mbps	2,133Mbps
I/O Pins	450	500	1,200
I/O Voltage	1.2V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V**
Packaging Options	Low cost wire bond	Low cost lidless flip chip and High performance flip chip	Highest performance flip chip

* Check Product Overview for device details on soft vs. hard Gen3 x8 and 2.5v and 3.3v support

Xilinx 7 Series Meets Next Generation Design Challenges

- **Highest System Performance**
  - Advanced features and industry leading capacity
- **Highest Productivity**
  - Unified architecture enables IP portability and design scalability saving engineering investments
- **Lowest Total Power**
  - Allowing additional system performance



Virtex-7 Family – Highest Performance and Capacity FPGAs

VIRTEX 7

	Industry's Highest System Performance	
		Optimized for communication systems requiring highest performance and serial connectivity. Enabling world's 1st Ultra High End FPGAs.
Logic Cells	285K – 2,000K	World's 1st 2M logic cell FPGA
DSP Slices	700 – 3,960	Max. DSP throughput = 2.4TMACS (symmetric FIR 4.7TMACS)
Max. Transceivers	80	Max. serial bandwidth = 1.9Tbps Max. parallel I/O bandwidth = 0.92Tbps
Transceivers Performance	10.3Gbps 13.1Gbps 28Gbps*	Combined bandwidth = 2.4Tbps
Memory Performance	2133Mbps	576 differential I/O pairs @ 1.6Gbps LVDS and DDR3-2133
Max. SelectIO™	1200	
Select IO Voltages	3.3V and below 1.8V and below	1.8V/3.3V I/O mixture optimized to meet the wide range of high performance application requirements

EasyPath™-7 for additional cost savings

* Information on 28Gbps serial transceiver support to be disclosed later this year

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Compute and Power Consumption experience

- Video and Signal processing Risc operations (mostly 16 bit) require in the range of 10- 20 Luts per Risc operation, profiled on actual designs
- With mostly 32 bit operations this goes to 20-30 Luts per Risc operation, profiled on actual designs.
- Floating Point supported with High Level Synthesis
- The power consumption of a total system is significant in the I/O subsystem: Drive to High Speed serial with low swing and to large devices with a large amount of logic/embedded memory/DSPs
- The communication between processors and FPGA requires low latency and lots of bandwidth: PCIe, cooperation with Intel on QPI, and integrated processors (ARM) for midrange
- New Virtex7 devices will have 568,000 6-input LUTs, and 3,960 DSP elements.
- This leads to compute in the range of (568,000 /20) + 3,960 *2 = 36,320 Risc operations
- This is in the range of 300Mhz * 36,320 ~ 10 * 10^{12} or 10 Tera ops

Summary

- It was an honor and pleasure to interact with the RAMP community.
- Contributed data to the direction in Xilinx
- Pleasure to contribute where we can with excellent Universities and Industry
- Personal thank you to Paul Hartke who helped beyond the standard XUP program.

Backup

- Detailed Series 7 parts

Artix-7 FPGA Family

Rev 3.16 data - This table updated 11 June 2010.
Get latest product information at www.xilinx.com/7.

Artix™-7 FPGAs

Optimized for Lowest Cost and Power with Small Form-Factor Packaging for the Highest Volume Applications (1.0 Volt, 0.9Volt)

	Part Number	XC7A20	XC7A40	XC7A105	XC7A175T	XC7A355T
Logic Resources	Slices [1]	2,800	6,200	16,200	27,050	55,050
	Logic Cells [2]	17,920	39,680	103,680	173,120	352,320
	CLB Flip-Flops	22,400	49,600	129,600	216,400	440,400
Memory Resources	Maximum Distributed RAM (Kbits)	225	450	1,275	2,063	4,188
	Block RAM/FIFO w/ ECC (36kbits each)	20	40	120	185	335
	Total Block RAM (Kbits)	720	1,440	4,320	6,660	12,060
Clock Resources	Mixed Mode Clock Managers (MMCM)	2	4	6	9	9
I/O Resources	Maximum Single-Ended I/O	100	200	300	450	450
	Maximum Differential I/O Pairs	48	96	144	216	216
Embedded Hard IP Resources	DSP48E1 Slices	40	80	240	400	700
	Gen1 PCI Express Interface Blocks	—	—	—	1	1
	Analog Front End (XADC) / SysMon Blocks	—	—	1	1	1
	Configuration AES / HMAC Blocks	—	—	1	1	1
	GTP 3.75Gpbs Transceivers	—	—	—	4	4
Speed Grades	Commercial	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2, -3
	Industrial	-L1, -1, -2	-L1, -1, -2	-L1, -1, -2	-L1, -1, -2	-L1, -1, 2
Configuration	Configuration Memory (Mbits)	5.2	10.4	27.0	45.0	84.6
Package [4]	**Area (Pitch)**	**Available User I/O: 3.3V SelectIO™ Pins[3] (GTP Transceivers)**				
Wire bond, chip scale BGA (0.5mm ball spacing)						
CPG236	10 x 10 mm	100 (0)	140 (0)	140 (0)		
Wire bond, chip scale BGA (0.8mm ball spacing)						
CSG324	15 x 15 mm		200 (0)	210 (0)	210 (0)	
CSG484	19 x 19 mm			285 (0)	285 (4)	285 (4)
Wire bond, fine pitch BGA (1.0 mm ball spacing)						
FTG256	17 x 17 mm	100 (0)	170 (0)			
FGG484	23 x 23 mm			300 (0)	325 (0)	325 (0)
FGG784	29 x 29 mm				450 (4)	450 (4)

Kintex-7 FPGA Family

Rev 3.16 data - This table updated 11 June 2010.
Get latest product information at www.xilinx.com/7.

Kintex-7™ FPGAs
Optimized for Highest Price-Performance
(1.0 Volt, 0.9Volt)

	Part Number	XC7K30T	XC7K70T	XC7K120T	XC7K230T	XC7K410T
Logic Resources	Slices [1]	4,750	10,550	18,350	35,550	63,550
	Logic Cells [2]	30,400	67,520	117,440	227,520	406,720
	CLB Flip-Flops	38,000	84,400	146,800	284,400	508,400
Memory Resources	Maximum Distributed RAM (Kbits)	413	838	1,500	3,038	5,663
	Block RAM/FIFO w/ ECC (36kbits each)	65	135	225	445	795
	Total Block RAM (Kbits)	2,340	4,860	8,100	16,020	28,620
Clock Resources	Mixed Mode Clock Managers (MMCM)	3	6	8	10	10
I/O Resources	Maximum Single-Ended I/O	150	300	400	500	500
	Maximum Differential I/O Pairs	72	144	192	240	240
Embedded Hard IP Resources	DSP48E1 Slices	120	240	400	840	1,540
	Gen2 PCI Express Interface Blocks	1	1	1	1	1
	Analog Front End (XADC) / SysMon Blocks	—	—	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1
	GTX 10.3125Gbps Transceivers	4	8	8	16	16
Speed Grades	Commercial	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2
	Industrial	-L1, -1, -2	-L1, -1, -2	-L1, -1, -2	-L1, -1, -2	-L1, -1, -2
Configuration	Configuration Memory (Mbits)	11.6	23.1	37.3	71.0	122.0
Package [5]	**Area (Pitch)**	**Available User I/O: 3.3V capable SelectIO™ Pins[3], 1.8V SelectIO Pins[4] (GTX Transceivers)**				
Lidless chip scale BGA supporting 6.6Gbps serial line rates (0.8mm ball spacing)						
SBG324	15 x 15 mm	100, 50 (4)	114, 50 (4)			
Lidless flip chip BGA supporting 6.6Gbps serial line rates (1.0mm ball spacing)						
FBG484	23 x 23 mm	100, 50 (4)	185, 100 (4)	185, 100 (4)		
FBG676	27 x 27 mm		200, 100 (8)	250, 150 (8)	250, 150 (8)	250, 150 (8)
FBG900	31 x 31 mm				350, 150 (16)	350, 150 (16)
Flip chip BGA supporting 10.3Gbps serial line rates (1.0mm ball spacing)						
FFG676	27 x 27 mm			250, 150 (8)	250, 150 (8)	250, 150 (8)
FFG900	31 x 31 mm				350, 150 (16)	350, 150 (16)

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Virtex-7 FPGA Family

Rev 3.16 data - This table updated 11 June 2010.
Get latest product information at www.xilinx.com/7.

Virtex®-7 FPGAs
Optimized for Highest System Performance and Capacity
(1.0 Volt, 0.9Volt)

	Part Number	XC7V285T	XC7V450T	XC7V585T	XC7V855T	XC7V1500T	XC7V2000T	XC7VX415T	XC7VX485T	XC7VX605T	XC7VX690T	XC7VX895T	XC7VX910T
	EasyPath™ Cost Reduction Solutions [1]	XCE7V285T	XCE7V450T	XCE7V585T	XCE7V855T	XCE7V1500T	XCE7V2000T	XCE7VX415T	XCE7VX485T	XCE7VX605T	XCE7VX690T	XCE7VX895T	XCE7VX910T
Logic Resources	Slices [2]	44,700	70,450	91,050	133,350	229,050	305,400	64,400	75,900	94,800	107,800	139,600	142,200
	Logic Cells [3]	286,080	450,880	582,720	853,440	1,465,920	1,954,560	412,160	485,760	606,720	689,920	893,440	910,080
	CLB Flip-Flops	357,600	563,600	728,400	1,066,800	1,832,400	2,443,200	515,200	607,200	758,400	862,400	1,116,800	1,137,600
Memory Resources	Maximum Distributed RAM (Kbits)	3,475	5,388	6,938	10,313	16,163	21,550	6,525	8,000	9,150	10,850	13,525	13,725
	Block RAM/FIFO w/ ECC (36kbits each)	410	615	795	1,155	1,155	1,540	880	1,030	1,200	1,460	1,740	1,800
	Total Block RAM (Kbits)	14,760	22,140	28,620	41,580	41,580	55,440	31,680	37,080	43,200	52,560	62,640	64,800
Clock Resources	Mixed Mode Clock Managers (MMCM)	14	14	18	18	18	24	12	14	12	20	18	18
I/O Resources [4, 5]	Maximum Single-Ended I/O	700	700	850	850	850	1200	600	700	600	1,000	880	640
	Maximum Differential I/O Pairs	336	336	408	408	408	576	288	336	288	480	422	307
Embedded Hard IP Resources	DSP48E1 Slices	700	980	1,260	1,800	1,620	2,160	2,160	2,800	2,640	3,600	3,960	3,960
	Gen2 PCI Express Interface Blocks	2	3	3	3	3	4	—	4	—	—	—	—
	Gen3 PCI Express Interface Blocks	—	—	—	—	—	—	2	—	—	4	4	—
	Analog Front End (XADC) / SysMon Blocks	1	1	1	1	3	4	1	1	2	1	3	3
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1	1	1	1	1	1
	GTX 10.3125Gbps Transceivers	28	28	36	36	36	36	24	56	—	56	48	—
	GTH 13.1Gbps Transceivers	—	—	—	—	—	—	24	—	48	24	24	72
Speed Grades	Commercial	1L, 1, 2, 3	1L, 1, 2, 3	1L, 1, 2, 3	1L, 1, 2, 3	1L, 1, 2	1L, 1, 2	1, 2, 3	1, 2, 3	1, 2	1, 2, 3	1, 2	1, 2
	Industrial	-1L, -1, -2, -3	-1L, -1, -2, -3	-1L, -1, -2	-1L, -1, -2	-1L, -1	-1L, -1	-1, -2	-1, -2	-1	-1, -2	-1	-1
Configuration	Configuration Memory (Mbits)	75.3	115.4	148.3	214.9	323.0	430.6	127.0	150.0	177.0	212.0	267.0	266.0
Package [6]	**Area**	**Available User I/O: 3.3V capable SelectIO™ Pins[4], 1.8V SelectIO Pins[5] (GTX Transceivers)**						**Available User I/O: 1.8V SelectIO™ Pins[5] (GTX, GTH Transceivers)**					
Flip chip, fine pitch BGA (1.0 mm ball spacing)													
FFG484	23 x 23 mm	0, 250 (8)											
FFG784	29 x 29 mm	50, 350 (12)	50, 350 (12)						400 (12, 0)				
FFG1157	35 x 35 mm	0, 600 (20)	0, 600 (20)	0, 600 (20)	0, 600 (20)	0, 600 (20)			600 (20, 0)				
FFG1761	42.5 x 42.5 mm	50, 650 (28)	50, 650 (28)	100, 750 (36)	100, 750 (36)	0, 850 (36)	0, 850 (36)		700 (28, 0)				
FFG1925	45 x 45 mm						1200 (16)						
FFG1158	35 x 35 mm								320 (48, 0)		320 (48, 0)		
FFG1159	35 x 35 mm							320 (24, 24)			320 (24, 24)		
FFG1926	45 x 45 mm							600 (24, 24)			640 (48, 24)	640 (48, 24)	
FFG1927	45 x 45 mm										880 (24, 24)	880 (24, 24)	
FFG1928	45 x 45 mm									600 (0, 48)			640 (0, 72)
FFG1929	45 x 45 mm								560 (56, 0)		560 (56, 24)		
FFG1930	45 x 45 mm										1000 (28, 0)		

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