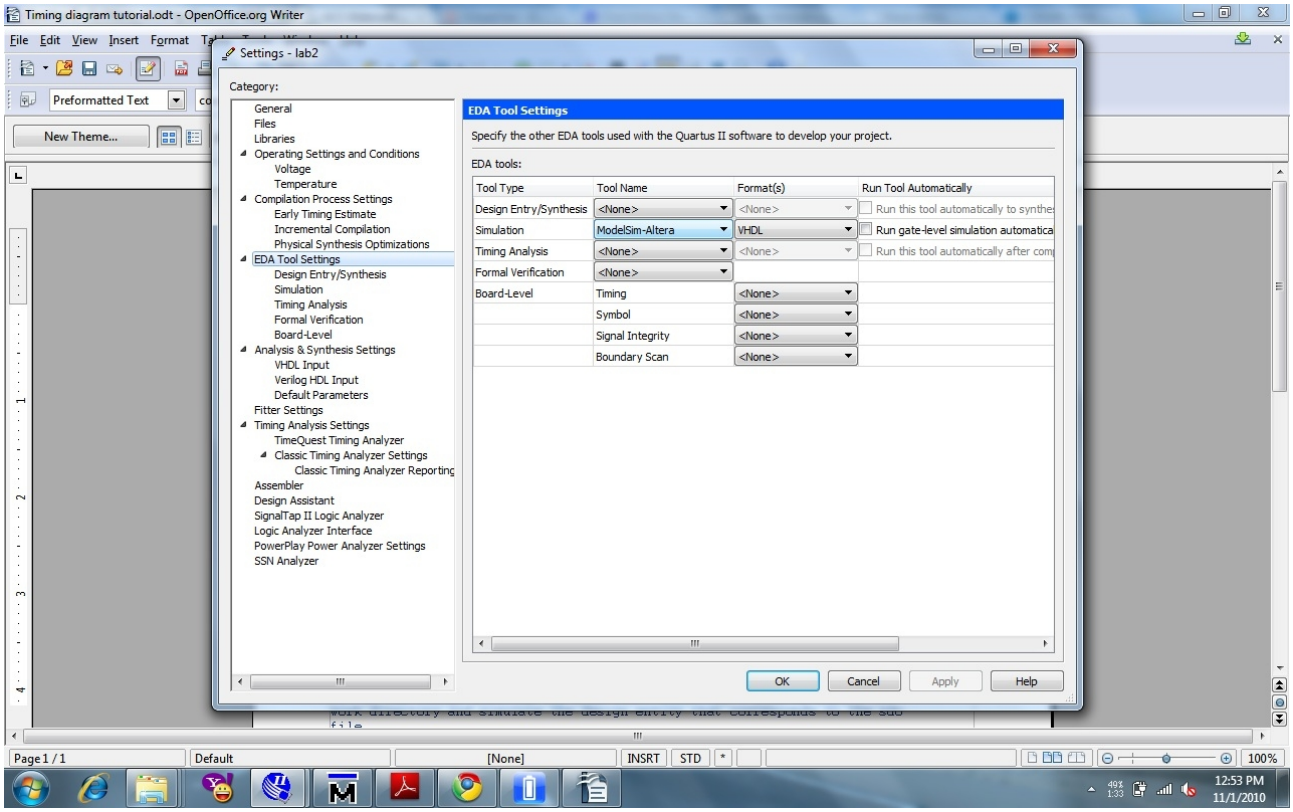
Timing Simulations:

ModelSim post synthesis simulation guide:

1. In the Quartus software, in the processing menu, point to Start and click start analysis and synthesis.

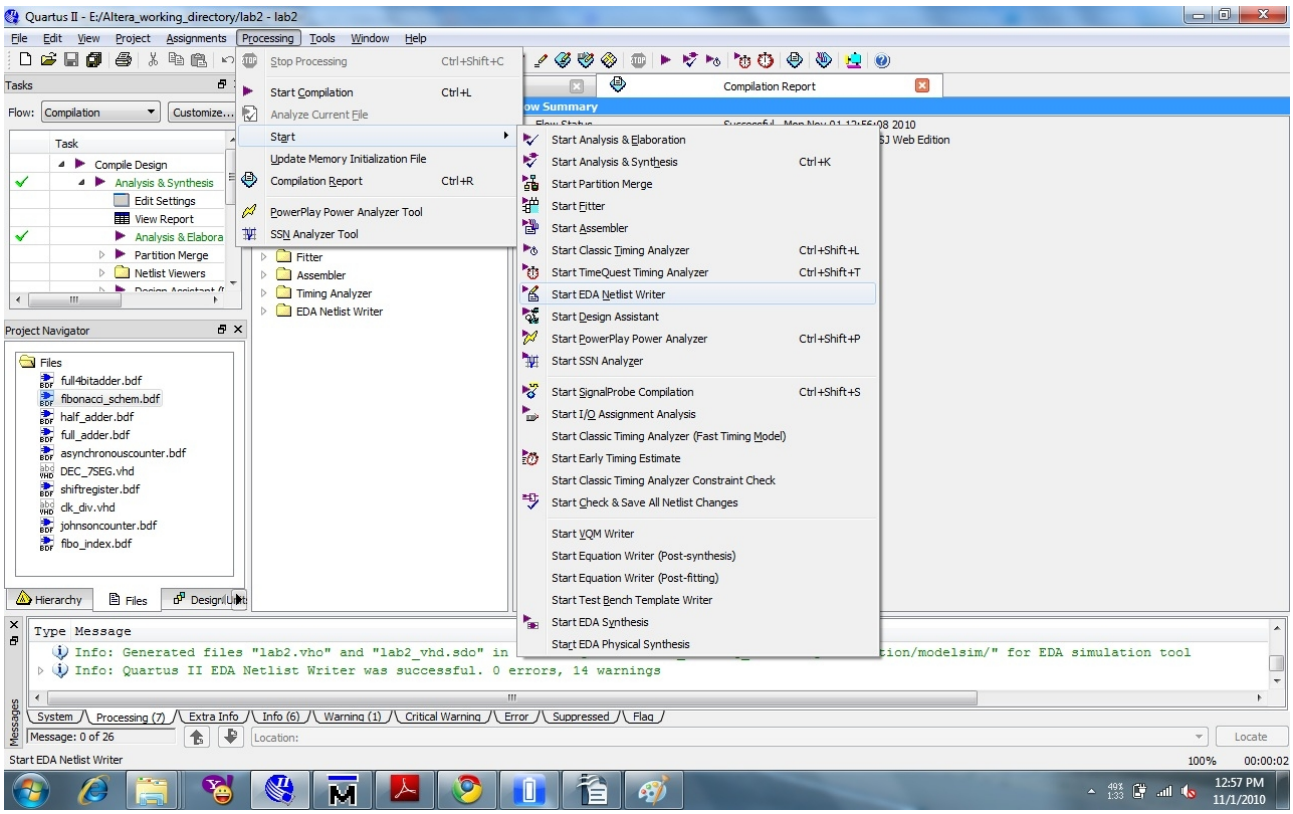
2. On the Assignments menu, click Settings.

3. In the Category list, select Simulation under EDA Tool Settings.



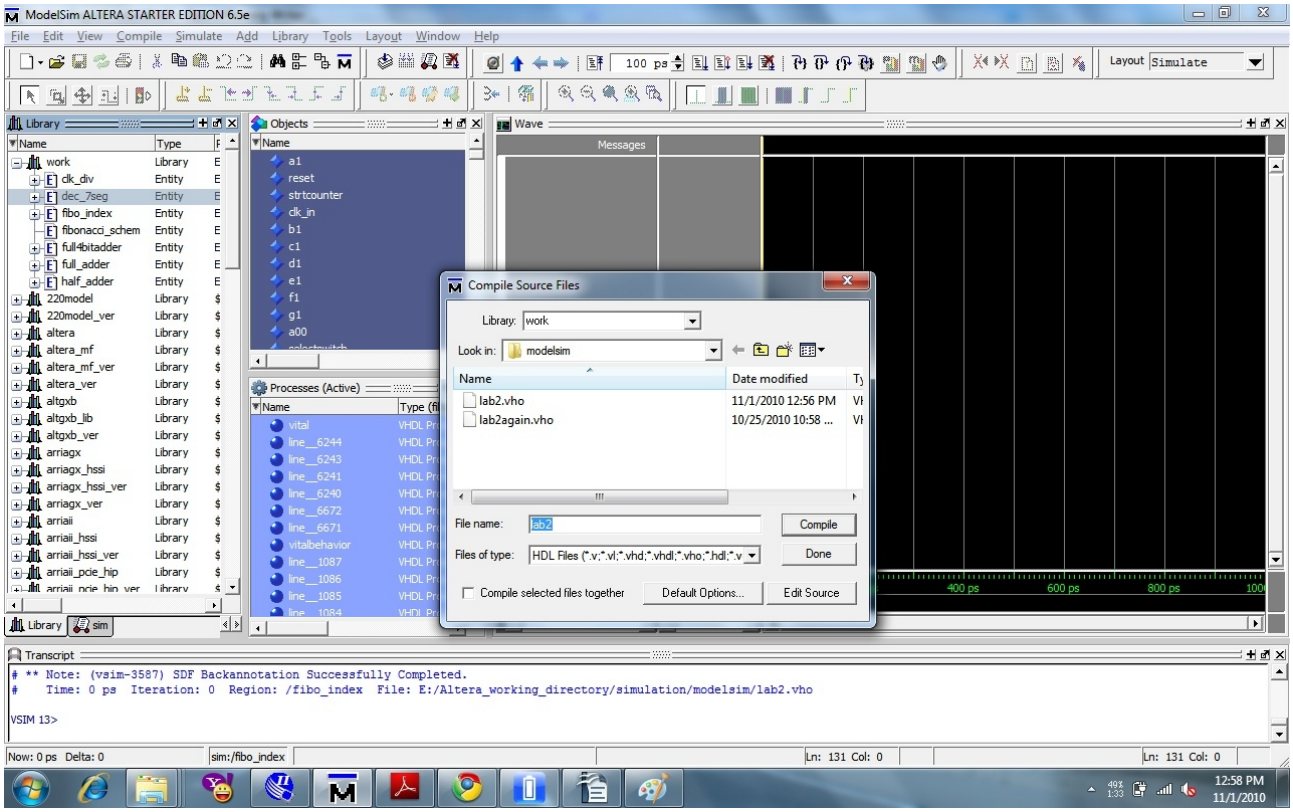
4. In the Tool name list, specify simulation tool as ModelSim-Altera. (DO NOT turn on Run gate level simulation automatically. Click OK.

5. Compile the design again. In the processing menu, point to Start and click on
Start EDA netlist writer.



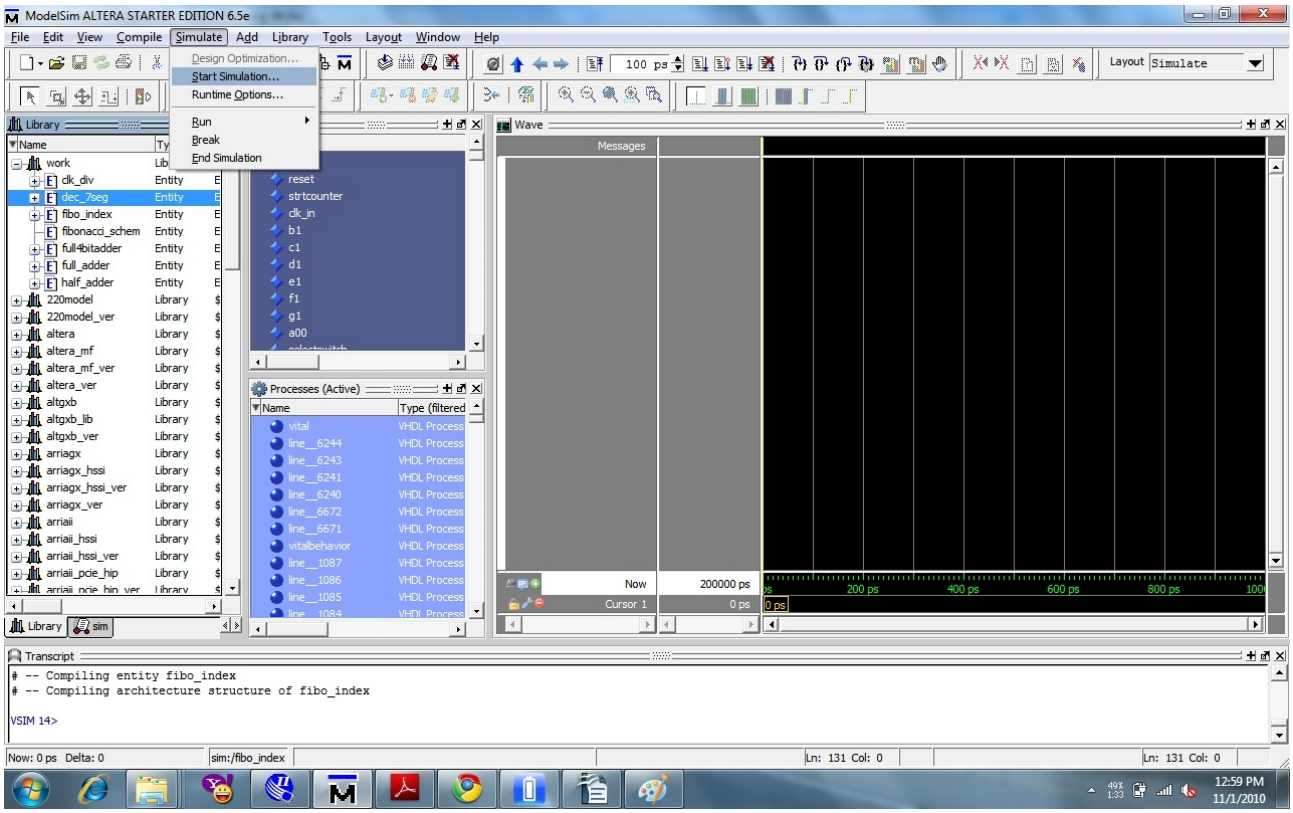
Now you have two files in the folder: simulation/modelsim/ in your altera working directory – (1) .vho (VHDL Output) file and (2) .sdo (Standard Delay Format Output) file.

6. To compile the VHDL Output File (.vho), open modelsim and on compile menu, click compile.

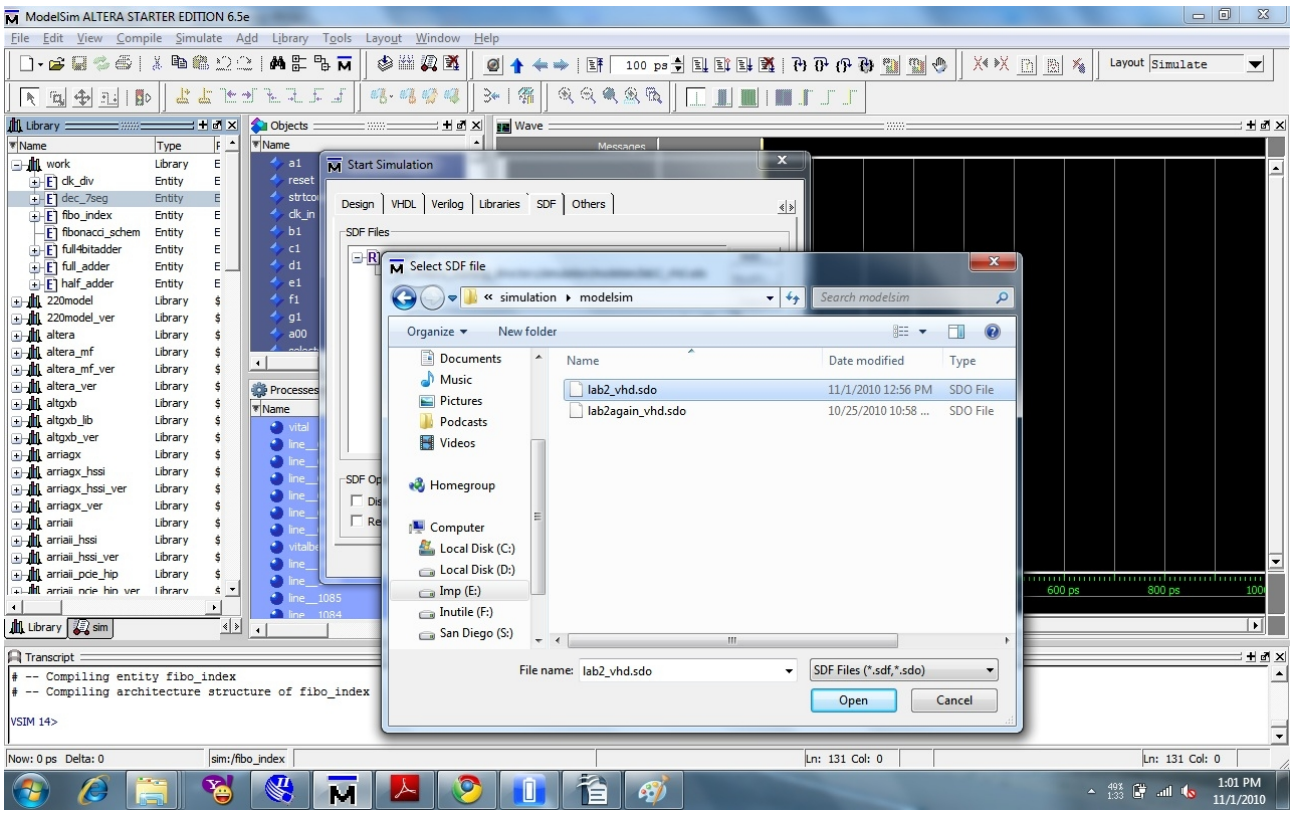


7. Search up for the .vho file you generate with Altera Quartus and compile it and click done.

8. In the Simulate menu click start simulation.

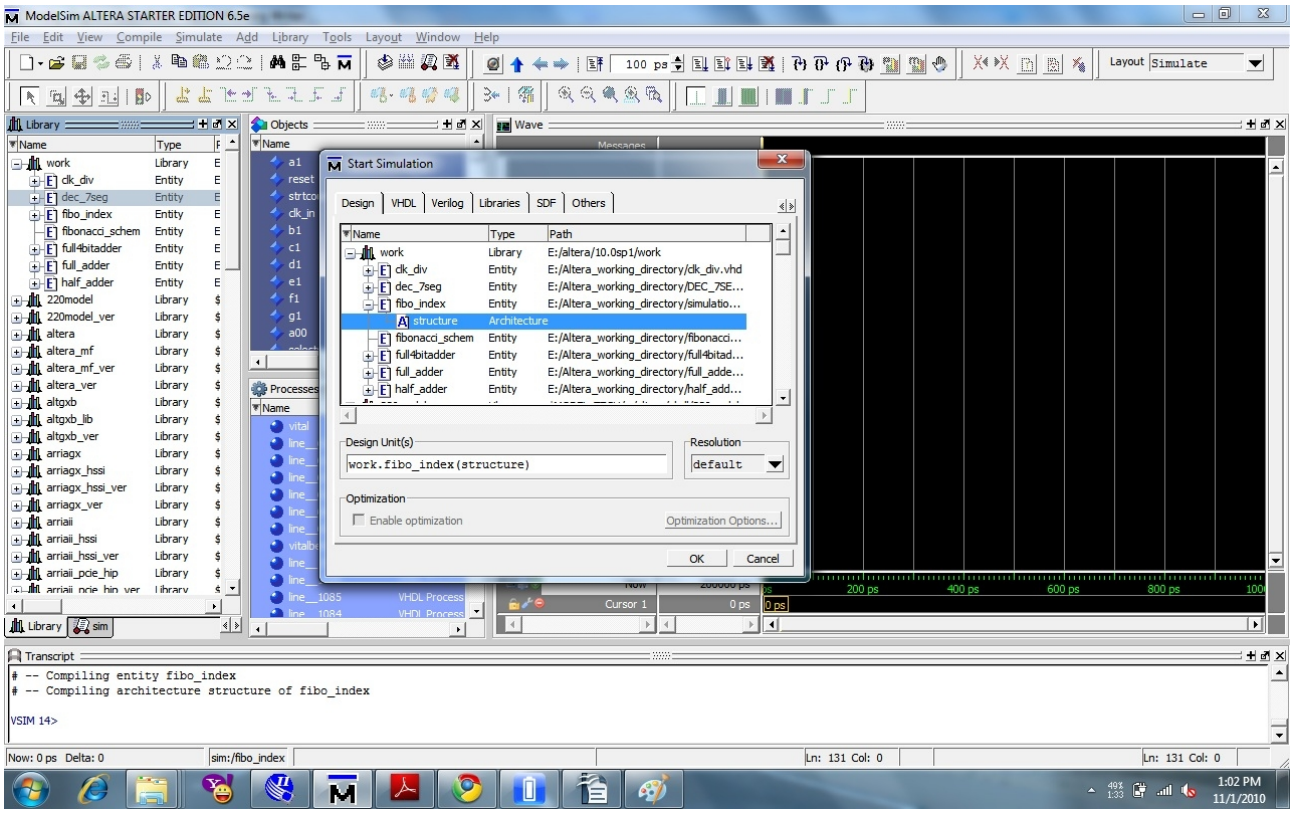


9. Click sdf tab and click add.



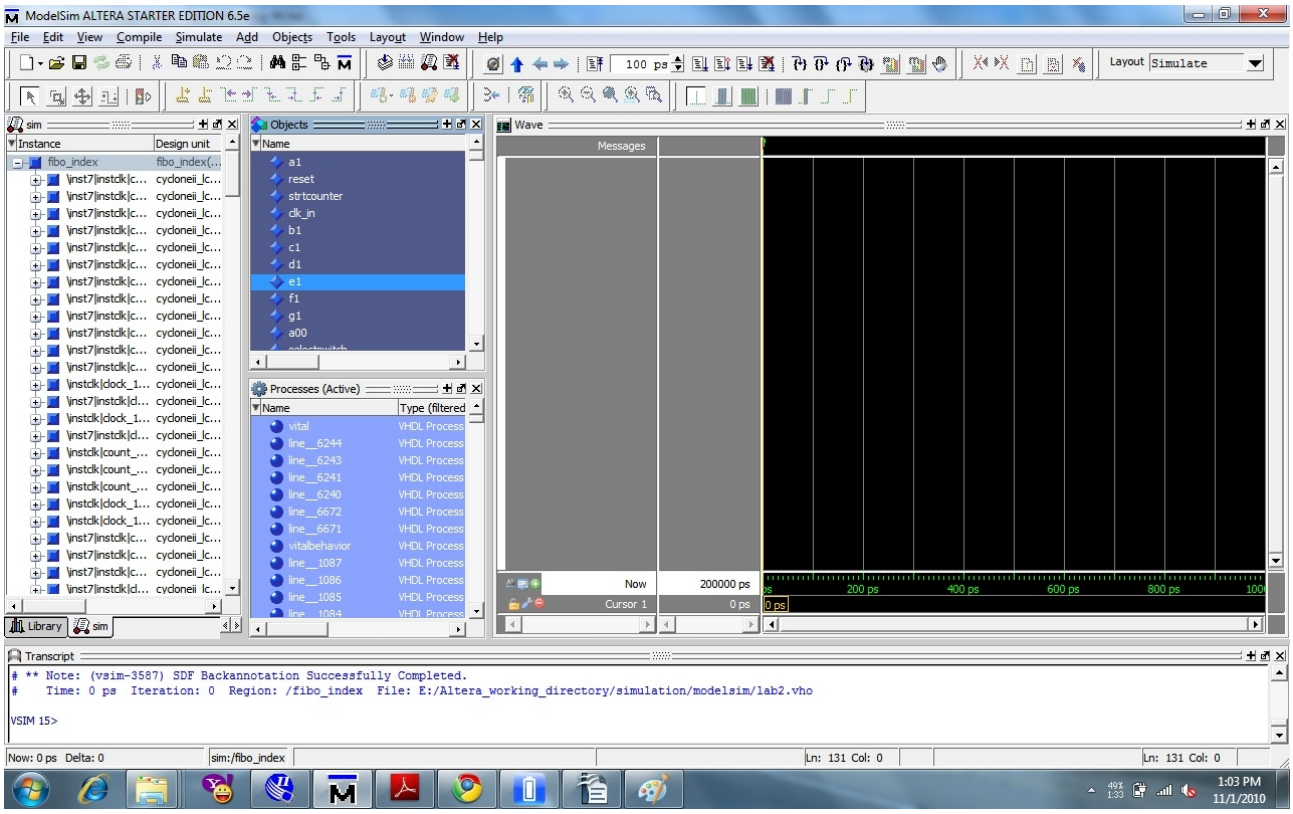
10. Browse for the .sdo file you created along with .vho using Altera Quartus. Click ok.

11. In the Design menu, In the Name list, click the + icon to expand the work directory and simulate the design entity that corresponds to the sdo file.



12. Click OK. This will simulate your design and you will be able to see your input output ports in the object window.

13. You can now add the signals to the wave and type "run XYZns".



This will generate waveforms with timing information. You can force particular inputs to 0 or 1 values and type "run ABCns" again to see the difference.