Introduction to Simulation with ModelSim-Altera and Altera Quartus II Setup

by

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Introduction:

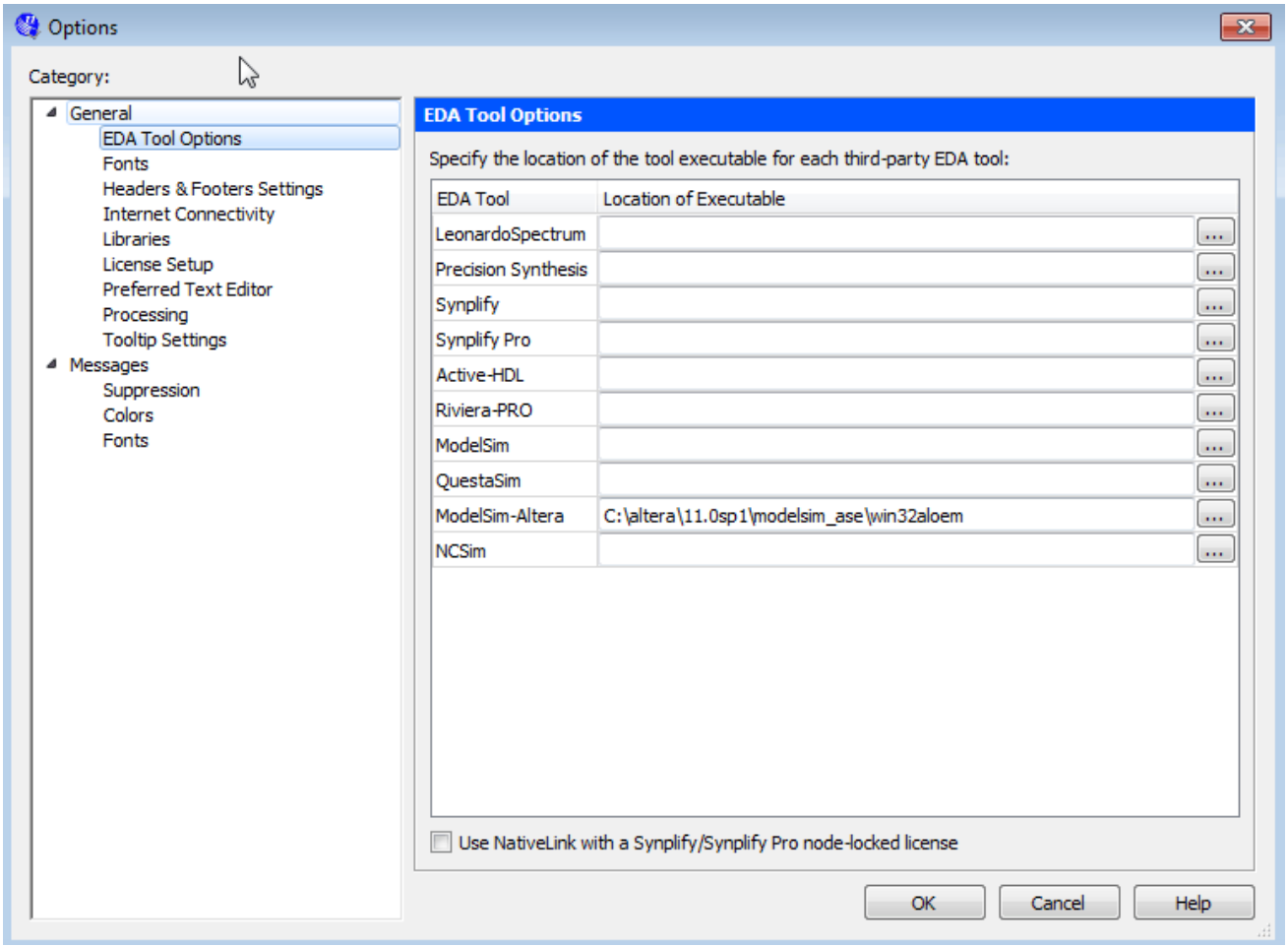
Altera Quartus II software allows the user to launch Modelsim-Altera simulator from within the software using the Quartus II feature called NativeLink. It facilitates the process of simulation by providing an easy to use mechanism and precompiled libraries for simulation..

Objective:

- Configure Modelsim-Altera with NativeLink Settings
- Running EDA RTL simulation
- Running Gate-level Timing Simulation

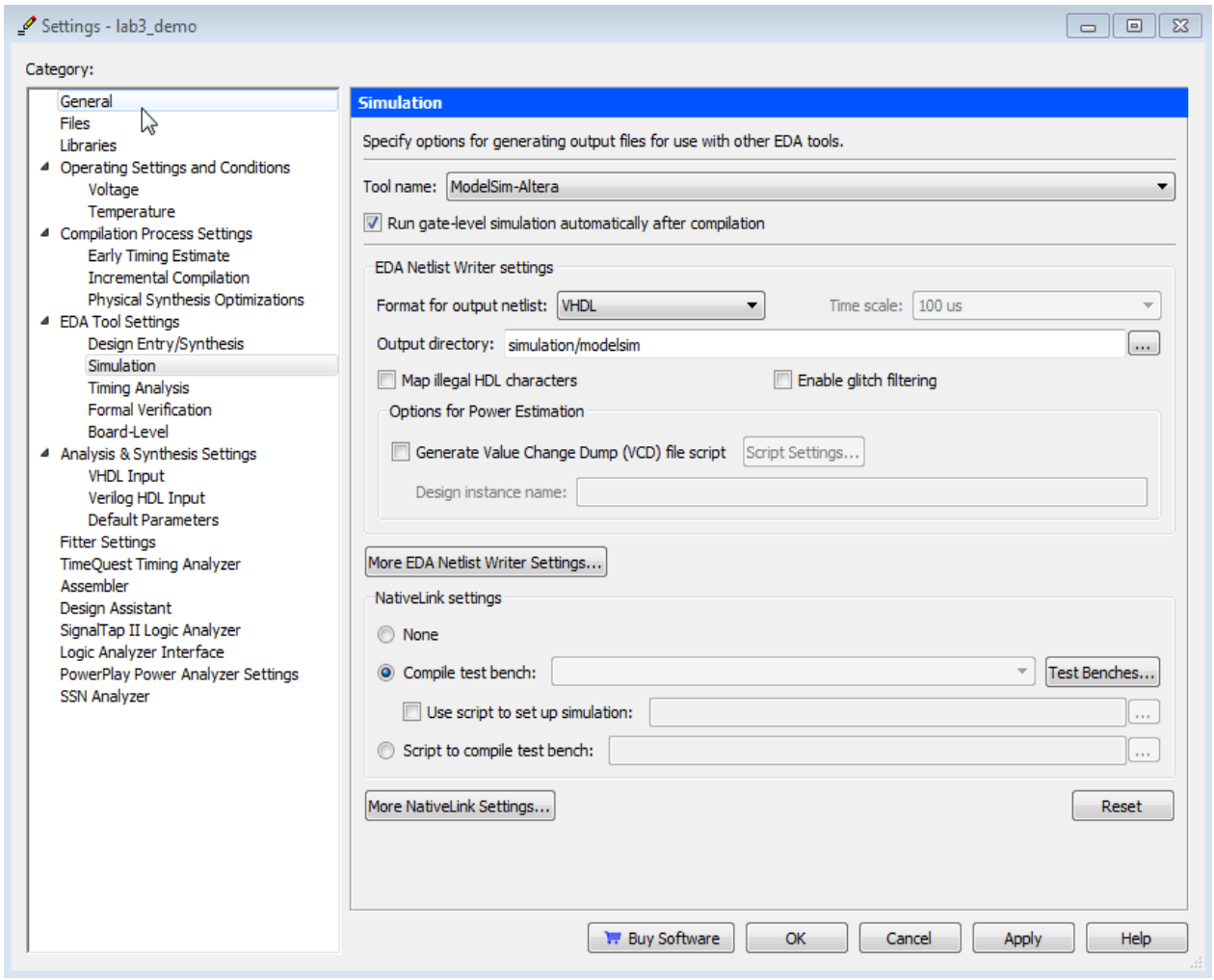
Step1: Specify the path to Modelsim-Altera

1. Go to the menu Tools > Options.
2. In the “General” category, select “EDA Tool Options”.
3. A dialogue box appears, where you can specify the location of the Modelsim-Altera executable.
4. Specify the path to the directory with the executable of Modelsim-Altera.
5. Click “OK”.

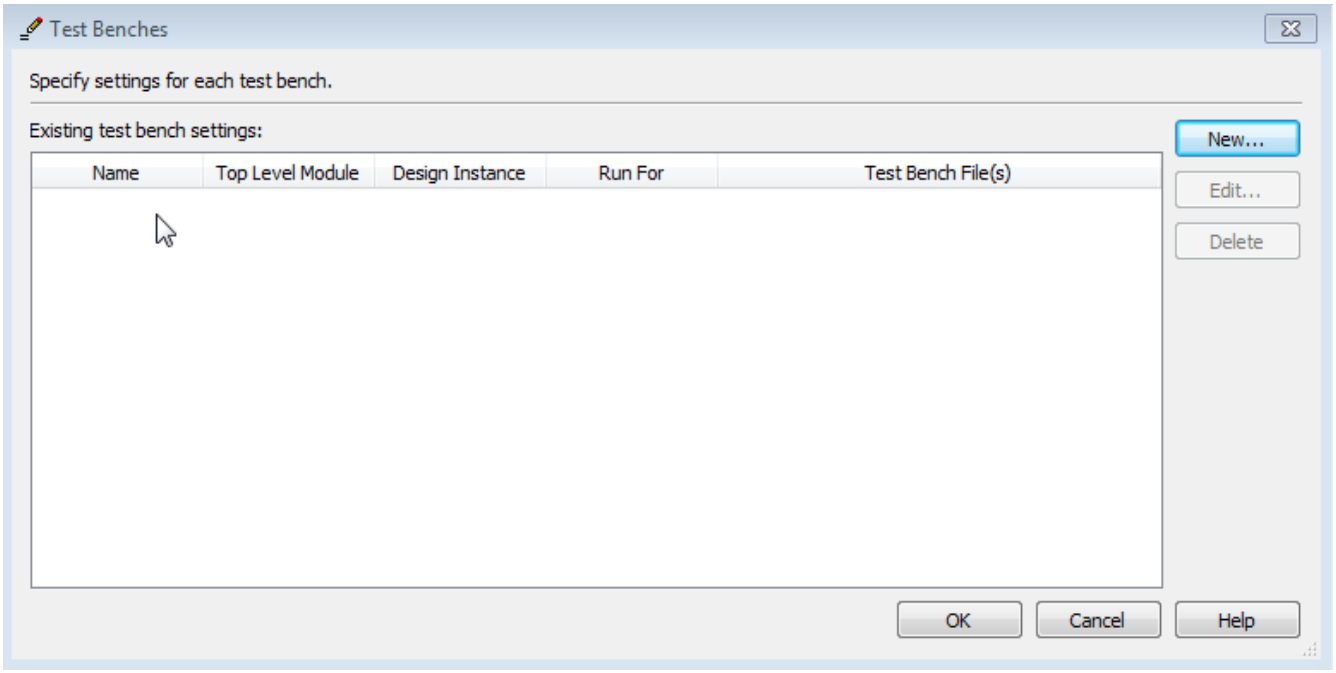


Step 2: NativeLink Settings to configure Modelsim-Altera:

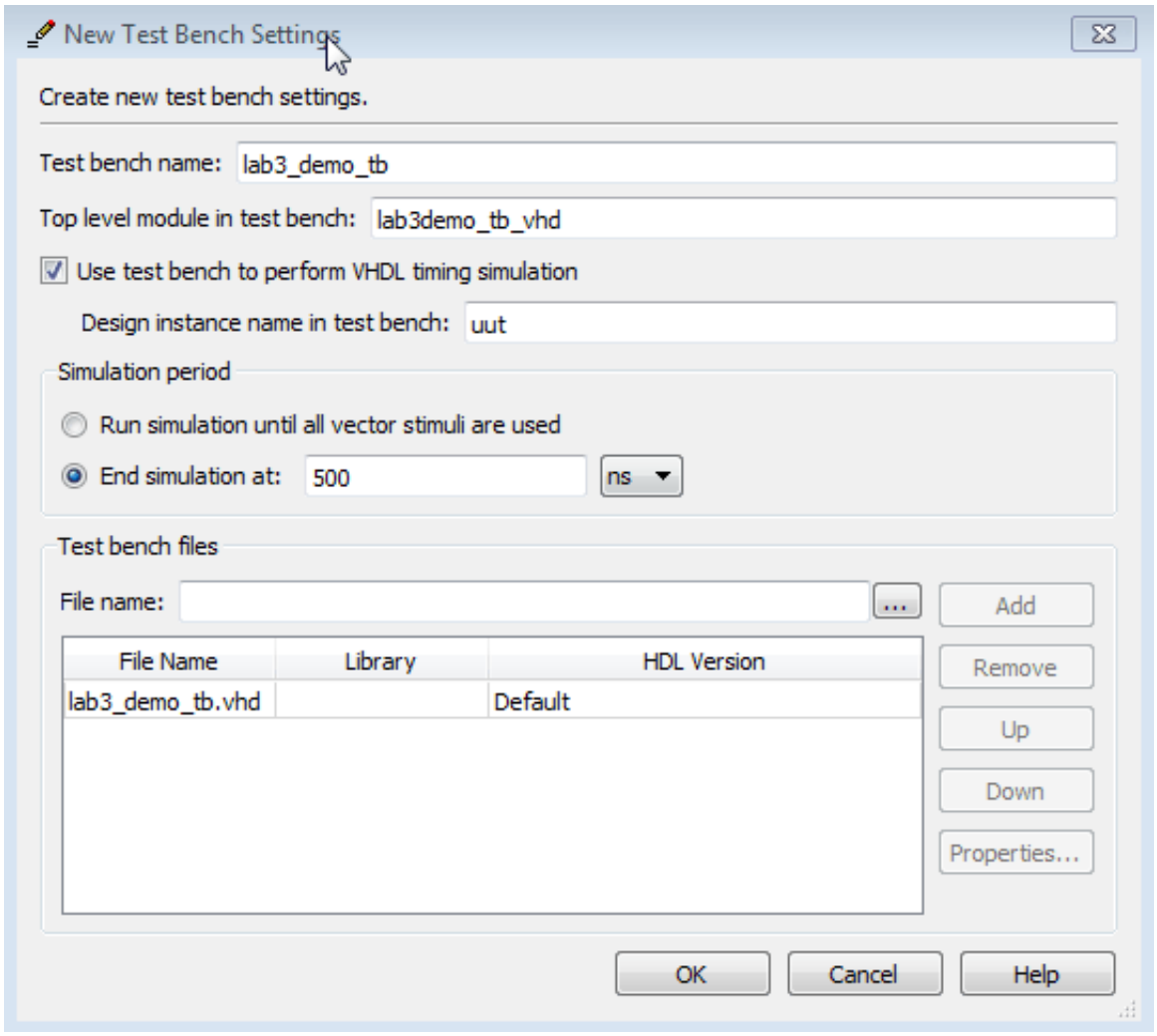
1. Go to the menu Assignments > Settings.
2. Under “EDA Tool Settings” choose “Simulation”. The dialogue box for simulation appears.
3. For Tool Name, choose “Modelsim-Altera”.
4. Select "VHDL" as the "Format for Output Netlist"
5. Select "simulation/modelsim" as the "Output Directory".

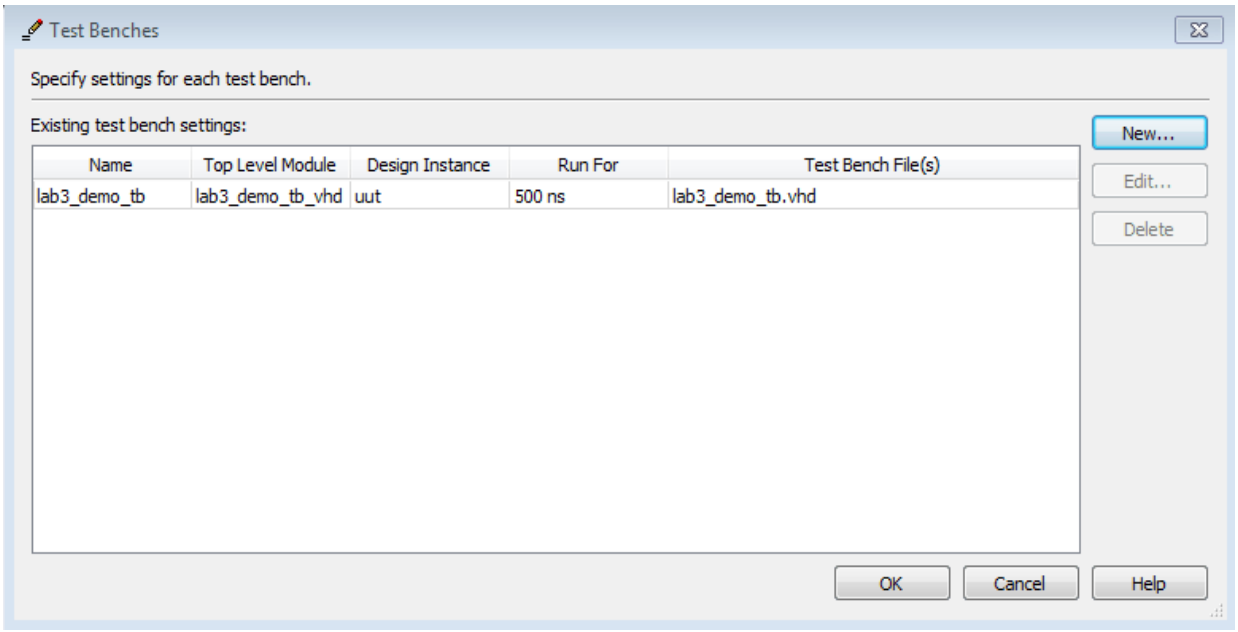


6. Under NativeLink Settings, Choose "Compile test bench". Then click on "Test Benches".
7. A new window appears, select "New".



8. Another window appears. Enter the "Test bench Name".
9. Enter the "Top-Level Module in Test Bench". Check the box "Use test bench to perform VHDL timing simulation".
10. Enter the "Design instance name in test bench". It is the "Name of the Instance" for Top-Level design under test.
11. Enter the simulation period. Add the test bench file and push "OK".


New Test Bench Settings
Create new test bench settings.
Test bench name: lab3_demo_tb
Top level module in test bench: lab3demo_tb_vhd
Use test bench to perform VHDL timing simulation
Design instance name in test bench: uut
Simulation period
Run simulation until all vector stimuli are used
End simulation at: 500 ns
Test bench files
File name:
...
Add
File Name
Library
HDL Version
lab3_demo_tb.vhd
Default
Remove
Up
Down
Properties...
OK
Cancel
Help



Functional Simulation using NativeLink Feature:

To run functional simulation using the NativeLink feature,

- Perform Step 1 and Step 2 from above.
- Using the menu "Processing", select "Start", and then click "Start Analysis & Elaboration". This step collects all file name information and builds the design hierarchy for simulation.
- Using the menu "Tools", click on "Run EDA Simulation Tool", and then click "EDA RTL Simulation" to automatically run the EDA simulator, compile all necessary design files, and complete a simulation.

Gate-level Timing Simulation using NativeLink Feature:

To run a gate-level timing simulation using the NativeLink feature,

- Perform Step 1 and Step 2 from above.
- Using the menu "Processing", click "Start Compilation" to perform full compilation, including analysis & synthesis, place & route and generation of an EDA netlist file.
- Using the menu "Tools", click "Run EDA Simulation Tool", and then click EDA Gate-level Simulation to automatically run the EDA simulator, compile all necessary design files, and complete a simulation.