

Design Rules Verification Report

Filename : C:\#PCB#\#DONGLE02\DONGLE02.PcbDoc

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max =1.27mm) (Preferred=0.305mm) (All)	0
Routing Topology Rule(Topology=Shortest) (All)	0
Routing Layers(All)	0
Routing Via (Templates Used To Check Via: v70h40) (All)	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.254mm) (Max=0.254mm) (Preferred=0.254mm)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	0
Pads and Vias to follow the Drill pairs settings	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	0
Silk To Solder Mask (Clearance=0.09mm) (IsPad),(All)	0
Silk to Silk (Clearance=0.127mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	0
Total	0