Design Rules Verification Report

Filename : D:\Users\BENADUCE\Documents\GitHub\Dongle01\DONGLE01.PcbDoc

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=5mil) (not InNetClass('USBI') and not InNetClass('USBE')),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=3.937mil) (Max=50mil) (Preferred=10mil) (All)	0
Routing Topology Rule(Topology=Shortest) (All)	0
Routing Layers(All)	0
Routing Via (MinHoleWidth=7.874mil) (MaxHoleWidth=39.37mil) (PreferredHoleWidth=15.748mil) (MinWidth=13.78mil)	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=4.506mil) (Max=4.506mil) (Prefered=4.506mil) and	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=10mil) (Max=10mil) (Prefered=10mil) and Width	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=4.506mil) (Max=4.506mil) (Prefered=4.506mil) and	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Hole Size Constraint (Min=1mil) (Max=100mil) (All)	0
Pads and Vias to follow the Drill pairs settings	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=6mil) (not InComponent('J1') and not InComponent('U2')),(All)	0
Silk To Solder Mask (Clearance=1mil) (IsPad),(All)	0
Silk to Silk (Clearance=10mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Board Clearance Constraint (Gap=0mil) (All)	0
Matched Lengths(Delay Tolerance=100ps) (InNetClass('USBI'))	0
Matched Lengths(Delay Tolerance=100ps) (InNetClass('USBE'))	0
Total	0