# Design Rules Verification Report

Filename : D:\Users\BENADUCE\Documents\GitHub\Dongle02\DONGLE02.PcbDoc

Warnings 0
Rule Violations 0

| Warnings | |
|---|---|
| Total | 0 |

| Rule Violations | |
|---|---|
| Clearance Constraint (Gap=6mil) (All),(All) | 0 |
| Short-Circuit Constraint (Allowed=No) (All),(All) | 0 |
| Un-Routed Net Constraint ( (All) ) | 0 |
| Modified Polygon (Allow modified: No), (Allow shelved: No) | 0 |
| Width Constraint (Min=10mil) (Max=50mil) (Preferred=12mil) (All) | 0 |
| Routing Topology Rule(Topology=Shortest) (All) | 0 |
| Routing Layers(All) | 0 |
| Routing Via (Templates Used To Check Via: v70h40) (All) | 0 |
| Differential Pairs Uncoupled Length using the Gap Constraints (Min=10mil) (Max=10mil) (Prefered=10mil) and Width | 0 |
| Power Plane Connect Rule(Relief Connect )(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4) | 0 |
| Hole Size Constraint (Min=1mil) (Max=100mil) (All) | 0 |
| Pads and Vias to follow the Drill pairs settings | 0 |
| Hole To Hole Clearance (Gap=10mil) (All),(All) | 0 |
| Minimum Solder Mask Sliver (Gap=10mil) (All),(All) | 0 |
| Silk To Solder Mask (Clearance=3.543mil) (IsPad),(All) | 0 |
| Silk to Silk (Clearance=5mil) (All),(All) | 0 |
| Net Antennae (Tolerance=0mil) (All) | 0 |
| Board Clearance Constraint (Gap=0mil) (All) | 0 |
| Total | 0 |