⚡ XILINX

ALL PROGRAMMABLE™

WP482 (v1.1) October 20, 2016

Managing Power and Performance with the Zynq UltraScale+ MPSoC

By: Glenn Steiner and Brian Philofsky

To meet critical system-level requirements, designers must offset power/heat against overall performance. The Zynq® UltraScale+™ MPSoC facilitates achieving this balance.

ABSTRACT

Modern embedded processing systems frequently have a diverse set of individually complex requirements, often including application processing, real-time processing, high data bandwidth processing, and requirements for peripherals to handle human-machine interfaces, data I/O, and system control. All of this must be managed within a power budget, and frequently, the power budget varies with the required functions to be performed. Such requirements typically cannot be met by a single type of processor.

With the introduction of the Zynq UltraScale+ MPSoC, Xilinx brings to market a new all-programmable device where multiple processing elements can be designed to focus independently on a subset of the required functions.

When these independently operable elements are assembled together in a heterogeneous system, a highly diverse set of processing requirements can be met with a very high level of operational efficiency. In addition, power and performance can be ideally balanced against each other, thanks to the many power management features implemented in the Zynq UltraScale+ MPSoC.

Introduction

As the complexity of a product solution increases, there is increased demand for computing functions. Generally, increased performance goes hand-in-hand with increased power. With each generation of higher-performance computing platforms, there are associated mechanisms to enable power reduction.

Approaches for addressing power management of ASSPs have been implemented and continue to evolve for high-volume computing platforms such as PCs, mobile phones, and tablets. However, power management techniques for many embedded applications are less well defined, as each application has its own unique power management needs.

Common techniques for power management in embedded systems include, but are not limited to:

- Managing processor utilization for power
- Active/inactive core management
- Frequency scaling
- Clock gating

With the Zynq UltraScale+ MPSoC, not only can the designer use the above techniques, but software tasks can be moved, via C to HDL tools, to programmable logic (PL). This offloading of software tasks to coprocessors has demonstrated not only higher performance processing, but also higher performance per watt.

Zynq UltraScale+ MPSoC Design Advantage

Building on the industry's first All Programmable SoC, Xilinx is enabling a generation ahead of integration and intelligence with unprecedented levels of heterogeneous multi-processing system on chip with the Zynq UltraScale+ MPSoC. By using the right engines for the right tasks, these devices provide a flexible, scalable processing platform with the highest levels of security and safety.

Based on the Xilinx UltraScale™ architecture, the Zynq UltraScale+ MPSoC enables extensive system-level differentiation, integration, and flexibility through hardware, software, and I/O programmability. It also delivers a heterogeneous multi-processing system with integrated programmable logic and is designed to meet embedded system power management requirements.

Flexible Architecture for Power Management

The processing system provides power/performance scaling via three distinct levels of processing systems: the high-performance application processors, the real-time processors, and the energy-efficient platform management unit, each with its own power management capabilities.

The latest generation programmable logic provides its own power reduction and management capabilities via next-generation lower power hard IP and enhanced performance soft IP.

Unlike ASSPs, the Zynq UltraScale+ MPSoC has the unique ability to move software tasks to the programmable logic, enabling dramatic software acceleration and higher performance per watt.

To enable user-level power management, Xilinx has architected an extensible software power management framework to support power reduction modes. Power management control is done through the platform management unit (PMU), a triple-redundant microcontroller enabling reliable power management control. This power management framework enables bare metal and Linux power management as well as customization for proprietary software implementations.

Power Domains for Power Isolation

The Zynq UltraScale+ MPSoC is composed of multiple power domains for efficient power management (Figure 1). Each power domain is provided power via external power regulators. If individual power domain control is not required, power rails can be shared between domains. The processing system has three power domains: the battery-power domain, the low-power domain, and the full-power domain. Within the low-power domain and the full-power domain, there are additional IP power-gating options. The fourth power domain is the programmable logic (PL).
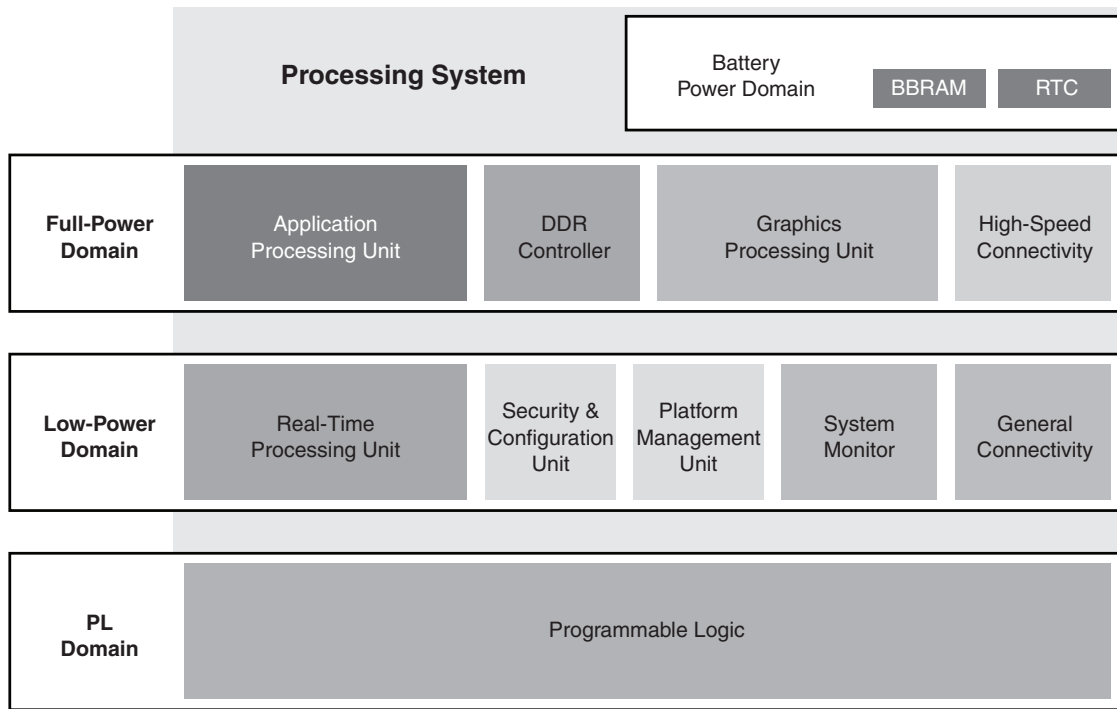
WP482_01_081016

Figure 1: **Zynq UltraScale+ MPSoC Power Domains**

Battery Power Domain

The battery power domain, which can be powered by an external battery, contains battery-backed RAM (BBRAM) for an encryption key, and a real-time clock with external crystal oscillator to maintain time even when the device is off.

Full-Power Domain

The full-power domain consists of the application processor unit (APU), with the ARM® Cortex™-A53 processors, the GPU, the DDR memory controller, and the high-performance peripherals including PCI Express®, USB 3.0, DisplayPort, and SATA.

Low-Power Domain

The low-power domain consists of a real-time processor unit (RPU) with the ARM Cortex-R5 processors, static on-chip memory (OCM), the platform management unit (PMU), the configuration and security unit (CSU), and the low-speed peripherals.

Programmable Logic

The programmable logic (PL) power domain consists of logic cells, block RAMs, DSP blocks, XADC, I/Os, and high-speed serial interfaces. Some devices include the video codec, PCIe Gen-4, UltraRAM, CMAC, and Interlaken.

Power Islands for Fine-Grain Power Management

Within the full- and low-power domains, there are multiple power islands. Each island is capable of being power-gated locally within the device. The following islands can be power-gated:

- Full-Power Domain
  - o 4 ARM Cortex-A53 applications processors; each can be individually power-gated
  - o L2 cache servicing the Cortex-A53 processors
  - o 2 pixel processors in GPU: Each can be individually power-gated
- Low-Power Domain
  - o 2 ARM Cortex-R5 processors: Power-gated as a pair
  - o 2 tightly coupled memories (TCM): Connected to the Cortex-R5s, each with 4 individually power-gated banks
  - o On-Chip Memory (OCM): 4 individually power-gated banks
  - o 2 USBs: Each individually power-gated

Additional Power Management Mechanisms

Additional mechanisms are available for power management in both the processing system (PS) and in the programmable logic (PL). Where reduced performance is acceptable, IP can be frequency-scaled. For example, the processor cores can be operated at lower clock rates to reduce power (with a commensurate reduction in performance). In cases where use of a peripheral or subsystem is no longer required, the device can be clock gated, thereby eliminating all dynamic power—with only static power being consumed. Such devices include processor cores, processor peripherals, and PL soft and hard cores.

Achieving Greater Performance per Watt

By managing power domains and islands via software control, the designer can achieve maximum performance per watt based on real-time application needs.

Zynq UltraScale+ MPSoC Power Modes Enable Performance/Power Optimization

The battery power mode is the lowest power mode, with power consumption ranging from 180 nanowatts when just powering the battery-backed RAM to 3 microwatts when the real-time clock is enabled.

The low-power mode, associated with the low-power domain, has power consumption based on processor activity ranging from about 30 milliwatts up to about 400 milliwatts.

The full-power mode enables the full-power domain. Depending on processor activity and how many cores are enabled, power consumption can range up to a couple of watts.

The PL, as a separate power domain, incorporates many features and capabilities to reduce power while still maintaining exceptional performance levels. One of the more prominent is the dual voltage offering of the -1LI and -2LE devices, where a lower voltage can be used to significantly reduce both dynamic and static power while still maintaining good performance. Conversely, for situations where very high-speed operation is required, the device can be operated at a higher voltage, thus achieving more than a 30% performance boost. This behavior allows the designer to choose the right performance characteristics for the task while maintaining the lowest power operation. This is just one of several features and options available in the silicon, IP, and software.

Software Power Management Framework Enables Effective Power Management

Xilinx provides a software power management framework enabling power management of both domains and islands. The framework is built on top of industry standards. Power is controlled through the PMU. Inter-processor interrupts are used to enable power-control messaging between the application processor unit (APU) in the full-power domain as well as the real-time processing unit (RPU) in the low-power domain and the PMU. Power management APIs via Linux and bare metal are provided, and source files are available for implementation customization.

Power management is a distributed function and occurs across multiple components. As the power management server, the PMU receives power management requests and initiates power management actions. It offers these services to system masters and controls external power management ICs, as well as all of the power island switches.

The PMU power management firmware and associated software framework running on the system masters (such as the Cortex-A53s and Cortex-R5s) assure that any power command sequence has been executed and completed. The framework also supports responding to wake-up interrupts, and will wake up the suspended system as needed.

The power management framework APIs available to the power management masters (Cortex-A53s and Cortex-R5s), enable these masters to request suspend operations and set conditions for resumption thereby enabling power savings.

Figure 2 shows power mode examples that can be selected via user applications and the Power Management Framework. These examples demonstrate the ability to trade performance and power savings.
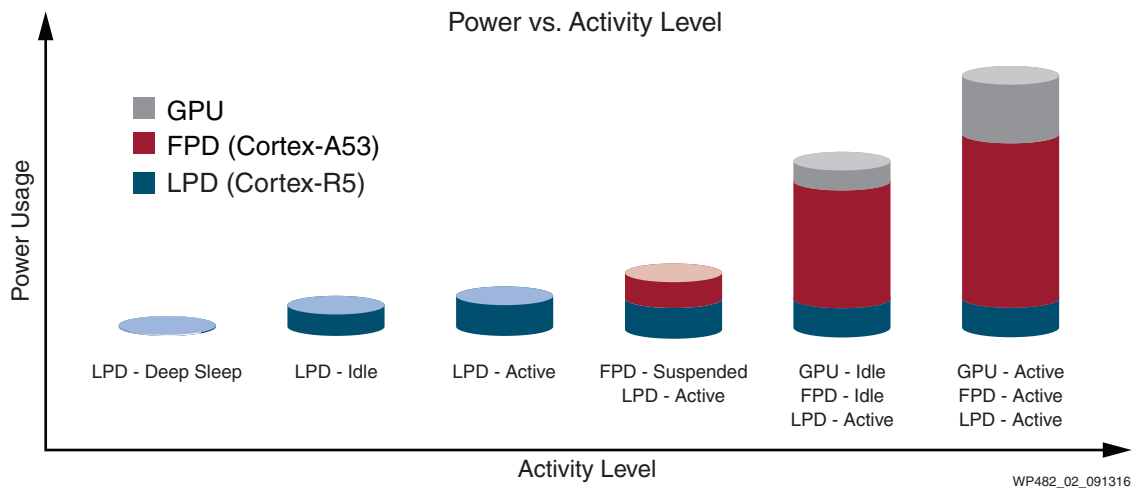

Figure 2: **Power Mode Examples**

Power Optimization via the Right Task on the Right Processing Element

Typically, data processing is done with the Cortex-A53 application processors. However, the dual-core Cortex-R5 processors, in the low-power domain, can also be used for data processing. The Cortex-R5 processors typically run either bare metal or a real-time operating system. Offloading select applications to the Cortex-R5 processors not only reduces APU workload, it also provides the opportunity for these applications to be run with determinism, and potentially lower latency in response to real-time events, while consuming lower static power. As a relative power comparison at 100% utilization, the two Cortex-R5 processors consume about one quarter the power of the four Cortex-A53 processors.

The PL in the Zynq device also enables processor offloading to hardware. Designers can either craft coprocessors by hand in HDL, or they can use the Xilinx SDSoC™ Development Environment to identify and partition compute-intensive applications, and then automatically create coprocessors in the programmable logic.

Demonstrating the Power Advantage

## Xilinx Power Estimator for Estimating Power Prior to Design Implementation

The Xilinx Power Estimator (XPE) is found on the Power Efficiency and Management page on Xilinx.com. With it, the designer can rapidly estimate power consumption for the target device. The tool includes the ability to select the device type, packaging, silicon speed grade, temperature grade, and if desired an estimate for typical or "maximum" silicon. The designer can select either a target junction temperature or ambient temperature. If ambient temperature is selected, the designer has further environmental selections to specify the thermal management characteristics of the system.

For the processing system, the designer selects the active processor cores, their utilization level, the planned memory type and its utilization, and the peripherals in use. There are additional options for fine-tuning the estimate. Similarly, for the PL, the designer selects what resources are used, their clock frequencies, and utilization.

The tool provides power estimates by domain, total power, and a computed junction temperature. It provides quick estimations of power enabling a user to optimize a system to meet power targets.

Increased Performance per Watt from One Generation to the Next

The Zynq-7000 All Programmable SoC is the first generation of the Zynq portfolio and integrates the software programmability of up to two ARM Cortex-A9 processors with the hardware programmability of an FPGA. Demonstrating the increased performance per watt of the Zynq UltraScale+ MPSoC processing system, the following information is computed using XPE and has been shown in design implementation (Figure 3).
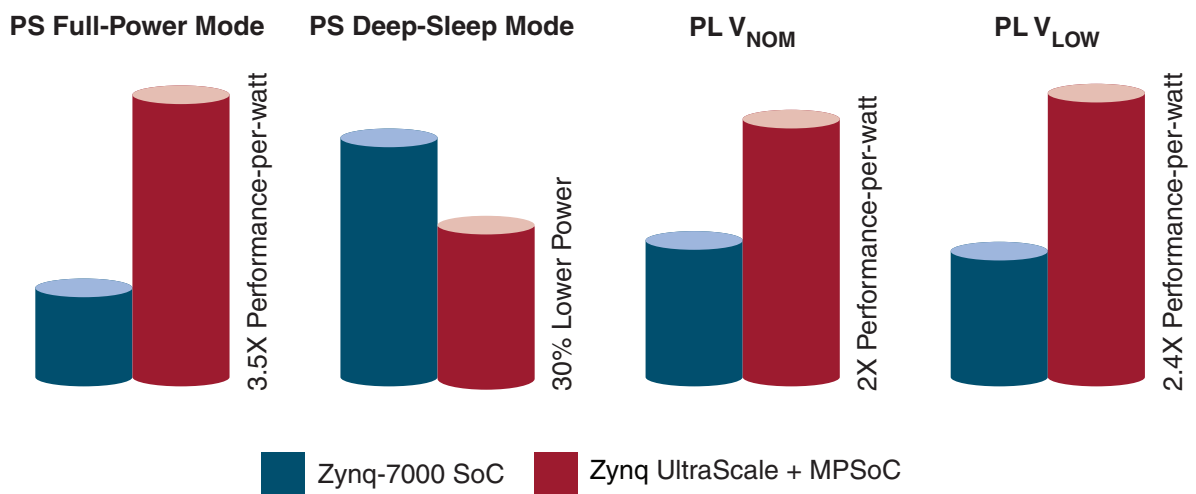
Figure 3: **Performance per Watt Comparison**

- 30% less static power for deep sleep mode
  - With domains and islands off and PMU in sleep
- Six Zynq UltraScale+ MPSoC active processor cores for the same power as two Cortex-A9 cores
  - Four Cortex-A53 cores at 1GHz and two Cortex-R5 cores at 600MHz consume the same power as two Cortex-A9 cores at 1GHz
- 3.5X SPEC2000 Integer performance for the same power
  - Four Cortex-A53 cores at 1.5GHz deliver 3.5X greater performance than two Cortex-A9s operating at 1.0GHz, while consuming the same power

Similar performance and power improvements are seen in the PL as well.

- At maximum performance a 2X performance per watt improvement
  - Operating at a nominal 0.85V core voltage, a performance increase of 60% can be seen over the Zynq-7000 AP SoC while still shaving off 20% power
- A 2.4X performance per watt improvement at low voltage operation
  - When operated at the lower voltage of 0.72V, performance improves by 20% while cutting power in half

Finally, by offloading software tasks to the PL, the designer will see dramatic performance and power improvement. The Software Acceleration Targeted Reference design available for the Zynq UltraScale+ MPSoC demonstrates:

- Up to 10X system-level acceleration of Fast Fourier Transforms and up to 6 times increase in performance per watt.

Conclusion

The Zynq UltraScale+ MPSoC has four major power domains for efficient power management. Within the PS, there are three domains: The battery-power domain, the low-power domain, and the full-power domain. The fourth power domain is the PL logic.

The system is architected for flexible power needs. The device domains can be individually powered on or off, while there are also power islands for finer-grain power management.

The Power Management Framework provides APIs for the applications processor unit and the real-time processing unit. This framework is built on industry standards, and designers can select which power modes are best suited for their application. This enables the designers to create a power architecture that meets their end application requirements.

With the heterogeneous architecture, the designer has the opportunity to assign the right processing element to the right task while turning off processing elements when not needed. This level of control enables the Zynq UltraScale+ MPSoC to meet the demands of modern applications requiring high performance while meeting power and heat dissipation goals.

More information about the Zynq UltraScale+ MPSoC can be found by visiting:
http://www.xilinx.com/products/silicon-devices/soc/zynq-ultrascale-mpsoc.html

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
10/20/2016	1.1	Updated Zynq UltraScale+ MPSoC Power Modes Enable Performance/Power Optimization; Figure 2; Increased Performance per Watt from One Generation to the Next; and Figure 3.
09/20/2016	1.0	Initial Xilinx release.

Disclaimer

Automotive Applications Disclaimer