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UltraZed™-EV SOM Hardware User Guide

Version 1.2

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1.0	12/11/2017	Initial Release
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1.2	06/26/2020	VCCO_HD rail assignment 47/48 updated

Contents

1 Introduction

The UltraZed™-EV SOM (System-On Module) is a high performance System-On-Module targeted for broad use in many applications. The features provided by the UltraZed-EV System-On-Module consist of:

- Xilinx XCZU7EV-1FBVB900 MPSoC
  - Pin Compatible with the 4EV and 5EV MPSoC devices in the same package
  - Optionally configurable to support the available EG and CG MPSoC devices in the same package
  - Primary configuration Options = eMMC or QSPI Flash
  - Auxiliary primary configuration options via End User Carrier Card
    - JTAG
    - microSD Card
- Memory
  - PS DDR4 SDRAM (4GB, x64)
  - PL DDR4 SDRAM (1GB, x16)
  - Dual QSPI Flash (64MB)
  - eMMC Flash (8GB, x8)
  - I2C EEPROM (2Kb)
- Interfaces
  - Gigabit Ethernet PHY (Connector required on End User Carrier Card)
  - USB 2.0 ULPI PHY (Connector required on End User Carrier Card)
  - I2C I/O Expander
  - Two Channel I2C Switch/MUX
  - 3 JX Micro Headers (2 x 200-pin and 1 x 120-pin)
    - 152 user PL I/O pins
    - 26 user PS MIO pins (one full MIO bank)
    - 4 PS GTR transceivers
    - 4 PS GTR reference clock inputs
    - 16 PL GTH transceivers
    - 8 PL GTH reference clock inputs
    - PS JTAG interface
    - PL SYSMON interface
    - USB 2.0 connector interface
    - Gigabit Ethernet RJ45 connector interface
    - PMBus interface
    - SOM PS VBATT battery input
    - Carrier Card I2C interface
    - SOM Reset input
    - Carrier Card interrupt input
    - Carrier Card Reset output
    - Power Good output
    - SOM to Carrier Card ground pins
    - SOM input voltages and output sense pins
- PS Reference Clock Input
  - 33.333 MHz OSC
- Power
  - On-Board 5-Output Voltage Regulators
  - Full Power Sequencing Pre-Programmed
  - Selectable VCCINT_VCU for EG and CG MPSoC support.

  - Bank I/O Voltage Rails, GTR Transceiver Voltage Rails, and GTH Transceiver Voltage Rails are powered from End User Carrier Card via JX Micro Headers
- Pertinent URLs
  - SOM: http://ultrazed.org/product/ultrazed-ev™-som

The following figure is a high level block diagram of the UltraZed-EV SOM and the peripherals attached to the Zynq UltraScale+ MPSoC Processing Sub-System and Programmable Logic Sub-System.

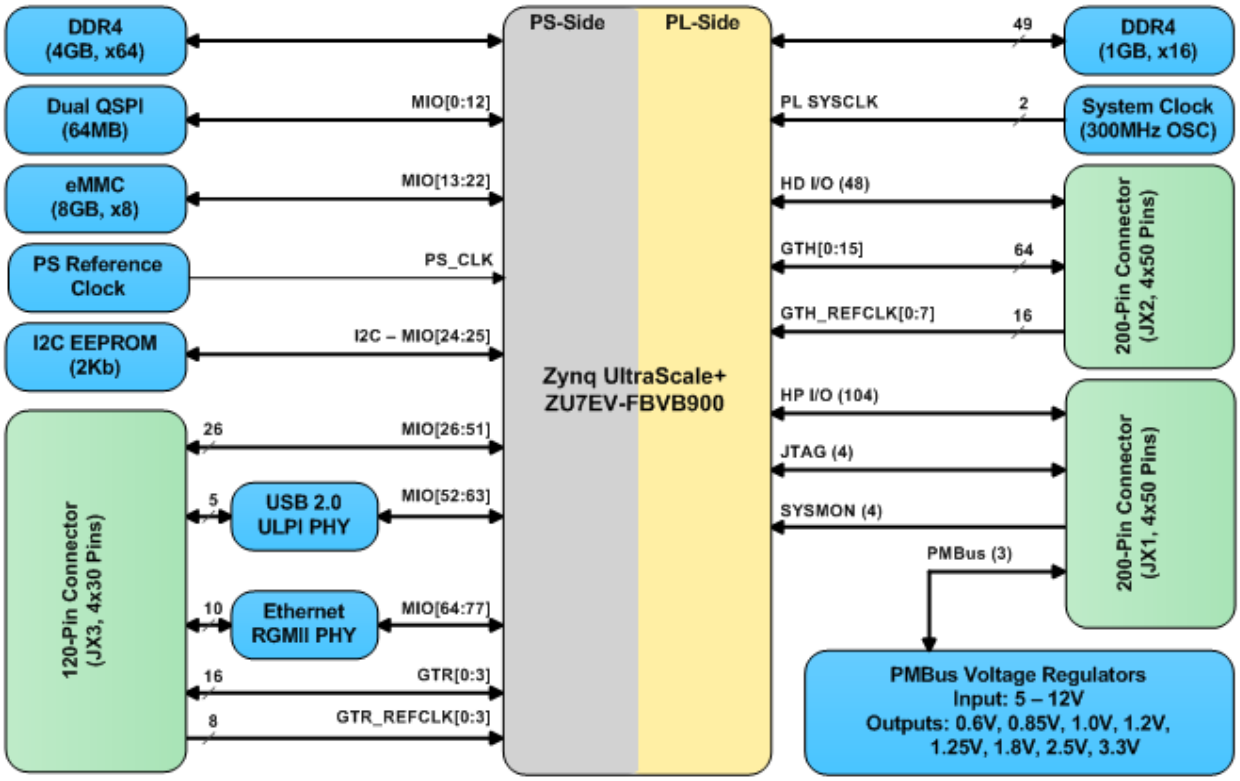

Figure 1 – UltraZed-EV SOM Block Diagram

2 Functional Description

2.1 Zynq UltraScale+ MPSoC

The UltraZed-EV SOM includes a Xilinx Zynq UltraScale+ MPSoC. The devices capable of being populated on the UltraZed-EV SOM are the XCZU7EV, XCZU5EV, or XCZU4EV in the FBVB900 package. The UltraZed-EV SOM also supports the CG and EG MPSoC devices via BOM modifications. Both extended and industrial temperature grade options are available as well as all of the speed grade options offered by Xilinx.

NOTE: Please contact your local Avnet FAE in regards to currently available options or custom device options for the UltraZed-EV SOM.

2.2 Memory

Zynq UltraScale+ contains a hardened PS memory interface unit. The memory interface unit includes a dynamic memory controller and static memory interface modules. The UltraZed-EV SOM takes advantage of these interfaces to provide system RAM as well as two different non-volatile memory sources.

2.2.1 PS-DDR4

The UltraZed-EV SOM includes four Micron **MT40A512M16JY-083E IT:B** (96-pin BGA package) DDR4 memory components creating a 512M x 64-bit interface, totalling 4 GB of random access memory. The DDR4 memory is connected to the hard memory controller in the PS of the Zynq UltraScale+ MPSoC via its Bank 504 PS Memory Interface. The Bank 504 PS Memory Interface incorporates both the DDR controller and the associated PHY, including its own set of IOs.

Speeds of up to 2,400 Mbps for DDR4 is supported. The DDR4 interface is designed to use 1.2V SSTL-compatible inputs.

DDR4 Termination is utilized on the UltraZed-EV SOM and configured for fly-by routing topology. Additionally the board trace lengths are matched, compensating for the internal package flight times of the Zynq UltraScale+ MPSoC FBVB900 package, to meet the requirements listed in the Xilinx PCB Design and Pin Planning Guide (UG583).

All single-ended signals are routed with 50 ohm trace impedance. Differential signals are set to 90 ohms trace impedance. Several signals are terminated through 40 ohms resistors to +PS_DDR4_VTT. Each DDR4 chip has its own 240-ohm pull-down on ZQ.

NOTE: +PS_DDR4_VREF is not the same as +PS_DDR4_VTT.

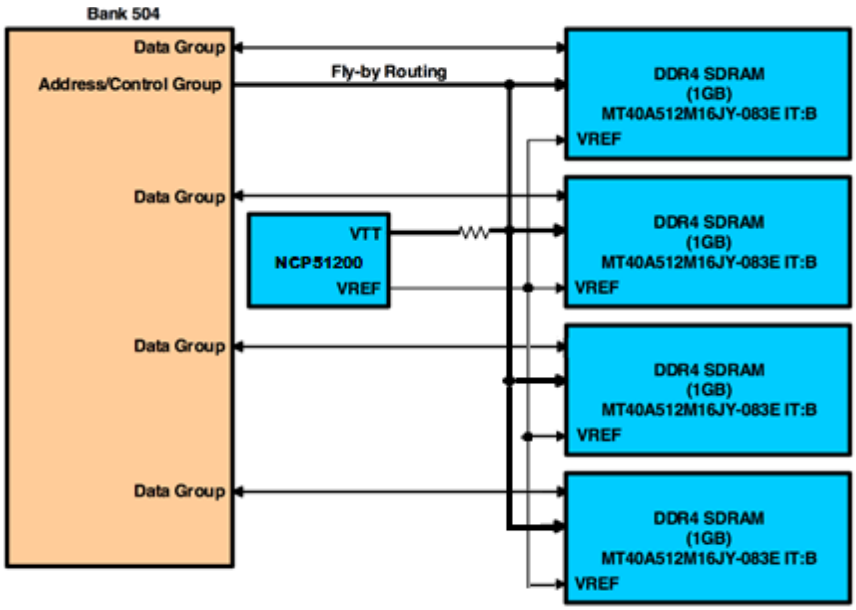

Figure 2 – PS-DDR4 Block Diagram

Signal Name	Description	Bank 504 MPSoC Pin	DDR4 Pin
PS_DDR_A0	DDR Address Input	AH30	P3
PS_DDR_A1	DDR Address Input	AG30	P7
PS_DDR_A2	DDR Address Input	AK29	R3
PS_DDR_A3	DDR Address Input	AJ30	N7
PS_DDR_A4	DDR Address Input	AK28	N3
PS_DDR_A5	DDR Address Input	AK27	P8
PS_DDR_A6	DDR Address Input	AF27	P2
PS_DDR_A7	DDR Address Input	AE27	R8
PS_DDR_A8	DDR Address Input	AF26	R2
PS_DDR_A9	DDR Address Input	AG26	R7
PS_DDR_A10	DDR Address Input	AE29	M3
PS_DDR_A11	DDR Address Input	AE28	T2
PS_DDR_A12	DDR Address Input	AH29	M7
PS_DDR_A13	DDR Address Input	AH28	T8
PS_DDR_A14	DDR Address / RAS Input	AG29	L2
PS_DDR_A15	DDR Address / CAS Input	AJ29	M8
PS_DDR_A16	DDR Address / WE_N Input	AH27	L8
PS_DDR_BA0	DDR Bank Address Inputs	AD27	N2
PS_DDR_BA1	DDR Bank Address Inputs	AC26	N8
PS_DDR_BG0	DDR Bank Group Address Inputs	AC28	M2
PS_DDR_CKE0	DDR Clock Enable Input	AC30	K2
PS_DDR_CK0_P	DDR Clock Device 0 Pair	AE30	K7
PS_DDR_CK0_N	DDR Clock Device 0 Pair	AF30	K8
PS_DDR_CS0_N	DDR Chip Select Input	AD30	L7
PS_DDR_ACT_N	DDR Activate Command Input	AD26	L3
PS_DDR_ALERT_N	DDR Alert Output	AB24	P9
PS_DDR_ODT0	DDR On-Die Termination	AB30	K3
PS_DDR_PARITY	DDR Command/Address Parity	AB26	T3

Signal Name	Description	Bank 504 MPSoC Pin	DDR4 Pin
PS_DDR_RAM_RST_N	DDR Active Low Reset Input	AB25	P1
PS_DDR_ZQ	ZQ Calibration Reference	AB23	F9
PS_DDR_DQ0	DDR Data Byte 0	AH22	U19-G2
PS_DDR_DQ1	DDR Data Byte 0	AH21	U19-F7
PS_DDR_DQ2	DDR Data Byte 0	AJ22	U19-H3
PS_DDR_DQ3	DDR Data Byte 0	AK22	U19-H7
PS_DDR_DQ4	DDR Data Byte 0	AK20	U19-H2
PS_DDR_DQ5	DDR Data Byte 0	AJ19	U19-H8
PS_DDR_DQ6	DDR Data Byte 0	AK19	U19-J3
PS_DDR_DQ7	DDR Data Byte 0	AH19	U19-J7
PS_DDR_DM0	DDR Data Byte 0 Data Mask	AJ20	U19-E7
PS_DDR_DQS0_P	DDR Data Byte 0 Data Strobe Pair	AJ21	U19-G3
PS_DDR_DQS0_N	DDR Data Byte 0 Data Strobe Pair	AK21	U19-F3
PS_DDR_DQ8	DDR Data Byte 1	AH23	U19-A3
PS_DDR_DQ9	DDR Data Byte 1	AK23	U19-B8
PS_DDR_DQ10	DDR Data Byte 1	AG24	U19-C3
PS_DDR_DQ11	DDR Data Byte 1	AK24	U19-C7
PS_DDR_DQ12	DDR Data Byte 1	AJ26	U19-C2
PS_DDR_DQ13	DDR Data Byte 1	AK25	U19-C8
PS_DDR_DQ14	DDR Data Byte 1	AG25	U19-D3
PS_DDR_DQ15	DDR Data Byte 1	AH26	U19-D7
PS_DDR_DM1	DDR Data Byte 1 Data Mask	AJ25	U19-E2
PS_DDR_DQS1_P	DDR Data Byte 1 Data Strobe Pair	AH24	U19-B7
PS_DDR_DQS1_N	DDR Data Byte 1 Data Strobe Pair	AJ24	U19-A7
PS_DDR_DQ16	DDR Data Byte 2	AD22	U20-G2
PS_DDR_DQ17	DDR Data Byte 2	AE22	U20-F7
PS_DDR_DQ18	DDR Data Byte 2	AF22	U20-H3
PS_DDR_DQ19	DDR Data Byte 2	AG21	U20-H7
PS_DDR_DQ20	DDR Data Byte 2	AD20	U20-H2
PS_DDR_DQ21	DDR Data Byte 2	AF20	U20-H8
PS_DDR_DQ22	DDR Data Byte 2	AE20	U20-J3
PS_DDR_DQ23	DDR Data Byte 2	AG20	U20-J7
PS_DDR_DM2	DDR Data Byte 2 Data Mask	AF21	U20-E7
PS_DDR_DQS2_P	DDR Data Byte 2 Data Strobe Pair	AC21	U20-G3
PS_DDR_DQS2_N	DDR Data Byte 2 Data Strobe Pair	AD21	U20-F3
PS_DDR_DQ24	DDR Data Byte 3	AG23	U20-A3
PS_DDR_DQ25	DDR Data Byte 3	AF23	U20-B8
PS_DDR_DQ26	DDR Data Byte 3	AF25	U20-C3
PS_DDR_DQ27	DDR Data Byte 3	AE23	U20-C7
PS_DDR_DQ28	DDR Data Byte 3	AC22	U20-C2
PS_DDR_DQ29	DDR Data Byte 3	AC23	U20-C8
PS_DDR_DQ30	DDR Data Byte 3	AD25	U20-D3
PS_DDR_DQ31	DDR Data Byte 3	AC24	U20-D7
PS_DDR_DM3	DDR Data Byte 3 Data Mask	AE25	U20-E2
PS_DDR_DQS3_P	DDR Data Byte 3 Data Strobe Pair	AD24	U20-B7
PS_DDR_DQS3_N	DDR Data Byte 3 Data Strobe Pair	AE24	U20-A7
PS_DDR_DQ32	DDR Data Byte 4	U24	U21-G2
PS_DDR_DQ33	DDR Data Byte 4	V23	U21-F7

Signal Name	Description	Bank 504 MPSoC Pin	DDR4 Pin
PS_DDR_DQ34	DDR Data Byte 4	U25	U21-H3
PS_DDR_DQ35	DDR Data Byte 4	V24	U21-H7
PS_DDR_DQ36	DDR Data Byte 4	Y25	U21-H2
PS_DDR_DQ37	DDR Data Byte 4	AA23	U21-H8
PS_DDR_DQ38	DDR Data Byte 4	AA25	U21-J3
PS_DDR_DQ39	DDR Data Byte 4	Y23	U21-J7
PS_DDR_DM4	DDR Data Byte 4 Data Mask	Y24	U21-E7
PS_DDR_DQS4_P	DDR Data Byte 4 Data Strobe Pair	W24	U21-G3
PS_DDR_DQS4_N	DDR Data Byte 4 Data Strobe Pair	W25	U21-F3
PS_DDR_DQ40	DDR Data Byte 5	P23	U21-A3
PS_DDR_DQ41	DDR Data Byte 5	R23	U21-B8
PS_DDR_DQ42	DDR Data Byte 5	T23	U21-C3
PS_DDR_DQ43	DDR Data Byte 5	P26	U21-C7
PS_DDR_DQ44	DDR Data Byte 5	T25	U21-C2
PS_DDR_DQ45	DDR Data Byte 5	U23	U21-C8
PS_DDR_DQ46	DDR Data Byte 5	T26	U21-D3
PS_DDR_DQ47	DDR Data Byte 5	P24	U21-D7
PS_DDR_DM5	DDR Data Byte 5 Data Mask	R24	U21-E2
PS_DDR_DQS5_P	DDR Data Byte 5 Data Strobe Pair	P25	U21-B7
PS_DDR_DQS5_N	DDR Data Byte 5 Data Strobe Pair	R25	U21-A7
PS_DDR_DQ48	DDR Data Byte 6	U26	U22-G2
PS_DDR_DQ49	DDR Data Byte 6	V26	U22-F7
PS_DDR_DQ50	DDR Data Byte 6	U28	U22-H3
PS_DDR_DQ51	DDR Data Byte 6	V27	U22-H7
PS_DDR_DQ52	DDR Data Byte 6	U30	U22-H2
PS_DDR_DQ53	DDR Data Byte 6	V30	U22-H8
PS_DDR_DQ54	DDR Data Byte 6	W30	U22-J3
PS_DDR_DQ55	DDR Data Byte 6	W29	U22-J7
PS_DDR_DM6	DDR Data Byte 6 Data Mask	V28	U22-E7
PS_DDR_DQS6_P	DDR Data Byte 6 Data Strobe Pair	U29	U22-G3
PS_DDR_DQS6_N	DDR Data Byte 6 Data Strobe Pair	V29	U22-F3
PS_DDR_DQ56	DDR Data Byte 7	R30	U22-A3
PS_DDR_DQ57	DDR Data Byte 7	T30	U22-B8
PS_DDR_DQ58	DDR Data Byte 7	P30	U22-C3
PS_DDR_DQ59	DDR Data Byte 7	P29	U22-C7
PS_DDR_DQ60	DDR Data Byte 7	T28	U22-C2
PS_DDR_DQ61	DDR Data Byte 7	T27	U22-C8
PS_DDR_DQ62	DDR Data Byte 7	P27	U22-D3
PS_DDR_DQ63	DDR Data Byte 7	R27	U22-D7
PS_DDR_DM7	DDR Data Byte 7 Data Mask	P28	U22-E2
PS_DDR_DQS7_P	DDR Data Byte 7 Data Strobe Pair	R28	U22-B7
PS_DDR_DQS7_N	DDR Data Byte 7 Data Strobe Pair	R29	U22-A7
+PS_DDR4_VREF	DDR Reference voltage	-	VREFCA
+PS_DDR4_VTT	DDR Termination voltage	-	-

Table 1– PS-DDR4 Connections

NOTE: (U19, U20, U21 or U22 indicates DDR4 Device Reference Designator)

2.2.2 PL-DDR4

The UltraZed-EV SOM includes a single Micron **MT40A512M16JY-083E IT:B** (96-pin BGA package) DDR4 memory components creating a 512M x 16-bit interface, totalling 1 GB of random access memory. The DDR4 memory is connected to a soft memory controller IP in the PL of the Zynq UltraScale+ MPSoC via Bank 66. The Bank 66 PL Memory Interface incorporates both the DDR controller and the associated PHY, including its own set of IOs.

Speeds of up to 2,400 Mbps for DDR4 is supported. The DDR4 interface is designed to use 1.2V SSTL-compatible inputs.

DDR4 Termination is utilized on the UltraZed-EV SOM and configured for fly-by routing topology. Additionally the board trace lengths are matched, compensating for the internal package flight times of the Zynq UltraScale+ MPSoC FBVB900 package, to meet the requirements listed in the Xilinx PCB Design and Pin Planning Guide (UG583).

All single-ended signals are routed with 50 ohm trace impedance. Differential signals are set to 90 ohms trace impedance. Several signals are terminated through 40 ohms resistors to +DDR4_VTT. Each DDR4 chip has its own 240-ohm pull-down on ZQ.

NOTE: +PL_DDR4_VREF is not the same as +PL_DDR4_VTT.

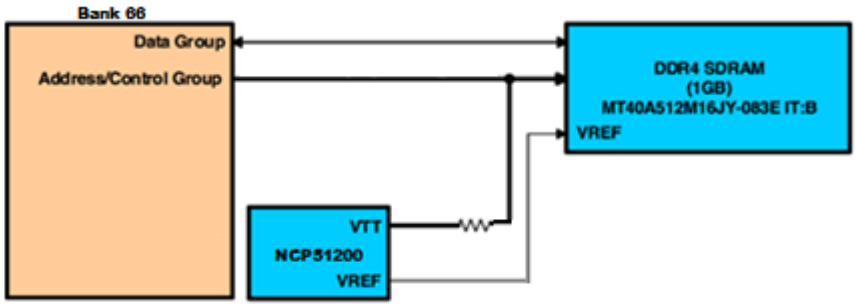

Figure 3 – PL-DDR4 Block Diagram

Signal Name	Description	Bank 66 MPSoC Pin	DDR4 Pin
PL_DDR4_A0	DDR Address Input	AC9	P3
PL_DDR4_A1	DDR Address Input	AD9	P7
PL_DDR4_A2	DDR Address Input	AC6	R3
PL_DDR4_A3	DDR Address Input	AD6	N7
PL_DDR4_A4	DDR Address Input	W8	N3
PL_DDR4_A5	DDR Address Input	Y8	P8
PL_DDR4_A6	DDR Address Input	AA8	P2
PL_DDR4_A7	DDR Address Input	AB8	R8
PL_DDR4_A8	DDR Address Input	W9	R2
PL_DDR4_A9	DDR Address Input	AC12	R7
PL_DDR4_A10	DDR Address Input	AD12	M3
PL_DDR4_A11	DDR Address Input	AA12	T2
PL_DDR4_A12	DDR Address Input	AA11	M7
PL_DDR4_A13	DDR Address Input	AB11	T8
PL_DDR4_A14	DDR Address / RAS Input	AD10	L2
PL_DDR4_A15	DDR Address / CAS Input	AD11	M8
PL_DDR4_A16	DDR Address / WE_N Input	AC11	L8

Signal Name	Description	Bank 66 MPSoC Pin	DDR4 Pin
PL_DDR4_BA0	DDR Bank Address Inputs	AB9	N2
PL_DDR4_BA1	DDR Bank Address Inputs	AB10	N8
PL_DDR4_BG	DDR Bank Group Address Inputs	Y10	M2
PL_DDR4_CKE	DDR Clock Enable Input	AE7	K2
PL_DDR4_CK_P	DDR Clock Device Pair	Y7	K7
PL_DDR4_CK_N	DDR Clock Device Pair	AA7	K8
PL_DDR4_CS_N	DDR Chip Select Input	AA10	L7
PL_DDR4_ACT_N	DDR Activate Command Input	AE2	L3
PL_DDR4_ALERT_N	DDR Alert Output	-	P9
PL_DDR4_ODT	DDR On-Die Termination	AE3	K3
PL_DDR4_PARITY	DDR Command/Address Parity	-	T3
PL_DDR4_RESET_N	DDR Active Low Reset Input	Y1	P1
PL_DDR4_ZQ	ZQ Calibration Reference	Y9	F9
PL_DDR4_DQ0	DDR Data Byte 0	AD1	U23-G2
PL_DDR4_DQ1	DDR Data Byte 0	AE1	U23-F7
PL_DDR4_DQ2	DDR Data Byte 0	AC3	U23-H3
PL_DDR4_DQ3	DDR Data Byte 0	AC2	U23-H7
PL_DDR4_DQ4	DDR Data Byte 0	AB1	U23-H2
PL_DDR4_DQ5	DDR Data Byte 0	AC1	U23-H8
PL_DDR4_DQ6	DDR Data Byte 0	AA2	U23-J3
PL_DDR4_DQ7	DDR Data Byte 0	AA1	U23-J7
PL_DDR4_DM_DBI_0_N	DDR Data Byte 0 Data Mask	AD2	U23-E7
PL_DDR4_DQS0_P	DDR Data Byte 0 Data Strobe Pair	AA3	U23-G3
PL_DDR4_DQS0_N	DDR Data Byte 0 Data Strobe Pair	AB3	U23-F3
PL_DDR4_DQ8	DDR Data Byte 1	AB6	U23-A3
PL_DDR4_DQ9	DDR Data Byte 1	AB5	U23-B8
PL_DDR4_DQ10	DDR Data Byte 1	AD5	U23-C3
PL_DDR4_DQ11	DDR Data Byte 1	AE5	U23-C7
PL_DDR4_DQ12	DDR Data Byte 1	AB4	U23-C2
PL_DDR4_DQ13	DDR Data Byte 1	AC4	U23-C8
PL_DDR4_DQ14	DDR Data Byte 1	AA6	U23-D3
PL_DDR4_DQ15	DDR Data Byte 1	AA5	U23-D7
PL_DDR4_DM_DBI_1_N	DDR Data Byte 1 Data Mask	AD7	U23-E2
PL_DDR4_DQS1_P	DDR Data Byte 1 Data Strobe Pair	AD4	U23-B7
PL_DDR4_DQS1_N	DDR Data Byte 1 Data Strobe Pair	AE4	U23-A7
+PL_DDR4_VREF	DDR Reference voltage	-	VREFCA
+PL_DDR4_VTT	DDR Termination voltage	-	-

Table 2– PL-DDR4 Connections

NOTE: (U23 indicates DDR4 Device Reference Designator)

2.2.3 Dual Parallel (x8) QSPI Flash

The UltraZed-EV SOM features two 4-bit SPI (quad-SPI) serial NOR flash devices organized in a dual parallel configuration. The **Micron MT25QU256ABAIEW7-0SIT** QSPI Flash devices are used on the UltraZed-EV SOM. The Multi-I/O SPI Flash memory is used to provide non-volatile boot, application code, and data storage. It can be used to initialize the PS subsystem as well as configure the PL subsystem (bitstream).

The Quad-SPI Flash connects to the Zynq UltraScale+ MPSoC PS QSPI interface. This requires connection to specific pins in MIO Bank 500, specifically MIO[0:12] as outlined in the Zynq UltraScale+ TRM (Technical Reference Manual, UG1085). Quad-SPI feedback mode is used, thus the CLK_FOR_LPBK signal tied to MIO[6] is left floating. This allows a QSPI clock frequency greater than FQSPICLK2.

The Zynq UltraScale+ MPSoC peripheral used to control the QSPI flash devices is named QSPI. The QSPI devices can be operated up to 166MHz depending on the operating mode and the possible performance of the QSPI controller in the MPSoC. The QSPI flash devices are physically connected to the QSPI controller in the PS of the Zynq UltraScale+ MPSoC via Bank 500.

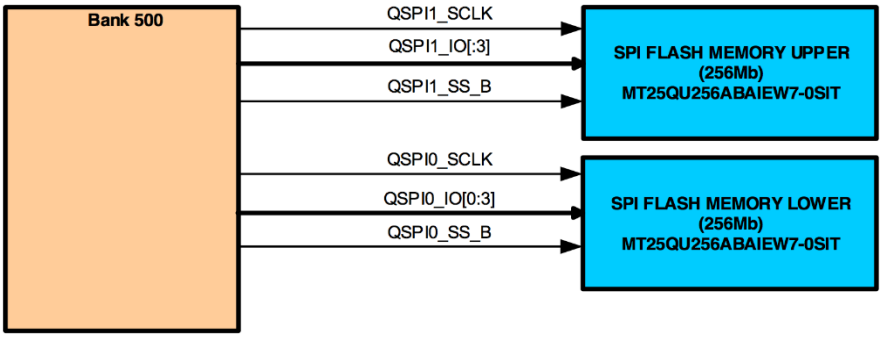

Figure 4 – Dual QSPI Block Diagram

Signal Name	Description	MPSoC Pin	MIO	Quad-SPI Pin
MIO0_QSPI0_SCLK	Lower QSPI Serial Clock	H17	PS_MIO0	U2-6
MIO1_QSPI0_IO1	Lower QSPI Data [1]	A20	PS_MIO1	U2-2
MIO2_QSPI0_IO2	Lower QSPI Data [2]	B19	PS_MIO2	U2-3
MIO3_QSPI0_IO3	Lower QSPI Data [3]	D19	PS_MIO3	U2-7
MIO4_QSPI0_IO0	Lower QSPI Data [0]	J17	PS_MIO4	U2-5
MIO5_QSPI0_SS_B	Lower QSPI Select	C19	PS_MIO5	U2-1
FLOAT (NC)	Loopback Clock	-	PS_MIO6	-
MIO7_QSPI1_SS_B	Upper QSPI Select	E19	PS_MIO7	U3-1
MIO8_QSPI1_IO0	Upper QSPI Data [0]	E20	PS_MIO8	U3-5
MIO9_QSPI1_IO1	Upper QSPI Data [1]	F20	PS_MIO9	U3-2
MIO10_QSPI1_IO2	Upper QSPI Data [2]	F18	PS_MIO10	U3-3
MIO11_QSPI1_IO3	Upper QSPI Data [3]	G18	PS_MIO11	U3-7
MIO12_QSPI1_SCLK	Upper QSPI Serial Clock	H18	PS_MIO12	U3-6

Table 3 – Quad-SPI Flash Pin Assignment and Definitions

NOTE: (U2 or U3 indicates QSPI Device Reference Designator)

2.2.4 eMMC x8 Flash (Multi-Media Controller)

The UltraZed-EV SOM features a Micron MTFC8GAKAJCN-4M IT eMMC Multi Media Controller and NAND Flash IC. The eMMC is used to provide non-volatile user data storage and/or primary or secondary boot storage.

The Zynq UltraScale+ MPSoC peripheral used to control the eMMC flash device is named **SD0**. The eMMC flash device can be operated up to 52MHz and is physically connected to the PS of the Zynq UltraScale+ MPSoC via Bank 500. The eMMC I/O has direct connections to the Zynq UltraScale+ MIO through the PS_MIO [13:22] pins.

The UltraZed-EV SOM end-user is capable of issuing a soft reset, **P0_EMMC0_RST_N**, to the eMMC flash device via an on board two-wire serial interface. The active low reset is assigned to Port 0 of the On Semiconductor PCA9654 I/O expander. The I/O expander is attached to an I2C peripheral on the Zynq UltraScale+ device. For further information on the I/O expander and its connections, please locate the I/O expander section within this hardware user guide.

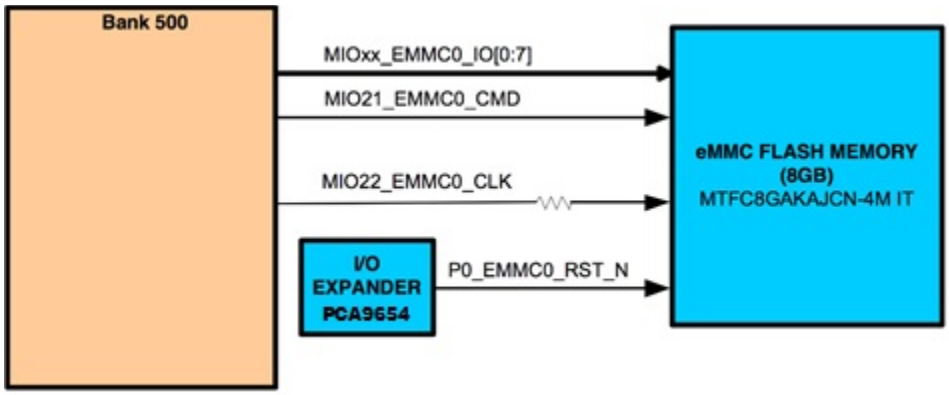

Figure 5 – eMMC Block Diagram

Signal Name	Description	MPSoC Pin	MIO	eMMC Pin
MIO13_EMMC0_IO0	EMMC Data IO [0]	G19	PS_MIO13	A3
MIO14_EMMC0_IO1	EMMC Data IO [1]	E18	PS_MIO14	A4
MIO15_EMMC0_IO2	EMMC Data IO [2]	J19	PS_MIO15	A5
MIO16_EMMC0_IO3	EMMC Data IO [3]	K17	PS_MIO16	B2
MIO17_EMMC0_IO4	EMMC Data IO [4]	C18	PS_MIO17	B3
MIO18_EMMC0_IO5	EMMC Data IO [5]	K18	PS_MIO18	B4
MIO19_EMMC0_IO6	EMMC Data IO [6]	K16	PS_MIO19	B5
MIO20_EMMC0_IO7	EMMC Data IO [7]	A19	PS_MIO20	B6
MIO21_EMMC0_CMD	EMMC Command	H19	PS_MIO21	M5
MIO22_EMMC0_CLK	EMMC Clock	F17	PS_MIO22	M6

Table 4 – eMMC Pin Assignment and Definitions

NOTE: EMMC18 Boot Mode: MODE PINS [3:0] – 0x6

2.2.5 FBVB900 Device Package Delay Compensation for Memory Interfaces

The Zynq UltraScale+ MPSoC device package delay is accommodated for in the layout of the each of the memory interfaces signal trace lengths. The average of min and max values for package delay is utilized to compensate for the flight time caused by the delay associated with this package.

2.3 GTH Transceivers

The UltraZed-EV SOM has 16 multi-gigabit transceiver lanes that reside on Quads 224, 225, 226, and 227 of the Zynq UltraScale+ MPSoC device. These transceivers can be used to interface to multiple high speed interface protocols. Examples of such interfaces are SFP+, HDMI, and 3G-SDI. These interfaces have reference designs provided via the Avnet UltraZed-EV Carrier Card. The GTH interfaces are not limited to those listed here as custom interfaces can be created.

The associated high speed protocol MAC layers are soft macros that would exist in the Programmable Logic (PL) subsystem of the Zynq UltraScale+ MPSoC device so additional Intellectual Property (IP) or targeted devices may be necessary to complete custom interfaces on an end user's custom carrier card.

The Zynq UltraScale+ MPSoC is enabled with 16 GTH transceivers which are capable of a transceiver data rates up to 16.3750 Gbps (In a proper speed/temperature grade device). By default, the UltraZed-EV SOM is populated with a -1 MPSoC device and supports data rates up to 12.5 Gbps.

Eight (8) differential MGT reference clock inputs are available to support the GTH transceiver lanes. The multi-gigabit transceiver lanes and their associated reference clocks are connected to the end-user carrier board via the JX2 Micro Header. The end user carrier card is responsible for sourcing the proper reference clocks to the UltraZed-EV SOM. Please review to the Xilinx UltraScale+ MPSoC data sheet for the requirements of these reference clocks. As an example, refer to the UltraZed-EV Carrier Card for a solution to providing the GTH reference clocks to the UltraZed-EV SOM.

Each of the UltraZed-EV SOM's Quads are length tuned from the Zynq UltraScale+ MPSoC device to the JX2 connector taking into account the device package delays. The MPSoC device package delay report provided by Xilinx and the PCB net length report provided by Avnet can be used to determine the required delay for each implemented interface on the end-user carrier card. If the implemented interface is wider than x4 (a single quad), it is imperative to length tune the wider implemented interface on the end user's customer carrier card taking into account each length across the multiple Quads.

The table below shows the connections between the Zynq UltraScale+ MPSoC device and the JX2 Micro Header.

PS IO Name	MPSoC Pin Number	Net Name	JX2 Connector
MGTHRXN0_224	V1	GTH12_RX_N	JX2.A43
MGTHRXN1_224	U3	GTH13_RX_N	JX2.C46
MGTHRXN2_224	T1	GTH14_RX_N	JX2.A46
MGTHRXN3_224	P1	GTH15_RX_N	JX2.C48
MGTHRXP0_224	V2	GTH12_RX_P	JX2.A42
MGTHRXP1_224	U4	GTH13_RX_P	JX2.C45
MGTHRXP2_224	T2	GTH14_RX_P	JX2.A45
MGTHRXP3_224	P2	GTH15_RX_P	JX2.C48
MGTHTXN0_224	W3	GTH12_TX_N	JX2.B42
MGTHTXN1_224	V5	GTH13_TX_N	JX2.D45
MGTHTXN2_224	T5	GTH14_TX_N	JX2.B45
MGTHTXN3_224	R3	GTH15_TX_N	JX2.D48
MGTHTXP0_224	W4	GTH12_TX_P	JX2.B41
MGTHTXP1_224	V6	GTH13_TX_P	JX2.D44
MGTHTXP2_224	T6	GTH14_TX_P	JX2.B44
MGTHTXP3_224	R4	GTH15_TX_P	JX2.D47
MGTREFCLK0N_224	R7	GTH_REFCLK6_N	JX2.B48
MGTREFCLK0P_224	R8	GTH_REFCLK6_P	JX2.B47
MGTREFCLK1N_224	N7	GTH_REFCLK7_N	JX2.A49
MGTREFCLK1P_224	N8	GTH_REFCLK7_P	JX2.A48
MGTHRXN0_225	N3	GTH8_RX_N	JX2.C37
MGTHRXN1_225	M1	GTH9_RX_N	JX2.A37
MGTHRXN2_225	K1	GTH10_RX_N	JX2.C40
MGTHRXN3_225	J3	GTH11_RX_N	JX2.A40
MGTHRXP0_225	N4	GTH8_RX_P	JX2.C36
MGTHRXP1_225	M2	GTH9_RX_P	JX2.A36
MGTHRXP2_225	K2	GTH10_RX_P	JX2.C39
MGTHRXP3_225	J4	GTH11_RX_P	JX2.A39
MGTHTXN0_225	P5	GTH8_TX_N	JX2.D36
MGTHTXN1_225	M5	GTH9_TX_N	JX2.B36
MGTHTXN2_225	L3	GTH10_TX_N	JX2.D39
MGTHTXN3_225	K5	GTH11_TX_N	JX2.B39
MGTHTXP0_225	P6	GTH8_TX_P	JX2.D35
MGTHTXP1_225	M6	GTH9_TX_P	JX2.B35
MGTHTXP2_225	L4	GTH10_TX_P	JX2.D38
MGTHTXP3_225	K6	GTH11_TX_P	JX2.B38
MGTREFCLK0N_225	L7	GTH_REFCLK4_N	JX2.D42
MGTREFCLK0P_225	L8	GTH_REFCLK4_P	JX2.D41
MGTREFCLK1N_225	J7	GTH_REFCLK5_N	JX2.C43
MGTREFCLK1P_225	J8	GTH_REFCLK5_P	JX2.C42
MGTAVTTRCAL_R	K7	MGTAVTTRCAL_R	-
MGTRREF_R	K8	MGTRREF_R	-
MGTHRXN0_226	H1	GTH4_RX_N	JX2.A28
MGTHRXN1_226	G3	GTH5_RX_N	JX2.C31
MGTHRXN2_226	F1	GTH6_RX_N	JX2.A31

MGTHRXN3_226	E3	GTH7_RX_N	JX2.C34
MGTHRXP0_226	H2	GTH4_RX_P	JX2.A27
MGTHRXP1_226	G4	GTH5_RX_P	JX2.C30
MGTHRXP2_226	F2	GTH6_RX_P	JX2.A30
MGTHRXP3_226	E4	GTH7_RX_P	JX2.C33
MGTHTXN0_226	H5	GTH4_TX_N	JX2.B27
MGTHTXN1_226	G7	GTH5_TX_N	JX2.D30
MGTHTXN2_226	F5	GTH6_TX_N	JX2.B30
MGTHTXN3_226	E7	GTH7_TX_N	JX2.D33
MGTHTXP0_226	H6	GTH4_TX_P	JX2.B26
MGTHTXP1_226	G8	GTH5_TX_P	JX2.D29
MGTHTXP2_226	F6	GTH6_TX_P	JX2.B29
MGTHTXP3_226	E8	GTH7_TX_P	JX2.D32
MGTREFCLK0N_226	H9	GTH_REFCLK2_N	JX2.B33
MGTREFCLK0P_226	H10	GTH_REFCLK2_P	JX2.B32
MGTREFCLK1N_226	F9	GTH_REFCLK3_N	JX2.A34
MGTREFCLK1P_226	F10	GTH_REFCLK3_P	JX2.A33
MGTHRXN0_227	D1	GTH0_RX_N	JX2.C22
MGTHRXN1_227	C3	GTH1_RX_N	JX2.A22
MGTHRXN2_227	B1	GTH2_RX_N	JX2.C25
MGTHRXN3_227	A3	GTH3_RX_N	JX2.A25
MGTHRXP0_227	D2	GTH0_RX_P	JX2.C21
MGTHRXP1_227	C4	GTH1_RX_P	JX2.A21
MGTHRXP2_227	B2	GTH2_RX_P	JX2.C24
MGTHRXP3_227	A4	GTH3_RX_P	JX2.A24
MGTHTXN0_227	D5	GTH0_TX_N	JX2.D21
MGTHTXN1_227	C7	GTH1_TX_N	JX2.B21
MGTHTXN2_227	B5	GTH2_TX_N	JX2.D24
MGTHTXN3_227	A7	GTH3_TX_N	JX2.B24
MGTHTXP0_227	D6	GTH0_TX_P	JX2.D20
MGTHTXP1_227	C8	GTH1_TX_P	JX2.B20
MGTHTXP2_227	B6	GTH2_TX_P	JX2.D23
MGTHTXP3_227	A8	GTH3_TX_P	JX2.B23
MGTREFCLK0N_227	D9	GTH_REFCLK0_N	JX2.D27
MGTREFCLK0P_227	D10	GTH_REFCLK0_P	JX2.D26
MGTREFCLK1N_227	B9	GTH_REFCLK1_N	JX2.C28
MGTREFCLK1P_227	B10	GTH_REFCLK1_P	JX2.C27

Table 5 – GTH Quads Pin Assignments

2.3.1 FBVB900 Device Package Delay Compensation for GTH Transceiver Interface

The Zynq UltraScale+ MPSoC device package delay is accommodated for in the layout of each of the GTH transceiver quads via matching of the signal trace lengths. The average of min and max values for package delay is utilized to compensate for the flight time caused by the delay associated with this package.

2.4 GTR Transceivers

The UltraZed-EV SOM has four multi-gigabit transceiver lanes that reside on Bank 505 of the Zynq UltraScale+ MPSoC device. These transceivers can be used to interface to multiple high speed interface protocols such as PCI Express, Serial ATA, USB3.0, and Display Port. The associated high speed protocol MAC layers are hardened macros that exist in the PS subsystem of the Zynq UltraScale+ MPSoC device so additional Intellectual Property (IP) or targeted devices are not necessary to complete the various interfaces.

The Zynq UltraScale+ MPSoC is enabled with four GTR transceivers which are capable of a transceiver data rates up to 6.0 Gbps. Four differential MGT reference clock inputs are available to support the GTR transceiver lanes. The multi-gigabit transceiver lanes and their associated reference clocks are connected to the end-user carrier board via the JX3 Micro Header.

The UltraZed-EV SOM is capable of implementing up to a PCIe x4 interface as the physical design of the GTRs are each length tuned from the Zynq UltraScale+ MPSoC device to the JX3 connector taking into account the device package delays. The MPSoC device package delay report provided by Xilinx and the PCB net length report provided by Avnet can be used to determine the required delay for each implemented interface on the end-user carrier card.

The table below shows the connections between the Zynq UltraScale+ MPSoC device and the JX3 Micro Header.

PS IO Name	MPSoC Pin Number	Net Name	JX3 Connector
PS_MGTRRXN0_505	L30	GTR_RX0_N	JX3.A9
PS_MGTRRXN1_505	J30	GTR_RX1_N	JX3.C9
PS_MGTRRXN2_505	H28	GTR_RX2_N	JX3.A5
PS_MGTRRXN3_505	G30	GTR_RX3_N	JX3.C5
PS_MGTRRXP0_505	L29	GTR_RX0_P	JX3.A8
PS_MGTRRXP1_505	J29	GTR_RX1_P	JX3.C8
PS_MGTRRXP2_505	H27	GTR_RX2_P	JX3.A4
PS_MGTRRXP3_505	G29	GTR_RX3_P	JX3.C4
PS_MGTRTXN0_505	M28	GTR_TX0_N	JX3.B7
PS_MGTRTXN1_505	K28	GTR_TX1_N	JX3.D7
PS_MGTRTXN2_505	J26	GTR_TX2_N	JX3.B3
PS_MGTRTXN3_505	G26	GTR_TX3_N	JX3.D3
PS_MGTRTXP0_505	M27	GTR_TX0_P	JX3.B6
PS_MGTRTXP1_505	K27	GTR_TX1_P	JX3.D6
PS_MGTRTXP2_505	J25	GTR_TX2_P	JX3.B2
PS_MGTRTXP3_505	G25	GTR_TX3_P	JX3.D2
PS_MGTREFCLK0N_505	M24	GTR_REFCLK0_N	JX3.A13
PS_MGTREFCLK0P_505	M23	GTR_REFCLK0_P	JX3.A12
PS_MGTREFCLK1N_505	L26	GTR_REFCLK1_N	JX3.C13
PS_MGTREFCLK1P_505	L25	GTR_REFCLK1_P	JX3.C12
PS_MGTREFCLK2N_505	K24	GTR_REFCLK2_N	JX3.B11
PS_MGTREFCLK2P_505	K23	GTR_REFCLK2_P	JX3.B10
PS_MGTREFCLK3N_505	H24	GTR_REFCLK3_N	JX3.D11
PS_MGTREFCLK3P_505	H23	GTR_REFCLK3_P	JX3.D10
PS_MGTRREF_505	M25	-	-

Table 6 – Bank 505 GTR Pin Assignments

2.4.1 FBVB900 Device Package Delay Compensation for GTR Transceiver Interface

The Zynq UltraScale+ MPSoC device package delay is accommodated for in the layout of the each of the GTR transceiver signal trace lengths. The average of min and max values for package delay is utilized to compensate for the flight time caused by the delay associated with this package.

2.5 USB 2.0 OTG

The Zynq UltraScale+ MPSoC contains a hardened PS USB 2.0 controller. The UltraZed-EV SOM takes advantage of one of the two available PS USB 2.0 controllers to provide USB 2.0 On-The-Go signalling to the JX3 connector.

An external PHY with an 8-bit ULPI interface is implemented. A Microchip USB3320 Standalone USB Transceiver Chip is used as the PHY. The PHY features a complete HS-USB Physical Front-End supporting speeds of up to 480Mbs. VDDIO for this device can be 1.8V or 3.3V, and on the UltraZed-EV SOM VDDIO is powered at 1.8V. The PHY is connected to MIO Bank 502 which is also powered at 1.8V. This is critical since a level translator cannot be used as it would impact the ULPI timing between the PHY and the Zynq UltraScale+ MPSoC device.

Additionally, the USB3320 must clock the ULPI interface which requires a 24 MHz crystal or oscillator (configured as ULPI Output Clock Mode). On the UltraZed-EV SOM, the 24 MHz oscillator is an Abracon ASDMB CMOS oscillator, ASDMB-24.000MHZ-LY-T.

The physical USB connector is not populated on the UltraZed-EV SOM. The SOM is designed to have the physical USB connector reside on the end-user carrier card. The four USB connector signals (USB_OTG_P, USB_OTG_N, USB_ID and USB_OTG_CPEN) and USB_OTG_VBUS are connected to the JX3 Micro Header. The table below shows the connections of these signals at JX3.

Signal Name	JX3 Pin
USB_OTG_N	JX3.D15
USB_OTG_P	JX3.D14
USB_ID	JX3.D17
USB_OTG_CPEN	JX3.C16
USB_OTG_VBUS	JX3.C17

Table 7 – USB 2.0 JX3 Pin Assignments

The USB0 peripheral is used on the PS, connected through MIO [52-63] in MIO Bank 502. The USB Reset signal is active-low and connected to the I/O expander via Port 1, **P1_USB0_RST_N**. Either of the push button resets, **PS_POR_B** or **PS_SRST_B** will also generate the active-low USB Reset signal.

The UltraZed-EV SOM, with additional circuitry on an end-user carrier card, can be configured to operate in Host Mode (OTG) or Device Mode. With a standard connection to an end-user carrier card (no power supply used to provide USB power to the connector) the device will operate in Device Mode. Using the USB_OTG_CPEN signal on JX3 allows the user to control an external power source for USB_OTG_VBUS on the end-user carrier card. Other considerations need to be made to accommodate Host Mode. Refer to the Avnet UltraZed-EV Carrier Card design for an example design for configuring the end-user carrier card for either Host Mode or Device Mode.

Signal Name	Description	MPSoC Bank	MIO	USB3320 Pin
DATA[7:0]	USB Data lines	MIO Bank 502	52:63*	D[7:0]
CLKOUT	USB Clock	MIO Bank 502	52	1
DIR	ULPI DIR output signal	MIO Bank 502	53	31
STP	ULPI STP input signal	MIO Bank 502	58	29
NXT	ULPI NXT output signal	MIO Bank 502	55	2
REFSEL[2:0]	USB Chip Select	N/C	N/C	8,11,14
DP	DP pin of USB Connector			18
DM	DM pin of USB Connector			19
ID	Identification pin of the USB connector			23
RESET_B	Active-Low Reset	MIO Bank 502	N/C	27**

Table 8 – USB 2.0 Pin Assignment and Definitions

** See UltraZed-EV Schematic for specific MIO connections*
*** Connected through AND-gates with PS_POR_B, PS_SRST_B, and P1_USB0_RST_N from the I/O expander*

2.5.1 FBVB900 Device Package Delay Compensation for USB2.0 Interface

The Zynq UltraScale+ MPSoC device package delay is accommodated for in the layout of the USB2.0 signal trace lengths. The average of min and max values for package delay is utilized to compensate for the flight time caused by the delay associated with this package.

2.6 10/100/1000 Ethernet PHY

The UltraZed-EV SOM provides a single 10/100/1000 Ethernet port. The Zynq UltraScale+ MPSoC contains hardened PS Gigabit Ethernet MAC (GEM) controllers. The UltraZed-EV SOM takes advantage of one of the available PS GEM controllers to provide RGMII Ethernet signalling to the JX3 connector. The Marvell 88E1512 Ethernet PHY device is used to implement the interface. The 10/100/1000 Ethernet PHY connects to the Zynq UltraScale+ MPSoC device through Bank 502.

The physical RJ45 connector and magnetics is not populated on the UltraZed-EV SOM. The SOM is designed to have the physical RJ45 connector and magnetics reside on the end-user carrier card. The RJ45 connector signals are connected to the JX3 Micro Header. The table below shows the connections of these signals to the JX3 Micro Header.

Signal Name	JX3 Pin
ETH_MD1_P	JX3.B14
ETH_MD1_N	JX3.B15
ETH_MD2_P	JX3.A15
ETH_MD2_N	JX3.A16
ETH_MD3_P	JX3.B17
ETH_MD3_N	JX3.B18
ETH_MD4_P	JX3.A18
ETH_MD4_N	JX3.A19
ETH_PHY_LED0	JX3.C20
ETH_PHY_LED1	JX3.C18

Table 9 – 10/100/1000 Ethernet JX3 Pin Assignments

The next table shows the pin assignments to Bank 502 of the Zynq UltraScale+ MPSoC device for the 10/100/1000 Ethernet Port.

Ethernet PHY Signals	MPSoC Pin
MIO77_GEM3_MDIO	E25
MIO76_GEM3_MDC	E28
MIO74_GEM3_RX_D3	E29
MIO73_GEM3_RX_D2	E30
MIO72_GEM3_RX_D1	E27
MIO71_GEM3_RX_D0	D30
MIO75_GEM3_RX_CTL	D29
MIO70_GEM3_RX_CLK	D26
MIO68_GEM3_TX_D3	C29
MIO67_GEM3_TX_D2	C28
MIO66_GEM3_TX_D1	C27
MIO65_GEM3_TX_D0	D25
MIO69_GEM3_TX_CTL	D27
MIO64_GEM3_TX_CLK	B30
GEM3_RST_N	N/C

Table 10 – 10/100/1000 Ethernet MPSoC Pin Assignments

The GEM3 peripheral is used on the PS, connected through MIO [64-77] in MIO Bank 502. The Ethernet Reset signal is active-low and connected to the I/O expander via Port 2, P2_GEM3_RST_N. Either of the push button resets, **PS_POR_B** or **PS_SRST_B** will also generate the active-low Ethernet Reset signal.

The UltraZed-EV SOM also contains an active-low Ethernet PHY interrupt signal that is connected to the I/O expander via Port 3, **P3_GEM3_INT_N**. The pin is an interrupt output and interrupts will be asserted low to the I/O Expander. Utilization of the interrupt requires register access to the Gigabit Ethernet PHY as well as a software polling mechanism for the I/O Expander to identify interrupt activity.

A high-level block diagram of the 10/100/1000 Ethernet interface is shown in the following figure.

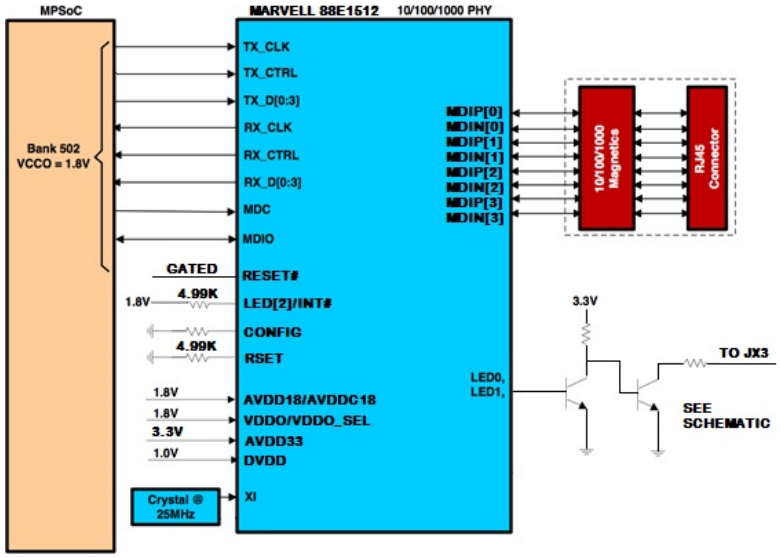

Figure 6 – 10/100/1000 Ethernet Interface Implementation

2.6.1 Ethernet PHY LEDs

On board the end-user carrier card or within the RJ45 Ethernet Jack on the end-user carrier card will be implemented two Ethernet PHY controlled LEDs. These LEDs can be programmed in the Marvell 88E1512 Ethernet PHY to create various link signals. Avnet's out of the box design sets the LED programming to LINK SPEED and ACTIVITY. Care must be taken when implementing LEDs on an end-user carrier card as the signals being driven onto the JX3 connector by the Ethernet PHY are at 3.3V. This voltage should be, buy may not be enough to illuminate the LEDs in an RJ45 jack or other on-board LED circuitry. A recommendation for the end-user carrier card would be to implement a circuit similar to those that exists on the UltraZed-EV Carrier Card.

2.6.2 FBVB900 Device Package Delay Compensation for 10/100/1000 Ethernet Interface

The Zynq UltraScale+ MPSoC device package delay is accommodated for in the layout of the Gigabit Ethernet signal trace lengths. The average of min and max values for package delay is utilized to compensate for the flight time caused by the delay associated with this package.

2.7 I2C I/O Expander

The UltraZed-EV SOM uses an **ON Semiconductor PCA9654E** (**16-pin TSSOP**) I2C and SMBUS Low- Power I/O Expander. The Zynq UltraScale+ MPSoC controller required for I2C is named I2C1 and it exists at MIO [25:24].

IO Name	TRM Signal Name	Net Name
PS_MIO24	SCL_OUT	MIO24_I2C1_SCL
PS_MIO25	SDA_OUT	MIO25_I2C1_SDA

Table 11 – I2C1 TRM Pin Mapping

Each of the ports of the I2C I/O Expander represents functions different control functions like resets and interrupts. The following tables describes the connections and functionality of the ports of the I2C I/O Expander.

I/O Expander Name	I/O Expander Pin	Function	Net Name
A0	1	ADDRESS	GND
A1	2	ADDRESS	GND
A2	3	ADDRESS	GND
P0	4	P-PORT	P0_EMMC0_RST_N
P1	5	P-PORT	P1_USB0_RST_N
P2	6	P-PORT	P2_GEM3_RST_N
P3	7	P-PORT	P3_GEM3_INT_N
GND	8	GROUND	GND
P4	9	P-PORT	P4_I2CMUX_INT_N
P5	10	P-PORT	P5_PMBUS_ALERT_N
P6	11	P-PORT	P6_I2CMUX_RST_N
P7	12	P-PORT	P7_CC_RST_N
INT_N	13	INTERRUPT	MIO23_INT_N
SCL	14	SERIAL CLOCK	MIO24_I2C1_SCL
SDA	15	SERIAL DATA	MIO25_I2C1_SDA
VCC	16	POWER	+VCCO_PSIO

Table 12 – ON Semiconductor PCA9654E Pin Mapping

I/O Name	Function	Direction	Active-State	Net Name
P0	eMMC Soft Reset	OUTPUT	LOW	P0_EMMC0_RST_N
P1	USB 2.0 ULPI PHY Soft Reset	OUTPUT	LOW	P1_USB0_RST_N
P2	Gigabit Ethernet PHY Soft Reset	OUTPUT	LOW	P2_GEM3_RST_N
P3	Gigabit Ethernet Interrupt	OUTPUT	LOW	P3_GEM3_INT_N
P4	2-Ch I2C Switch/Mux Interrupt	INPUT	LOW	P4_I2CMUX_INT_N
P5	PMBUS Alert #	INPUT	LOW	P5_PMBUS_ALERT_N
P6	2-Ch I2C Switch/Mux Soft Reset	OUTPUT	LOW	P6_I2CMUX_RST_N
P7	Carrier Card Reset	OUTPUT	LOW	P7_CC_RST_N

Table 13 – IO Expander Pin Functions and Definitions

The following figure describes the addressing required to access the I2C I/O Expander. The address is programmable based on the address inputs AD[2:0]. On the UltraZed-EV SOM these address inputs are set to GND which corresponds to an address of 0x40. Please see the appropriate device datasheet for further details regarding accessing this device.

Address Input			Slave Address							
AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	HEX
GND	GND	GND	0	1	0	0	0	0	0	40h

Figure 7 – I2C I/O Expander Addressing

2.8 I2C Switch/Multiplexer

The UltraZed-EV SOM uses an NXP PCA9543A (14-pin TSSOP) Serial Bus Switch/MUX with Interrupt. The Zynq UltraScale+ MPSoC controller required for I2C is named I2C1 and it exists at MIO [25:24].

IO Name	TRM Signal Name	Net Name
PS_MIO24	SCL_OUT	MIO24_I2C1_SCL
PS_MIO25	SDA_OUT	MIO25_I2C1_SDA

Table 14 – I2C1 TRM Pin Mapping

The I2C Switch/MUX allows for selection of control of the end-user carrier card two-wire serial interface or alternatively one could select the PMBUS interface that is tied to the UltraZed-EV SOM main multi-output power supplies as well as any device that may exist on the end-user carrier card PMBUS through the JX1 connector. The two-wire serial interface on the Zynq UltraScale+ MPSoC is used as the serial source for to the PCA9543A.The following table shows the connections to the PCA9543A device.

SWITCH/MUX Name	SWITCH/MUX Pin	Function	Net Name
A0	1	ADDRESS	GND
A1	2	ADDRESS	GND
RESET_N	3	RESET	P6_I2CMUX_RST_N
INT0_N	4	INTERRUPT0	CC_INT_N
SD0	5	SERIAL DATA0	CC_SDA
SC0	6	SERIAL CLOCK0	CC_SCL
GND	7	GROUND	GND
INT1_N	8	INTERRUPT1	N/C
SD1	9	SERIAL DATA1	PMBUS_SDA
SC1	10	SERIAL CLOCK1	PMBUS_SCL
INT_N	11	INTERRUPT	P4_I2CMUX_INT_N
SCL	12	SERIAL CLOCK	MIO24_I2C1_SCL
SDA	13	SERIAL DATA	MIO25_I2C1_SDA
VCC	14	POWER	+2.5V

Table 15 – NXP PCA9543A Pin Mapping

The following table should provide a clearer understanding of how the PCA9543A is expected to function in the system.

Switch/MUX Channel	Usage	Notes
Master Channel (SDA/SCL/INT)	This channel is connected to the PS I2C port, MIO [24:25] and operated at 1.8V. The master **INT_N** output is connected to the P4 port of the I2C 8-bit I/O expander.	Pulled-up to 1.8V on the SOM
Slave Channel 0 (SD0/SC0/INT0)	This channel is connected to the JX3 connector (**CC_SDA**, **CC_SCL**, and **CC_INT_N** signals) to allow slave I2C devices on the Carrier Card to be virtually placed on the same PS I2C bus (MIO [24:25]) as the I2C devices on the UltraZed-EV SOM so that software can use a single PS I2C core to communicate with all I2C devices in the system.	Pulled-up to 1.8V, 2.5V, or 3.3V on the Carrier Card
Slave Channel 1 (SD1/SC1/INT1)	This channel is connected to the PMBus (**PMBUS_SDA** and **PMBUS_SCL** signals) of the UltraZed-EV SOM PMBus voltage regulators and used to control all PMBus voltage regulators on the UltraZed-EV SOM as well as the Carrier Card (the PMBus is connected to the Carrier Card via JX1 connector). This feature will allow the PS to control/monitor the PMBus voltage regulators on the UltraZed-EV SOM as well as the Carrier Card for the purpose of power management and/or measurements.	Pulled-up to 3.3V on the SOM The unused slave channel 1 **INT1_N** input must be pulled up to the VCC (2.5V) rail.

Table 16 – I2C MUX/SWITCH Channel Usage

The following figure describes the addressing required to access the I2C Switch/MUX. The address is hardware selectable based on the address inputs A[1:0]. On the UltraZed-EV SOM these address inputs are set to GND which corresponds to an address of 0xE0. Please see the appropriate device datasheet for further details regarding transactions to and from this device.

Pin connectivity		Address of PCA9543A								Address byte value		7-bit hexadecimal address without R/W
A1	A0	A6	A5	A4	A3	A2	A1	A0	R/W	Write	Read	
V_{SS}	V_{SS}	1	1	1	0	0	0	0	-	E0h	E1h	70h

Figure 8 – I2C Switch/MUX Addressing

2.8.1 End-User Carrier Card I2C Interface

The UltraZed-EV SOM provides a master two-wire serial bus (**CC_SDA**, **CC_SCL**, and **CC_INT_N**) to the end-user carrier card via the JX3 connector so that software can communicate with all I2C devices on the UltraZed-EV SOM as well as the slave I2C devices on the end-user carrier card using a single two-wire serial interface.

The end-user carrier card two-wire serial interface is connected to channel 0 of the 2-channel switch/mux device. End-user carrier cards can drive the **INT0_N** of the channel 0 via **CC_INT_N**, if they so desire. The **CC_INT_N** (an **active low** signal) is not specific to the I2C interface and can be used as a general-purpose interrupt from end-user carrier cards to the UltraZed-EV SOM. If not used, the **CC_INT_N** signal is to be pulled up to 1.8V, 2.5V, or 3.3V on the Carrier Card. Since channel 0 I2C bus is dedicated to the end-user carrier card, two-wire serial devices with any address can reside on this bus without conflicting with the I2C devices on the UltraZed-EV SOM.

Switch/MUX Name	Switch/MUX Pin	Function	Net Name	JX3 Connector
INT0_N	4	INTERRUPT0	CC_INT_N	JX3.D19
SD0	5	SERIAL DATA0	CC_SDA	JX3.C1
SC0	6	SERIAL CLOCK0	CC_SCL	JX3.A1

Table 17 – Carrier Card I2C Net Mapping

2.8.2 PMBUS Interface

A PMBus is used on the UltraZed-EV SOM to program/control/monitor all on-board PMBus voltage regulators. The UltraZed-EV SOM has access to the end-user carrier card PMBus signals via the JX1 connector (**PMBUS_SDA, PMBUS_SCL, and P5_PMBUS_ALERT_N** signals).

After the initial programming of all PMBus voltage regulators, the UltraZed-EV SOM can drive the PMBus (via channel 1 of the I2C switch/mux and P5 port of the I2C 8-bit I/O expander) in order to control/monitor the PMBus voltage regulators on the UltraZed-EV SOM for the purpose of power management and/or measurements. If the PMBus is implemented on the end-user carrier card, the UltraZed-EV SOM PMBus can monitor/control the end-user carrier card PMBus voltage regulators as well.

NOTE: If not used, the UltraZed-EV SOM PMBus interface must be left unconnected on the end-user carrier cards so that the UltraZed-EV SOM can still control/monitor its on-board PMBus regulators.

PMBUS Name	JX1 Connector
PMBUS_SDA	JX1.B1
PMBUS_SCL	JX1.B2
P5_PMBUS_ALERT_N	JX1.A1

Table 18 – PMBUS JX1 Connector Mapping

The following figure shows how the PMBus will be connected on the UltraZed-EV SOM and the UltraZed-EV Carrier Card from Avnet.

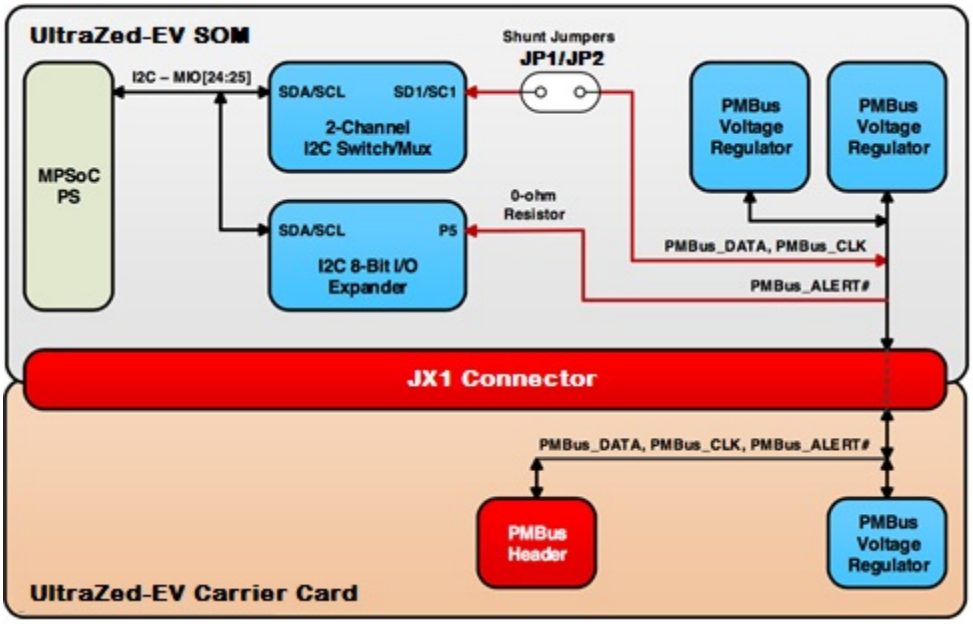

Figure 9 – PMBUS Connections

2.9 I2C EEPROM

The UltraZed-EV SOM uses an **Atmel AT34C02D-MAHM** 2-Kbit I2C EEPROM device. The Zynq UltraScale+ MPSoC controller required for serial access is named I2C1 and it exists at MIO [25:24].

IO Name	TRM Signal Name	Net Name
PS_MIO24	SCL_OUT	MIO24_I2C1_SCL
PS_MIO25	SDA_OUT	MIO25_I2C1_SDA

Table 19 – I2C1 TRM Pin Mapping

The following table describes the connections to the I2C EEPROM

EEPROM Name	EEPROM Pin	Function	Net Name
A0	1	ADDRESS INPUT	GND
A1	2	ADDRESS INPUT	GND
A2	3	ADDRESS INPUT	GND
VSS	4	GROUND	GND
SDA	5	SERIAL ADDR/DATA	MIO25_I2C1_SDA
SCL	6	SERIAL CLOCK	MIO24_I2C1_SCL
WP	7	WRITE PROTECT	GND
VCC	8	POWER	+VCCO_PSIO

Table 20 – Atmel AT34C02D Pin Mapping

The following figure describes the addressing required to access the I2C EEPROM. The address is hardware selectable based on the address inputs A[2:0]. On the UltraZed-EV SOM these address inputs are set to GND which corresponds to an address of 0xA0. Please see the appropriate device datasheet for further details regarding transactions to and from this device.

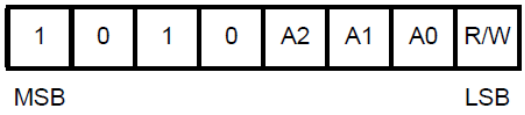

Figure 10 – I2C EEPROM Addressing

2.10 PS General Purpose Interrupt

The UltraZed-EV SOM contains a general purpose interrupt IO that is attached to PS_MIO[23]. This interrupt signal will contain a pull-up to +VCCO_PSIO. The interrupt output (INT#) of the ON Semiconductor PCA9654E device is connected to the PS_MIO[23] pin.

IO Name	Net Name
PS_MIO23	MIO23_INT_N

Table 21 – PS Interrupt Pin Mapping

2.11 User I/O

2.11.1 PS MIO User Pins

The UltraZed-EV SOM provides 26 end-user PS MIO pins directly from Bank 501 of the Zynq UltraScale+ MPSoC to the JX3 Connector. The 26 PS MIO pins connect to the Zynq UltraScale+ Processor Sub-System for the implementation of peripherals such as USB, SPI, SDIO, CAN, UART, and I2C. These I/O pins can also be used as general purpose I/O to connect push buttons, LEDs and/or switches to the UltraZed-EV SOM from the end-user carrier card.

The VCCO for Bank 501 is set via pin D18 on the JX3 connector. VCCO for Bank 501 can be set to 1.8V, 2.5V, and 3.3V depending on what peripheral/circuitry may need to be implemented on the end-user carrier card.

NOTE: The Bank 501 PS MIO interface to the JX3 connector is provided in a master table that documents all of the JX Connections to the Zynq UltraScale+ MPSoC.

2.11.2 PL IO User Pins

The UltraZed-EV SOM provides 24 user PL IO pins from Bank 47, 24 user PL IO pins from Bank 48, 52 user PL IO pins from bank 64, and 52 user PL IO pins from Bank 65 of the Zynq UltraScale+ MPSoC. The 152 PL IO pins on the UltraZed-EV SOM connect to the Zynq UltraScale+ Programmable Logic Sub-System for user implementation of most any feasible interface.

The PL IO pins are routed with matched lengths to each of the JX connectors by the Bank they are associated with. The matched pairs, noted by “DP” in the net name may be used as either single ended I/O or differential pairs depending on the end users design requirements.

Bank 47 and Bank 48 are high density banks that each contain 24 single ended signals. The I/O supply voltage for the high density banks are +VCCO_HD_47 and +VCCO_HD_48. The supply voltage range for high density banks is +1.2V to +3.3V.

Bank 64 and Bank 65 IO are high performance banks that contain a mix of single ended signals and differential pairs. The I/O supply voltage for Bank 64 and Bank 65 can be individually controlled. The I/O supply voltages for Bank 64 and Bank 65 are +VCCO_HP_64 and +VCCO_HP_65. The I/O supply voltage range for these high performance banks is +1.0V to +1.8V.

Use of these signals for various interfaces depends on the bank voltages assigned. The end-user carrier card is responsible for providing the appropriate bank voltages to the VCCO pins for Bank 47, Bank48, Bank 64, and Bank 65 depending on what interfaces are being implemented.

PL I/O Bank 64 and Bank 65 contain 52 I/O per bank capable of up to 24 differential pairs per bank with additional single ended signals. Differential LVDS pairs on a -1 speed grade device are capable of 1250Mbps of DDR data (625Mbps SDR data). Each differential pair from Bank 64 and Bank 65 is isolated by a power or ground pin on the JX connector. Additionally, 4 differential pairs per bank I/O can used to connect clock inputs. These differential clock inputs are identified with a *_GC_* in the net name.

It is recommended that any custom interface be designed and run through the Vivado tool suite that supports the desire device that is to be implemented for a sanity check on place and route and timing closure in advance of end-user carrier card manufacturing.

NOTE: The Bank 47, Bank48, Bank 64, and Bank 65 PL IO interface to the JX1 and JX2 connectors is provided in a master table that documents all of the JX Connections to the Zynq UltraScale+ MPSoC.

2.12 Clock Sources

The UltraZed-EV SOM connects a dedicated 33.3333 MHz clock source to the Zynq UltraScale+ MPSoC PS to act as a system reference clock. An ABRACON ASDMB-33.333MHZ-LC-T or similar oscillator with 40-ohm series termination is used.

Zynq UltraScale+ MPSoC provides a built-in Real-Time Clock (RTC). A 32.768 KHz crystal is connected to the PS bank 503 **PS_PADI** and **PS_PADO** pins for the RTC. The on-chip RTC will use the **VCC_PSBATT** pin (provided by the end-user carrier card via JX3 connector) for the backup battery. Carrier Cards will drive the **VCC_PSBATT** pin with a 1.5V battery.

MIO Name	Package Pin Number	Net Name	JX3 Connector
PS_PADI	M21	PS_PADI	-
PS_PADO	N21	PS_PADO	-
VCC_PSBATT	U20	PS_VBATT	JX3.C21

Table 22 – RTC Crystal Pin Assignments

2.13 Control Signal Sources

2.13.1 Power-On Reset (PS_POR_B) and Carrier Card Reset (CC_RESET_OUT_N)

The Zynq UltraScale+ MPSoC PS supports an external power-on reset signal. The power-on reset is the master reset of the entire chip. This signal resets every register in the device capable of being reset. On UltraZed-EV SOM, this signal is labelled **PS_POR_B** and it is connected to push button, **SW3**. To stall Zynq UltraScale+ MPSoC boot-up, this signal should be held low. No other signal (**PS_SRST_B**, **PROGRAM_B**, or **INIT_B**) is capable of doing this as in other Xilinx FPGA architectures. Toggling **SW3** illuminates the **POR_RST_B** LED, **D4**.

NOTE: By default, the **SW3** push button is **NOT** populated on production level UltraZed-EV SOMs.

The power-on-reset, **PS_POR_B**, is capable of resetting the end-user carrier card thru an open drain signal on the JX1 connector, **CC_RESET_OUT_N**. The UltraZed-EV SOM end-user is also capable of issuing a soft reset, **P7_CC_RST_N**, to the end-user carrier card via an on board two-wire serial interface. The soft reset is capable of resetting the end-user carrier card thru the same open drain signal on the JX1 connector (Pin C46), **CC_RESET_OUT_N**. The end-user carrier card is required to pull-up the **CC_RESET_OUT_N** signal to a voltage level suitable to the circuitry on the end-user carrier card that requires this reset signal.

The active low reset, **P7_CC_RST_N**, is assigned to Port 7 of the ON Semiconductor PCA9654 I/O expander. The I/O expander is attached to an I2C peripheral on the Zynq UltraScale+ device. For further information on the I/O expander and its connections, please locate the I/O expander section within this hardware user guide.

NOTE: A custom end-user carrier card should design the on-board power solution to account for the bring up time of the individual power supplies and devise a method to ensure that power is valid prior to the booting of the Zynq UltraScale+ device. The custom end-user carrier card should use the SOM_PG_OUT signal to enable the on-board power supplies.

NOTE: The time required for all power rails to be stable is approximately 400ms.

2.13.2 PS_PROG_B, PS_DONE, PS_INIT_B, PUDC_B, POR_OVERRIDE, and ERROR

PS_INIT_B, PS_PROG_B and **PUDC_B** have pull-up resistors to appropriate voltages applied.

The **PS_PROG_B** signal is capable of being activated by push button, **SW1**. The **PUDC_B** and **POR_OVERRIDE** signals are pulled high by default or low through resistor placements (BOM modification).

NOTE: By default, the **SW1** push button is **NOT** populated on production level UltraZed-EV SOMs.

There are several status LEDs on the UltraZed-EV SOM. There is a blue DONE LED indicator. When configuration is complete **PS_DONE** will be pulled high illuminating the blue DONE LED. There is a green ERROR STATUS LED indicator and a red ERROR OUT LED indicator that will illuminate indicating that configuration did not complete properly via signalling from the **PS_ERROR_STATUS** and **PS_ERROR_OUT** pins on the Zynq UltraScale+ MPSoC**.**

2.13.3 Processor Subsystem Reset (PS_SRST_B) and SOM Reset (SOM_RESET_IN_N)

The system reset, labelled **PS_SRST_B**, resets the processor as well as erases all debug configurations.

On the UltraZed-EV SOM, this signal is labelled **PS_SRST_B** and it is connected to push button, **SW4**. The UltraZed-EV SOM is also capable of being issued an external system reset from the end-user carrier card via the JX1 Connector (Pin A2) signal **SOM_RESET_IN_N**.

The active-low external system resets, **SW4** or **SOM_RESET_IN_N** allows the user to reset all of the functional logic within the device without disturbing the debug environment. Toggling **SW4** should illuminate the **POR_RST_B** LED, **D4**. The **SOM_RESET_IN** signal should have a minimum pulse width of 3 PS_CLK cycles (90ns).

NOTE: By default, the **SW4** push button is **NOT** populated on production level UltraZed-EV SOMs.

NOTE: This signal cannot be asserted while the boot ROM is executing following a power-on reset (**PS_POR_B**). If **PS_SRST_B** is asserted while the boot ROM is running through a power-on reset sequence it will trigger a lock-down event preventing the boot ROM from completing. To recover from lockdown the device either needs to be power cycled or **PS_POR_B** needs to be asserted.

2.14 Expansion Headers

2.14.1 Micro Headers

The UltraZed-EV SOM features three Micro Headers for connection to end-user carrier cards. The three Micro Headers consist of two 200-pin connectors and one 120-pin connector.

The JX1 and JX2 connectors are the main interface to PL signals for the end-user carrier card. The JX1 and JX2 connectors also provide access to high performance GTH MGTs, dedicated JTAG signals, various power rails, system monitor signals, PMBUS interface, and control signals. The JX3 connector interfaces to peripheral interfaces such as the GTR MGTs, Gigabit Ethernet, USB 2.0, and Bank 501 PS MIO. The JX3 connector also contains various power rails, the end-user carrier card I2C interface, as well as voltage sense signals for the end-user carrier card power supply feedbacks.

The connectors are Samtec 0.8mm SEARAY Ultra-High Density Open-Pin-Field with 200 Positions or 120 Positions situated in Quad-Rows. These connectors have two stack heights, 7mm and 10mm, making it easy to connect to a variety of expansion or system boards depending on the end-user requirements. By default, the mating solution with the UltraZed-EV Carrier Card is set to 7mm. Each pin is capable of carrying 1400mA of current and support I/O speeds in excess of what Zynq UltraScale+ MPSoC can deliver with performance at 39Gbps @ 7mm mated stack heights.

The tables listed below show the connection types to the JX Micro Headers.

Micro Header JX1			
Interface	**Signal Name**	**Source**	**Pins**
PL	Bank 64 Single Ended I/Os	Zynq UltraScale+ Bank 64	4
	Bank 65 Single Ended I/Os	Zynq UltraScale+ Bank 65	4
	Bank 64 Differential Pair I/Os	Zynq UltraScale+ Bank 64	48
	Bank 65 Differential Pair I/Os	Zynq UltraScale+ Bank 65	48
JTAG	JTAG_TMS	Zynq UltraScale+ Bank 503	4
	JTAG_TDI		
	JTAG_TCK		
	JTAG_TDO		
Power	GND	Carrier Card	62
	VIN		8
	VCCO_HP_64		3
	VCCO_HP_65		3
	VCCO_HD_47		3
	VCCO_HD_48		3
Control	PMBus	Carrier Card or UltraZed-EV SOM	3
	SOM_PG_OUT	UltraZed-EV SOM	1
	SOM_RESET_IN_N	Carrier Card	1
	CC_RESET_OUT_N	UltraZed-EV SOM	1
	SYSMON_*	Carrier Card	4
		Total	**200**

Table 23 – Micro Header JX1 Summary

Micro Header JX2			
Interface	**Signal Name**	**Source**	**Pins**
PL	Bank 47 Single Ended I/Os	Zynq UltraScale+ Bank 47	24
	Bank 48 Single Ended I/Os	Zynq UltraScale+ Bank 48	24
	GTH[15:0] and REFCLK[7:0]	Zynq UltraScale+ Quads 227-224	80
Power	MGTAVCC	Carrier Card	6
	MGTAVTT		6
	MGTVCAUX		2
	GND		58
		Total	**200**

Table 24 – Micro Header JX2 Summary

Micro Header JX3			
Interface	**Signal Name**	**Source**	**Pins**
GTR	Bank 505 Differential Pair I/Os	Zynq UltraScale+ Bank 505	24
PS	Bank 501 PS MIO	Zynq UltraScale+ Bank 501	26
Comm	USB2.0 PHY Interface	UltraZed-EV SOM	4
	Gigabit Ethernet PHY Interface		10
	CC I2C BUS		3
Power	GND	Carrier Card	36
	MGTRAVCC		3
	MGTRAVTT		2
	VCCO_PSIO_501		1
	PS_VBATT		1
	USB_OTG_VBUS		1
	Voltage Feedback Sense Pins	UltraZed-EV SOM	9
		Total	**120**

Table 25 – Micro Header JX3 Summary

2.14.2 JX Connector Master Table

The following tables list the UltraZed-EV SOM JX Connectors connections in master tables targeting each connector.

Zynq Pin Number	UltraZed-EV Net Name	JX1 Pin Number		UltraZed-EV Net Name	Zynq Pin Number
L19	**JTAG_TCK**	D1	C1	**JTAG_TMS**	L21
M20	**JTAG_TDO**	D2	C2	**JTAG_TDI**	L20
AE11	**VCCO_HP_65**	D3	C3	**VCCO_HP_65**	AH10
AG7	**VCCO_HP_65**	D4	C4	HP_DP_01_P	AE18
AG18	HP_DP_00_P	D5	C5	HP_DP_01_N	AF18
AH18	HP_DP_00_N	D6	C6	**GND**	**N/A**
N/A	**GND**	D7	C7	HP_DP_05_P	AA16
AC17	HP_DP_04_P	D8	C8	HP_DP_05_N	AB16
AC18	HP_DP_04_N	D9	C9	**GND**	**N/A**
N/A	**GND**	D10	C10	HP_DP_09_P	AC16

Zynq Pin Number	UltraZed-EV Net Name	JX1 Pin Number		UltraZed-EV Net Name	Zynq Pin Number
AG16	HP_DP_08_P	D11	C11	HP_DP_09_N	AD16
AH16	HP_DP_08_N	D12	C12	GND	N/A
N/A	GND	D13	C13	GND	N/A
N/A	GND	D14	C14	HP_DP_13_GC_P	AD17
AF16	HP_DP_12_GC_P	D15	C15	HP_DP_13_GC_N	AE17
AF17	HP_DP_12_GC_N	D16	C16	GND	N/A
N/A	GND	D17	C17	GND	N/A
N/A	GND	D18	C18	HP_DP_17_P	AG13
AK13	HP_DP_16_P	D19	C19	HP_DP_17_N	AH13
AK12	HP_DP_16_N	D20	C20	GND	N/A
N/A	GND	D21	C21	HP_DP_21_P	AE14
AC14	HP_DP_20_P	D22	C22	HP_DP_21_N	AE13
AD14	HP_DP_20_N	D23	C23	GND	N/A
N/A	GND	D24	C24	HP_DP_25_P	AJ10
AF10	HP_DP_24_P	D25	C25	HP_DP_25_N	AK10
AG10	HP_DP_24_N	D26	C26	GND	N/A
N/A	GND	D27	C27	HP_DP_29_P	AK7
AJ5	HP_DP_28_P	D28	C28	HP_DP_29_N	AK6
AK5	HP_DP_28_N	D29	C29	GND	N/A
N/A	GND	D30	C30	GND	N/A
N/A	GND	D31	C31	HP_DP_33_GC_P	AH6
AG6	HP_DP_32_GC_P	D32	C32	HP_DP_33_GC_N	AJ6
AG5	HP_DP_32_GC_N	D33	C33	GND	N/A
N/A	GND	D34	C34	GND	N/A
N/A	GND	D35	C35	HP_DP_37_P	AJ4
AJ11	HP_DP_36_P	D36	C36	HP_DP_37_N	AK4
AK11	HP_DP_36_N	D37	C37	GND	N/A
N/A	GND	D38	C38	HP_DP_41_P	AG11
AH9	HP_DP_40_P	D39	C39	HP_DP_41_N	AH11
AJ9	HP_DP_40_N	D40	C40	GND	N/A
N/A	GND	D41	C41	HP_DP_45_P	AK3
AH3	HP_DP_44_P	D42	C42	HP_DP_45_N	**AK2**
AH2	HP_DP_44_N	D43	C43	VCCO_HD_48	E16
D13	VCCO_HD_47	D44	C44	VCCO_HD_48	H15
G12	VCCO_HD_47	D45	C45	VCCO_HD_48	N/A
N/A	VCCO_HD_47	D46	C46	CC_RESET_OUT_N	N/A
N/A	SOM_PG_OUT	D47	C47	GND	N/A
N/A	GND	D48	C48	SYSMON_DX_N	V14
U14	SYSMON_V_N	D49	C49	SYSMON_DX_P	V15
T15	SYSMON_V_P	D50	C50	VIN	N/A
N/A	PMBus_SDA	B1	A1	PMBus_ALERT_N	N/A
N/A	PMBus_SCL	B2	A2	SOM_RESET_IN_N	N/A
AC15	VCCO_HP_64	B3	A3	VCCO_HP_64	AG17
AF14	VCCO_HP_64	B4	A4	HP_DP_03_P	AD19
AH17	HP_DP_02_P	B5	A5	HP_DP_03_N	AE19
AJ17	HP_DP_02_N	B6	A6	GND	N/A
N/A	GND	B7	A7	HP_DP_07_P	AK17

Zynq Pin Number	UltraZed-EV Net Name	JX1 Pin Number		UltraZed-EV Net Name	Zynq Pin Number
AJ16	HP_DP_06_P	B8	A8	HP_DP_07_N	AK18
AK16	HP_DP_06_N	B9	A9	GND	N/A
N/A	GND	B10	A10	HP_DP_11_P	AJ15
AJ14	HP_DP_10_P	B11	A11	HP_DP_11_N	AK15
AK14	HP_DP_10_N	B12	A12	GND	N/A
N/A	GND	B13	A13	GND	N/A
N/A	GND	B14	A14	HP_DP_15_GC_P	AF15
AG14	HP_DP_14_GC_P	B15	A15	HP_DP_15_GC_N	AG15
AH14	HP_DP_14_GC_N	B16	A16	GND	N/A
N/A	GND	B17	A17	GND	N/A
N/A	GND	B18	A18	HP_DP_19_P	AA15
AA13	HP_DP_18_P	B19	A19	HP_DP_19_N	AB15
AB13	HP_DP_18_N	B20	A20	GND	N/A
N/A	GND	B21	A21	HP_DP_23_P	AD15
AA14	HP_DP_22_P	B22	A22	HP_DP_23_N	AE15
AB14	HP_DP_22_N	B23	A23	GND	N/A
N/A	GND	B24	A24	HP_DP_27_P	AF12
AF8	HP_DP_26_P	B25	A25	HP_DP_27_N	AF11
AF7	HP_DP_26_N	B26	A26	GND	N/A
N/A	GND	B27	A27	HP_DP_31_P	AK9
AF6	HP_DP_30_P	B28	A28	HP_DP_31_N	AK8
AF5	HP_DP_30_N	B29	A29	GND	N/A
N/A	GND	B30	A30	GND	N/A
N/A	GND	B31	A31	HP_DP_35_GC_P	AG8
AH7	HP_DP_34_GC_P	B32	A32	HP_DP_35_GC_N	AH8
AJ7	HP_DP_34_GC_N	B33	A33	GND	N/A
N/A	GND	B34	A34	GND	N/A
N/A	GND	B35	A35	HP_DP_39_P	AF3
AJ2	HP_DP_38_P	B36	A36	HP_DP_39_N	AF2
AJ1	HP_DP_38_N	B37	A37	GND	N/A
N/A	GND	B38	A38	HP_DP_43_P	AE9
AH12	HP_DP_42_P	B39	A39	HP_DP_43_N	AE8
AJ12	HP_DP_42_N	B40	A40	GND	N/A
N/A	GND	B41	A41	HP_DP_47_P	AG4
AG1	HP_DP_46_P	B42	A42	HP_DP_47_N	AG3
AH1	HP_DP_46_N	B43	A43	VIN	N/A
N/A	VIN	B44	A44	HP_SE_04	AF1
AF13	HP_SE_00	B45	A45	HP_SE_05	AH4
AG19	HP_SE_01	B46	A46	VIN	N/A
N/A	VIN	B47	A47	HP_SE_06	AG9
AC13	HP_SE_02	B48	A48	HP_SE_07	AE10
AC19	HP_SE_03	B49	A49	VIN	N/A
N/A	VIN	B50	A50	VIN	N/A

Table 26 – JX1 Connector Master Table

Zynq Pin Number	UltraZed-EV Net Name	JX2 Pin Number		UltraZed-EV Net Name	Zynq Pin Number
N/A	GND	D1	C1	MGTAVCC	M8
B15	HD_SE_00_P	D2	C2	MGTAVCC	P8
A15	HD_SE_00_N	D3	C3	HD_SE_01_P	A17
A10	MGTAVCC	D4	C4	HD_SE_01_N	A16
G16	HD_SE_04_GC_P	D5	C5	GND	N/A
G15	HD_SE_04_GC_N	D6	C6	HD_SE_05_GC_P	E15
C10	MGTAVCC	D7	C7	HD_SE_05_GC_N	D15
D16	HD_SE_08_P	D8	C8	GND	N/A
C16	HD_SE_08_N	D9	C9	HD_SE_09_P	J15
F8	MGTAVCC	D10	C10	HD_SE_09_N	J14
B12	HD_SE_12_P	D11	C11	GND	N/A
A12	HD_SE_12_N	D12	C12	HD_SE_13_P	A14
H8	MGTAVCC	D13	C13	HD_SE_13_N	A13
D14	HD_SE_16_GC_P	D14	C14	GND	N/A
C13	HD_SE_16_GC_N	D15	C15	HD_SE_17_GC_P	E14
N/A	GND	D16	C16	HD_SE_17_GC_N	E13
D12	HD_SE_20_P	D17	C17	GND	N/A
C12	HD_SE_20_N	D18	C18	HD_SE_21_P	H13
N/A	GND	D19	C19	HD_SE_21_N	H12
D6	GTH0_TX_P	D20	C20	GND	N/A
D5	GTH0_TX_N	D21	C21	GTH0_RX_P	D2
N/A	GND	D22	C22	GTH0_RX_N	D1
B6	GTH2_TX_P	D23	C23	GND	N/A
B5	GTH2_TX_N	D24	C24	GTH2_RX_P	B2
N/A	GND	D25	C25	GTH2_RX_N	B1
D10	GTH_REFCLK0_P	D26	C26	GND	N/A
D9	GTH_REFCLK0_N	D27	C27	GTH_REFCLK1_P	B10
N/A	GND	D28	C28	GTH_REFCLK1_N	B9
G8	GTH5_TX_P	D29	C29	GND	N/A
G7	GTH5_TX_N	D30	C30	GTH5_RX_P	G4
N/A	GND	D31	C31	GTH5_RX_N	G3
E8	GTH7_TX_P	D32	C32	GND	N/A
E7	GTH7_TX_N	D33	C33	GTH7_RX_P	E4
N/A	GND	D34	C34	GTH7_RX_N	E3
P6	GTH8_TX_P	D35	C35	GND	N/A
P5	GTH8_TX_N	D36	C36	GTH8_RX_P	N4
N/A	GND	D37	C37	GTH8_RX_N	N3
L4	GTH10_TX_P	D38	C38	GND	N/A
L3	GTH10_TX_N	D39	C39	GTH10_RX_P	K2
N/A	GND	D40	C40	GTH10_RX_N	K1
L8	GTH_REFCLK4_P	D41	C41	GND	N/A
L7	GTH_REFCLK4_N	D42	C42	GTH_REFCLK5_P	J8
N/A	GND	D43	C43	GTH_REFCLK5_N	J7
V6	GTH13_TX_P	D44	C44	GND	N/A
V5	GTH13_TX_N	D45	C45	GTH13_RX_P	U4
N/A	GND	D46	C46	GTH13_RX_N	U3
R4	GTH15_TX_P	D47	C47	GND	N/A
R3	GTH15_TX_N	D48	C48	GTH15_RX_P	P2

Zynq Pin Number	UltraZed-EV Net Name	JX2 Pin Number		UltraZed-EV Net Name	Zynq Pin Number
N/A	GND	D49	C49	GTH15_RX_N	P1
N/A	GND	D50	C50	GND	N/A
N/A	GND	B1	A1	MGTAVTT	E6, U6
J16	HD_SE_02_P	B2	A2	MGTAVTT	G6
H16	HD_SE_02_N	B3	A3	HD_SE_03_P	K15
A6, J6	MGTAVTT	B4	A4	HD_SE_03_N	K14
F16	HD_SE_06_GC_P	B5	A5	MGTVCCAUX	E10
F15	HD_SE_06_GC_N	B6	A6	HD_SE_07_GC_P	E17
B8, L6	MGTAVTT	B7	A7	HD_SE_07_GC_N	D17
C17	HD_SE_10_P	B8	A8	MGTVCCAUX	G10
B16	HD_SE_10_N	B9	A9	HD_SE_11_P	L15
C6, N6	MGTAVTT	B10	A10	HD_SE_11_N	L14
C14	HD_SE_14_P	B11	A11	GND	N/A
B14	HD_SE_14_N	B12	A12	HD_SE_15_P	H14
D8, R6	MGTAVTT	B13	A13	HD_SE_15_N	G14
G13	HD_SE_18_GC_P	B14	A14	GND	N/A
F13	HD_SE_18_GC_N	B15	A15	HD_SE_19_GC_P	F12
N/A	GND	B16	A16	HD_SE_19_GC_N	E12
K13	HD_SE_22_P	B17	A17	GND	N/A
J12	HD_SE_22_N	B18	A18	HD_SE_23_P	K12
N/A	GND	B19	A19	HD_SE_23_N	K11
C8	GTH1_TX_P	B20	A20	GND	N/A
C7	GTH1_TX_N	B21	A21	GTH1_RX_P	C4
N/A	GND	B22	A22	GTH1_RX_N	C3
A8	GTH3_TX_P	B23	A23	GND	N/A
A7	GTH3_TX_N	B24	A24	GTH3_RX_P	A4
N/A	GND	B25	A25	GTH3_RX_N	A3
H6	GTH4_TX_P	B26	A26	GND	N/A
H5	GTH4_TX_N	B27	A27	GTH4_RX_P	H2
N/A	GND	B28	A28	GTH4_RX_N	H1
F6	GTH6_TX_P	B29	A29	GND	N/A
F5	GTH6_TX_N	B30	A30	GTH6_RX_P	F2
N/A	GND	B31	A31	GTH6_RX_N	F1
H10	GTH_REFCLK2_P	B32	A32	GND	N/A
H9	GTH_REFCLK2_N	B33	A33	GTH_REFCLK3_P	F10
N/A	GND	B34	A34	GTH_REFCLK3_N	F9
M6	GTH9_TX_P	B35	A35	GND	N/A
M5	GTH9_TX_N	B36	A36	GTH9_RX_P	M2
N/A	GND	B37	A37	GTH9_RX_N	M1
K6	GTH11_TX_P	B38	A38	GND	N/A
K5	GTH11_TX_N	B39	A39	GTH11_RX_P	J4
N/A	GND	B40	A40	GTH11_RX_N	J3
W4	GTH12_TX_P	B41	A41	GND	N/A
W3	GTH12_TX_N	B42	A42	GTH12_RX_P	V2
N/A	GND	B43	A43	GTH12_RX_N	V1
T6	GTH14_TX_P	B44	A44	GND	N/A
T5	GTH14_TX_N	B45	A45	GTH14_RX_P	T2
N/A	GND	B46	A46	GTH14_RX_N	T1

Zynq Pin Number	UltraZed-EV Net Name	JX2 Pin Number		UltraZed-EV Net Name	Zynq Pin Number
R8	GTH_REFCLK6_P	B47	A47	GND	N/A
R7	GTH_REFCLK6_N	B48	A48	GTH_REFCLK7_P	N8
N/A	GND	B49	A49	GTH_REFCLK7_N	N7
N/A	GND	B50	A50	GND	N/A

Table 27 – JX2 Connector Master Table

Zynq Pin Number	UltraZed-EV Net Name	JX3 Pin Number		UltraZed-EV Net Name	Zynq Pin Number
N/A	GND	D1	C1	CC_SDA	N/A
G25	GTR_TX3_P	D2	C2	GND	N/A
G26	GTR_TX3_N	D3	C3	GND	N/A
N/A	GND	D4	C4	GTR_RX3_P	G29
N/A	GND	D5	C5	GTR_RX3_N	G30
K27	GTR_TX1_P	D6	C6	GND	N/A
K28	GTR_TX1_N	D7	C7	GND	N/A
N/A	GND	D8	C8	GTR_RX1_P	J29
N/A	GND	D9	C9	GTR_RX1_N	J30
H23	GTR_REFCLK3_P	D10	C10	GND	N/A
H24	GTR_REFCLK3_N	D11	C11	GND	N/A
N/A	GND	D12	C12	GTR_REFCLK1_P	L25
N/A	GND	D13	C13	GTR_REFCLK1_N	L26
N/A	USB_OTG_P	D14	C14	GND	N/A
N/A	USB_OTG_N	D15	C15	GND	N/A
N/A	GND	D16	C16	USB_OTG_CPEN	N/A
N/A	USB_ID	D17	C17	USB_OTG_VBUS	N/A
B22, D23, E21	VCCO_PSIO_501	D18	C18	ETH_PHY_LED1	N/A
N/A	CC_INT_N	D19	C19	GND	N/A
N/A	MGTRAVCC_SENSE	D20	C20	ETH_PHY_LED0	N/A
B20	MIO_26	D21	C21	PS_VBATT	U20
A21	MIO_28	D22	C22	MIO_27	B21
C21	MIO_30	D23	C23	MIO_29	D21
N/A	VCCO_HD_47_SENSE	D24	C24	MIO_31	A22
G20	MIO_32	D25	C25	MGTRAVTT_SENSE	N/A
B24	MIO_34	D26	C26	MIO_33	C22
D22	MIO_36	D27	C27	MIO_35	B23
N/A	VCCO_HD_48_SENSE	D28	C28	MIO_37	F21
C23	MIO_38	D29	C29	VCCO_HP_65_SENSE	N/A
N/A	VCCO_HP_64_SENSE	D30	C30	MIO_39	E22
N/A	GND	B1	A1	CC_SCL	N/A
J25	GTR_TX2_P	B2	A2	GND	N/A
J26	GTR_TX2_N	B3	A3	GND	N/A
N/A	GND	B4	A4	GTR_RX2_P	H27
N/A	GND	B5	A5	GTR_RX2_N	H28
M27	GTR_TX0_P	B6	A6	GND	N/A
M28	GTR_TX0_N	B7	A7	GND	N/A
N/A	GND	B8	A8	GTR_RX0_P	L29
N/A	GND	B9	A9	GTR_RX0_N	L30
K23	GTR_REFCLK2_P	B10	A10	GND	N/A
K24	GTR_REFCLK2_N	B11	A11	GND	N/A
N/A	GND	B12	A12	GTR_REFCLK0_P	M23

N/A	GND	B13	A13	GTR_REFCLK0_N	M24
N/A	ETH_MD1_P	B14	A14	GND	N/A
N/A	ETH_MD1_N	B15	A15	ETH_MD2_P	N/A
N/A	GND	B16	A16	ETH_MD2_N	N/A
N/A	ETH_MD3_P	B17	A17	GND	N/A
N/A	ETH_MD3_N	B18	A18	ETH_MD4_P	N/A
N/A	GND	B19	A19	ETH_MD4_N	N/A
C24	MIO_40	B20	A20	GND	N/A
E23	MIO_42	B21	A21	MIO_41	D24
E24	MIO_44	B22	A22	MIO_43	F22
N/A	MGTVCCAUX_Sense	B23	A23	MIO_45	F23
K20	MIO_46	B24	A24	MGTAVCC_Sense	N/A
H25, L27	MGTRAVTT	B25	A25	MIO_47	K21
J21	MIO_48	B26	A26	GND	N/A
K25	MGTRAVTT	B27	A27	MIO_49	G21
J20	MIO_50	B28	A28	MGTAVTT_Sense	N/A
J23	MGTRAVCC	B29	A29	MIO_51	H21
L23	MGTRAVCC	B30	A30	MGTRAVCC	N/A

Table 28 – JX3 Connector Master Table

Signal Name	ZU7EV Bank	Voltage Domain	I/O Usage
HP_DP_[00:23]_P/N	64	VCCO_HP_64	Single-Ended or Differential I/O
HP_DP_[24:47]_P/N	65	VCCO_HP_65	Single-Ended or Differential I/O
HP_SE_[00:03]	64	VCCO_HP_64	Single-Ended
HP_SE_[04:07]	65	VCCO_HP_65	Single-Ended
HD_SE_[00:11]_P/N	48	VCCO_HD_48	Single-Ended or Differential Input
HD_SE_[12:23]_PN	47	VCCO_HD_47	Single-Ended or Differential Input
GTR_TX[0:3]_P/N	505	MGTRAVCC / MGTRAVTT	Differential I/O
GTR_RX[0:3]_P/N	505	MGTRAVCC / MGTRAVTT	Differential I/O
GTR_REFCLK[0:3]_P/N	505	MGTRAVCC / MGTRAVTT	Differential I/O
MIO_[26:51]	501	VCCO_PSIO_501	Single-Ended
GTH[0:3]_TX_P/N	227	MGTAVCC/MGTAVTT	Differential I/O
GTH[0:3]_RX_P/N	227	MGTAVCC/MGTAVTT	Differential I/O
GTH_REFCLK[0:1]_P/N	227	MGTAVCC/MGTAVTT	Differential I/O
GTH[4:7]_TX_P/N	226	MGTAVCC/MGTAVTT	Differential I/O
GTH[4:7]_RX_P/N	226	MGTAVCC/MGTAVTT	Differential I/O
GTH_REFCLK[2:3]_P/N	226	MGTAVCC/MGTAVTT	Differential I/O
GTH[8:11]_TX_P/N	225	MGTAVCC/MGTAVTT	Differential I/O
GTH[8:11]_RX_P/N	225	MGTAVCC/MGTAVTT	Differential I/O
GTH_REFCLK[4:5]_P/N	225	MGTAVCC/MGTAVTT	Differential I/O
GTH[12:15]_TX_P/N	224	MGTAVCC/MGTAVTT	Differential I/O
GTH[12:15]_RX_P/N	224	MGTAVCC/MGTAVTT	Differential I/O
GTH_REFCLK[6:7]_P/N	224	MGTAVCC/MGTAVTT	Differential I/O

Table 29 – JX Connector Signal Decoder

The following descriptions are provided to aid in determining the type of signal in the JX connector master table:

Pins in **Red** are Power or Ground signals.
Pins in **Blue** are dedicated signals.

Pins in **Black** are multi-function/general-purpose pins.
Pins in **Black** with **_GC** designators are multi-function/general-purpose pins or Global Clock inputs.
HP_DP stands for High Performance Differential Pairs
HP_SE stands for High Performance Single-Ended
HD_SE stands for High Density Single-Ended.
HD_SE signals can be used as Single-Ended or Differential Inputs.

2.14.3 Powering the PL Banks (SOM_PG_OUT)

The UltraZed-EV SOM does not power the PL VCCIO banks. This is required to be provided by the end- user carrier card. This gives the end-user carrier card the flexibility to control the I/O bank voltages depending on the interfaces the end-user decides to implement.

The Zynq UltraScale+ MPSoC has 4 PL I/O banks that are each capable of being powered separately by the end-user carrier card. There is a 5th PL I/O bank that is powered by the SOM that contains the PL DDR4 interface. The UltraZed-EV SOM provides an active-high **SOM_PG_OUT** signal out to the end-user carrier card. The end-user carrier card shall not provide power to the PL VCCIO pins on the JX connectors until the **SOM_PG_OUT** signal becomes active.

2.15 Configuration Modes

The Zynq UltraScale+ MPSoC device uses a multi-stage boot process that supports both non-secure and secure boot. The PS is the master of the boot and configuration process. Upon reset, the device PS MODE pins are read to determine the primary boot device to be used. The UltraZed-EV SOM allows several of those boot devices: QSPI, SD Card, eMMC, and JTAG boot are easily accessible by changing the Boot Mode Switch, SW2, settings.

NOTE: The JTAG or SD Card interface is to be implemented on the end-user carrier card.

The boot mode pins on Zynq UltraScale+ MPSoC are dedicated pins unlike the Zynq SoC which shared the mode pins with PS MIO pins. All PS MODE pins are pulled either high or low through the Boot Mode Switch. The table below shows the available boot mode configuration settings using the Boot Mode Switch, SW2.

Boot Mode	Mode Pin [3:0]	SW2 [1:4]
JTAG *	0x0	ON-ON-ON-ON
QSPI24	0x1	OFF-ON-ON-ON
QSPI32	0x2	ON-OFF-ON-ON
SD1/MMC33 *	0x5	OFF-ON-OFF-ON
EMMC18	0x6	ON-OFF-OFF-ON
SD1/MMC33 *	0xE	ON-OFF-OFF-OFF

Table 30 – UltraZed-EV SOM Configuration Modes

**Interfaces on the End-User Carrier Card*

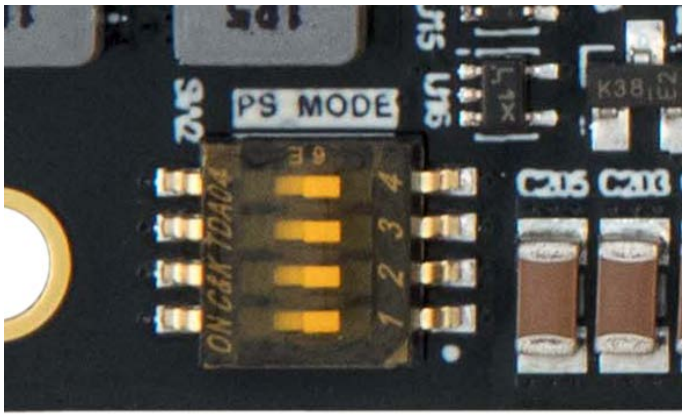

Figure 11 – UltraZed-EV SOM Boot Mode Switch

The boot time to application start may be affected by a number of circumstances such as the hardware definition, the peripherals in use and their driver load times, the Ethernet interface not being connected and active, as well as pre-installed applications load time. Avnet's Petalinux 2017.3 Out-of-Box design contains items that load at boot time that may not exist in end-user applications. It is expected that the load times for Avnet's Out-of-Box design can be decreased depending on the end-user optimizing their Linux environment.

The Zynq UltraScale+ MPSoC has many configuration options; The UltraZed-EV SOM uses this configuration:

- VCCO_0 does not require a rail as it has an internal 1.8V.
- PUDC_B can be pulled high or low on the UltraZed-EV SOM. This active-low input enables internal pull-ups during configuration on all SelectIO pins. By default, the resistor jumper is populated with a 1K resistor in the 1-2 position, which pulls up PUDC_B and disables the pull-ups during configuration.
- PS_INIT_B is pulled high via a 4.7KΩ resistor.
- PS_PROG_B is pulled high via a 4.7KΩ resistor with activation control through a push button.

The PS is responsible for configuring the PL. The Zynq UltraScale+ MPSoC will not automatically reconfigure the PL as in standard FPGAs by toggling PROG. Likewise, it is not possible to hold off Zynq boot up with INIT_B as this is done with PS_POR_B. If the application needs to reconfigure the PL, the software design must do this, or you can toggle the PS_POR_B to restart everything. When PL configuration is complete a blue DONE LED will illuminate.

2.15.1 JTAG Connections

The UltraZed-EV SOM requires an external JTAG cable connector populated on the carrier card for JTAG operations. JTAG signals are routed from Bank 503 of the Zynq UltraScale+ MPSoC to the Micro Header JX1. The following table shows the JTAG signal connections between the Zynq and the Micro Header.

The Zynq UltraScale+ MPSoC Bank 503 reference voltage, +VCCO_PSIO, is connected to 1.8V. The JTAG VREF on the end-user carrier card should be connected to 1.8V to ensure compatibility between the interfaces. For reference, see the UltraZed-EV carrier card schematics.

MPSoC Pin #	UltraZed-EV SOM Net Name	JX1 Pin #
L19	JTAG_TCK	JX1.D1
L21	JTAG_TMS	JX1.C1
M20	JTAG_TDO	JX1.D2
L20	JTAG_TDI	JX1.C2

Table 31 – UltraZed-EV SOM JTAG Connections

NOTE: JTAG 4.7-kΩ Pull-ups will exist on the end-user carrier card. Also, JTAG series termination resistors will exist on the end-user carrier card if required

NOTE: Further documentation on the pull-ups and series terminations will exist in the UltraZed Carrier Card Design Guide

2.16 Power Supplies

2.16.1 Voltage Rails and Sources

The UltraZed-EV SOM is powered through the Micro Header connection between itself and the end-user carrier card.

There are eight regulators that reside on the UltraZed-EV SOM that provide 0.85V, 1.0V, 1.2V, 1.8V, 2.5V, 3.3V, 5V and 0.6V power rails. These voltages are used to power the peripheral devices as well as the UltraZed-EV SOM. Most of these regulators are powered from the end-user carrier card via the **+VIN** pins on the Micro Headers and are expected to carry +5V or +12V to the UltraZed-EV SOM regulator inputs.

There are also five bank voltages that are supplied from the end-user carrier card to the UltraZed-EV SOM. Bank 47 (**+VCCO_HD_47**), Bank 48 (**+VCCO_HD_48**), Bank 64 (**+VCCO_HP_64**), Bank 65 (**+VCCO_HP_65**), and Bank 501 (**+VCCO_PSIO_501**) voltages are generated on the end-user carrier card and connected to the UltraZed-EV SOM via the Micro Headers. The voltage at which these banks operate is up to the end-user carrier card design as all I/O that connect to these banks is exclusive to the Micro Headers (no on-board device is connected to these banks).

The diagram below shows a high level depiction of the power provided by the end-user carrier card through the Micro Headers as well as the regulators that exist on the UltraZed-EV SOM.

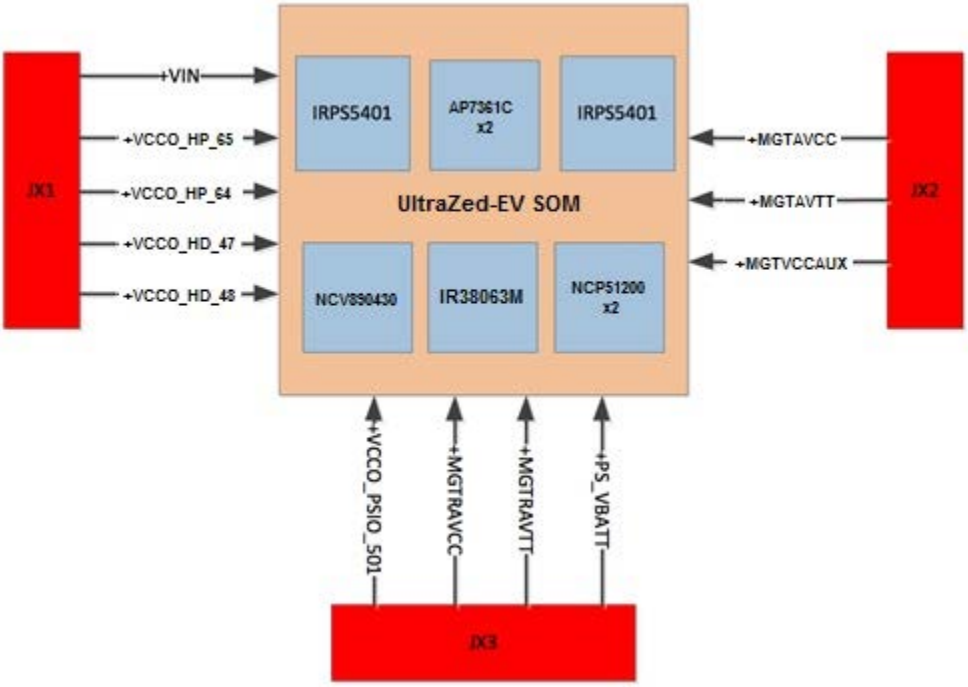

Figure 12 – UltraZed-EV SOM Power Solution

The table below shows the various voltage rails names on the schematic, the associated voltage for each rail, where they are connected on the Zynq UltraScale+ MPSoC, and where the voltage originates from.

Schematic Voltage Name	Voltage Level	Zynq Connection	Voltage Origination
+5VREG	5.0V	N/A	UltraZed-EV SOM
+2.5V	2.5V		
+1.0V	1.0V		
+PS_DDR4_VREF	1.2V		
+PL_DDR4_VREF	1.2V		
+PS_DDR4_VTT	0.6V		
+PL_DDR4_VTT	0.6V		
+VCCO_PSIO	1.8V	VCCO_PSIO0_500	
		VCCO_PSIO2_502	
		VCCO_PSIO3_503	
		VCC_PSADC	
		VCC_PSAUX	
+VCCAUX	1.8V	VCCAUX	
		VCCAUX_IO	
		VCCADC	
+VCC_PSINTLP	0.85V	VCC_PSINTLP	
+VCC_PSINTFP	0.85V	VCC_PSINTFP	
		VCC_PSINTFP_DDR	
+VCC_PSPLL	1.2V	VCC_PSPLL	
+VCCO_PSDDR_504	1.2V	VCCO_PSDDR_504	
+VCCINT_IO	0.85V	VCCBRAM	
		VCCINT_IO	
+3.3V	3.3V	N/A	
+VCCINT	0.85V	VCCINT	
+VCCINT_VCU	0.85V	VCCINT_VCU	
+VCC_PSDDR_PLL	1.8V	VCC_PSDDR_PLL	
+VIN	5V or 12V	N/A	JX1
+VCCO_HP_64	1.0V to 1.8V	VCCO_64 (Bank 64)	JX1
+VCCO_HP_65	1.0V to 1.8V	VCCO_65 (Bank 65)	JX1
+VCCO_HD_47	1.2V to 3.3V	VCCO_47 (Bank47)	JX1
+VCCO_HD_48	1.2V to 3.3V	VCCO_48 (Bank 48)	JX1
+MGTAVCC	0.9V	MGTAVCC_R	JX2
+MGTAVTT	1.2V	MGTAVTT_R	JX2
+MGTVCCAUX	1.8V	MGTVCCAUX_R	JX2
+VCCO_PSIO_501	1.8V to 3.3V	VCCO_PSIO1_501	JX3
+MGTRAVCC	0.85V	PS_MGTRAVCC	JX3
+MGTRAVTT	1.8V	PS_MGTRAVTT	JX3
+PS_VBATT	1.5V	VCC_PSBATT	JX3

Table 32 – UltraZed-EV SOM Voltage Rails

2.16.2 Voltage Regulators

The following block diagram contains the on-board power solution for the UltraZed-EV SOM.

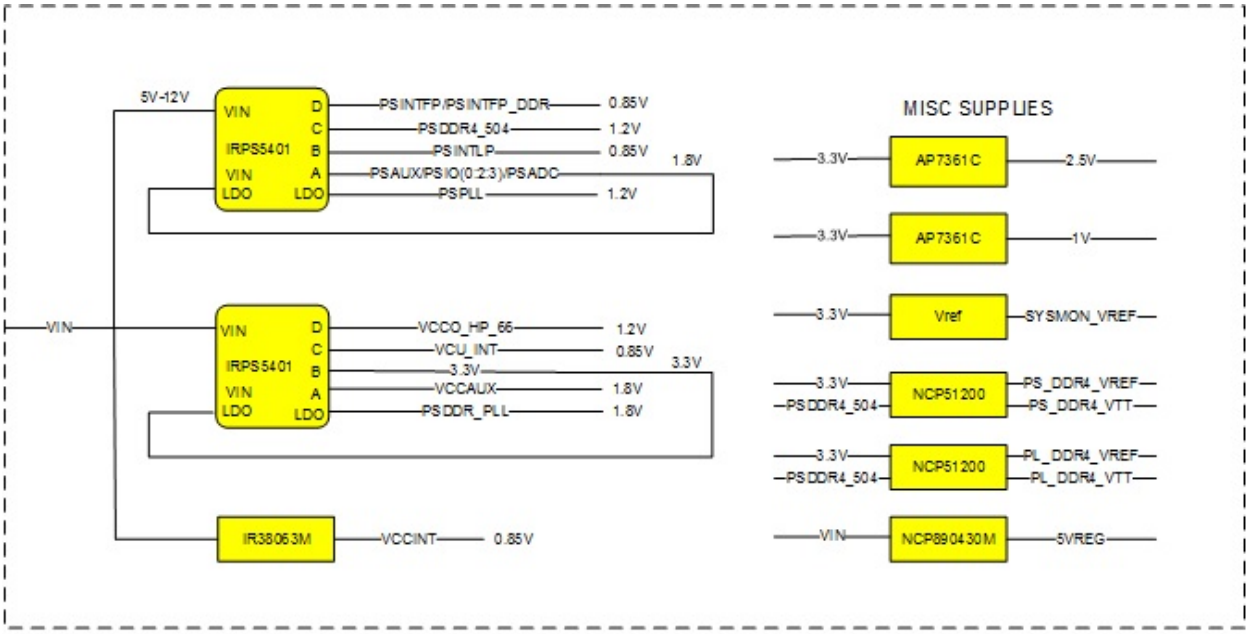

Figure 13 – On-Board Regulation Circuits

The POWER GOOD output of the +3.3V rail is used to ENABLE the DDR termination regulator and the AP7361C regulators completing the power sequence. These three supplies are the last regulators to be brought up.

The UltraZed-EV SOM provides a power good signal to the end-user carrier card to signal that the SOM power sequencing has completed and the end-user carrier card is free to bring up the VCCO supplies. This signal is called **SOM_PG_OUT** and is tied to JX1.D47. **SOM_PG_OUT** on the Micro Header serves to gate the power supplies for Bank 501, Bank 47, Bank48, Bank 64, Bank 65, MGTRAVCC, MGTRAVTT, MGTAVCC, MGTAVTT, and MGTVCCAUX on the end-user carrier card. **SOM_PG_OUT** is provided by the power good output of the PS DDR termination regulator.

The table below shows the maximum output current for each regulator on the UltraZed-EV SOM. Also listed in the table below are the supported power modes and whether or not the rail is to remain active during the power mode that the UltraZed-EV SOM is being operated in.

Voltage Rail	Voltage (V)	Max Current (A)	Power Domain	Power Modes		
				Full Power	PS Only	PS Low Power
+5VREG	5.0V	0.5A	N/A	Y	Y	Y
+2.5V	2.5V	0.3A	N/A	Y	Y	Y
+PS_DDR4_VREF	1.2V	0.04A	N/A	Y	Y	Y
+PL_DDR4_VREF	1.2V	0.04A	N/A	Y	Y	Y
+1.0V	1.0V	0.3A	N/A	Y	Y	Y
+PS_DDR4_VTT	0.6V	5.5A	N/A	Y	Y	Y
+PL_DDR4_VTT	0.6V	5.5A	N/A	Y	Y	Y
+VCCO_PSIO	1.8V	0.5A *	PS LP	Y	Y	Y
+VCCAUX	1.8V	1.1A *	PL	Y	N	N
+VCC_PSINTLP	0.85V	0.6A *	PS LP	Y	Y	Y
+VCC_PSINTFP	0.85V	3.7A *	PS FP	Y	Y	N
+VCC_PSPLL	1.2V	0.2A *	PS LP	Y	Y	Y
+VCCO_PSDDR_504	1.2V	1.2A *	PS LP	Y	Y	N
+VCCINT_IO	0.85V	0.6A *	PL	Y	N	N
+3.3V	3.3V	1.0A *	N/A	Y	Y	Y
+VCCINT	0.85V	11.0A *	PL	Y	N	N
+VCCINT_VCU	0.85V	4.0A *	VCU	Y	N	N
+VCC_PSDDR_PLL	1.8V	0.5A *	PS FP	Y	Y	N
+VIN	5V or 12V	-	N/A	Y	Y	Y
+VCCO_HP_64	1.0V to 1.8V	1.5A **	PL	Y	N	N
+VCCO_HP_65	1.0V to 1.8V	1.5A **	PL	Y	N	N
+VCCO_HP_66	1.0V to 1.8V	1.5A **	PL	Y	N	N
+VCCO_HD_47	1.2V to 3.3V	1.5A **	PL	Y	N	N
+VCCO_HD_48	1.2V to 3.3V	1.5A **	PL	Y	N	N
+VCCO_PSIO_501	1.8V to 3.3V	0.5A **	PS LP	Y	Y	Y
+MGTRAVCC	0.85V	0.22A *	PS FP	Y	Y	N
+MGTRAVTT	1.8V	0.04A *	PS FP	Y	Y	N
+MGTAVCC	0.9V	1.8A *	PL	Y	N	N
+MGTAVTT	1.2V	2.0A *	PL	Y	N	N
+MGTVCCAUX	1.8V	0.05A *	PL	Y	N	N
+PS_VBATT	1.5V	0.5A *	N/A	Y	Y	Y

Table 33 – Voltage Rails Max Current and Power Modes

** Max Current Derived using Preliminary Xilinx Power Estimator Tools (On-Board)*

*** Max Current Derived using Micro Header Pin Current Carrying Capacity (Carrier Card)*

2.16.3 Power Supply Sequencing and Power Modes

Sequencing for the power supplies follows the datasheet recommendations for the Zynq UltraScale+ device. The power configuration programmed into the International Rectifier IRPS5401MTRPBF and IR3806MTRPBF devices controls the power supply sequencing. An end-user may utilize the PMBUS on the carrier-card or utilize the Zynq UltraScale+ MPSoC

interface to the PMBUS to power down individual rails to implement the different power modes supported by the MPSoC.

Sequencing is needed for board power up, as well as entering and exiting different power modes. There are 3 power domains, PS LP (Processing Subsystem Low Power), PS FP (Processing Subsystem Full Power) and PL (Programmable Logic Power). The PS LP domain shall come up first followed by the PS FP and PL power domains.

PS LP Power Domain Sequence:

DS925 (V1.8) Recommended:

VCC_PSINTLP → VCC_PSAUX / VCC_PSADC / VCC_PSPLL → VCCO_PSIO

UltraZed-EV SOM Implementation:

VCC_PSINTLP → VCCO_PSIO / VCC_PSPLL → VCCO_PSIO_501 (From Carrier Card)

PS FP Power Domain Sequence:

DS925 (V1.8) Recommended:

VCC_PSINTFP / VCC_PSINTFP_DDR → PS_MGTRAVCC / VCC_PSDDR_PLL → PS_MGTRAVTT / VCCO_PSDDR

UltraZed-EV SOM Implementation:

VCC_PSINTFP → MGTRAVCC (From Carrier Card) / VCC_PSDDR_PLL (Generated from +3.3V on SOM) → MGTAVTT (From Carrier Card) / VCCO_PSDDR4_504

PL Power Domain Sequence:

DS925 (V1.8) Recommended:

VCCINT → VCCINT_IO / VCCBRAM / VCCINT_VCU → VCCAUX / VCCAUX_IO → VCCO_HD_47 / VCCO_HD_48 / VCCO_HP_64 / VCCO_HP_65 / VCCO_HP_66 / MGTAVCC / MGTAVTT / MGTVCCAUX

UltraZed-EV SOM Implementation:

VCCINT → VCU_INT → VCCAUX →
VCCO_HD_47 (From Carrier Card) / VCCO_HD_48 (From Carrier Card) / VCCO_HP_64 (From Carrier Card) / VCCO_HP_65 (From Carrier Card) / VCCO_HP_66 / MGTAVCC (From Carrier Card) / MGTAVTT (From Carrier Card) / MGTVCCAUX (From Carrier Card)

Entering / Exiting Power Domains:

To enter power down modes, the reverse order of start-up should be followed (last supply to come up should be the first to be shut down, etc.). The PL and PS FP domains can be powered down independently and either can be powered down before or after the other. When shutting down power to a domain however, sequencing must be followed in relation to the specific power domain group. Upon repowering these domains, proper sequencing should again be followed.

The following diagrams are indicative of the pre-programmed power-on and power-off sequences that exist on the UltraZed-EV SOM and the UltraZed-EV Carrier Card.

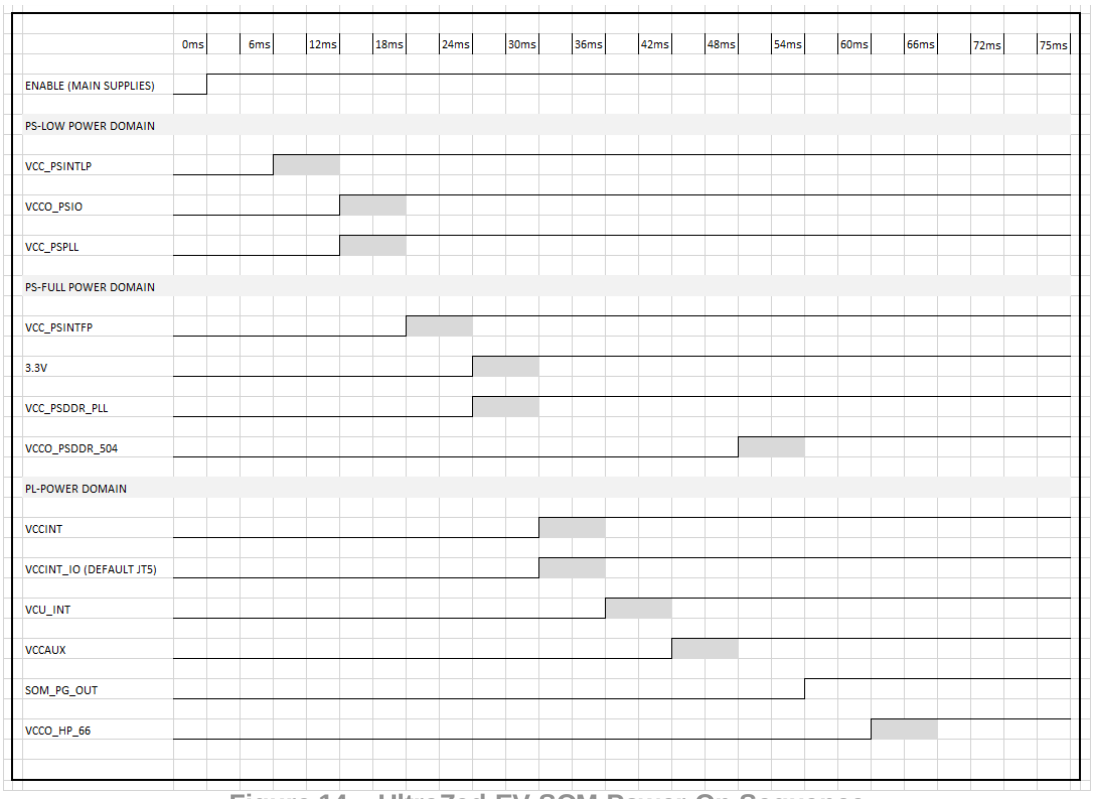

Figure 14 – UltraZed-EV SOM Power-On Sequence

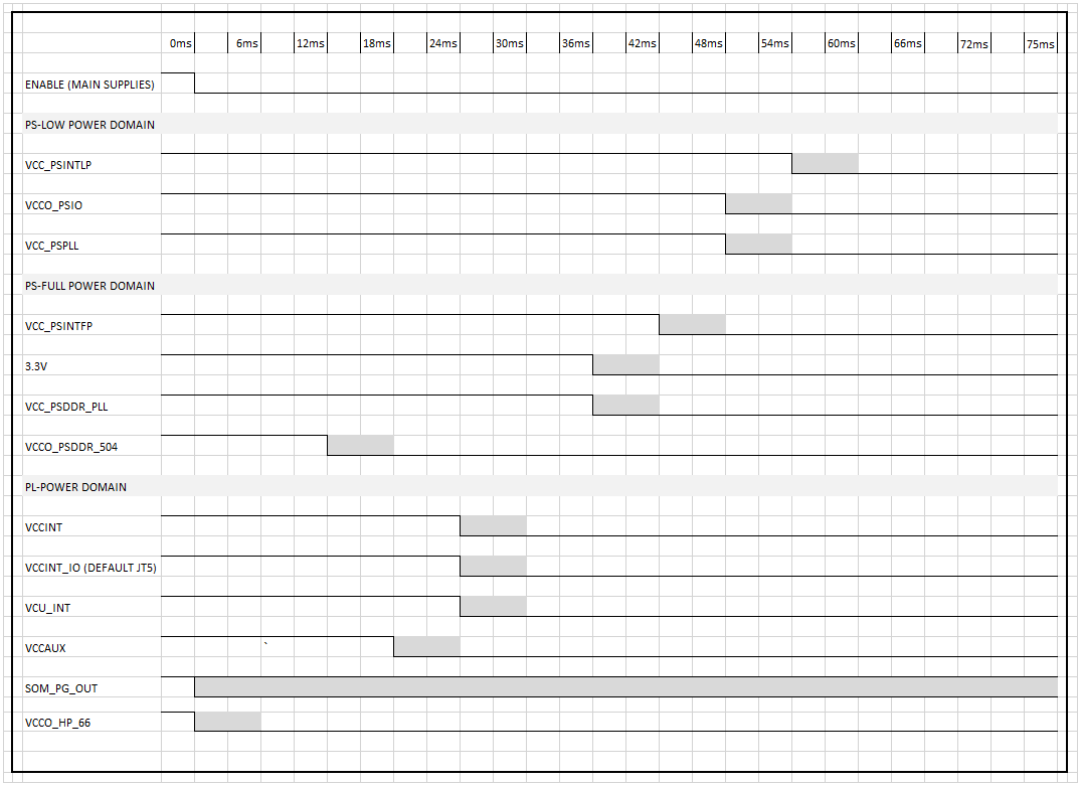

Figure 15 – UltraZed-EV SOM Power-Off Sequence

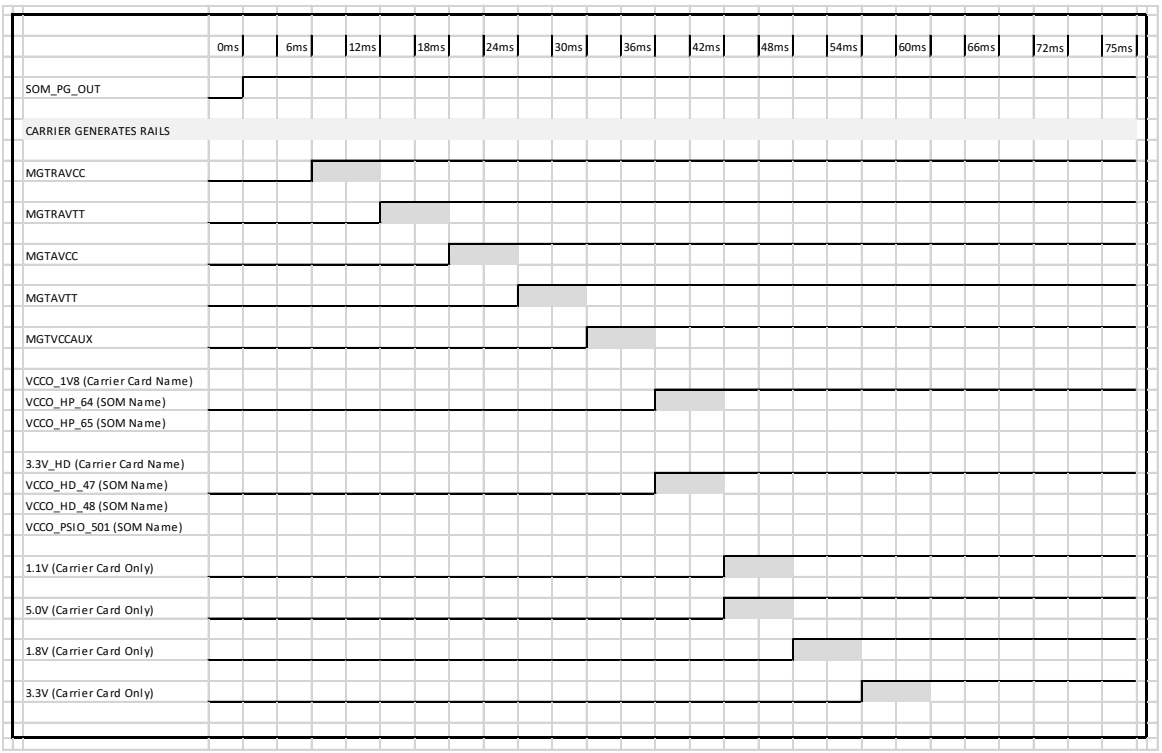

Figure 16 – UltraZed-EV Carrier Card Example Power-On Sequence

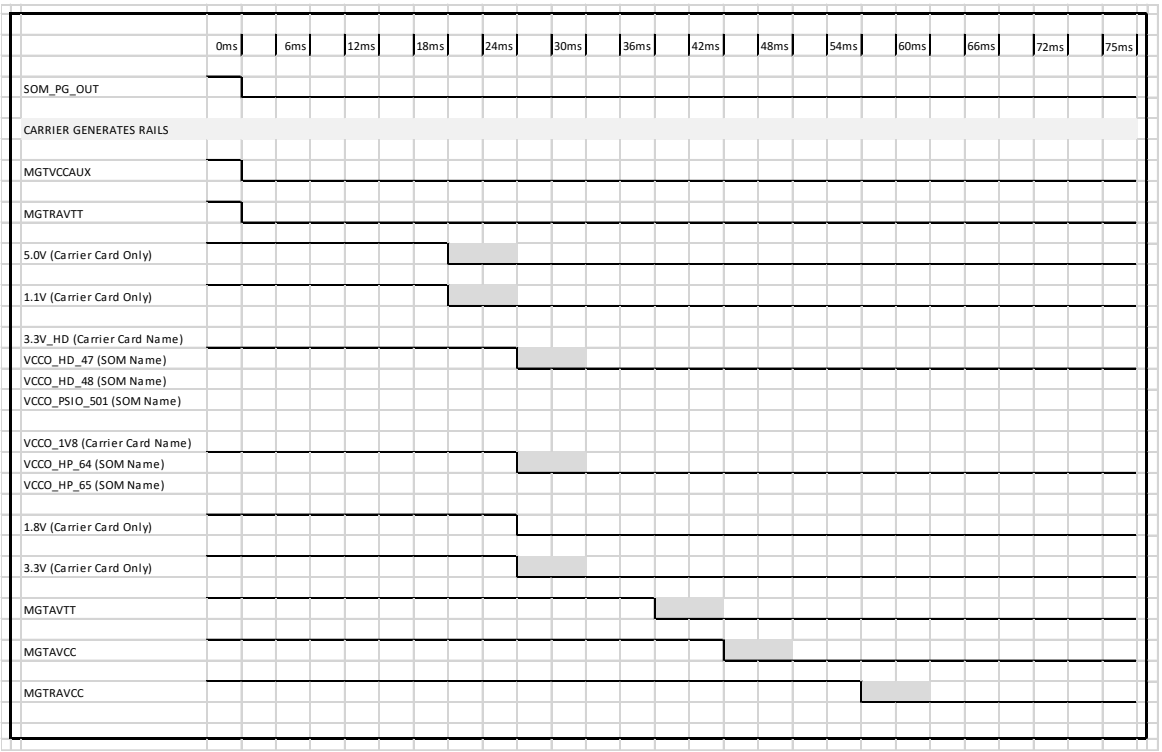

Figure 17 – UltraZed-EV Carrier Card Example Power-Off Sequence

The following diagram illustrates the power-up flow with an end-user carrier card:

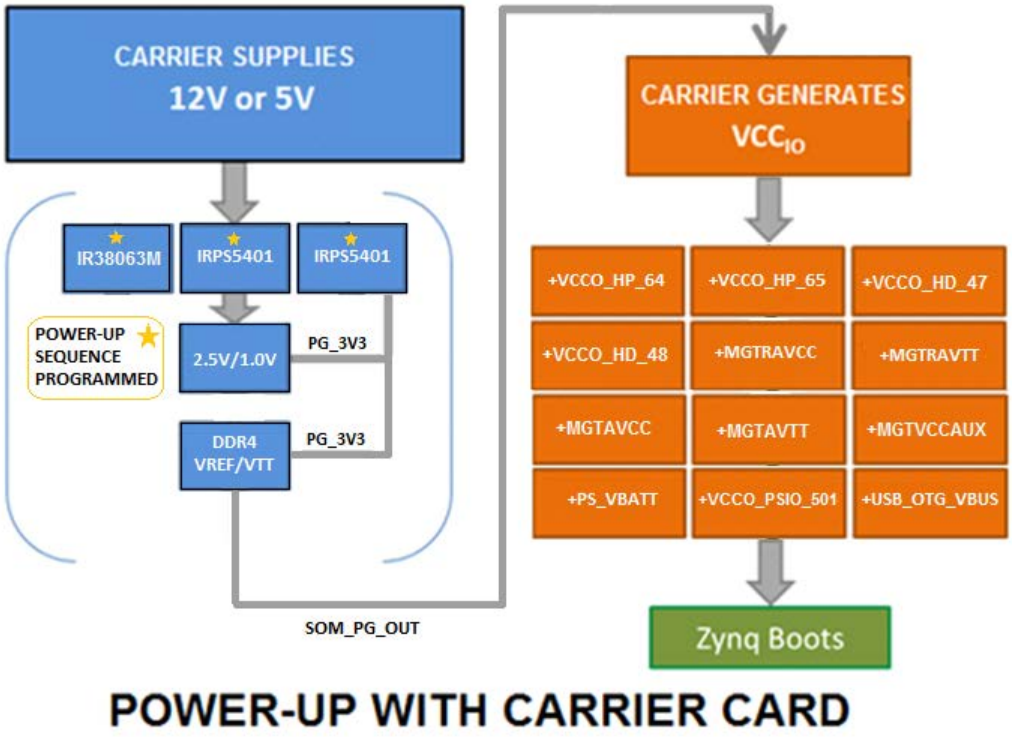

Figure 18 – Power-Up Flow with Carrier Card

2.16.4 PCB Bypass / Decoupling Strategy

The UltraZed-EV SOM design follows at a minimum the PCB decoupling strategy as outlined in UG583 for the Zynq UltraScale+ MPSoC in the FBVB900 package.

NOTE: These quantities are considered preliminary and subject to change because power and package modelling is still in progress at Xilinx. A review of these requirements is required as this design moves from engineering silicon to production silicon.

	V_{CCINT}/V_{CCINT_IO} [1]				V_{CCBRAM}/V_{CCINT_IO} [2]		V_{CCAUX}/V_{CCAUX_IO}		HDIO [4]	HPIO [4]
	680 µF [5]	100 µF	4.7 µF	0.47 µF	47 µF	4.7 µF	47 µF	4.7 µF	47 µF	47 µF
EV Devices										
XCZU4EV-FBVB900	1	1	1	0	1	1	1	2	1	1
XCZU5EV-FBVB900	1	1	2	0	1	1	1	2	1	1
XCZU7EV-FBVB900	1	1	3	0	1	1	1	2	1	1
EG Devices										
XCZU4EG-FBVB900	1	1	1	0	1	1	1	2	1	1
XCZU5EG-FBVB900	1	1	2	0	1	1	1	2	1	1
XCZU7EG-FBVB900	1	1	3	0	1	1	1	2	1	1
CG Devices										
XCZU4CG-FBVB900	1	1	1	0	1	1	1	2	1	1
XCZU5CG-FBVB900	1	1	2	0	1	1	1	2	1	1
XCZU7CG-FBVB900	1	1	3	0	1	1	1	2	1	1

Notes:

1. Connect V_{CCINT} and V_{CCINT_IO} together for -3, -2, and -1 speed grades.
2. Connect V_{CCBRAM} and V_{CCINT_IO} together for -2L and -1L speed grades.
3. V_{CCINT}, V_{CCINT_IO}, and V_{CCBRAM} can be tied together if all three rails are operated at the same voltage.
4. One 47 µF capacitor is required for up to four HP/HD I/O banks when powered by the same voltage.
5. 470 µF capacitors can be used in place of 680 µF capacitors at a rate of four 470 µF capacitors per three 680 µF capacitors. See Table 1-4 for 470 µF capacitor specifications.
6. PCB decoupling capacitors cover down to approximately 100 kHz, depending on voltage regulator design. See PCB Bulk Capacitors about the need for 680 µF and/or 100 µF capacitors.

Figure 19 – PCB PL Decoupling Capacitor Requirements

VCCINT_VCU Decoupling Capacitor Recommendations

10 µF	4.7 µF	1.0 µF
1	2	2

Figure 20 – PCB VCU_INT Decoupling Capacitor Requirements

$V_{CC\_PSINTLP}$		$V_{CC\_PSINTFP}$		V_{CC_PSAUX}		V_{CC_PSPLL}		PS_MGTRAVCC	PS_MGTRAVTT	$V_{CC\_PSINTFP\_DDR}$		V_{CCO_PSIOx} (Each)		V_{CC_PSBATT}		V_{CCO_PSDDR}		
100 µF	4.7 µF	100 µF	4.7 µF	100 µF	4.7 µF	100 µF	4.7 µF	4.7 µF	4.7 µF	100 µF	4.7 µF	100 µF	4.7 µF	100 µF	4.7 µF	100 µF	4.7 µF	0.47 µF
1	1	1	1	1	1	1	1	See note 1	See note 1	1	1	1	1	1	1	1	2	4

Notes:

1. For PS MGT supply decoupling, see PS-GTR Transceiver Interfaces, page 171.

Figure 21 – PCB PS Decoupling Capacitor Requirements

NOTE: The PS-GTR Transceiver Interfaces, PS_MGTRAVCC and PS_MGTRAVTT each require a single 4.7uF 10% ceramic.

GTH Transceiver PCB Capacitor Recommendations

Quantity Per Group			Capacitance (µF)	Tolerance	Type
MGTAVCC	MGTAVTT	MGTVCCAUX			
1	1	1	4.70	±10%	Ceramic

Figure 22 – PCB GTH Decoupling Capacitor Requirements

2.16.5 Power Estimation

Since the total power consumption of the system heavily depends on many factors with regard to the configuration/utilization of the Zynq UltraScale+ MPSoC device, it is highly recommended that the end user perform some power estimation and analysis using the Xilinx Power Estimator (XPE). This tool is very useful for plugging in various parameters and getting an estimated power consumption estimate for the system.

When designing the UltraZed-EV SOM architecture, the XPE tool was used to ensure that the UltraZed-EV SOM system could supply enough power to the Zynq UltraScale+ and its on-board peripherals using worst case parameters including logic utilization, operating frequency and temperature while still supporting low power modes and various speed grade options.

Since the power supply for the VCCIO rails for banks 47, 48, 64, 65, and 501 are supplied from the end-user carrier card, it is important to make sure that the end-user carrier card power supplies are adequate to power these rails over the desired and/or estimated operating scenario.

NOTE: When designing a custom UltraZed-EV carrier board, be sure to use XPE (Xilinx Power Estimator) to estimate the power needed by the Zynq UltraScale+ MPSoC device. The designer will need this figure in sizing the input supply to the UltraZed-EV SOM.

NOTE: In addition to the XPE results for the Zynq UltraScale+ MPSoC, the end user will need to add to their power estimate to compensate for the power that is needed for the on-board devices that exist on the UltraZed-EV SOM such as the various memory, USB and Ethernet PHY devices, and serial devices.

2.16.6 VCU Migration (Supporting EG and CG Devices) - Optional

The Video Codec Unit (VCU) is only available in EV devices. The EV devices have a number of VCCINT_VCU power pins that correspond to ground pins on the CG and EG devices. If moving from the EV device to a CG or EG device, the corresponding pins (VCCINT_VCU) should be grounded.

IMPORTANT: ***If moving from an EV device to a CG or EG device, the four VCCINT_VCU pins must be grounded to avoid a short circuit!!***

The UltraZed-EV SOM has the ability to support CG or EG devices via a modification to the UltraZed-EV SOM. Resistor jumper, JT4, on board the UltraZed-EV SOM is set by default (Pin 1 to Pin 2) to provide the proper voltage to the VCCINT_VCU power rail. We can optionally change the position of resistor jumper JT4 (Pin 3 to Pin 2) to properly ground the VCCINT_VCU pins.

NOTE: Please contact customize@avnet.com to order UltraZed-EV SOMs populated with EG or CG devices.

2.16.7 Power Supply Differences across Speed and Temperature Grades - Optional

For the Programmable Logic (PL), the power rails VCCINT, VCCINT_IO, and VCCBRAM can have voltage limits that can differ across the various available speed and temperature grades. For the Processing System (PS), the power rails VCC_PSINTFP, VCC_PSINTPL, VCC_PSINTFP_DDR, and VPS_MGTRAVCC can have voltage limits that can differ across the various speed and temperature grades.

The UltraZed-EV SOM is capable of supporting the requirements for the different speed and temperature grades. In order to support the various speed and temperature grades, two changes may be necessary to make to the UltraZed-EV SOM depending on the desired end solution.

The first change that may be necessary is to adjust the programming of the IR PMIC Regulators to support the lower or higher voltages required by the PS or PL.

NOTE: Please contact customize@avnet.com to order UltraZed-EV SOMs that support programming of the IR PMIC Regulators with lower or higher voltages. The IR PMICs that are populated on the UltraZed-EV SOM come pre-programmed and are unique part numbers to Avnet.

Here are a couple of tables that show the voltage differences depending on the speed and temperature grades for the PS and PL.

Speed/Temp Grade	VCC_PSINTFP (V)	VCC_PSINTLP (V)	VCC_PSINTFP_DDR (V)	VPS_MGTRAVCC (V)
-1E	0.85	0.85	0.85	0.85
-2LE	0.85	0.85	0.85	0.85
-3E	0.90	0.90	0.90	0.90
-1I	0.85	0.85	0.85	0.85
-1LI	0.85	0.85	0.85	0.85
-2I	0.85	0.85	0.85	0.85

Figure 23 – MPSoC PS Voltage by Speed/Temp Grade

Speed/Temp Grade	VCCINT (V)	VCCINT_IO (V)	VCCBRAM (V)
-1E	0.85	0.85	0.85
-2LE	0.72 or 0.85	0.85	0.85
-3E	0.90	0.90	0.90
-1I	0.85	0.85	0.85
-1LI	0.72 or 0.85	0.85	0.85
-2I	0.85	0.85	0.85

Figure 24 – MPSoC PL Voltage by Speed/Temp Grade

As you can see from the PL Voltage by Speed/Temp Grade table, VCCINT_IO/VCCBRAM can different from VCCINT when using a **–L** MPSoC device. In order to support this feature, we need to remove VCCINT_IO/VCCBRAM from the VCCINT power rail as these would be required to be different.

The difference in voltages is accommodated via a modification to the UltraZed-EV SOM. Resistor jumper, JT5, on board the UltraZed-EV SOM is set by default (Pin 1 to Pin 2) to create VCCINT_IO and VCCBRAM from the VCCINT power rail. We can optionally change the position of resistor jumper JT5 (Pin 3 to Pin 2) to create VCCINT_IO and VCCBRAM from the VCU_INT rail.

NOTE: Please contact customize@avnet.com to order UltraZed-EV SOMs populated with different speed grades, temperature grades, or to get boards capable of operating with **–L** devices.

2.16.8 Speed Grade Migration - Optional

CG devices are not available in the -3 speed grade. CG devices can only migrate to EG or EV devices in non -3 speed grades in order to maintain similar performance. Likewise, EG and EV devices can only migrate to a CG device in non -3 speed grades in order to maintain similar performance. EG to EV devices can migrate to any speed grades, as well as EV to EG devices.

NOTE: Please contact customize@avnet.com to order UltraZed-EV SOMs populated with EG or CG devices.

2.16.9 System Monitor (SYSMON)

The Zynq UltraScale+ Architecture supports an on-chip system monitor. SYSMON monitors the physical environment via on-chip temperature and supply sensors with integrated analog-to-digital converters (ADC). An overview of the System Monitor primitive, SYSMON, is provided by Xilinx User Guide **UG580 – UltraScale Architecture System Monitor**.

The UltraZed-EV SOM supports System Monitor functionality thru the JX connectors to a SYSMON header that would be implemented on the end-user carrier card. The UltraZed-EV SOM contains selectable reference voltages via a 0-ohm resistor jumper. The following figure depicts the implementation of the system monitor on the UltraZed-EV SOM.

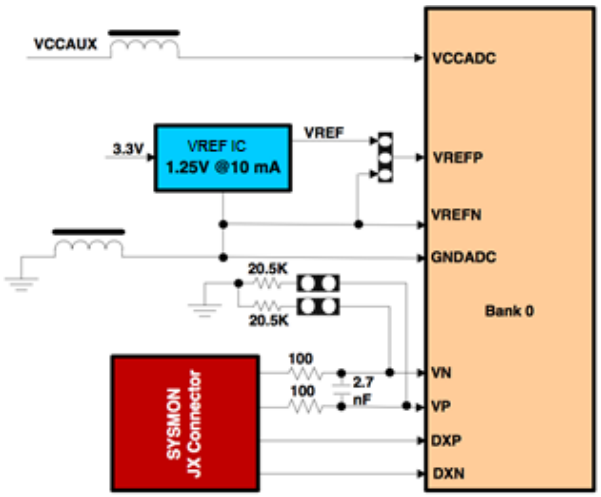

Figure 25 – UltraZed-EV SOM SYSMON Circuit

The following table shows the SYSMON interface connections to the JX1 connector.

NOTE: The SYSMON header is to be implemented on the end-user carrier card.

MPSoC Pin #	UltraZed-EV SOM Net Name	JX1 Pin #
U14	SYSMON_VR_N	JX1.D49
T15	SYSMON_VR_P	JX1.D50
V14	SYSMON_DX_N	JX1.C48
V15	SYSMON_DX_P	JX1.C49

Table 34 – UltraZed-EV SOM SYSMON Connections

2.16.10 Battery Backup – Device Secure Boot Encryption Key

The Zynq UltraScale+ MPSoC power rail +PS_VBATT is a 1.0V to 1.89V voltage typically supplied by a battery. This supply is typically used to maintain an encryption key in battery-backed RAM for device secure boot. The encryption key can alternatively be stored in eFuse which does not require a battery.

On the UltraZed-EV SOM, +PS_VBATT is interfaced to the JX3 connector relying on the end-user carrier card to properly implement the battery functionality. To apply an external battery to Zynq UltraScale+ MPSoC from the end-user carrier card the proper voltage should be applied to the +PS_VBATT pin on the JX3 connector, JX3-PIN C21.

MIO Name	Package Pin Number	Net Name	JX3 Connector
VCC_PSBATT	U20	+PS_VBATT	JX3.C21

Table 35 – UltraZed-EV SOM +PS_VBATT Connection

NOTE: When the final solution does not require battery backup, the end-user carrier card should tie the +PS_VBATT pin to the appropriate voltage range from +1.0V to +1.8V.

2.16.11 Thermal Management: Heatsink and Fan Assembly

Depending on the end-user application, the performance of the UltraZed-EV SOM will require a thermal solution to help maintain performance across temperature.

The UltraZed-EV SOM comes with an example thermal solution of a 31mm Heatsink and Fan assembly. This active arrangement is secured directly to the Zynq UltraScale+ MPSoC via thermal tape and a 31mm clip solution that is pre-secured to the Zynq UltraScale+ device. A 31mm Heat Sink and a Sunon 5V DC Fan (PN: **MC30100V1-000U-A99**) solution are assembled and shipped with the UltraZed-EV SOM.

The 31mm clip solution arrives pre-secured to the Zynq device from the factory. Please review the installation instructions necessary to secure the heatsink/fan assembly to the clip provided on the UltraZed-EV SOM. The 31mm clip solution provides for a more ruggedly secure thermal solution versus thermal tape only if the end application warrants it.

The active heat sink is powered by connecting a three position connector to the 5V fan mating connector on an end-user carrier card. This 3-pin keyed connector is .100” pitch and has the 5V conductor as pin 2 on the connector. For reference, the fan supplied with the UltraZed-EV SOM mates with the fan header on the UltraZed-EV Carrier Card.

Under most circumstances this 31mm Heatsink and Fan assembly should provide adequate relief across temperature, but it cannot be guaranteed to support all environmental conditions due to lack of knowledge regarding end-users thermal environment and the possible enclosure of the UltraZed-EV SOM. For aggressive applications it is recommended that an accurate worst-case power analysis be performed in order to avoid the pitfalls of over designing or under designing your product’s power and thermal management system.

NOTE: End users should design a custom Heatsink and Fan assembly that is more conducive to the requirements of their system including alternative mounting techniques for the assembly which could enhance the thermal reliability of the system.

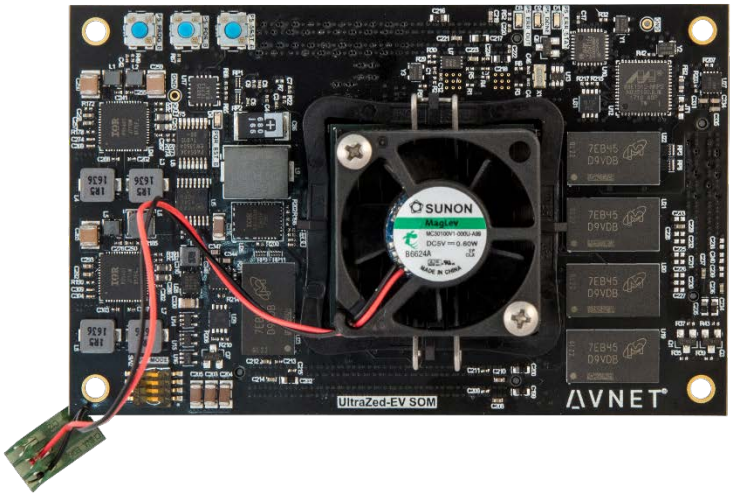

Figure 26 – UltraZed-EV SOM w/ 31mm 5VDC Heat Sink and Fan Assembly

3 Zynq UltraScale+ MPSoC I/O Bank Allocation

3.1 PS MIO Bank Allocation

There are 78 I/O available in the PS MIO Banks. The tables below lists the number of required I/O per peripheral and the MIO locations where the interface exists.

Interface	I/O Required	MIO
QSPI FLASH	12	0-5, 7-12
USB	12	52-63
ETHERNET	14	64-77
eMMC	10	13-22
I2C	2	24-25
TOTAL	**50**	

Table 36 – PS MIO Bank Interface Requirements

The General Purpose I/O assignments aren't specifically defined interfaces such as those that are defined in Table 32. The table below provides the MIO locations of the PS MIO general purpose pins and also MIO pins that support other functions.

Interface	I/O Required	MIO
QSPI FB CLK	1	6
MIO23_INT_N	1	23
General Purpose PS MIO	26	26-77
TOTAL	**28**	

Table 37 – PS MIO Bank Interface Requirements

The end-user is encouraged to utilize the Zynq UltraScale+ MPSoC TRM in defining the MIO peripheral mappings that they would like to utilize on a custom UltraZed Carrier Card.

3.2 Zynq UltraScale+ MPSoC Bank Voltages

The I/O bank voltage assignments are shown in the table below.

Bank	Voltage (default)	Source
PS-Side		
MIO Bank 500	+VCCO_PSIO (1.8V)	SOM
MIO Bank 501	+VCCO_PSIO_501 (ADJ)	Carrier Card
MIO Bank 502	+VCCO_PSIO (1.8V)	SOM
MIO Bank 503	+VCCO_PSIO (1.8V)	SOM
MIO Bank 504	+VCCO_PSDDR4_504 (1.2V)	SOM
MIO Bank 505	+MGTRAVCC / +MGTRAVTT	Carrier Card
PL-Side		
Bank 0	1.8V (Internal)	Zynq UltraScale+
Bank 47	+VCCO_HD_47 (ADJ)	Carrier Card
Bank 48	+VCCO_HD_48 (ADJ)	Carrier Card
Bank 64	+VCCO_HP_64 (ADJ)	Carrier Card
Bank 65	+VCCO_HP_65 (ADJ)	Carrier Card
Bank 66	+VCCO_HP_66 (1.2V)	SOM

Table 38– Zynq Bank Voltage Assignments

PL I/O Banks 47, 48, 64, 65, and 501 are powered from the end-user carrier card. These bank supplies are designed to be independent on the UltraZed-EV SOM. Maximum flexibility is allowed to the designer for these banks as the voltage level and standards are left to the end-user carrier card design. The designer of the end-user carrier card VCCO supplies is provided the choice of whether the IO banks use a shared voltage supply or independent voltage supplies.

When designing a customer end-user carrier card, please review the Zynq UltraScale+ MPSoC data sheet for the appropriate supported bank voltages and tolerances.

4 Specifications and Ratings

This section contains the absolute maximum and the recommended operating ranges for SOM temperature, supply voltages, and I/O voltages. Values listed are those available at the time of publication. Users may want to consult the latest device manufacturer's specifications if their application approaches any of the limits.

4.1 Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes	Reference Document
Storage Temperature	-40	85	°C		

Table 39 – Absolute Maximum Temperature Rating

Parameter	Min	Max	Units	Notes	Reference Document
SOM					
VIN	-0.3	16.0	V		UltraZed-EV Designer's Guide
*Sense	-	-	V	Voltage Sense outputs- Do not drive from carrier	
Xilinx Zynq UltraScale+					
+PS_VBATT	-0.5	2.0	V	VCC_PSBATT – supply for battery backed BRAM and RTC	Xilinx Datasheet DS925
+VCCO_PSIO_501	-0.5	3.63	V	Supply voltage for PS MIO bank 501	
+VCCO_HD_*	-0.5	3.4	V	PL supply voltage for HD I/O bank 47, 48	
+VCCO_HP_*	-0.5	2.0	V	PL supply voltages for HP I/O banks 64, 65	
+MGTRAVCC	-0.5	1.0	V	PS-GTR supply voltage	
+MGTRAVTT	-0.5	2.0	V	PS-GTR termination voltage	
+MGTAVCC	-0.5	1.0	V	GTH supply voltage	
+MGTAVTT	-0.5	1.3	V	GTH termination voltage	
+MGTVCCAUX	-0.5	1.9	V	GTH Auxiliary analog Quad PLL (QPLL) voltage	
Peripheral Devices					
USB_VBUS_OTG	-0.5	6.0	V	Resistor required on carrier	Microchip Datasheet USB3320

Table 40 – Absolute Maximum Ratings for Supply Voltages

Parameter	Min	Max	Units	Notes	Reference Document
SOM Control / Handshaking					
SOM_RESET_IN_N	-0.5	6.5	V		UltraZed-EV Designer's Guide
CC_RESET_OUT_N	0	50	V	This is an open-drain output with pull up required on the Carrier Card.	
SOM_PG_OUT	-0.3	N/A	V	Open-drain signal. Do not drive high by the Carrier Card	
PMBus_ALERT_N	-0.3	5.3	V	Open-drain output from SOM with 2 KΩ pull-up to 3.3V on the SOM	
PMBus_SCL	-0.3	5.3	V		
PMBus_SDA	-0.3	5.3	V		
CC_INT_N	-0.5	7.0	V		
CC_SDA	-0.5	7.0	V		
CC_SCL	-0.5	7.0	V		
Xilinx Zynq UltraScale+					
SYSMON*	-0.5	2.35	V	Bank0	Xilinx Datasheet DS925
JTAG_*	-0.5	2.35	V	Bank 503	
HP_DP_[00:23]*	-0.5	+VCCO_HP_64 + 0.55	V	Bank 64	
HP_DP_[24:47]*	-0.5	+VCCO_HP_65 + 0.55	V	Bank 65	
HD_SE_[00:11]*	-0.5	+VCCO_HD_48 + 0.55	V	Bank 48	
HD_SE_[12:23]*	-0.5	+VCCO_HD_47 + 0.55	V	Bank 47	
HP_SE_[00:03]	-0.5	+VCCO_HP_64 + 0.55	V	Bank 64	
HP_SE_[04:07]	-0.5	+VCCO_HP_65 + 0.55	V	Bank 65	
MIO*	-0.5	+VCCO_PSIO_501 + 0.55	V	Bank 501	
GTR_TX*/GTR_RX*	-0.5	1.2	V	Bank 505	
GTR_REFCLK*	-0.5	2.0	V	AC coupled - Bank 505	
GTH*_TX/GTH*_RX	-0.5	1.25	V	Quad 224, Quad 225, Quad 226, Quad 227	
GTH_REFCLK*	-0.5	2.0	V	AC coupled - Quad 224, Quad 225, Quad 226, Quad 227	
Peripheral Devices					
ETH_MD*	-	-	V		88E1512 Datasheet
ETH_LED*	-0.3	+VDDO + 0.6	V		
USB_ID	-0.5	6.0	V		Microchip Datasheet USB3320
USB_OTG*	-0.5	6.0	V		
USB_OTG_CPEN	-0.5	6.0	V		

Table 41 – Absolute Maximum Ratings for I/O Voltages

4.2 Recommended Operating Conditions

Parameter	Min	Max	Units	Notes	Reference Document
E-Grade SOM	0	85	°C	Zynq UltraScale+ Tj < 100°C Micron DDR4 Tc < 95°C USB3320 Tj < 100°C	Xilinx Datasheet DS925 Micron Datasheet Microchip Datasheet USB3320
I-Grade SOM	-40	85	°C	Zynq UltraScale+ Tj < 100°C Micron DDR4 Tc < 95°C[1] USB3320 Tj < 100°C.	

Table 42 – Recommended Ambient Operating Temperature

Parameter	Min	Max	Units	Notes	Reference Document
SOM					
VIN	5.0	12.0	V		UltraZed-EV Designer's Guide
*Sense	-	-	V	Voltage Sense outputs- Do not drive from carrier	
Xilinx Zynq UltraScale+					
+PS_VBATT	1.2	1.5	V	VCC_PSBATT – supply for battery backed BRAM and RTC	Xilinx Datasheet DS925
+VCCO_PSIO_501	1.71	3.465	V	Supply voltage for PS MIO bank 501	
+VCCO_HD_*	1.14	3.4	V	PL supply voltage for HD I/O bank 47, 48	
+VCCO_HP_*	0.95	1.9	V	PL supply voltages for HP I/O banks 64, 65	
+MGTRAVCC	0.825	0.875	V	PS-GTR supply voltage	
+MGTRAVTT	1.746	1.854	V	PS-GTR termination voltage	
+MGTAVCC	0.873	0.927	V	GTH supply voltage	
+MGTAVTT	1.164	1.236	V	GTH termination voltage	
+MGTVCCAUX	1.746	1.854	V	GTH Auxiliary analog Quad PLL (QPLL) voltage	
Peripheral Devices					
USB_VBUS_OTG	0	5.5	V	Resistor required on carrier	Microchip Datasheet USB3320

Table 43 – Recommended Supply Voltages

[1] Enable temperature-controlled refresh mode if T_c exceeds 85°C.

Parameter	Dir[2]	Min	Max	Units	Notes	Reference Document
SOM Control / Handshaking						
SOM_RESET_IN_N	I	0	+VCCO_PSIO_501	V	This signal has a 10KΩ pullup to +VCCO_PSIO on the SOM	
CC_RESET_OUT_N	Open-drain	0	3.3	V	This is an open-drain output with a pull-up required on the Carrier Card	
SOM_PG_OUT	Open-drain	0	N/A	V	This is an open-drain signal with 10KΩ pull-up to 3.3V on the SOM. Do not drive high from the Carrier Card	
PMBus_ALERT_N	O	0	4.0	V	Open-drain output from SOM with 2 KΩ pull-up to 3.3V on the SOM	UltraZed-EV Designer's Guide
PMBus_SCL	IO	0	3.3	V	2 KΩ pull-up to 3.3V on the SOM if JP3 installed	
PMBus_SDA	IO	0	3.3	V	2 KΩ pull-up to 3.3V on the SOM if JP2 installed	
CC_INT_N	I	0	3.0	V	Pull up to 1.8V, 2.5V, or 3.3V on carrier card	
CC_SDA	IO	0	5.5	V		
CC_SCL	O	0	5.5	V	Open-drain output. Pull up to 1.8V, 2.5V, or 3.3V on carrier card	
Xilinx Zynq UltraScale+						
JTAG_TCK	I	-0.2	2.0	V	Bank 503 I/O voltage set to 1.8V on SOM	
JTAG_TDI	I	-0.2	2.0	V		
JTAG_TDO	O	0	1.8	V		
JTAG_TMS	I	-0.2	2.0	V		
SYSMON*	I	See System Monitor Guide UG580			VCC_PSADC set to 1.8V on SOM	Xilinx Datasheet DS925
HP_DP_[00:23]*	IO	-0.2	+VCCO_HP_64 + 0.2	V	Bank 64 I/O voltage set by carrier	
HP_DP_[24:47]*	IO	-0.2	+VCCO_HP_65 + 0.2	V	Bank 65 I/O voltage set by carrier	
HD_SE_[00:11]*	IO	-0.2	+VCCO_HD_48+ 0.2	V	Bank 48 I/O voltage set by carrier	Xilinx System Monitor Guide UG580
HD_SE_[12:23]	IO	-0.2	+VCCO_HD_47 + 0.2	V	Bank 47 I/O voltage set by carrier	
HP_SE_[00:03]	IO	-0.2	+VCCO_HP_64 + 0.2	V	Bank 64 I/O voltage set by carrier	
HP_SE_[04:07]	IO	-0.2	+VCCO_HP_65 + 0.2	V	Bank 65 I/O voltage set by carrier	
MIO*	IO	-0.2	+VCCO_PSIO_501 + 0.2	V	Bank 501 I/O voltage set by carrier	
GTR_TX*/GTR_RX*	IO	0.075	+MGTRAVCC	V	Bank 505 I/O voltage set by carrier	
GTR_REFCLK*	IO	0.25	2.0	V	AC coupled. Bank 505 I/O voltage set by carrier	
GTH*_TX/GTH*_RX	IO	0.15	1.25	V	Quad 224, Quad 225, Quad 226, Quad 227 I/O voltage set by carrier	
GTH_REFCLK*	IO	0.25	2.0	V	AC coupled - Quad 224, Quad 225, Quad 226, Quad 227 I/O voltage set by carrier	

[2] "Dir" is the Direction of the signal relative to the SOM. For example, SOM_RESET_IN_N is listed as "I" which is Input to the SOM; therefore, this signal is an output from the Carrier.

Peripheral Devices						
ETH_MD*	IO	See 88E1512 Datasheet and UltraZed-EV Designer's Guide for details				88E1512 Datasheet
ETH_PHY_LED	O					
USB_ID	I	0	3.3	V		Microchip Datasheet USB3320
USB_OTG*	IO	0	3.3	V	DM/DP on USB3320	
USB_OTG_CPEN	O	0	3.3	V	External 5V supply enable	

Table 44 – Recommended I/O Voltages

5 Mechanical

The UltraZed-EV SOM measures 2.25” x 4.00” (57.15 mm x 101.6 mm).

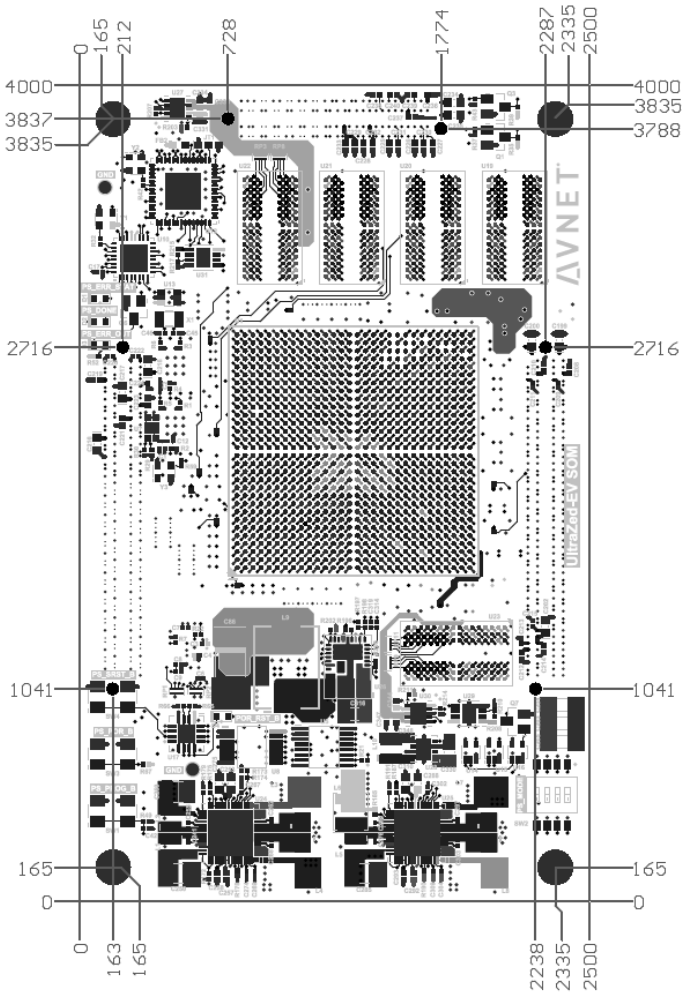

Figure 27 – UltraZed-EV SOM Top View Mechanical Dimensions (mils)

The UltraZed-EV SOM has a maximum vertical dimension of 0.607” (15.42 mm).

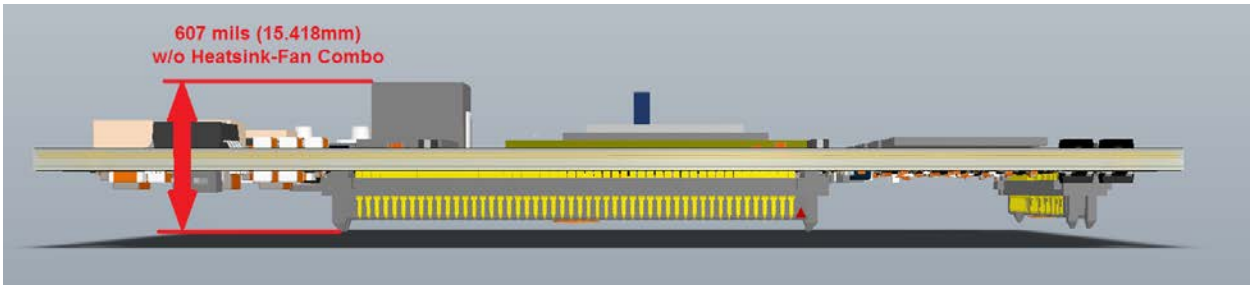

Figure 28 – UltraZed-EV SOM Side View Mechanical Dimensions

The UltraZed-EV SOM is delivered with an active fan (10.0 mm) and heatsink (14.5 mm) combination that has a vertical dimension of 965 mils (24.5 mm). The heatsink is available in a three other vertical sizes (9.5 mm, 19.5 mm, and 24.5 mm). The fan is available in a two other vertical sizes (6.9 mm and 15.0 mm).

The fan delivered with the UltraZed-EV SOM is designed to provide good thermal performance in a vertical size that is less than 1000 mils. The vertical dimension of the combination of the fan, heatsink, PCB, and connectors is 1334 mils (33.88 mm) and is documented below.

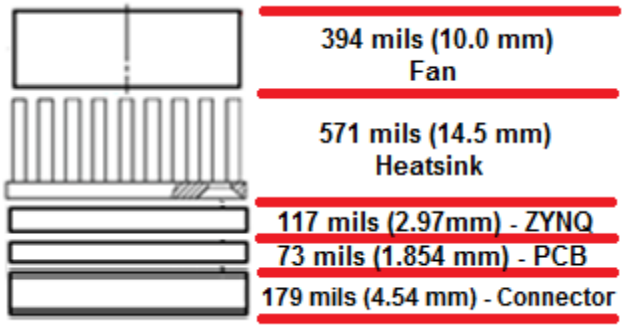

Figure 29 – UltraZed-EV SOM Overall Vertical Dimension

The minimum vertical dimension of the fan and heatsink combination using the smallest heatsink and smallest fan is 646 mils (16.4 mm) and the maximum vertical dimension of the fan and heatsink combination using the largest heatsink and largest fan is 1555 mils (39.5 mm).

Figure 30 – UltraZed-EV SOM Fan and Heatsink MIN/MAX Combinations

NOTE: The above figures do not show the additional hardware required to bolt the fan to the heatsink. This additional hardware coincides with additional height to the solution accounting for the head of the screw.