Design Guide: TIDA-01393

Power Reference Design for Xilinx® Zynq® UltraScale+™ MPSoC Applications

Description

This reference design is a configurable power solution designed to handle the entire Xilinx® Zynq® UltraScale+ (ZU+) family of MPSoC devices across various use cases. The various versions of the TPS65086x PMIC allow this design to power devices from the basic ZU2CG device with a dual-core Arm® Cortex®-A53 application processor and dual-core Arm Cortex-R5 real-time processor to the higher end ZU7EV, ZU19EG, and ZU21DR devices, which add other components to the MPSoC such as a graphics processing unit, video Codec unit and up to 16 16.3-Gbps transceivers. This design includes many additional components that can be used with the TPS65086x device such as external load switches, pre-regulators, and a push button circuit.

Resources

TIDA-01393	Design Folder
TPS650864	Product Folder
TPS650861	Product Folder
CSD87381P	Product Folder
TPS22920	Product Folder
LMR64010	Product Folder
TPS54308	Product Folder
SN74LVC1G175	Product Folder
SN74LVC1G17	Product Folder
SN74LVC1G14	Product Folder

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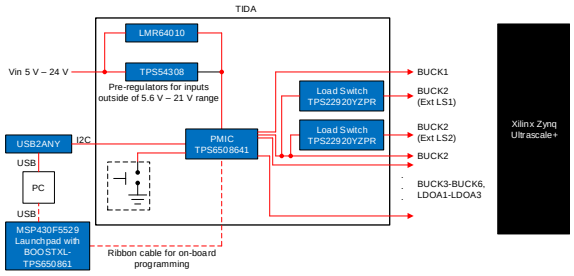
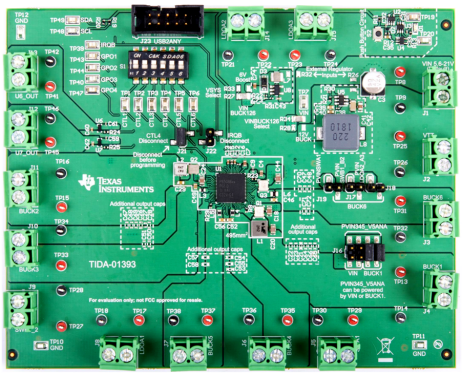
Features

- 10 programmable output rails
  - 3 BUCK converters, 3 BUCK controllers, 3 LDOs, 1 VTT LDO for DDR memory termination
- 5 load switches
  - 3 internal to TPS65086x device, 2 external TPS22920 load switches
- Wide input voltage range (5 V to 24 V)
- 4 GPOs
- Sequencing control with 6 CTL pins, or I^2C

Applications

- Factory automation and control
- Single board computer
- Computer on module
- Industrial robot CPU board
- Machine vision: vision computer
- Programmable logic controller (PLC): CPU PLC controller
- Industrial monitor
- Test and measurement





1 System Description

While this reference design is designed to handle the entire Xilinx® Zynq® UltraScale+ (ZU+) family of MPSoC devices across various use cases, the default configuration for this device uses the TPS6508641 PMIC device, and is targeted at powering the ZU3EG MPSoC. This design is by default made to follow the power map shown in Figure 5, which offers full power domain flexibility. Many of the external components such as the output inductors chosen for this reference design are designed to be similar to the Ultra96 Zynq UltraScale+ ZU3EG Development Board. Schematics for this design can be found here. External components can be adjusted to fit different use cases, and the PMIC itself can even be swapped out with different variants of the TPS65086x PMIC device.

1.1 Key System Specifications

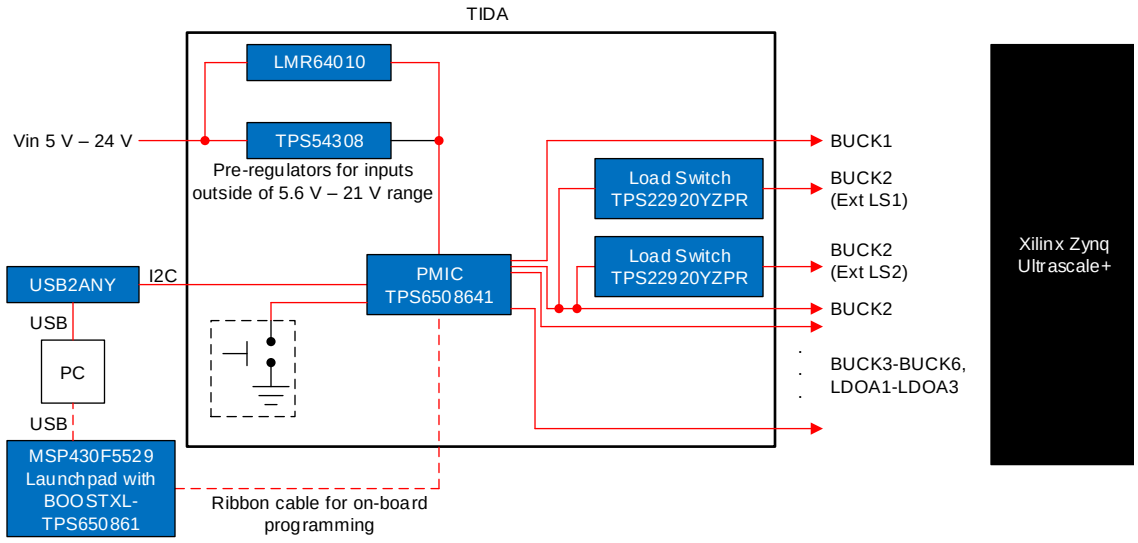
Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Input Power Source	DC 5 V to 24 V, depending on configuration	Section 2.2.5
BUCK1	5 V ±5%	Section 2.2.1
BUCK2	0.85 V ±5%	Section 2.2.1
BUCK3	1.1 V / 1.2 V ±3%, 3 A	Section 2.2.1
BUCK4	3.3 V ±3%, 3 A	Section 2.2.1
BUCK5	1.2 V ±3%, 3 A	Section 2.2.1
BUCK6	1.8 V ±3%	Section 2.2.1
LDOA1	1.8 V ±2%, 200 mA	Section 2.2.1
LDOA2	1.2 V -2% +3%, 600 mA	Section 2.2.1
LDOA3	1.2 V -2% +3%, 600 mA	Section 2.2.1
VTT LDO	0.9 V ±25 mV, 1.8 A	Section 2.2.1
SWA1	3.3 V, 300 mA	Section 2.2.1
SWB1/SWB2, SWB1_2	1.8 V, 400 mA (800 mA, combined)	Section 2.2.1
U6_OUT	0.85 V ±5%, 4 A	Section 2.2.4
U7_OUT	0.85 V ±5%, 4 A	Section 2.2.4
Operating Ambient Temperature	-40°C to +85°C	TPS650864 datasheet
Solution Size	495mm^2	Figure 14

2 System Overview

2.1 Block Diagram

Figure 1. TIDA-01393 Block Diagram



2.2 Design Considerations

This design has a lot of components that can be modified to fit different use cases. All of these components are broken down in this section.

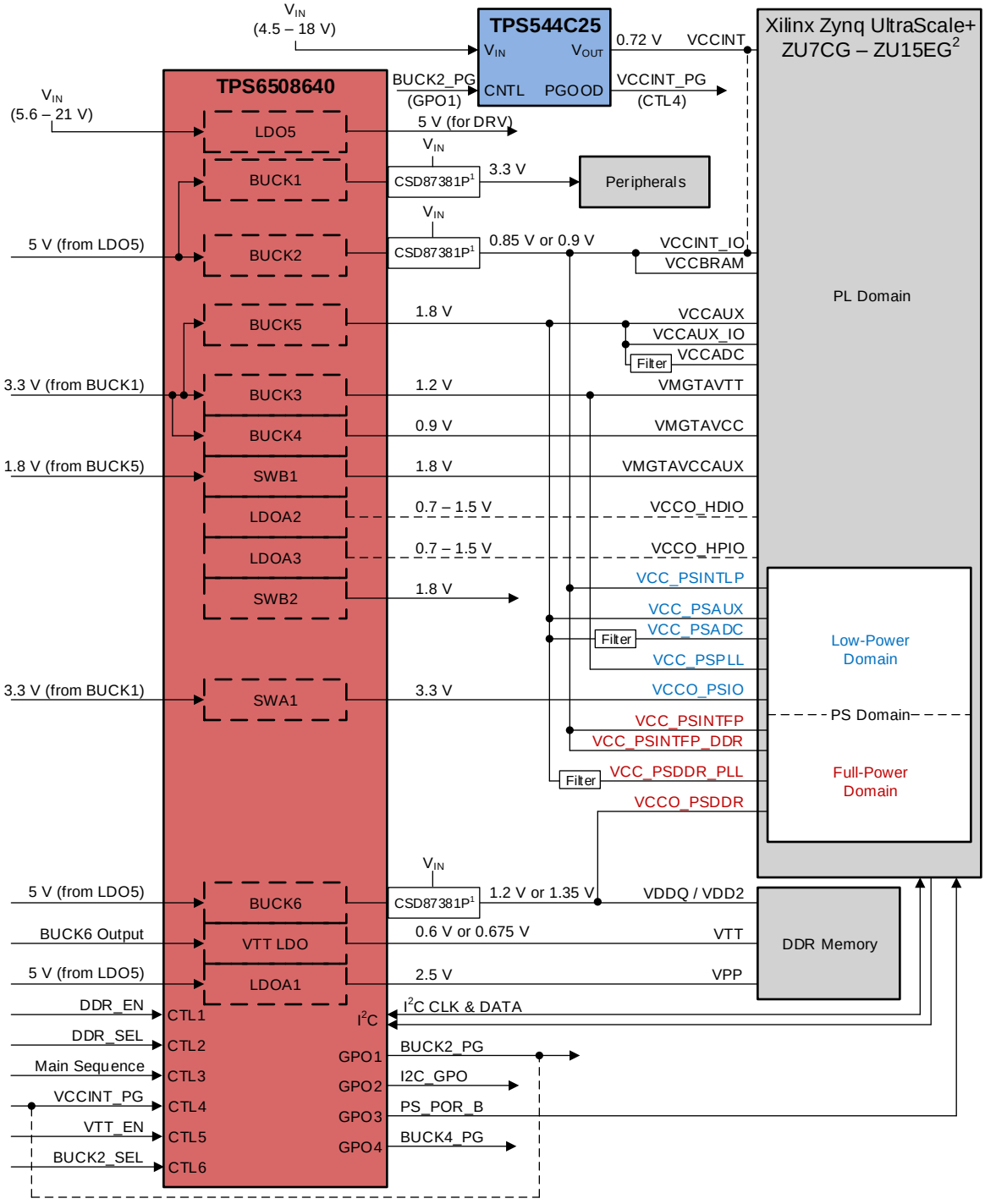
2.2.1 TPS650864 Variants

The TPS65086x PMIC device uses one-time-programmable (OTP) memory, which is programmed at the factory to specific settings depending on the requirements of the design. There are multiple pre-defined OTPs of the TPS65086x PMIC device under the TPS650864x family, which are designed for different uses cases and MPSoCs. Table 2 shows the voltage settings for all of the TPS650864x variants. The specific variant used for this design is the TPS6508641. The power maps for these various pre-defined variants are shown in Figure 2 through Figure 6. While most of these power maps are focused on the Xilinx® Zynq® UltraScale+ (ZU+) family of MPSoC devices, the flexibility of the TPS65086x PMIC device makes it a good option for other MPSoCs and FPGAs as well. Please see the TPS650864 datasheet for more information on these pre-defined OTPs.

Table 2. TPS650864x Variants

PART NUMBER	APPLICATION	BUCK1	BUCK2	BUCK3	BUCK4	BUCK5	BUCK6	LDOA1	LDOA2	LDOA3	Power Map
TPS6508640	Xilinx Zynq Ultrascale+ ZU6 - ZU15	3.3 V (25 mV)	0.85 V, 0.9 V (10 mV)	1.2 V (25 mV)	0.9 V (25 mV)	1.8 V (25 mV)	1.2 V, 1.35 V (10 mV)	2.5 V	1.5 V	1.2 V	Figure 2
TPS65086401	Xilinx Zynq Ultrascale+ ZU2 - ZU5	1.8 V (25 mV)	0.85 V (10 mV)	0.85 V (25 mV)	3.3 V (25 mV)	3.3 V (25 mV)	1.5 V, 1.2 V, 1.1 V (10 mV)	1.8 V	1.2 V	1.2 V	Figure 3
TPS6508641	Xilinx Zynq Ultrascale+ ZU2 - ZU5	Ext FB	0.85 V (10 mV)	1.1 V, 1.2 V (25 mV)	3.3 V (25 mV)	1.2 V (25 mV)	1.8 V (25 mV)	1.8 V	1.2 V	1.2 V	Figure 4
TPS65086470	Xilinx Artix 7	1 V (10 mV)	1.8 V (25 mV)	1.2 V (25 mV)	2.5 V (25 mV)	3.3 V (25 mV)	1.35 V, 1.5 V (25 mV)	1.8 V	0.7 V	0.7 V	Figure 6

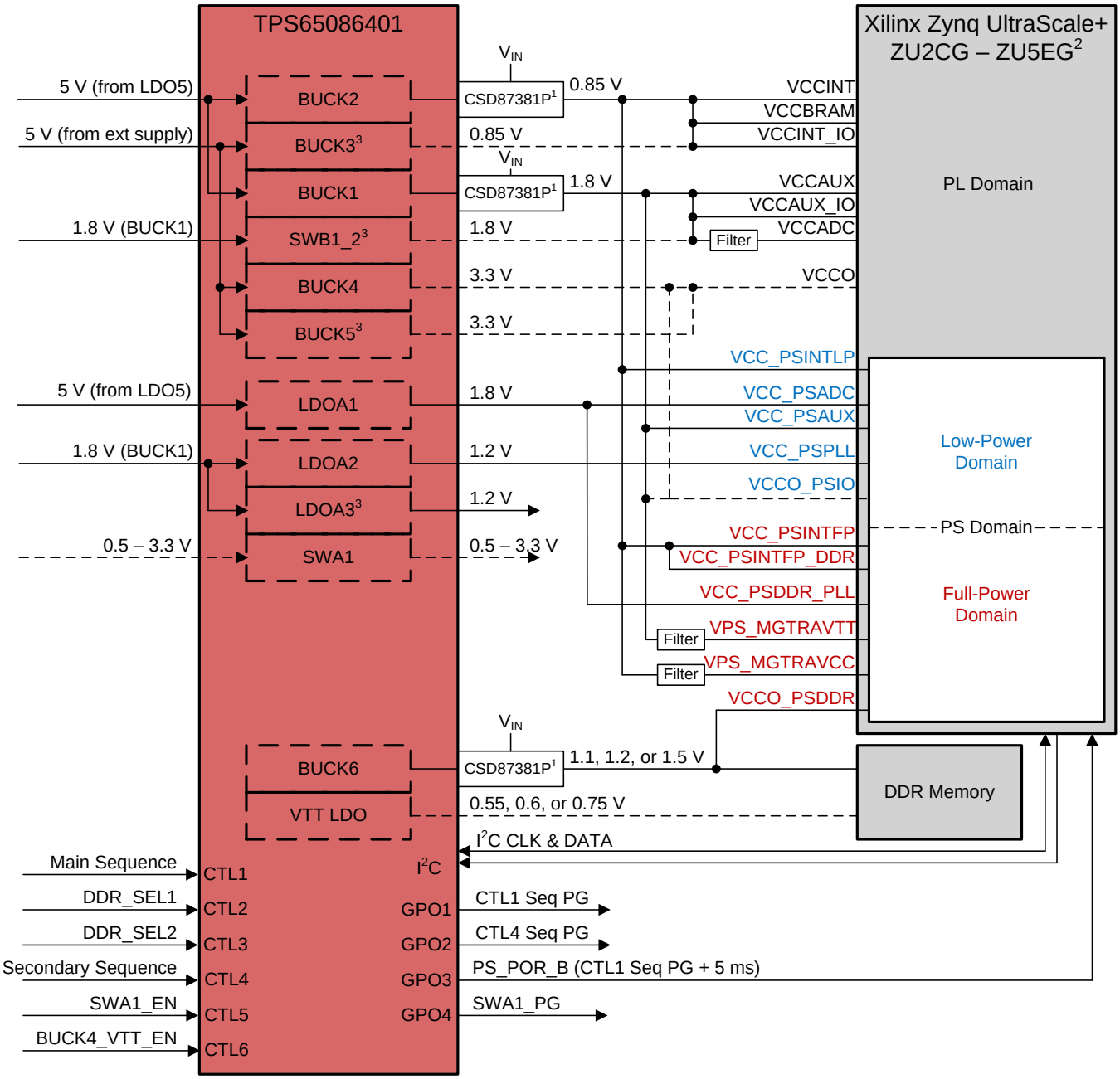
Figure 2. TPS6508640 Power Map Example



(1) External FETs can be scaled to meet the current requirements of each design; CSD87381P is suitable up to approximately 15 A.

(2) The TPS6508640 is not limited to the ZU7CG - ZU15EG. It can support other Ultrascale+ devices as long as the use case does not exceed the maximum specifications of the TPS6508640.

Figure 3. TPS65086401 Power Map Example

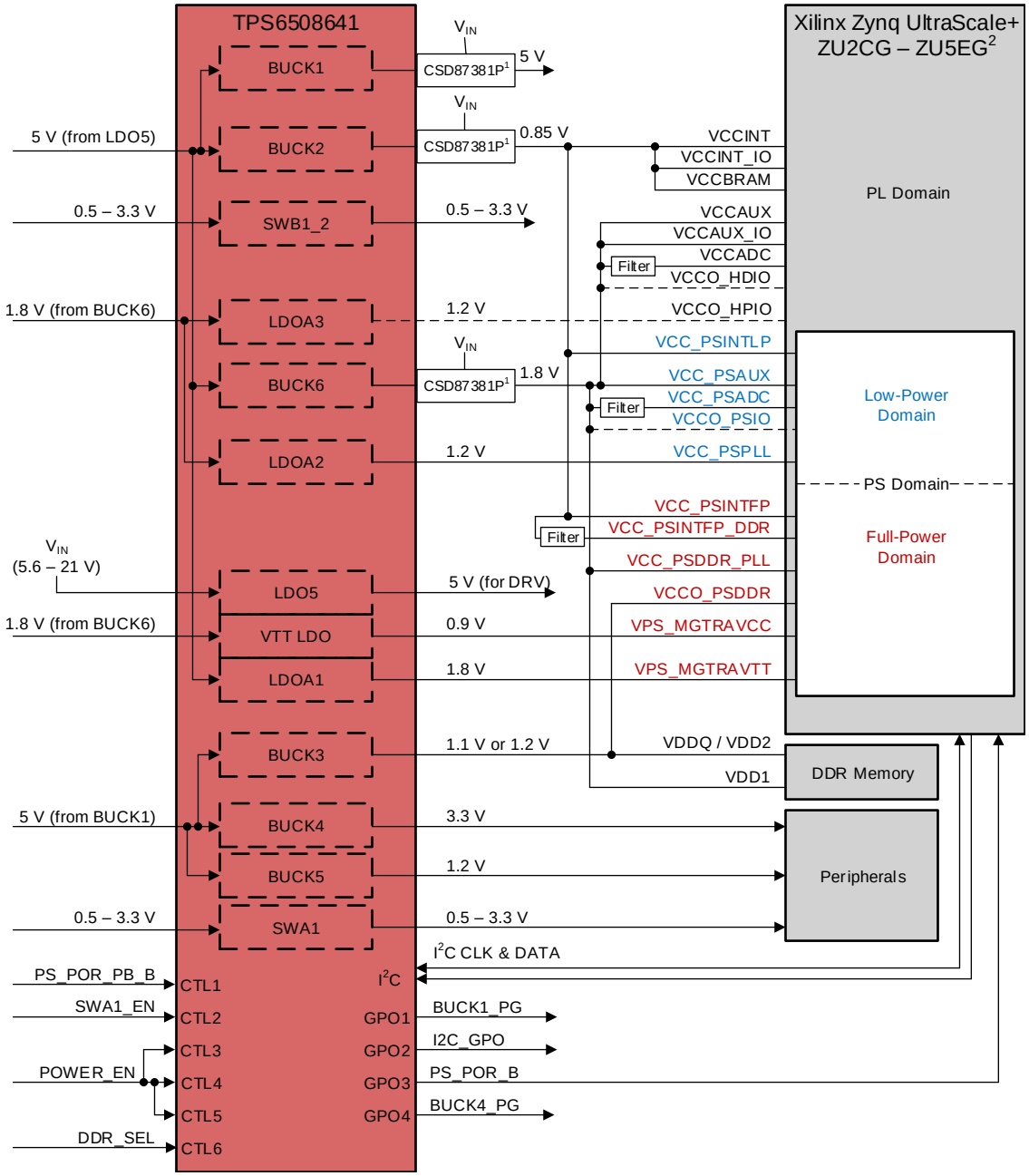


(1) External FETs can be scaled to meet the current requirements of each design; CSD87381P is suitable up to approximately 15 A.

(2) The TPS65086401 is not limited to the ZU2CG - ZU5EG. It can support other Ultrascale+ devices as long as the use case does not exceed the maximum specifications of the TPS65086401.

(3) PL Domain can be optionally powered by BUCK3, SWB1_2, BUCK5, and LDOA3 to allow it to be enabled and disabled by CTL4. This applies only to use cases where VCCINT current is less than 3 A.

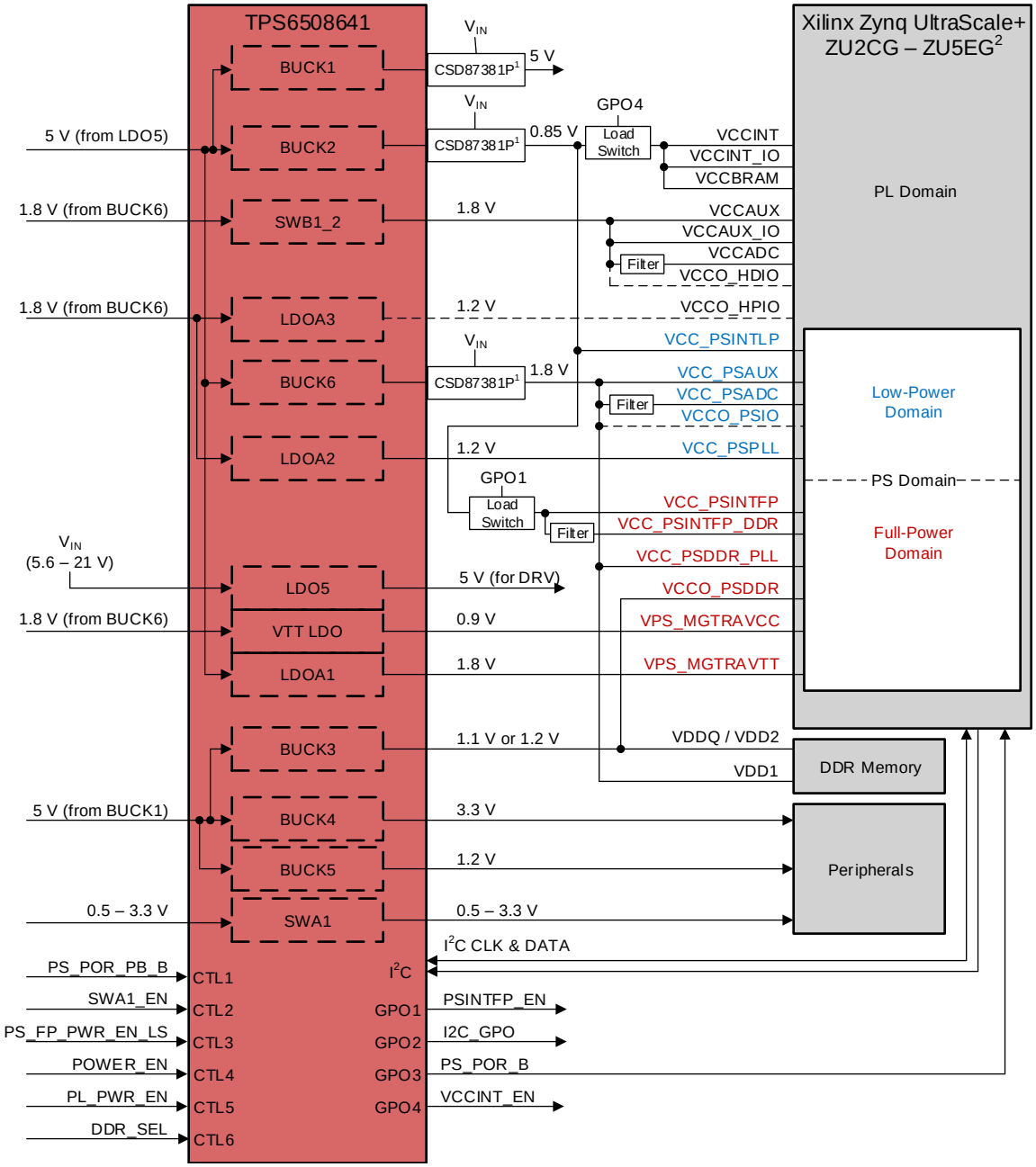
Figure 4. TPS6508641 Always-On Power Map Example



(1) External FETs can be scaled to meet the current requirements of each design; CSD87381P is suitable up to approximately 15 A.

(2) The TPS6508641 is not limited to the ZU2CG - ZU5EG. It can support other Ultrascale+ devices as long as the use case does not exceed the maximum specifications of the TPS6508641.

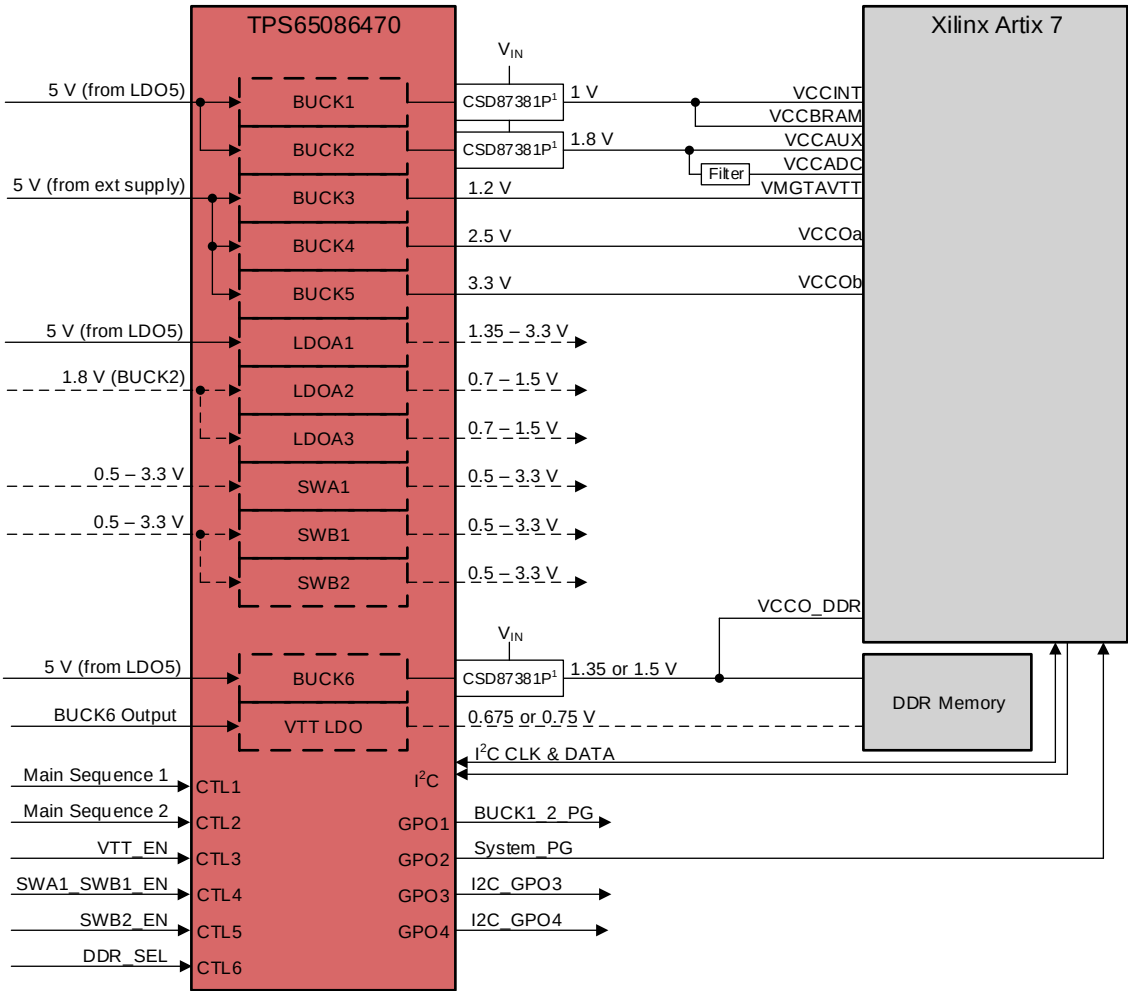
Figure 5. TPS6508641 Full Power Domain Flexibility Power Map Example



(1) External FETs can be scaled to meet the current requirements of each design; CSD87381P is suitable up to approximately 15 A.

(2) The TPS6508641 is not limited to the ZU2CG - ZU5EG. It can support other Ultrascale+ devices as long as the use case does not exceed the maximum specifications of the TPS6508641.

Figure 6. TPS65086470 Power Map Example



(1) External FETs can be scaled to meet the current requirements of each design; CSD87381P is suitable up to approximately 15 A.

2.2.2 The User Programmable TPS65086100

For designs that require different OTP settings on the TPS65086x PMIC device than what is available in the pre-defined OTPs there are a few options. The first option is to get a new OTP defined that will be programmed in at the factory. The second option is to use one of the pre-defined OTPs, and change the settings as needed through I²C communication. The third option is to use the user-programmable version of the TPS65086x, the TPS65086100. This version of the TPS65086x PMIC device is designed to have the OTP memory programmed by the user to fit their specific design requirements. Please see the TPS650861 datasheet, and TPS65086100 Non-Volatile Memory Programming Guide for more information on this device.

The two ways to program this device in a final production setting is either through a 3rd party programming vendor, or by programming on the end-product after PCB assembly. This design includes a ribbon cable connector, labeled J20 which can be used to connect this design to the BOOSTXL-TPS650861 BoosterPack programming board. Once soldered to the PCB the ribbon cable connector can be used for programming the TPS65086100, similar to how it could be programmed on the end-product after PCB assembly. It is recommended to first program the TPS65086100 in the programming board socket to confirm the settings are correct before soldering it to the PCB. Please refer to the BOOSTXL-TPS650861 EVM User's Guide for more information on this programming board.

The OTP Generator excel sheet is a tool used to generate all of the I²C commands that are needed for programming the TPS65086100, based on the settings that are chosen by the user. There are also pre-filled versions of the OTP Generator that have the settings filled in to match other OTP variants such as the TPS6508641, TPS6508640, and TPS65086401. All of these pre-filled OTP Generators can be found in the technical documents of the TPS650861 product folder on TI.com. Table 3 shows which PMIC devices can be used to cover different Xilinx SoCs. While there are pre-defined variants for different SoCs, the user-programmable version of the TPS65086x PMIC device can be used across a very wide range of SoCs.

Table 3. Xilinx Devices Powered by TPS65086x Family

Xilinx Family	Zynq-7000 Artix-7	Zynq-7000 Kintex	ZU+ MPSoC CG		ZU+ MPSoC EG			ZU+ MPSoC EV	ZU+ RFSoCs[1]
Device Names	XC7Z007S to XC7Z020	XC7Z030 to XC7Z100	ZU2CG to ZU5CG	ZU6CG to ZU9CG	ZU2EG to ZU5EG	ZU6EG to ZU15EG	ZU17EG to ZU19EG	ZU4EV to ZU7EV	ZU21DR
TPS65086470	X								
TPS65086401/ TPS6508641			X		X				
TPS6508640				X		X			X
TPS650861	X	X	X	X	X	X	X	X	X

(1) For RFSoCs above ZU21DR (ZU25DR, ZU27DR, ZU28DR, and ZU29DR), additional RF power regulators should be added. An example of this is to use TPS7A8300 to power ADC_AVCC, TPS7A84 for DAC_AVCC, and three TPS62097s for ADC_AVCCAUX, DAC_AVCCAUX, and DAC_AVTT.

2.2.3 Controller Design Procedure

The TPS65086x PMIC device has 3 BUCK controllers with external FETs, allowing for the device to handle a wide range of load requirements. The external FETs can be chosen based on maximum load current so that the higher load requirements can be met, while reducing board area for the rails with lower load requirements. TI's CSD85301Q2, CSD87331Q3D, CSD87381P, CSD87588N, and CSD87350Q5D devices are recommended for the controllers, depending on the required maximum current. The default FETs used for this design are the CSD87381P. In addition to the external FETs, the output inductors, output capacitors, and other passive components can all be adjusted based on the design requirements. Please refer to the TPS650864 datasheet for more information on how to choose the right components to fit specific design requirements.

2.2.4 External Load Switches

In some use cases, such as the one shown in Figure 5 external load switches are required to allow for more flexibility in the power domain control. This is most common for battery powered applications, and other applications where independent control over the different power domains is required to achieve higher efficiency. This design uses two of the TPS22920 load switches to achieve this increased flexibility in the power domain. In this design the load switches are controlled using GPO1 and GPO4, and the load switch input is coming from the BUCK2 output. This is identical to the power map shown in Figure 5.

2.2.5 Pre-Regulators (LMR64010 and TPS54308)

The input voltage range of the TPS65086x PMIC device is 5.6 V to 21 V. In some cases it may be desired to power the PMIC from a 5 V supply or a 24 V supply, which requires an additional pre-regulator to keep the PMIC input voltage within the 5.6 V to 21 V range. This section will go through the two regulators that are available in this design for pre-regulation of the input voltage.

2.2.5.1 Input Voltages <5.6 V (LMR64010)

The LMR64010 is used for input voltages that are below 5.6 V. This regulator is a boost converter that will boost the input voltage to 6 V so that it can be used to power the VSYS pin of the TPS65086x PMIC device. The input of this boost converter can be connected to the input of the board by populating R32 with a 0Ω resistor. The output of this boost converter can be connected to the VSYS pin by populating R33 with a 0Ω resistor.

2.2.5.2 Input Voltages >21 V (TPS54308)

The TPS54308 is used for input voltages that are above 21 V. This regulator is a buck converter that will bring the input voltage to 12 V so that it can be used to power the VSYS pin and the BUCK controller inputs of the TPS65086x PMIC device. The input of this buck converter can be connected to the input of the board by populating R26 with a 0Ω resistor. The output of this boost converter can be connected to the buck controller inputs and VSYS pin by populating R28 and R27 with a 0Ω resistor.

Table 4. Resistors to Populate Based on Input Voltage

Vin	R26	R27	R28	R32	R33	R34
< 5.6 V				X	X	X
5.6 V - 21 V		X				X
> 21 V	X	X	X			

2.2.6 Push-Button Circuit

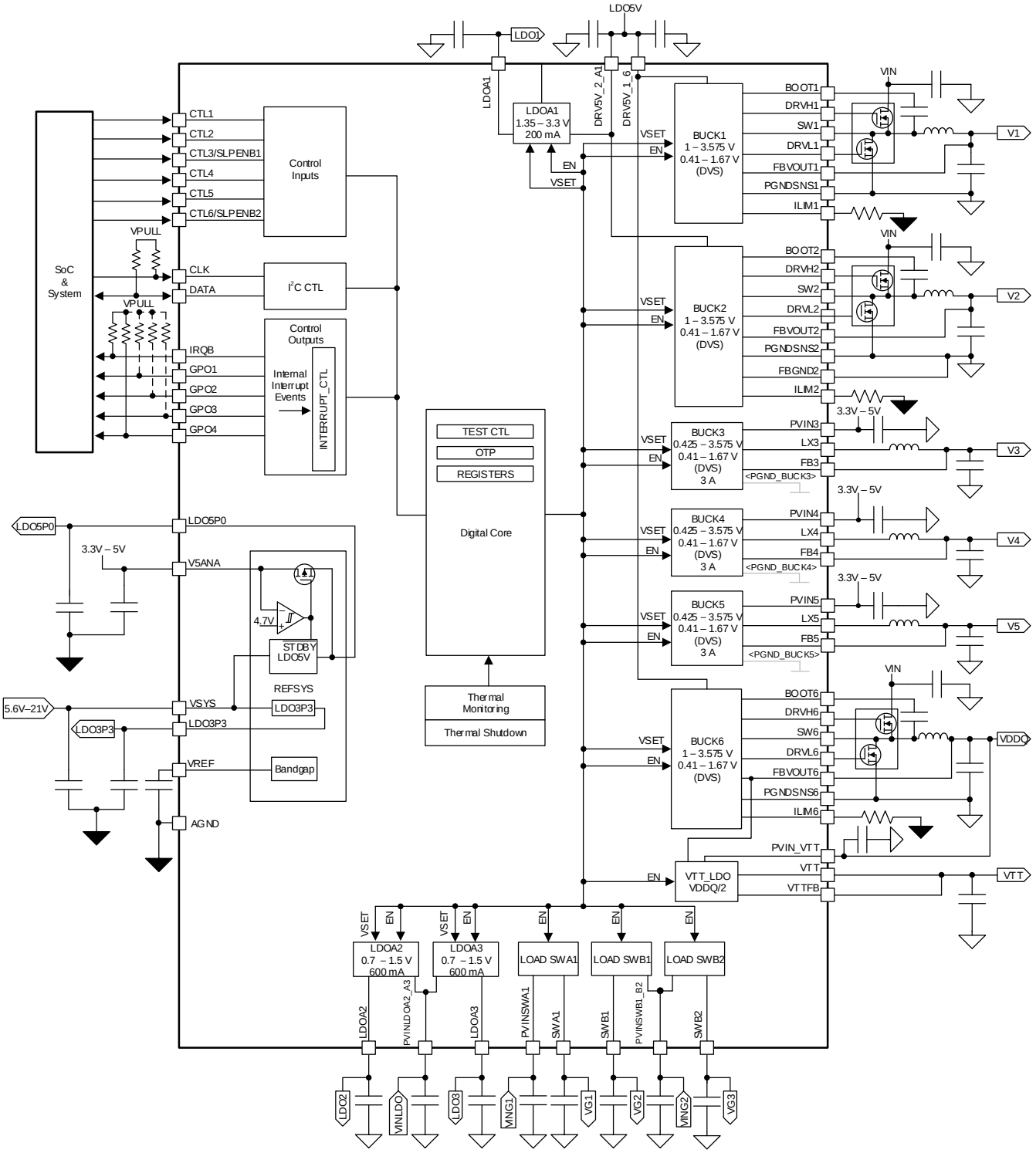
The push-button circuit included in this design in commonly used to turn on and shut down the outputs of the PMIC. This circuit can be used to turn on the PMIC outputs by setting the CTL1 pin high on a short key press, and turn off the PMIC outputs by setting the CTL1 pin low on a long key press. Please refer to the Push-Button Circuit app note for more information on how this circuit works.

2.3 Highlighted Products

2.3.1 TPS65086x

The TPS65086x is a highly versatile PMIC device that can provide system power for a wide variety of applications with 3 BUCK converters, 3 BUCK controllers, 3 general purpose LDOs, 3 load switches, and a VTT LDO for DDR memory termination. The BUCK controllers provide flexible power capable of up to 30A. External FETs can be made larger for high power designs, but can scale down in both size and cost for smaller designs. Voltage levels, sequencing, and other settings are defined in pre-programmed OTP memory, but can be modified using the I^2C interface. The D-CAP2™ and DCS-Control high-frequency voltage regulators use small passives to achieve a small solution size. The D-CAP2 and DCS-Control topologies have excellent transient response performance, ideal for processor core and system memory rails that have fast load switching. The PMIC comes in an 8-mm × 8-mm, single-row VQFN package with thermal pad for good thermal dissipation.

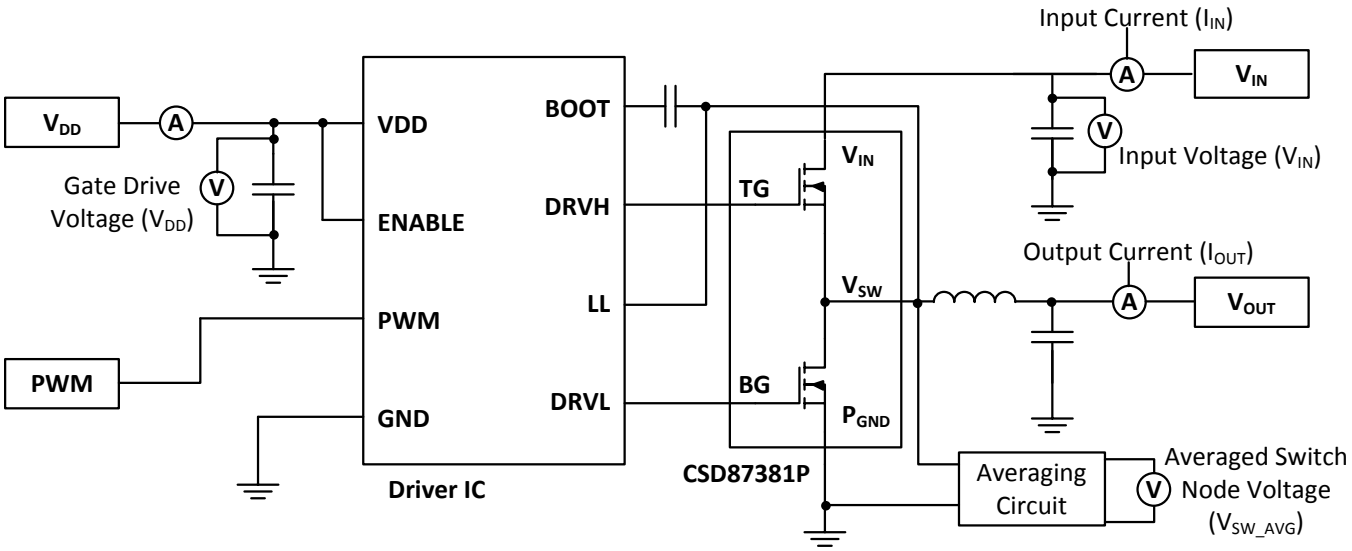
Figure 7. TPS65086x Functional Block Diagram



2.3.2 CSD87381P

The CSD87381P NexFET™ power block II is a highly optimized design for synchronous buck applications offering high current and high efficiency capability in a small 3 mm × 2.5 mm outline. Optimized for 5 V gate drive applications, this product offers an efficient and flexible solution capable of providing a high density power supply when paired with any 5 V gate driver from an external controller/driver. The CSD87381P is capable of supporting loads up to 15 A, but this device can be swapped out with other parts depending on if the load current is expected to be higher or lower.

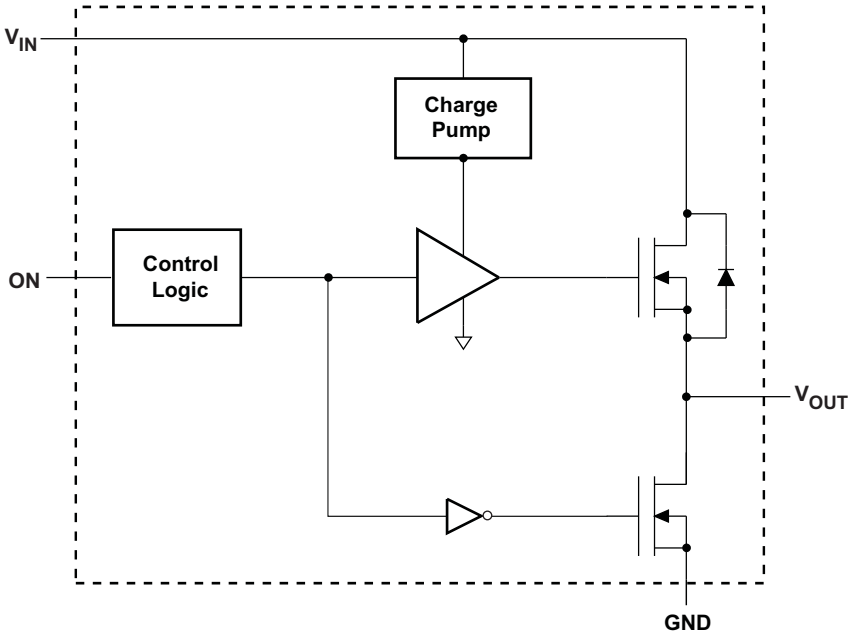
Figure 8. CSD87381P Functional Block Diagram



2.3.3 TPS22920

The TPS22920 is a small, space-saving load switch with controlled turn on to reduce inrush current. The device contains a N-channel MOSFET that can operate over an input voltage range of 0.75 V to 3.6 V and switch currents up to 4 A. An integrated charge pump biases the NMOS switch in order to achieve a minimum switch ON resistance. The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals. The TPS22920 has a 1250-Ω on-chip resistor for quick output discharge when the switch is turned off which insures that the output is not left floating. The TPS22920 has an internally controlled rise time in order to reduce inrush current. The TPS22920 is available in an ultra-small, space-saving 8-pin CSP package.

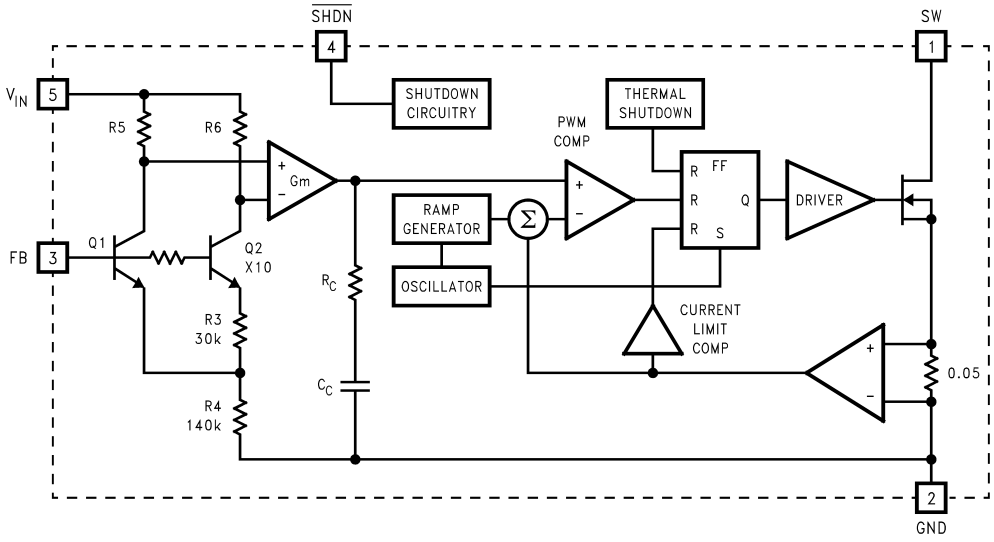
Figure 9. TPS22920 Functional Block Diagram



2.3.4 LMR64010

The LMR64010 switching regulator is a current-mode boost converter operating at a fixed frequency of 1.6 MHz. The use of SOT-23 package, made possible by the minimal power loss of the internal 1A switch, and use of small inductors and capacitors result in the industry's highest power density. The LMR64010 has a logic-level shutdown pin that can be used to reduce quiescent current and extend battery life. Protection is provided through cycle-by-cycle current limiting and thermal shutdown. Internal compensation simplifies design and reduces component count.

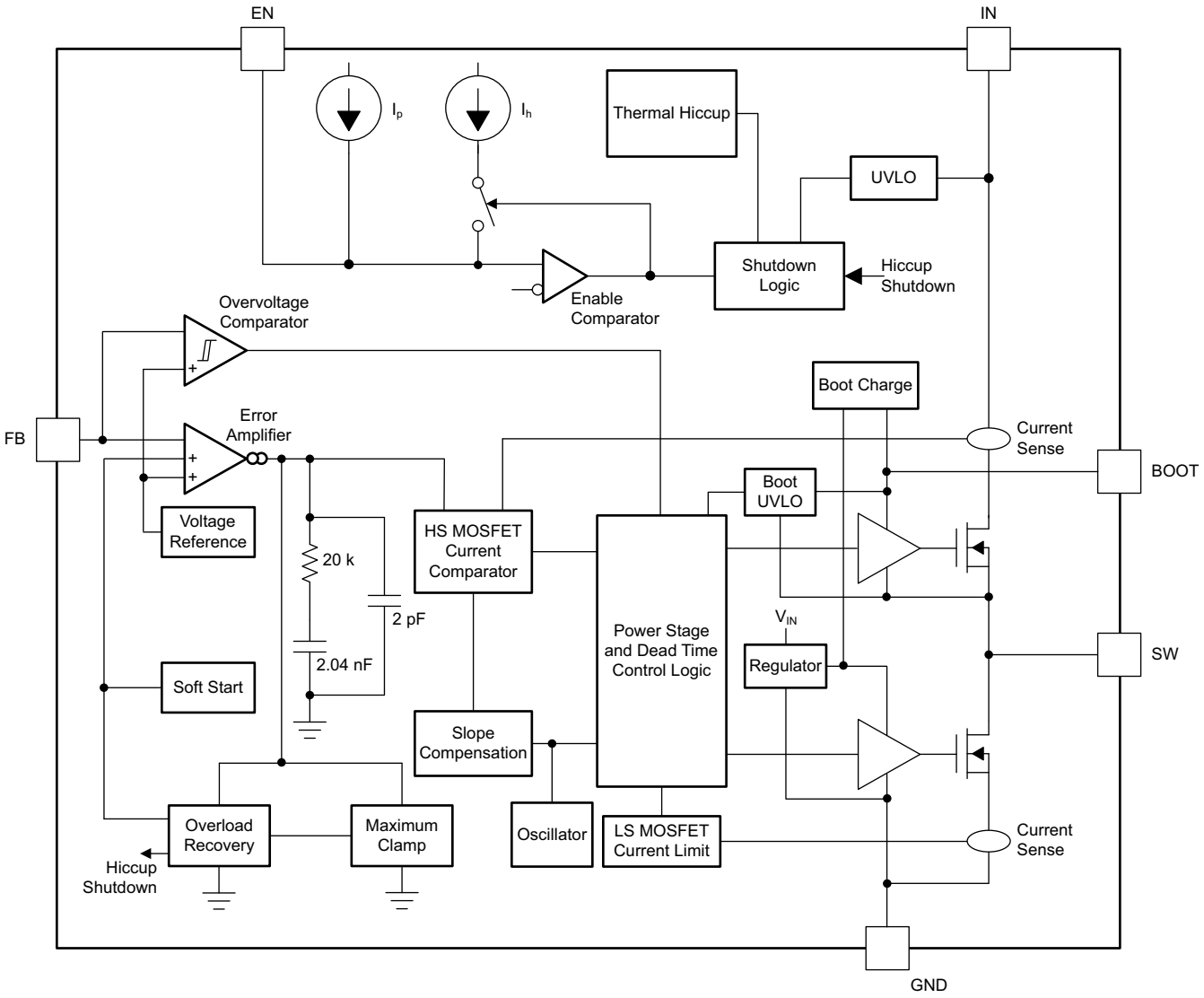
Figure 10. LMR64010 Functional Block Diagram



2.3.5 TPS54308

The TPS54308 is a 4.5-V to 28-V input voltage range, 3-A synchronous buck converter. The device includes two integrated switching FETs, internal loop compensation and 5-ms internal soft start to reduce component count. By integrating the MOSFETs and employing the SOT23 package, the TPS54308 achieves the high power density and offers a small footprint on the PCB. The TPS54308 operates in force continuous conduction mode (FCCM) during light load conditions, the switching frequency is maintained at an almost constant level over entire load range. Cycle-by-cycle current limit in both high-side MOSFET protects the converter in an overload condition and is enhanced by a low-side MOSFET freewheeling current limit which prevents current runaway. Hiccup mode protection is triggered if the over-current condition has persisted for longer than the present time.

Figure 11. TPS54308 Functional Block Diagram

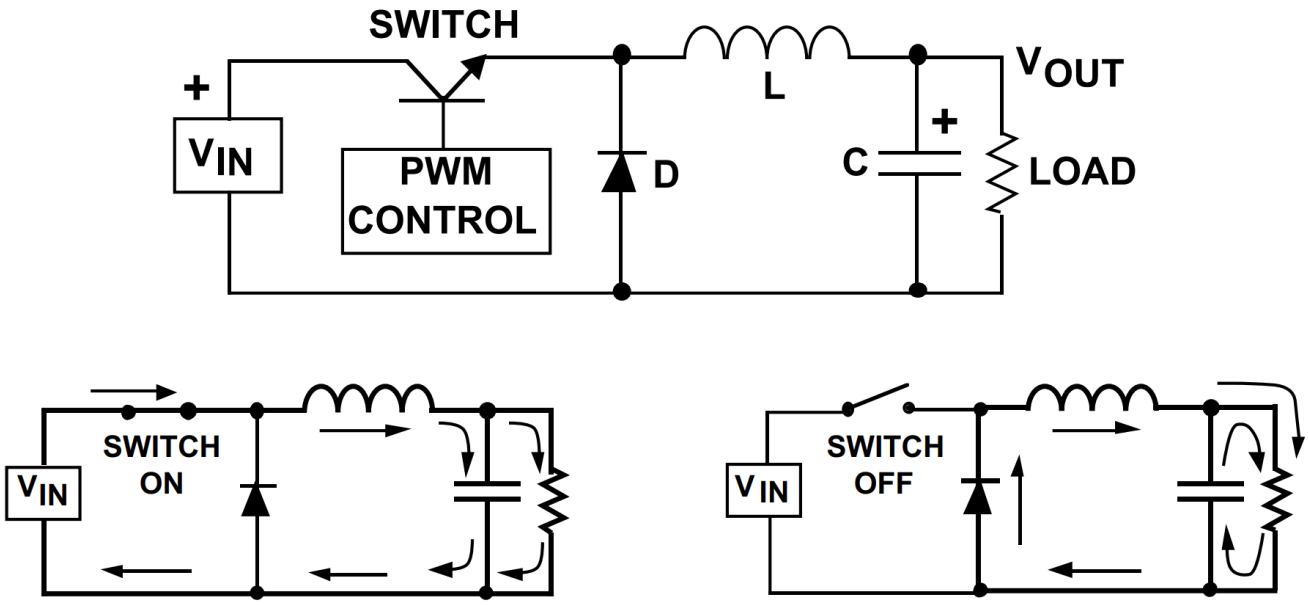


2.4 System Design Theory

PMICs allow for control of multiple power regulators with all sequencing and voltage level control built into one IC. The four types of regulators used in this PMIC are BUCK converters, BUCK controllers, LDOs and load switches. LDOs and load switches are very simple designs which do not require much explanation. Load switches use a FET to act as a switch connecting the input supply to the output while LDOs use a FET to dissipate power, adjusting the FET input voltage based to mantain a constant output.

The buck converter/controller uses a pair of FETs to switch the input voltage to an inductor between Vin and ground. In a BUCK controller the FETs are external to the IC, allowing for higher currents and better heat dissipation, while in a BUCK converter they are internal, allowing for smaller solution size. When the high side FET turns on, the input voltage is connected to the inductor, and when the low side FET turns on, the inductor is connected to ground. The difference between the input and output voltages is then forced across the inductor, causing current through the inductor to increase. During the ON time (high side FET on), the inductor current flows into both the load and the output capacitor, which charges the output capacitor. During the OFF time (low side FET on), the input voltage applied to the inductor is connected to ground. However, because the current in an inductor can not change instantly, the current through the inductor will slowly decrease. During this time, the output capacitor discharges into the load, maintaining a consistent load current. The total load current during the OFF time is the sum of the inductor and capacitor current. Figure 13 demonstrates how a BUCK converter/controller functions. In this figure the low side FET is replaced with a diode, which can also be used to ground the inductor input during the OFF time.

Figure 12. BUCK Basic Function



3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

The list below shows all of the hardware needed in order to power up the design and communicate with the PMIC. The power supply must be able to supply a minimum of 5 V and must be able to supply a current of at least 1 A. When loading the design a power supply capable of 10 A is recommended.

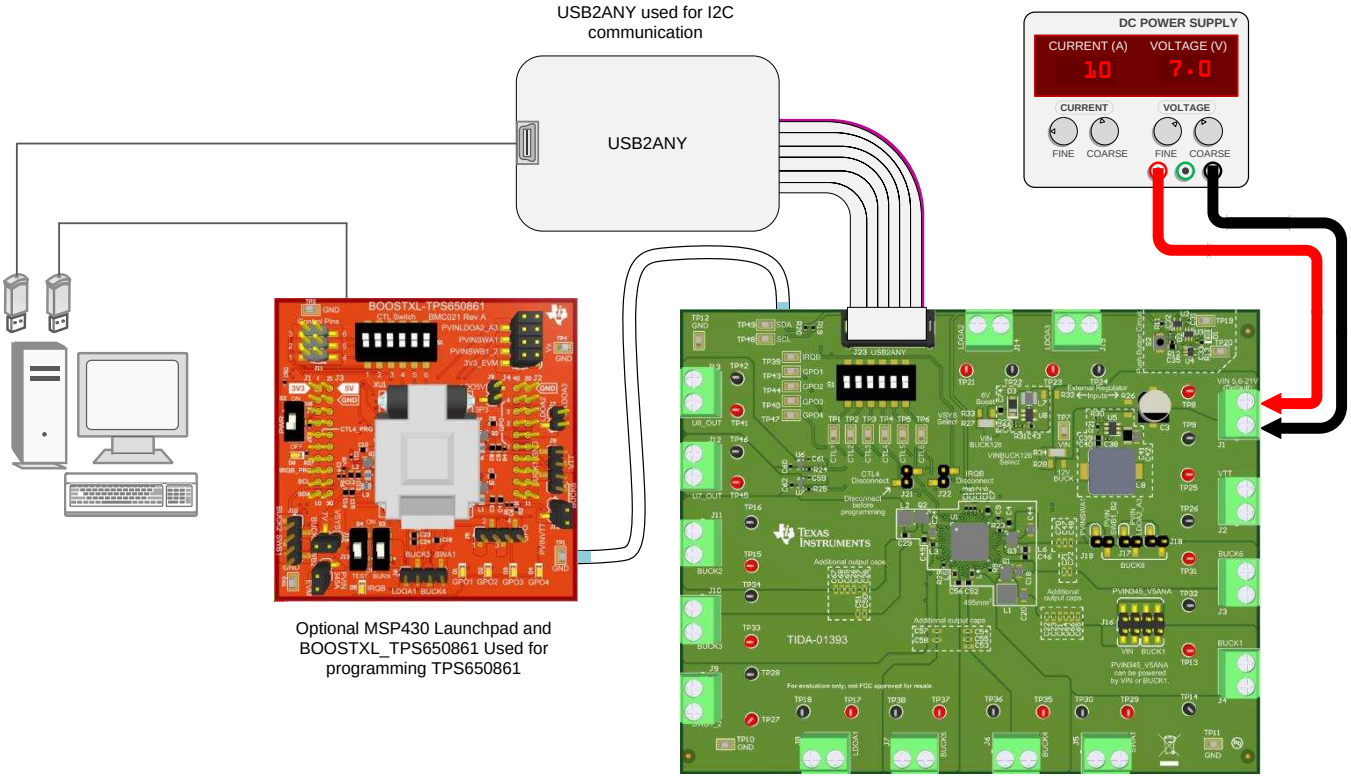
- PC with a USB port
- USB2ANY Interface Adaptor
- Power supply

The list below shows some of the optional hardware that is only needed if attempting to replace the TPS6508641 with the user-programmable TPS65086100.

- BOOSTXL-TPS650861 Programming BoosterPack
- MSP430F5529 USB LaunchPad Evaluation Kit

Figure 13 shows how to set up the hardware for this design.

Figure 13. Hardware Setup



3.1.2 Software

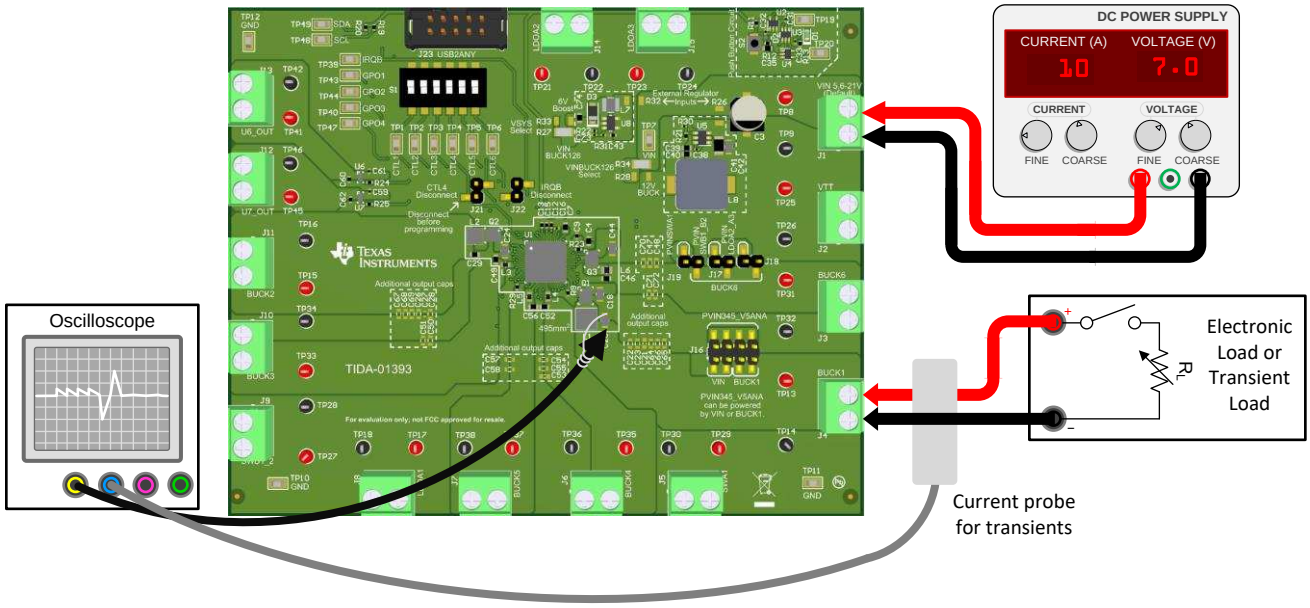
The IPG-UI GUI is supplied to provide a simple way to communicate to the device via I^2C communication. The GUI can be downloaded from http://www.ti.com/tool/IPG-UI. If the TPS65086100 is going to be used in the design, then an additional device file and script file will be required in order to program the device. The additional needed files can be downloaded here. In order to use the BOOSTXL-TPS650861 programming BoosterPack a firmware update is required on the MSP430F5529 LaunchPad. The latest MSP430F5529 LaunchPad USB2ANY firmware (USB2ANY_2.7.0.0_LP.txt) can be downloaded here, and the firmware update tool (MSP430_USB_Firmware_Upgrade_Example-1.3.1.1-Setup.exe) can be downloaded from here.

3.2 Testing and Results

3.2.1 Test Setup

Figure 14 shows how the board is set up for these test measurements. For ripple and transient measurements the output is measured across the output capacitor using a co-ax cable soldered to the pads. BUCKs 4 and 5 are excluded from most tests as the BUCK design is identical to BUCK3.

Figure 14. Board Test Setup



3.2.2 Test Results

3.2.2.1 Voltage Ripple

Voltage ripple measurements are taken at no load and 1 A loads to show the difference in ripple between pulse frequency modulation (PFM) mode at low loads and pulse width modulation (PWM) mode at higher loads. All measurements are taken at the default outputs for the TPS6508641 with a 12 V input.

Figure 15. BUCK1 Voltage Ripple- 1 A Load

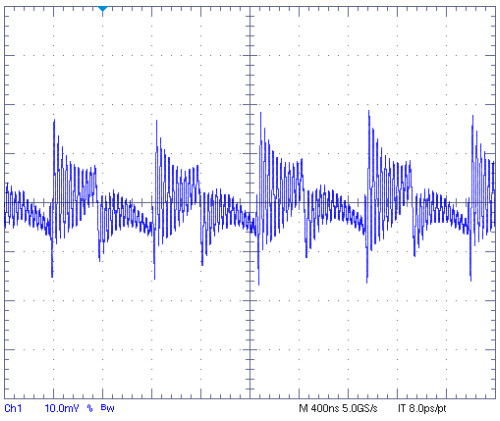


Figure 16. BUCK2 Voltage Ripple- 1 A Load

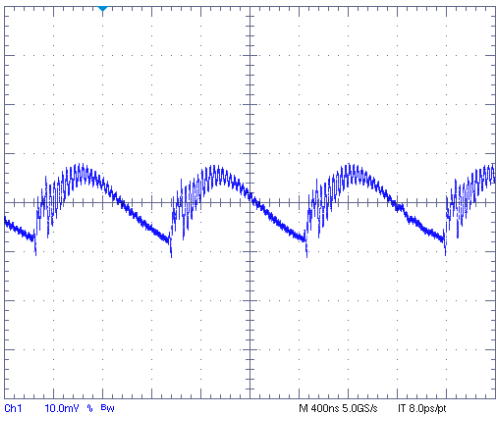


Figure 17. BUCK3 Voltage Ripple- 1 A Load

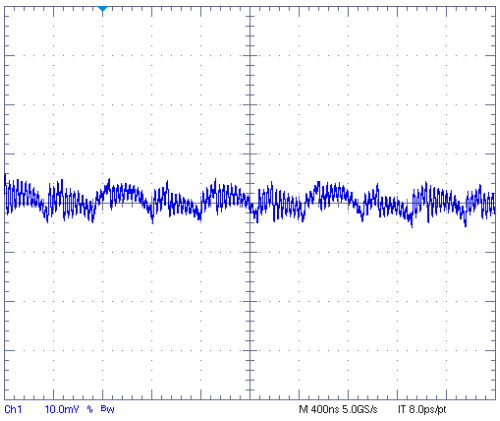


Figure 18. BUCK6 Voltage Ripple- 1 A Load

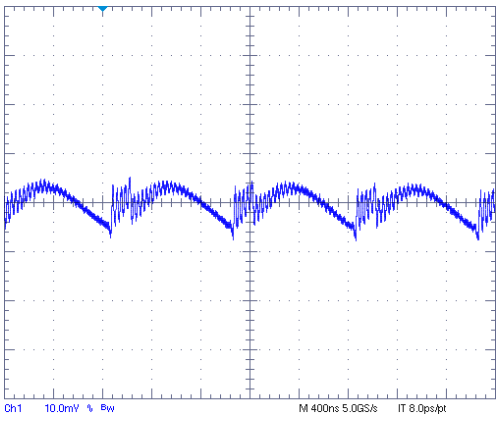


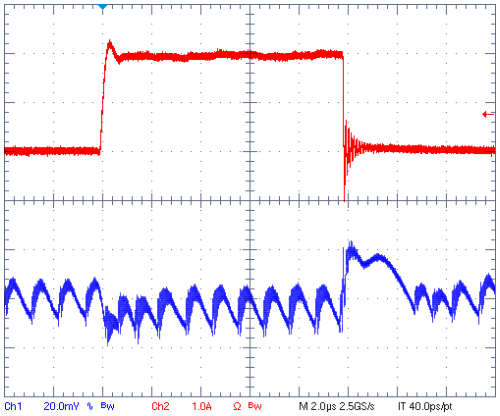
Table 5. Summary of Ripple Test Results

Regulator	Input Voltage	Output Voltage	Load	Inductance	Capacitance	Ripple
BUCK1	12 V	5 V	1 A	2.2 µH (PN: 74438356022)	22 µF (PN: GRM21BR61E226ME44L) + 2 x 47 µF (PN: GRM21BR61A476ME15L)	35.5 mV
BUCK2	12 V	0.85 V	1 A	470 nH (PN: 744383360047)	22 µF (PN: GRM187R61A226ME15D) + 2 x 47 µF (PN: GRM21BR61A476ME15L)	19.1 mV
BUCK3	12 V	1.2 V	1 A	470 nH (PN: 74479262147)	22 µF (PN: GRM187R61A226ME15D)	8.58 mV
BUCK6	12 V	1.8 V	1 A	1 µH (PN: 74479275210)	22 µF (PN: GRM187R61A226ME15D) + 2 x 47 µF (PN: GRM21BR61A476ME15L)	12.9 mV

3.2.2.2 Transients

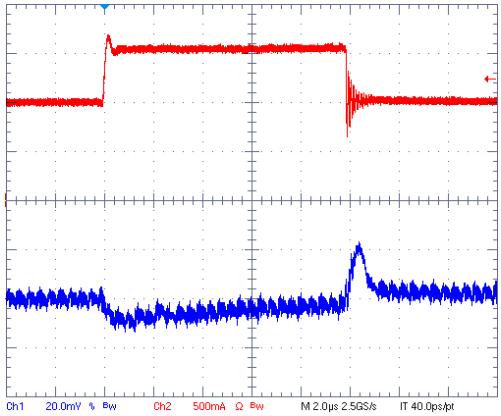
Transients are done at load steps that would be expected based on the power map shown in Figure 5 for the ZU3EG MPSoC. Some of the ZU3EG power rails are not expected to have large transients or are not sensitive power rails, so the TPS6508641 regulators that would map to those power rails are not included in the transient tests. These power rails include LDOA2 (VCC_PSPLL), LDOA3 (VCCO_HP), BUCK4 (VCC_3V3), BUCK1 (VCC_5V0), and BUCK5 (VCC_1V2). All transients are with a rise time of about 10 A/µs.

Figure 19. BUCK2 Transient 1 A to 3 A



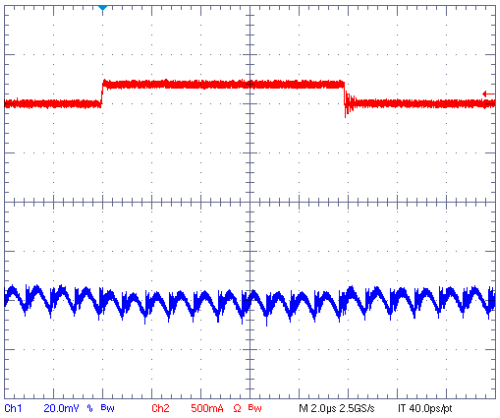
Transient that would be expected on BUCK2 if it were powering the VCC_PSINTLP rail on the ZU3EG.

Figure 20. BUCK3 Transient 1 A to 1.5 A



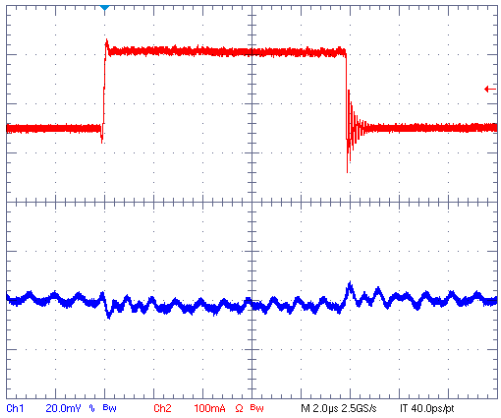
Transient that would be expected on BUCK3 if it were powering the VCCO_PSDDR rail on the ZU3EG.

Figure 21. BUCK6 Transient 1 A to 1.2 A



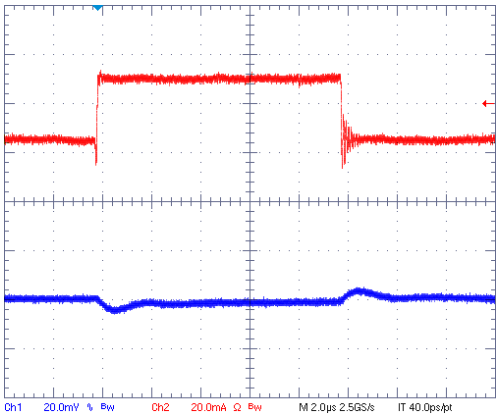
Transient that would be expected on BUCK6 if it were powering the VCCAUX rail on the ZU3EG.

Figure 22. VTT_LDO Transient 150 mA to 300 mA



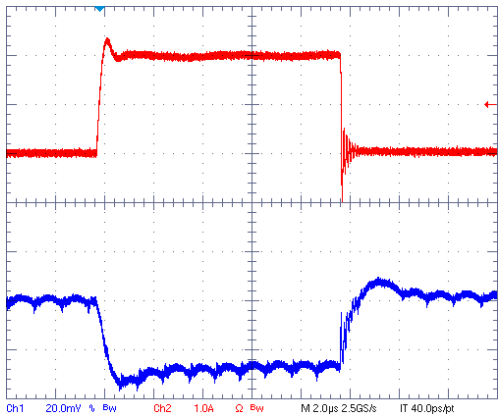
Transient that would be expected on VTT_LDO if it were powering the MGTRAVCC rail on the ZU3EG.

Figure 23. LDOA1 Transient 25 mA to 50 mA



Transient that would be expected on LDOA1 if it were powering the MGTRAVTT rail on the ZU3EG.

Figure 24. External Load Switch (TPS22920) Transient 1 A to 3 A



Transient that would be expected on the external TPS22920 load switch (U6) if it were powering the VCC_PSINTFP rail on the ZU3EG.

Table 6. Summary of Transient Test Results

Regulator	Step Size	Inductance	Capacitance	Overshoot	Undershoot
BUCK2	1 A to 3 A	470 nH (PN: 744383360047)	22 µF (PN: GRM187R61A226ME15D) + 2 x 47 µF (PN: GRM21BR61A476ME15L)	24.6 mV	-20 mV
BUCK3	1 A to 1.5 A	470 nH (PN: 74479262147)	22 µF (PN: GRM187R61A226ME15D)	20.6 mV	-14.4 mV
BUCK6	1 A to 1.2 A	1 µH (PN: 74479275210)	22 µF (PN: GRM187R61A226ME15D) + 2 x 47 µF (PN: GRM21BR61A476ME15L)	6.2 mV	-9.6 mV
VTT_LDO	150 mA to 300 mA	-	4.7 µF (PN: C1005X5R0J475M050BC)	8.2 mV	-9.6 mV
LDOA1	25 mA to 50 mA	-	4.7 µF (PN: C1005X5R0J475M050BC)	6.7 mV	-8 mV
External Load Switch	1 A to 3 A	-	22 µF (PN: GRM188R61A226ME15D)	22.5 mV	-40 mV

3.2.2.3 *Efficiency*

Efficiency measurements are taken on a system level, meaning system voltage, push button circuitry, external load switches, and pre-regulators are all included in the efficiency measurements. Regulators that aren't being tested are disabled for these measurements.

Figure 25. BUCK1 Efficiency

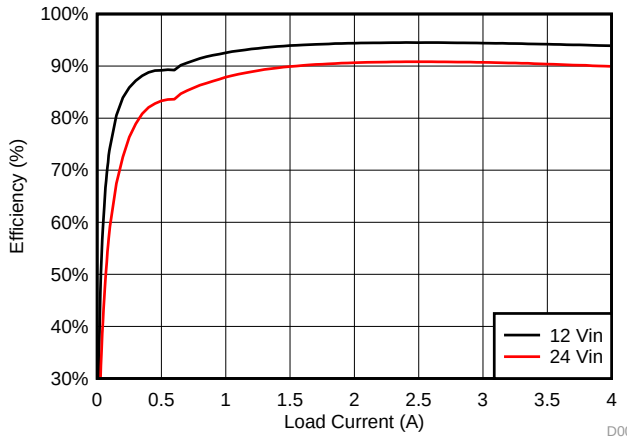


Figure 26. BUCK2 Efficiency

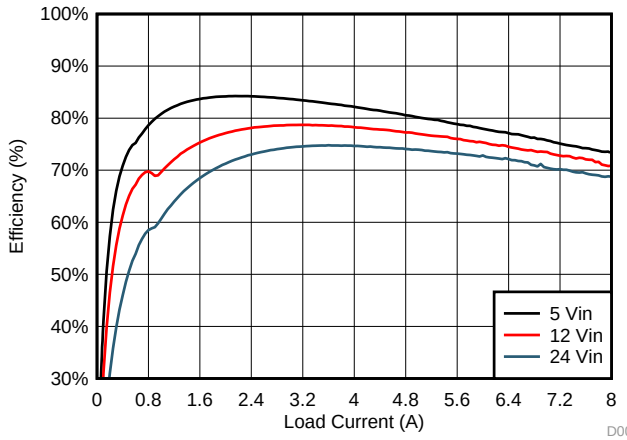


Figure 27. BUCK3 Efficiency

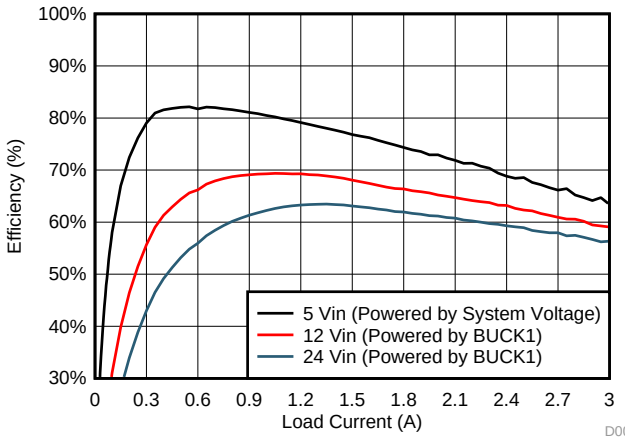
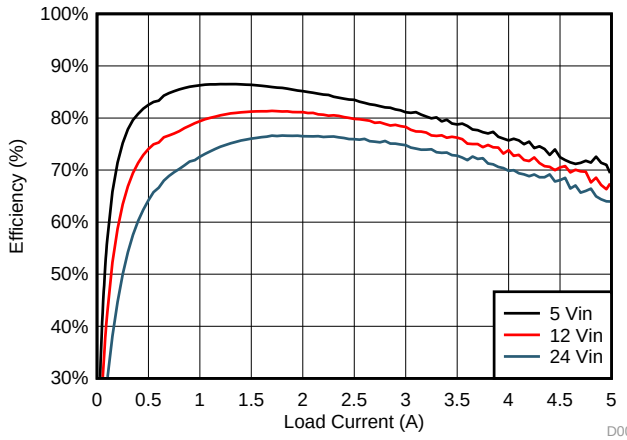


Figure 28. BUCK6 Efficiency



3.2.2.4 Sequencing and Control

The tests in this section show the functionality of the PMIC sequencing and some of the other external components.

Figure 29 shows how a short key press will set the CTL1 pin high, enabling the PMIC. Figure 30 shows how a long key press will set the CTL1 pin low, disabling the PMIC.

Figure 29. Push-Button Enable

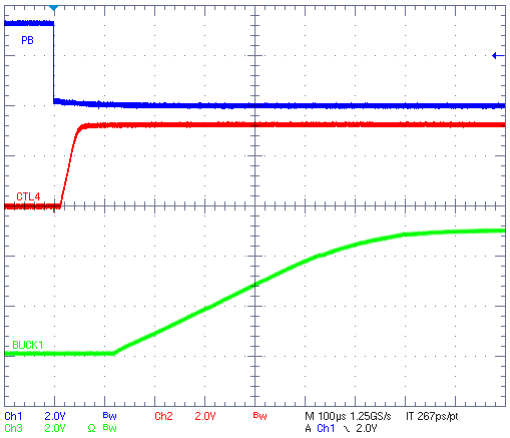


Figure 30. Push-Button Disable

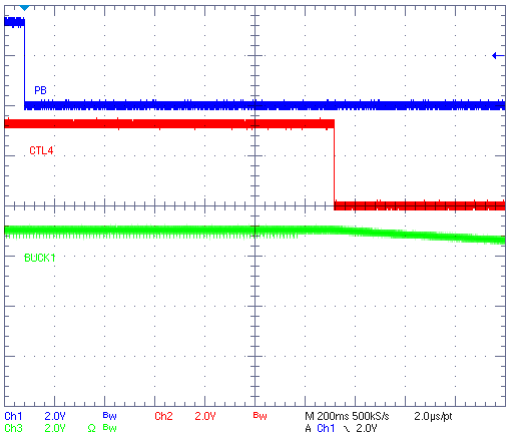


Figure 31 shows how one of the external load switches can be enabled using a GPO output.

Figure 31. External Load Switch Functionality

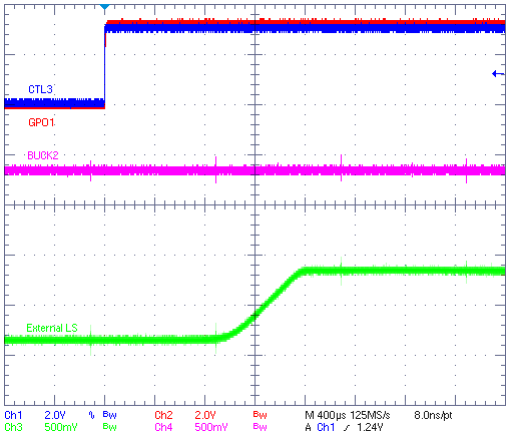
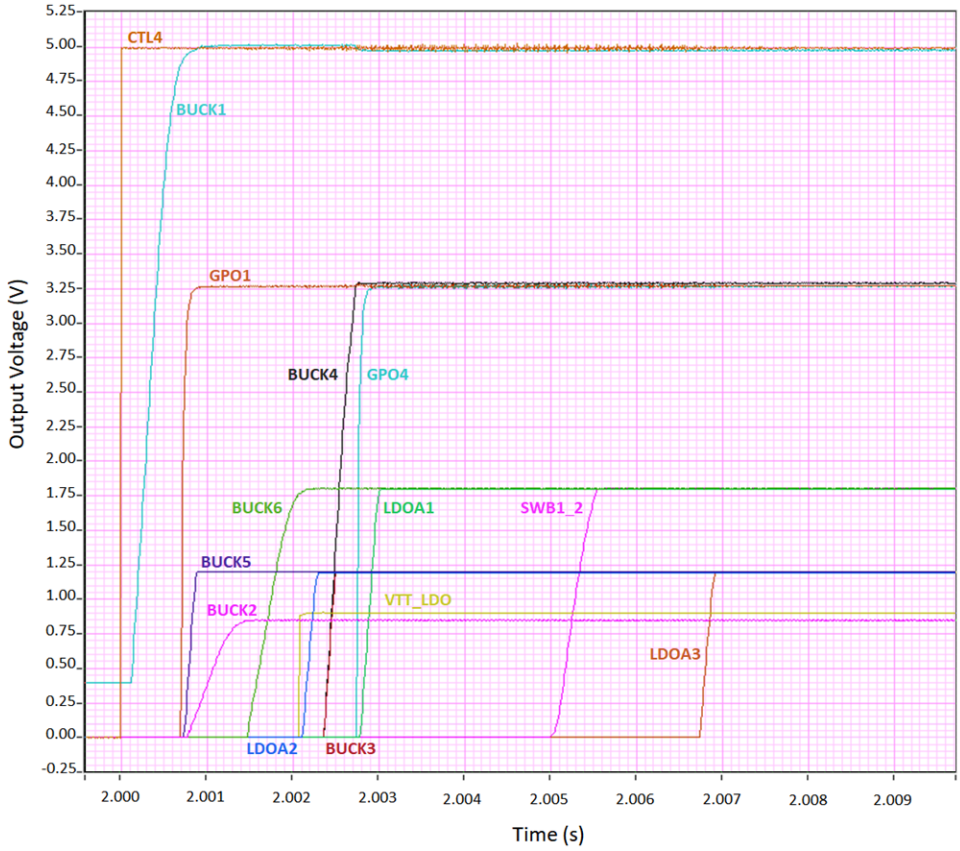


Figure 32 demonstrates the sequencing capabilities of the PMIC.

Figure 32. PMIC Sequencing



4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01393.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01393.

4.3 PCB Layout Recommendations

The layout guidelines in each device's data sheet should be used as a starting point for placement of critical components for each device.

This reference design is a 6 layer PCB with 1-oz. copper thickness and a total thickness of 62 mils. The top (first) and bottom (sixth) layers are used for component placement and for routing signals and power. The second and fifth layers are solid copper GND planes, with only a handful of traces when needed. The innermost layers (third and fourth) are reserved for routing low-speed digital signals and low-current power traces, such as the LDOs.

When doing layout for BUCK converters it is important to make sure the input capacitors are located close to the input pins, and have a strong connection to ground. The same is true for PMIC system power and to a lesser extend the LDO inputs. It is also very important that BUCK converters have output capacitors with a strong connection to ground, and that the switch nodes of the BUCK regulators have short wide traces. It is also important for the TPS65086x device to have a short, strong connection from the VREF capacitor to the AGND pin, and that the AGND pin only connects to the ground plane through a single via. The AGND pin should not connect directly to the power pad of the PMIC.

For more help on PCB layout please refer to the TPS65086x Schematic and Layout Checklist in the TPS65086 technical documents

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01393.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-01393.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01393.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01393.

5 Software Files

To download the software files, see the design files at TIDA-01393.

6 Related Documentation

1. Texas Instruments, *TPS65086x Evaluation Module User's Guide*
2. Texas Instruments, *BOOSTXL-TPS650861 EVM User's Guide*
3. Texas Instruments, *Push-Button Circuit app note*
4. Texas Instruments, *TPS22920EVM-002 User's Guide*
5. Texas Instruments, *AN-2183 LMR62014/LMR64010 Demo Board*
6. Texas Instruments, *TPS54308EVM-876 3-A Regulator Evaluation Module*

7. Xilinx, *AES-ULTRA96-G*

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2019) to A Revision	Page
• Changed ZUS9DR to ZU21DR because the design does not include the additional RF rails	1
• Added note explaining additional power requirements for RFSoCs	9

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