Descriptive Set Theory and Circuit Complexity

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December 15, 2025

Abstract

We discuss the deep connections between countable circuits and Borel/analytic sets, which inspired the original proofs that PARITY $\notin$ AC^0 and that the AC^0 hierarchy does not collapse. We prove the correspondence between countable circuits and Borel/analytic sets, describe the history of early AC^0 lower bounds and their relation to the Borel hierarchy theorem, and outline other potential ways in which descriptive set theory could be used to give new results about finite circuits. Our main technical results are new circuit-based proofs of the Borel hierarchy theorem and a Ramsey-theoretic result about Borel functions.

Contents

1   Introduction

We examine a beautiful connection between circuit complexity and descriptive set theory. First explored in the early 1980s, this connection links countable deterministic and nondeterministic circuits with Borel and analytic sets, respectively. The link has inspired new proofs of results from descriptive set theory, as well as new theorems about finite circuits.

I am deeply grateful for my mentor, Professor Anton Bernshteyn, who worked with me on this project. He introduced me to descriptive set theory and its connection to circuit complexity, suggested theorems and problems I should look into, and helped me refine my ideas and proofs. His insights and support were invaluable, and this project could not have happened without him.

1.1   Outline

In Section 2, we provide a brief overview of our definitions and notation.

We then describe the key link between descriptive set theory and circuit complexity in Section 3. We prove the equivalence of Borel sets with countable deterministic circuits, and demonstrate the equivalence of analytic sets with countable nondeterministic circuits, and then illustrate how results from descriptive set theory can be translated into the language of circuits.

We then examine the Borel hierarchy theorem in Section 4, which has played a formative role in early circuit complexity. We describe the origins of AC^0 lower bounds in this section, as well as the process of converting results from descriptive set theory to results about finite circuits. The remainder of this section contains our circuit-based proof of the Borel hierarchy theorem. In Section 5, we explore some elegant consequences of the machinery used in the proof.

Finally, we outline our future directions in Section 6. We discuss the Galvin-Prikry theorem, a Ramsey-theoretic result about Borel functions, in Section 6.1. We examine the Lusin separation theorem, as well as the dramatic consequences it would have if adapted to the finite case, in Section 6.2.

1.2   Summary of results

The technical highlight of this report is a new combinatorial proof of the Borel hierarchy theorem in Section 4.3. Michael Sipser provided a combinatorial proof for the finite case in [6], but we prove the claim for the full transfinite hierarchy.

To prove the theorem, we develop a restriction lemma which also gives us a useful Ramsey-like result about countable circuits in Section 5. This result also follows from the Galvin-Prikry theorem, but our we provide the first purely combinatorial proof.

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2 Basic notions

The reader is assumed to have some familiarity with descriptive set theory and circuit complexity. The following definitions are intended to clarify our conventions.

2.1 Borel and analytic sets

We consider the binary alphabet $\Sigma = \{0,1\}$ and *Cantor space* Σ^ω, equipped with the topology generated by basic open sets of the form $x\Sigma^\omega$ for $x \in \Sigma^*$.

Definition 2.1. We call a set $S \subseteq \Sigma^\omega$ a $\boldsymbol{\Sigma}_1$-set (resp. $\boldsymbol{\Pi}_1$) if it is open (resp. closed). A set is $\boldsymbol{\Sigma}_k$ (resp. $\boldsymbol{\Pi}_k$) if it is a countable union (resp. intersection) of sets $S_1, S_2, \ldots$, each of which are in $\boldsymbol{\Pi}_j$ (resp. $\boldsymbol{\Sigma}_j$) for some $j < k$.

Definition 2.2. A set $S \subseteq \Sigma^\omega$ is *Borel* if it is $\boldsymbol{\Sigma}_\alpha$ for some $\alpha < \omega_1$. The *rank* of a Borel set B is the smallest α such that $B \in \boldsymbol{\Sigma}_\alpha \cup \boldsymbol{\Pi}_\alpha$.

Definition 2.3. A set $S \subseteq \Sigma^\omega$ is *analytic* if it is the projection of a Borel set $B \subseteq \Sigma^\omega \times \Sigma^\omega$ equipped with the product topology (i.e. we can write

$$\{x \in \Sigma^\omega : (x,y) \in B \text{ for some } y \in \Sigma^\omega\}).$$

2.2 Deterministic circuits

We consider countable and well-founded circuits C with $\wedge$- and $\vee$-gates over the literals $x_1 \overline{x}_1, x_2, \overline{x}_2, \ldots$, which compute functions $f_C \colon \Sigma^\omega \to \{0,1\}$ and sets $f_C^{-1}(\{1\})$.

Definition 2.4. We call a circuit $\boldsymbol{\Sigma}_0$ or $\boldsymbol{\Pi}_0$ if it is finite. A $\boldsymbol{\Sigma}_k$-circuit (resp. $\boldsymbol{\Pi}_k$-circuit) is a $\vee$-gate (resp. $\wedge$-gate) with countably many children $C_1, C_2, \ldots$, each of which are $\boldsymbol{\Pi}_j$-circuits (resp. $\boldsymbol{\Sigma}_j$-circuits) for some $j < k$.

Definition 2.5. The *rank* of a circuit C is the smallest α such that C is a $\boldsymbol{\Sigma}_\alpha$- or $\boldsymbol{\Pi}_\alpha$-circuit.

The rank of any countable and well-founded circuit is the supremum of countably many countable ordinals and is therefore less than ω_1. We also see that the rank of a circuit is either equal to its depth d or to $d+1$.

2.3 Nondeterministic circuits

A nondeterministic circuit C over the deterministic literals $x_1 \overline{x}_1, x_2, \overline{x}_2, \ldots$ and nondeterministic literals $y_1 \overline{y}_1, y_2, \overline{y}_2, \ldots$ computes the function

$$f_C(x) = \begin{cases} 1 & \text{if } C(x,y) = 1 \text{ for some } y \in \Sigma^\omega \\ 0 & \text{otherwise} \end{cases}$$

and set $f_C^{-1}(\{1\})$. We define rank and the classes of $\mathbf{\Sigma}_k$-circuits and $\mathbf{\Pi}_k$-circuits analogously to the deterministic case.

3 Equivalence of circuits and Borel/analytic sets

Our similar choice of notation between Borel sets and deterministic circuits is no coincidence. These objects correspond precisely, and we observe a similar connection between analytic sets and nondeterministic circuits. These correspondences, which we prove in this section, allow us to translate results from one field to the other. In this section, all circuits are well-founded and countable.

3.1 Borel sets and deterministic circuits

Theorem 3.1. *For $k \geq 1$, a set $S \subseteq \Sigma^\omega$ is $\mathbf{\Sigma}_k$ (resp. $\mathbf{\Pi}_k$) if and only if it can be computed by a deterministic $\mathbf{\Sigma}_k$ (resp. $\mathbf{\Pi}_k$)-circuit.*

Proof. We will prove the claim for $\mathbf{\Sigma}_1$, since the $\mathbf{\Pi}_1$ case is dual and the inductive step is immediate.

If $S \in \mathbf{\Sigma}_0$, then S can be written as a countable union of basic open sets $x\Sigma^\omega$ by the separability of Σ^ω. Each of these basic open sets can be computed by a finite $\mathbf{\Pi}_0$-circuit, and taking an $\vee$-gate with each of these circuits as children gives us our desired $\mathbf{\Sigma}_1$-circuit.

Conversely, every set computed by $\mathbf{\Pi}_0$-circuit is either $\emptyset$ or of the form

$$\Sigma^{i_i} x_i \Sigma^{i_2} x_2 \cdots \Sigma^{i_n} x_n \Sigma^\omega$$

for some $n \geq 0$ and $i_1, \ldots, i_n \geq 0$. Such sets can be written as the union of the basic open sets

$$w_1 x_i w_2 x_2 \cdots w_n x_n \Sigma^\omega$$

for $w_1 \in \Sigma^{i_1}, w_2 \in \Sigma^{i_2}, \ldots$ and are therefore open. Thus any set computed by a $\mathbf{\Sigma}_1$-circuit is open as a union of open sets. $\square$

The above proof explains why we consider the rank of a circuit instead of just its depth: to ensure that $\mathbf{\Sigma}_1$-circuits can compute open sets.

Corollary 3.2. *A subset of Σ^ω is Borel if and only if it is definable by a countable deterministic circuit.*

Because any two uncountable Polish spaces are Borel isomorphic ([5]), this result also applies to $\mathbb{R}$. In other words, we can fix some Borel isomorphism $\varphi \colon \mathbb{R} \to \Sigma^\omega$, and we then

have that a subset S of $\mathbb{R}$ is Borel if and only if some deterministic circuit computes $\varphi(S)$.

We can characterize Borel subsets of $\mathbb{R}$ more explicitly with binary representations. If we exclude binary representations which are eventually all ones, then the binary representation map is a Borel isomorphism from $[0, 1)$ to a Borel subset of 2^ω. This means that a subset of $[0, 1)$ is Borel if and only if its image under this map can be computed by a deterministic circuit.

3.2 Analytic sets and nondeterministic circuits

Theorem 3.3. *Analytic subsets of Σ^ω are precisely those which can be defined by countable nondeterministic circuits.*

Proof. A similar argument as the one in the previous proof tells us that a circuit over $\Sigma^\omega \times \Sigma^\omega$ is $\mathbf{\Sigma}_1$ if and only if the set it computes is open in the product topology on $\Sigma^\omega \times \Sigma^\omega$. This means that a set $B \subseteq \Sigma^\omega \times \Sigma^\omega$ is Borel if and only if it can be computed by a countable deterministic circuit over $\Sigma^\omega \times \Sigma^\omega$. The claim follows.

$\square$

3.3 Translating a theorem about G_δ sets

There are many ways one can take advantage of this connection. The fields of descriptive set theory and circuit complexity are quite different. Proofs in the former field are often topological in nature, while proofs in the latter field are often combinatorial. It is often instructive to translate a theorem from one field to the other and then try to find an alternative proof of the theorem that doesn't rely on the machinery of its "native" subject. The following result, for example, is typically proven with a topological argument ([5]). However, by translating it to the realm of circuits, we can provide an elegant combinatorial proof:

Theorem 3.4. *A set $S \subseteq \Sigma^\omega$ is analytic if and only if it is the projection of a G_δ (i.e. $\mathbf{\Pi}_2$) subset of $\Sigma^\omega \times \Sigma^\omega$.*

Proof. It suffices to show that every nondeterministic circuit C can be simulated by a depth-2 nondeterministic circuit whose root note is an $\wedge$-gate. To this end, we let $G_1, G_2, \ldots$ denote the gates of C, with G_1 being the root. We define a new circuit C' over the deterministic variables $x_1, x_2, \ldots$ and nondeterministic variables $y_1, z_1, y_2, z_2, \ldots$, where the y_i's correspond to the nondeterministic inputs of C and each z_i corresponds to G_i. The goal of the z_i's is to nondeterministically guess the value of the gates in C. To this end, we do the following for each $i = 1, 2, \ldots$:

- If G_i is an $\vee$-gate with inputs $c_1, c_2, \cdots \in \{x_1, \overline{x}_1, \ldots, y_1, \overline{y}_1, \ldots, G_1, G_2, \ldots\}$, create a depth-1 circuit $\neg z_i \vee c_1 \vee c_2 \vee \ldots$, where any inputs G_j are replaced by z_j.

- If G_i is an $\wedge$-gate with inputs $c_1, c_2, \ldots$, create countably many depth-1 circuits $\neg z_i \vee c_1, \neg z_i \vee c_2, \ldots$, where any inputs G_j are replaced by z_j.

If we create an $\wedge$-gate and connect it to z_1 and each of these depth-1 circuits created above, we obtain a depth-2 nondeterministic circuit which is equivalent to C.

$\square$

Often, finite circuit complexity stands to benefit from this connection. Descriptive set theory is the older of the two fields, with many established results and techniques. This all carries over into the realm of countable circuits, and once we find a combinatorial proof for a fact about these circuits, it is often possible to adapt the argument to the finite case. We will see such an example in the next section.

4   The Borel hierarchy theorem

The Borel hierarchy theorem is a classical result from descriptive set theory, which claims the following:

Theorem 4.1 (Borel hierarchy)**.** *We have for every $0 \leq \alpha < \beta < \omega_1$ that $\mathbf{\Sigma}_\alpha \subsetneq \mathbf{\Sigma}_\beta$.*

In other words, the result is that the Borel hierarchy does not collapse. The standard proof of this fact is based on showing that $\mathbf{\Sigma}_\alpha \subsetneq \mathbf{\Pi}_\alpha$ via universal sets and diagonalization, and such a proof is provided as Theorem 22.4 in [5]. Later in this section, we will provide a new, purely combinatorial proof of this fact.

This result ultimately led to the groundbreaking AC^0 depth hierarchy theorem, and we describe the history of this development below.

4.1   The origins of AC^0 lower bounds

Recall that AC^0_d is the set of problems which can be computed by depth-d polynomial-sized circuit families and $\mathsf{AC}^0 = \bigcup_{d=0}^{\infty} \mathsf{AC}^0_d$.

In 1981, Merrick Furst, James Saxe, and Michael Sipser found the first super-polynomial lower bound on constant depth circuits computing an explicit function when they showed in [2] that PARITY $\notin \mathsf{AC}^0$. Even as early as in this paper, they describe connections to descriptive set theory, referencing a proof that there is no countable deterministic circuit computing an infinite parity function (a function whose output flips if any one input bit is flipped). The authors use the measurability of Borel sets to show this, and we will provide two alternative proofs later. They also describe an analogy between polynomial growth and countable sets: Loosely speaking, the power set operation is "forbidden" in both settings as it takes us to exponential growth in the former setting and uncountable sets in the letter. Most other operations, on the other hand, are "allowed" in both settings.

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In 1983, Sipser established the full AC^0 hierarchy in [6] by proving that $\mathsf{AC}_d^0 \subsetneq \mathsf{AC}_{d+1}^0$ for every $d \geq 0$. His proof used probabilistic restrictions, which were the tool of choice in early circuit lower bounds. This techniques were later improved by Håstad in [3], where he developed his famous switching lemma and used it to prove sharp bounds on the size of depth-d circuits computing PARITY. Probabilistic restrictions remain a common tool in circuit complexity, and many theorists are unaware of how Sipser actually came up with his proof technique.

4.2 From descriptive set theory to finite circuits

The Borel hierarchy theorem can also be interpreted as saying that depth-$\alpha+1$ deterministic countable circuits are more powerful than depth-α circuits, and this connection inspired Sipser's AC^0 depth hierarchy proof in the following manner:

1. Sipser first found a new combinatorial circuit-based proof of the Borel hierarchy theorem in the case where α is finite (i.e. for finite-depth countable circuits).

2. Then, Sipser used probabilistic restrictions to adapt this proof to polynomial-sized circuit families to obtain an analogous result for the AC^0 hierarchy.

Sipser outlines this process precisely in his paper.

This is perhaps the greatest success story of using analogies to descriptive set theory in order to derive results about polynomial-sized circuits. Even if probabilistic restrictions are the main ingredient in Sipser's proof, descriptive set theory was the primary inspiration. The Borel hierarchy theorem is just a single result in descriptive set theory which had a profound impact on circuit complexity. One naturally wonders whether other theorems have analogues for polynomial-sized circuits.

4.3 A combinatorial proof of the Borel hierarchy theorem

Sipser only proves the finite-depth case of the Borel hierarchy theorem, and it is a natural question whether the full result can be proven combinatorially. We now provide such a proof.

4.3.1 Setup and the restriction lemma

Definition 4.2. The *full alternating trees* of rank $\alpha < \omega_1$ are the circuits defined recursively as follows:

- The full rank-0 $\vee$-tree and $\wedge$-tree are both the identity circuit on a single bit.

- For any successor ordinal $\alpha + 1$, we define the full rank-$\alpha + 1$ $\vee$ (resp. $\wedge$)-tree to be an $\vee$-gate with countably many rank-α $\wedge$ (resp. $\vee$)-trees as children.

- If α is a limit ordinal, we define the full rank-α $\vee$ (resp. $\wedge$)-tree to be an $\vee$-gate with a full rank-β $\wedge$ (resp. $\vee$)-tree child for every $\beta < \alpha$ (note that there are countably many such β's).

We identify the set of (countably many) leaves of each full alternating $\vee$-tree with $x_1, x_2, \ldots$, and we let $f_\alpha \colon \mathcal{P}(\{x_1, x_2 \ldots \}) \to \{0, 1\}$ denote the function computed by each such tree.

Since each f_β is computed by a circuit in $\boldsymbol{\Sigma}_\beta$, it suffices to show that f_β cannot be computed by a circuit in $\boldsymbol{\Sigma}_\alpha$ when $\alpha < \beta$. We prove this using *restrictions,* functions $\rho : \omega \to \{0, 1, *\}$ which, for every circuit C on ω, induce a restricted circuit C^ρ whose inputs x_i are left untouched if $\rho(x_i) = *$ and replaced with $\rho(x_i)$ otherwise.

Definition 4.3. We call a circuit *forced* by ρ if it is equivalent to a constant 0- or 1-circuit. We call a circuit *suppressed* if its top gate is an $\vee$-gate and it is forced to 1 or if its top gate is an $\wedge$-gate and it is forced to 0. A forced circuit is *overriding* if it is not suppressed. We call a circuit *preserved* by ρ if it is equivalent to the identity circuit on a single literal.

We write "child of a circuit/tree" to refer to a child of the uppermost gate/root node of the circuit/tree. Notice that, in an alternating circuit, suppressed children do not affect the value of their parents and overriding children force their parents. Notice also that any depth-1 circuit can be suppressed by assigning a single literal, while it can only be made overriding if all of its literals are assigned. A circuit can be preserved by assigning one of its literals to $*$ and the rest to 0 or 1.

The following lemma is the heart of our argument:

Lemma 4.4 (The restriction lemma). *For any ordinal $\alpha < \omega_1$, countable disjoint collection of full rank-α alternating trees $(T_{ij})_{i,j \in \mathbb{N}}$, and at most countable collection of $\boldsymbol{\Sigma}_\alpha$- or $\boldsymbol{\Pi}_\alpha$-circuits $(C_i)_{i \in \mathbb{N}}$ defined on the leaves of these trees, there exists a restriction ρ such that each C_i^ρ is equivalent to a finite circuit, each T_{ij}^ρ is either suppressed or preserved, and infinitely many trees T_{ij}^ρ are preserved for each fixed j.*

We will prove the lemma by transfinite induction. The claim is immediate for $\alpha = 0$, so we just need to address the successor and limit cases. Before this though, let us see how the lemma implies the full theorem:

Proof of Theorem 4.1. Suppose $\alpha < \beta$. The full alternating $\vee$-tree of rank β contains a full alternating tree of rank $\alpha + 1$ as a subtree, and by applying a suitable restriction ρ and relabeling, we obtain a circuit equivalent to a full alternating tree of rank $\alpha + 1$. If we could compute f_β with a $\boldsymbol{\Sigma}_\alpha$-circuit, the restriction of this circuit would be a $\boldsymbol{\Sigma}_\alpha$-circuit computing the same function as this tree. The claim therefore reduces to proving that a full alternating tree of rank $\alpha + 1$ is not equivalent to any $\boldsymbol{\Sigma}_\alpha$-circuit.

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To this end, suppose for the sake of contradiction that C is a $\boldsymbol{\Sigma}_\alpha$-circuit computing the same function as a full alternating tree of rank $\alpha + 1$. We apply the restriction lemma to the rank-α children of the root node in this tree, labeled arbitrarily, and to the $\boldsymbol{\Sigma}_\alpha$-circuit C. Applying the restriction we obtain gives us a finite circuit C^ρ equivalent to a full $\vee$- or $\wedge$-tree of depth 1. This is exactly our desired contradiction.

$\square$

4.3.2 The successor case

We begin with the case where $\alpha = 1$, and the proof is very similar to Sipser's original argument.

Proof when $\alpha = 1$. In this case, we are given a disjoint collection $(T_{ij})_{i,j \in \mathbb{N}}$ of $\vee$- or $\wedge$-gates, each with countably many inputs, as well as $\boldsymbol{\Sigma}_1$- or $\boldsymbol{\Pi}_1$-circuits $(C_i)_{i \in \mathbb{N}}$ defined on these inputs. Our goal is to find a restriction ρ such that each T_{ij}^ρ is suppressed or preserved, infinitely many T_{ij}^ρ's are preserved for each fixed j, and each C_i^ρ is equivalent to a finite circuit.

The challenge of constructing ρ is that we need to assign infinitely many $*$'s in order to ensure that infinitely many T_{ij}^ρ's are preserved for each fixed j, but not in a manner that makes any C_i^ρ depends on infinitely many $*$'s. To address this difficulty, we define the *queue sequence* $(q_n)_{n \in \mathbb{N}} = (1, 1, 2, 1, 2, 3, 1, 2, 3, 4, \ldots)$ so that each $n \in \mathbb{N}$ appears infinitely many times in (q_n). We define ρ via a sequence of partial restrictions ρ_i such that each ρ_i assigns i $*$'s and the circuit C_i depends only on these $*$'s. Let the domain of ρ_0 be empty. Then do the following for $i = 1, 2, \ldots$:

1. Preserve some tree $T_{q_i j}$ by extending ρ_{i-1} (assigning one $*$).

2. For each of the 2^i possible settings of the bits x_i with $\rho_{i-1}(x_i) = *$ to 0 or 1, do the following:

   (a) If C_i is unforced under this assignment, it must have an unforced $\boldsymbol{\Sigma}_0/\boldsymbol{\Pi}_0$ child. Extend ρ_{i-1} to force this child to be overriding by assigning finitely many bits to 0 or 1.

   (b) For each T_{ij} containing a bit so assigned, extend ρ_{i-1} to assign all other bits of T_{ij} such that T_{ij} is suppressed.

After all of these steps, we see that each C_i depends only on the finitely many bits x_i such that $\rho_i(x_i) = *$ and is hence equivalent to a finite circuit. We also have that infinitely T_{ij}'s are preserved for each fixed j. By assigning all remaining literals so that every other T_{ij} is preserved, we get our desired restriction ρ.

$\square$

The proof of the successor case is now immediate:

Proof of the successor case. Let $(T_{ij})_{i,j\in\mathbb{N}}$ be full rank-$\alpha+1$ alternating trees and $C_1, C_2, \ldots$ be $\mathbf{\Sigma}_{\alpha+1}$- or $\mathbf{\Pi}_{\alpha+1}$-circuits defined on these leaves. We obtain a restriction from the inductive hypothesis, applied to the collection of all rank-α children of the root nodes of the T_{ij}'s and to the collection of all $\mathbf{\Sigma}_\alpha$- or $\mathbf{\Pi}_\alpha$-children of the uppermost gates in the C_i's. We group the rank-α subtrees by their parent, so the hypotheses of the lemma ensure that each root node of a tree T_{ij} has infinitely many preserved children. After applying the resulting restriction, each T_{ij} is equivalent to a full rank-1 tree, and each C_i is equivalent to a $\mathbf{\Sigma}_1$- or $\mathbf{\Pi}_1$-circuit. Then by applying a further restriction obtained from the $\alpha = 1$ case, we achieve our desired overall restriction.

$\square$

At this point, we have already proven the Borel hierarchy theorem for finite-depth circuits, matching Sipser. To obtain the full result, we just need to address the limit case.

4.3.3 Tree decomposition

The proof of the limit case is much more delicate than that of the successor case, since each circuit can use as input leaves from trees with different heights. In order to apply the inductive hypothesis, we therefore need to develop a few properties of tree decomposition.

Proposition 4.5 (Left subtraction)**.** Given ordinals α and β with $\beta < \alpha$, there exists a unique ordinal γ such that $\beta + \gamma = \alpha$.

Proposition 4.6 (Right monotonicity)**.** Given ordinals β, γ and δ, we have $\beta + \delta < \beta + \gamma$ if and only if $\delta < \gamma$.

See [4] for a detailed treatment of ordinal arithmetic.

Definition 4.7. Given two full trees L and U we define the *grafted* tree $L + U$ by replacing each leaf of U by a copy of L.

A simple transfinite induction verifies that $\mathrm{rank}(L + U) = \mathrm{rank}(L) + \mathrm{rank}(U)$. We also have the following:

Lemma 4.8. *let T_α denote the full tree of rank α for any $\alpha < \omega_1$. Then we have whenever $\beta + \gamma = \alpha$ that $T_\beta + T_\gamma$ is a subtree of T_α rooted at the root node of T_α, a fact which we denote by $T_\beta + T_\gamma \leq T_\alpha$.*

Proof. We proceed by transfinite induction on γ. If $\gamma = 0$, then the result is immediate as $T_\beta + T_\gamma = T_\beta = T_\alpha$. For the successor step, suppose $\gamma = \delta + 1$ and that the claim holds for δ. Then $\alpha = \beta + \delta + 1$ is a successor ordinal, so the root node of T_α has countably many $T_{\beta+\delta} \geq T_\beta + T_\delta$ trees as children. Similarly, the root node of T_γ has countably many T_δ

trees as children, so the root node of $T_\beta + T_\gamma$ has countably many $T_\beta + T_\delta$ trees as children. Thus $T_\beta + T_\gamma \leq T_\alpha$, proving the successor case.

Now suppose γ is a limit ordinal and the claim holds for every $\delta < \gamma$. Then the root node of T_γ contains as children the trees T_δ for each $\delta < \gamma$. Thus $T_\beta + T_\gamma$ contains as children the trees $T_\beta + T_\delta \leq T_{\beta+\delta}$ for each $\delta < \gamma$. Since each $\beta + \delta < \beta + \gamma = \alpha$ by right monotonicity, the trees $T_{\beta+\delta}$ are all children of the root node of T_α. Thus $T_\beta + T_\gamma \leq T_\alpha$, proving the limit case.

$\square$

Finally, we prove a technical claim about embedding full trees in a copy of itself with "missing branches:"

Lemma 4.9. *let T_α denote the full tree of rank α for any $\alpha < \omega_1$, and let T'_α denote any tree obtained by removing a coinfinite number of children from each node in T_α. Then $T_\alpha \leq T'_\alpha$.*

Proof. We proceed by transfinite induction on α. The claim clearly holds for $\alpha = 0$. Now suppose $\alpha = \delta + 1$ for some ordinal δ and the claim holds for δ. Then the root node of T'_α has countably many T'_δ children, and each of these T'_δ children contains T_δ as a subtree. Thus $T_\alpha \leq T'_\alpha$.

Now suppose α is a limit ordinal and the claim holds for every $\delta \leq \alpha$. Then if we let $\gamma'_1, \gamma'_2, \ldots$ denote the ranks of the children of the root node of T'_α, we see that $\alpha = \sup_{i \in \mathbb{N}} \gamma'_i$. Thus we can map every rank-γ child T_γ of the root node of T_α to a distinct child T'_γ of T'_α with $\gamma < \gamma'$. Applying the inductive hypothesis tells us that $T_\gamma \leq T'_\gamma$ whenever $\gamma \leq \gamma'$, and we conclude that $T_\alpha \leq T'_\alpha$.

$\square$

4.3.4 The limit case

With this lemma in hand, we are now ready to prove the limit case of the restriction lemma. Our strategy will be similar to the $\alpha = 1$ case, but instead of repeatedly forcing $\mathbf{\Sigma}_1$- or $\mathbf{\Pi}_1$-circuits to be constant by setting finitely many literals (as in the $\alpha = 1$ case), we will repeatedly apply the inductive hypothesis to force each child of the root nodes of the C_i's to depend on only finitely many inputs.

Proof of the limit case. Suppose α is a limit ordinal, let $(T_{ij})_{i,j \in \mathbb{N}}$ be full rank-α alternating trees, and suppose $C_1, C_2, \ldots$ are $\mathbf{\Sigma}_\alpha$- or $\mathbf{\Pi}_\alpha$-circuits defined on these leaves. Let $D_1, D_2, \ldots$ denote the children of the uppermost gates of the C_i's. We write $S_{ij1}, S_{ij2}, \ldots$ to denote the children of the root nodes of the T_{ij}'s. We construct ρ via a series of nested restrictions, identifying the restricted circuits and trees with their simplified versions. At each stage, we maintain the invariant

$$\text{rank}(D_k) < \sup_{\ell \in \mathbb{N}} \left(\text{rank}\left(S_{ij\ell} \right) \right)$$

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for all $i, j, k \in \mathbb{N}$, which evidently holds before applying any restrictions since the right hand side is equal to α. Define the queue sequence $(q_n r_n)$ so that every pair of indices $(q, r) \in \mathbb{N}^2$ appears infinitely many times, and do the following for $s = 1, 2, \ldots$:

1. Choose a subtree $S_{q_s r_s \ell}$ which has not been forced and permanently preserve it, assigning one $*$. This "permanent" assignment means that we consider the $*$ fixed and cannot change it to a 0 or 1 in any subsequent step.

2. Let $\beta_s = \mathrm{rank}(D_s)$, and suppress all subtrees $S_{ij\ell}$ such that $\mathrm{rank}(S_{ij\ell}) < \beta_s$. The invariant ensures that infinitely many subtrees of each T_{ij} remain.

3. For each unforced $S_{ij\ell}$, let $\gamma_{ij\ell}$ denote the unique ordinal such $\beta_s + \gamma_{ij\ell} = \mathrm{rank}(S_{ij\ell})$. Using 4.8, we can restrict some nodes of $S_{ij\ell}$ so that $S_{ij\ell}$ is equivalent to an alternating tree $T_{\beta_s} + T_{\gamma_{ij\ell}}$.

4. Let $\mathcal{F}$ denote the family of all gates G in some D_k which are the uppermost gate of a subcircuit with rank at most β_s and whose parents are the uppermost gate of a subcircuit with rank strictly greater than β_s. Note that $D_s \in \mathcal{F}$. Extend the subcircuits rooted at each $G \in \mathcal{F}$ to be $\mathbf{\Sigma}_{\beta_s}$- or $\mathbf{\Pi}_{\beta_s}$-circuits.

5. Replace the subcircuit C rooted at each $G \in \mathcal{F}$ with the $\mathbf{\Sigma}_{\beta_s+1}$-circuit

$$\bigvee_{\sigma_1 \cdots \sigma_s \in \Sigma^s} \left(C^{\sigma_1 \cdots \sigma_s} \wedge \bigwedge_{i=1}^{s} x_i = \sigma_i \right),$$

where $C^{\sigma_1 \cdots \sigma_s}$ denotes the circuit C with each starred literal x_i set to σ_i.

6. Now apply the inductive hypothesis to the $\mathbf{\Sigma}_{\beta_s}$- or $\mathbf{\Pi}_{\beta_s}$-circuits with uppermost gates in $\mathcal{F}$ and to the subtrees T_{β_s} grouped so the lemma guarantees each node in $T_{\gamma_{ij\ell}}$ with infinitely many trees T_{β_s} as children has infinitely many of those children preserved. Let ρ_s denote the restriction so obtained.

7. For each $(S_{ij\ell})^{\rho_s}$, apply a further restriction so that we can identify the restricted tree with $T_{\gamma_{ij\ell}}$. Lemma 4.9 ensures that this is possible.

8. Replace all circuits and trees with their equivalent simplified versions.

We make a few observations about the resulting circuit at the end of each step. First, since each $(C^{\sigma_1 \cdots \sigma_s})^{\rho_s}$ depends on only finitely many preserved literals, the circuit

$$\left(\bigvee_{\sigma_1 \cdots \sigma_s \in \Sigma^s} \left(C^{\sigma_1 \cdots \sigma_s} \wedge \bigwedge_{i=1}^{s} x_i = \sigma_i \right) \right)^{\rho_s}$$

also depends on only finitely many preserved or permanently preserved literals and hence lies in $\mathbf{\Sigma}_0/\mathbf{\Pi}_0$. Each restricted $(D_k)^{\rho_s}$ therefore has rank δ_k, where δ_k is the unique ordinal

such that $\beta_s + \delta_k = \operatorname{rank}(D_k)$. In particular, we see that $(D_s)^{\rho_s}$ is equivalent to a finite circuit.

Each restricted subtree $(S_{ij\ell})^{\rho_s}$ has rank $\gamma_{ij\ell}$ with $\beta_s + \gamma_{ij\ell} = \operatorname{rank}(S_{ij\ell})$. Fix $i, j \in \mathbb{N}$. Then there exists some $S_{ij\ell}$ with $\operatorname{rank}(D_k) < \operatorname{rank}(S_{ij\ell})$, and thus

$$\beta_s + \delta_k = \operatorname{rank}(D_k) < \sup_{\ell \in \mathbb{N}} \left(\operatorname{rank}(S_{ij\ell})\right) = \beta_s + \sup_{\ell \in \mathbb{N}} \gamma_{ij\ell}.$$

This means that $\delta_k < \sup_{\ell \in \mathbb{N}} \gamma_{ij\ell}$ by right monotonicity, and this shows that the invariant is preserved after each step.

After all stages are complete, we can preserve any remaining subtrees and apply the resulting restriction ρ. After this application, each T_{ij} is equivalent to a full rank-1 tree, and each C_i is equivalent to a $\mathbf{\Sigma}_1$- or $\mathbf{\Pi}_1$-circuit. Thus we can apply a further restriction obtained from the $\alpha = 1$ case to complete the induction in the limit case and proves the theorem.

$\square$

There does not seem to be a natural way to extend the class of rank-α circuits to the finite case, but perhaps there is some clever way to make this notion precise. If so, our combinatorial proof of the Borel hierarchy theorem or the ideas within could perhaps be adapted to provide a hierarchy theorem in this setting. The restriction lemma, however, gives us some elegant new results about Borel functions, which we explore in the following section.

5   Consequences of the restriction lemma

The restriction lemma is a powerful tool, and in this section, we will establish two Ramsey-like results for Borel functions/countable circuits with incredibly short proofs.

Corollary 5.1 (Constant restriction). *For any countable, well-founded, deterministic circuit C defined on infinitely many variables, there exists a restriction ρ preserving infinitely many variables such that C^ρ is constant.*

Proof. Partition the variables $x_1, x_2, \ldots$ of C into countably many countably infinite sets $S_1, S_2, \ldots$. Create countably many full rank-α alternating trees T_i with leaves S_i. Then the restriction lemma gives us a restriction ρ' such that $C^{\rho'}$ depends on only finitely many variables and infinitely many trees are preserved. This implies that ρ' preserves infinitely many variables. By extending ρ' to assign 0 or 1 to each of the finitely many variables $C^{\rho'}$ depends on, we obtain a new restriction ρ' satisfying the conditions of the corollary.

$\square$

Corollary 5.2. *No countable, well-founded, deterministic circuit C can compute an infinite parity function f (whose output flips when any input bit is flipped).*

Proof. Suppose for the sake of contradiction such a circuit C computes f. Then the previous corollary gives us a restriction ρ such that C^ρ computes f^ρ. This is impossible, since C^ρ is constant and f^ρ is another infinite parity function.

$\square$

The above proof, unlike that presented in [2], does not rely on any external machinery from descriptive set theory. Furthermore, both the Ramsey-like result and the corollary about PARITY follow a similar argument to the classical approach in the finite case, where analogous results are proven using Håstad's switching lemma ([3], [1]). This approach in the infinite case therefore seems to be the most "compatible" with the finite case.

6 Future directions

6.1 The Galvin-Prikry theorem

The Galvin-Prikry theorem is a Ramsey-like result in descriptive set theory which states the following:

Theorem 6.1 (Galvin-Prikry). *For any Borel function $f \colon \mathcal{P}(\mathbb{N}) \to \{0, 1\}$, there exists an infinite set $S \subseteq \mathbb{N}$ such that f is constant on every infinite subset of S.*

This theorem immediately implies that no Borel function computes an infinite parity function, since the restriction of such a parity function to an infinite set S is another infinite parity function. The Galvin-Prikry theorem also implies Corollary 5.1. That corollary is equivalent to the following statement, rephrased to avoid the language of circuits and restrictions:

Corollary 6.2. *For any Borel function $f \colon \mathcal{P}(\mathbb{N}) \to \{0, 1\}$, there exists an infinite set $S \subseteq \mathbb{N}$ and set $R \subseteq \mathbb{N} \setminus S$ such that f is constant on every set of the form $X \cup R$ with $X \subseteq S$.*

Proof. Using Theorem 6.1, we obtain $S' \subseteq \mathbb{N}$ and $y \in \{0, 1\}$ be such that S is infinite and $f(X) = y$ for all infinite subsets X of S'. Partition S' into two disjoint infinite sets S and R. Then S is infinite and $f(X \cup R) = y$ for any $X \subseteq S$, as desired.

$\square$

The standard proof of the Galvin-Prikry theorem relies on a topological argument ([5]), but our circuit-based proof in the preceding section gives a purely combinatorial proof relying on no external machinery.

Given the analogy between countable deterministic circuits and polynomial-sized circuit families, one might naively expect a Galvin-Prikry-like result to hold for the class $\mathsf{P/poly}$. However, the fact that PARITY $\in \mathsf{P/poly}$ implies that no nontrivial Ramsey-like result can be proven for these circuits. We are currently trying to prove a version of the Galvin-Prikry theorem for AC^0, which would give us an easy method to prove that certain problems lie outside of this class.

6.2 The Lusin separation theorem

In [7], Michael Sipser provides a purely combinatorial proof of the foundational result from descriptive set theory that analytic sets are not closed under complement. Sipser observes that an analogous proof of this fact for polynomial-sized circuits would show that $\mathsf{NP/poly} \neq \mathsf{coNP/poly}$ and thus $\mathsf{P} \neq \mathsf{NP}$. Sipser's proof does not extend to the polynomial case, and he acknowledges that this approach seems unlikely to succeed.

We are investigating a different foundational result, namely the Lusin separation theorem:

Theorem 6.3 (Lusin separation). *For any two disjoint analytic sets $A, C \subseteq \Sigma^\omega$, there exists a Borel set $B \subseteq \Sigma^\omega$ such that $A \subseteq B$ and $B \cap C = \emptyset$.*

If we take C to be A^c in the above theorem, we see that any analytic set A whose complement is also analytic must actually be a Borel set. In other words, if a set and its complement can both be computed by countable nondeterministic circuits, then the set can be computed by a countable deterministic circuit. The polynomial analogue of this theorem is the claim that $\mathsf{P/poly} = \mathsf{NP/poly} \cap \mathsf{coNP/poly}$.

There are constructive proofs of the Lusin separation theorem, and applying these proofs directly to the polynomial case gives us a circuit family that grows exponentially. However, we are searching for ways to control the "separation tree" ([5]) used in the construction to find polynomial-sized circuits for a suitable subclass of $\mathsf{NP/poly} \cap \mathsf{coNP/poly}$.

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