

# Descriptive Set Theory and Circuit Complexity

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## Abstract

We discuss the deep connections between countable circuits and Borel/analytic sets, which inspired the original proofs that PARITY  $\notin \text{AC}^0$  and that the  $\text{AC}^0$  hierarchy does not collapse. We prove the correspondence between countable circuits and Borel/analytic sets, describe the history of early  $\text{AC}^0$  lower bounds and their relation to the Borel hierarchy theorem, and outline other potential ways in which descriptive set theory could be used to give new results about finite circuits. Our main technical results are new circuit-based proofs of the Borel hierarchy theorem and a Ramsey-theoretic result about Borel functions.

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# 1 Introduction

We examine a beautiful connection between circuit complexity and descriptive set theory. First explored in the early 1980s, this connection links countable deterministic and nondeterministic circuits with Borel and analytic sets, respectively. The link has inspired new proofs of results from descriptive set theory, as well as new theorems about finite circuits.

I am deeply grateful for my mentor, Professor Anton Bernshteyn, who worked with me on this project. He introduced me to descriptive set theory and its connection to circuit complexity, suggested theorems and problems I should look into, and helped me refine my ideas and proofs. His insights and support were invaluable, and this project could not have happened without him.

## 1.1 Outline

In Section 2, we provide a brief overview of our definitions and notation.

We then describe the key link between descriptive set theory and circuit complexity in Section 3. We prove the equivalence of Borel sets with countable deterministic circuits, and demonstrate the equivalence of analytic sets with countable nondeterministic circuits, and then illustrate how results from descriptive set theory can be translated into the language of circuits.

In Sections 4, 5, and 6, we explore some classic theorems from descriptive set theory and the implications they have on circuit complexity. We examine the Borel hierarchy theorem in Section 4, which has historically had the most consequences in circuit complexity. We examine the origins of  $\text{AC}^0$  lower bounds in this section, as well as the process of converting results from descriptive set theory to results about finite circuits.

We then turn our attention to the Galvin-Prikry theorem, a Ramsey-theoretic result about Borel functions, in Section 5. Finally, we examine the Lusin separation theorem, as well as the dramatic consequences it would have if adapted to the finite case, in Section 6.

## 1.2 Summary of results

The technical highlight of this report is a new combinatorial proof of the Borel hierarchy theorem in Section 4.3. Michael Sipser provided a combinatorial proof for the finite case in [6], but we prove the claim for the full transfinite hierarchy.

To prove the theorem, we develop a restriction lemma which also gives us a useful Ramsey-like result about countable circuits in Section 5.1. This result also follows from the Galvin-Prikry theorem, but our we provide the first purely combinatorial proof.

We are currently pursuing results relating to the Lusin separation theorem and Galvin-Prikry theorem, and our research directions are detailed in Sections 5 and 6.

## 2 Basic notions

The reader is assumed to have some familiarity with descriptive set theory and circuit complexity. The following definitions are intended to clarify our conventions.

### 2.1 Borel and analytic sets

We consider the binary alphabet  $\Sigma = \{0, 1\}$  and *Cantor space*  $\Sigma^\omega$ , equipped with the topology generated by basic open sets of the form  $x\Sigma^\omega$  for  $x \in \Sigma^*$ .

**Definition 2.1.** We call a set  $S \subseteq \Sigma^\omega$  a  $\Sigma_1$ -set (resp.  $\Pi_1$ ) if it is open (resp. closed). A set is  $\Sigma_k$  (resp.  $\Pi_k$ ) if it is a countable union (resp. intersection) of sets  $S_1, S_2, \dots$ , each of which are in  $\Sigma_j$  (resp.  $\Pi_j$ ) for some  $j < k$ .

**Definition 2.2.** A set  $S \subseteq \Sigma^\omega$  is *Borel* if it is  $\Sigma_\alpha$  for some  $\alpha < \omega_1$ . The *rank* of a Borel set  $B$  is the smallest  $\alpha$  such that  $B \in \Sigma_\alpha \cup \Pi_\alpha$ .

**Definition 2.3.** A set  $S \subseteq \Sigma^\omega$  is *analytic* if it is the projection of a Borel set  $B \subseteq \Sigma^\omega \times \Sigma^\omega$  equipped with the product topology (i.e. we can write

$$\{x \in \Sigma^\omega : (x, y) \in B \text{ for some } y \in \Sigma^\omega\}.$$

### 2.2 Deterministic circuits

We consider countable and well-founded circuits  $C$  with  $\wedge$ - and  $\vee$ -gates over the literals  $x_1\bar{x}_1, x_2, \bar{x}_2, \dots$ , which compute functions  $f_C: \Sigma^\omega \rightarrow \{0, 1\}$  and sets  $f_C^{-1}(\{1\})$ .

**Definition 2.4.** We call a circuit  $\Sigma_0$  or  $\Pi_0$  if it is finite. A  $\Sigma_k$ -circuit (resp.  $\Pi_k$ -circuit) is a  $\vee$ -gate (resp.  $\wedge$ -gate) with countably many children  $C_1, C_2, \dots$ , each of which are  $\Pi_j$ -circuits (resp.  $\Sigma_j$ -circuits) for some  $j < k$ .

**Definition 2.5.** The *rank* of a circuit  $C$  is the smallest  $\alpha$  such that  $C$  is a  $\Sigma_\alpha$ - or  $\Pi_\alpha$ -circuit.

The rank of any countable and well-founded circuit is the supremum of countably many countable ordinals and is therefore less than  $\omega_1$ . We also see that the rank of a circuit is either equal to its depth  $d$  or to  $d + 1$ .

### 2.3 Nondeterministic circuits

A nondeterministic circuit  $C$  over the deterministic literals  $x_1\bar{x}_1, x_2, \bar{x}_2, \dots$  and nondeterministic literals  $y_1\bar{y}_1, y_2, \bar{y}_2, \dots$  computes the function

$$f_C(x) = \begin{cases} 1 & \text{if } C(x, y) = 1 \text{ for some } y \in \Sigma^\omega \\ 0 & \text{otherwise} \end{cases}$$

and set  $f_C^{-1}(\{1\})$ . We define rank and the classes of  $\Sigma_k$ -circuits and  $\Pi_k$ -circuits analogously to the deterministic case.

### 3 Equivalence of circuits and Borel/analytic sets

Our similar choice of notation between Borel sets and deterministic circuits is no coincidence. These objects correspond precisely, and we observe a similar connection between analytic sets and nondeterministic circuits. These correspondences, which we prove in this section, allow us to translate results from one field to the other. In this section, all circuits are well-founded and countable.

#### 3.1 Borel sets and deterministic circuits

**Theorem 3.1.** *For  $k \geq 1$ , a set  $S \subseteq \Sigma^\omega$  is  $\Sigma_k$  (resp.  $\Pi_k$ ) if and only if it can be computed by a deterministic  $\Sigma_k$  (resp.  $\Pi_k$ )-circuit.*

*Proof.* We will prove the claim for  $\Sigma_1$ , since the  $\Pi_1$  case is dual and the inductive step is immediate.

If  $S \in \Sigma_0$ , then  $S$  can be written as a countable union of basic open sets  $x\Sigma^\omega$  by the separability of  $\Sigma^\omega$ . Each of these basic open sets can be computed by a finite  $\Pi_0$ -circuit, and taking an  $\vee$ -gate with each of these circuits as children gives us our desired  $\Sigma_1$ -circuit.

Conversely, every set computed by  $\Pi_0$ -circuit is either  $\emptyset$  or of the form

$$\Sigma^{i_1}x_1\Sigma^{i_2}x_2 \cdots \Sigma^{i_n}x_n\Sigma^\omega$$

for some  $n \geq 0$  and  $i_1, \dots, i_n \geq 0$ . Such sets can be written as the union of the basic open sets

$$w_1x_1w_2x_2 \cdots w_nx_n\Sigma^\omega$$

for  $w_1 \in \Sigma^{i_1}, w_2 \in \Sigma^{i_2}, \dots$  and are therefore open. Thus any set computed by a  $\Sigma_1$ -circuit is open as a union of open sets.

□

The above proof explains why we consider the rank of a circuit instead of just its depth: to ensure that  $\Sigma_1$ -circuits can compute open sets.

**Corollary 3.1.** *A subset of  $\Sigma^\omega$  is Borel if and only if it is definable by a countable deterministic circuit.*

Because any two uncountable Polish spaces are Borel isomorphic ([5]), this result also applies to  $\mathbb{R}$ . In other words, we can fix some Borel isomorphism  $\varphi: \mathbb{R} \rightarrow \Sigma^\omega$ , and we then

have that a subset  $S$  of  $\mathbb{R}$  is Borel if and only if some deterministic circuit computes  $\varphi(S)$ .

We can characterize Borel subsets of  $\mathbb{R}$  more explicitly with binary representations. If we exclude binary representations which are eventually all ones, then the binary representation map is a Borel isomorphism from  $[0, 1)$  to a Borel subset of  $2^\omega$ . This means that a subset of  $[0, 1)$  is Borel if and only if its image under this map can be computed by a deterministic circuit.

### 3.2 Analytic sets and nondeterministic circuits

**Theorem 3.2.** *Analytic subsets of  $\Sigma^\omega$  are precisely those which can be defined by countable nondeterministic circuits.*

*Proof.* A similar argument as the one in the previous proof tells us that a circuit over  $\Sigma^\omega \times \Sigma^\omega$  is  $\Sigma_1$  if and only if the set it computes is open in the product topology on  $\Sigma^\omega \times \Sigma^\omega$ . This means that a set  $B \subseteq \Sigma^\omega \times \Sigma^\omega$  is Borel if and only if it can be computed by a countable deterministic circuit over  $\Sigma^\omega \times \Sigma^\omega$ . The claim follows.  $\square$

### 3.3 Translating a theorem about $G_\delta$ sets

There are many ways one can take advantage of this connection. The fields of descriptive set theory and circuit complexity are quite different. Proofs in the former field are often topological in nature, while proofs in the latter field are often combinatorial. It is often instructive to translate a theorem from one field to the other and then try to find an alternative proof of the theorem that doesn't rely on the machinery of its "native" subject. The following result, for example, is typically proven with a topological argument ([5]). However, by translating it to the realm of circuits, we can provide an elegant combinatorial proof:

**Theorem 3.3.** *A set  $S \subseteq \Sigma^\omega$  is analytic if and only if it is the projection of a  $G_\delta$  (i.e.  $\Pi_2$ ) subset of  $\Sigma^\omega \times \Sigma^\omega$ .*

*Proof.* It suffices to show that every nondeterministic circuit  $C$  can be simulated by a depth-2 nondeterministic circuit whose root note is an  $\wedge$ -gate. To this end, we let  $G_1, G_2, \dots$  denote the gates of  $C$ , with  $G_1$  being the root. We define a new circuit  $C'$  over the deterministic variables  $x_1, x_2, \dots$  and nondeterministic variables  $y_1, z_1, y_2, z_2, \dots$ , where the  $y_i$ 's correspond to the nondeterministic inputs of  $C$  and each  $z_i$  corresponds to  $G_i$ . The goal of the  $z_i$ 's is to nondeterministically guess the value of the gates in  $C$ . To this end, we do the following for each  $i = 1, 2, \dots$ :

- If  $G_i$  is an  $\vee$ -gate with inputs  $c_1, c_2, \dots \in \{x_1, \bar{x}_1, \dots, y_1, \bar{y}_1, \dots, G_1, G_2, \dots\}$ , create a depth-1 circuit  $\neg z_i \vee c_1 \vee c_2 \vee \dots$ , where any inputs  $G_j$  are replaced by  $z_j$ .

- If  $G_i$  is an  $\wedge$ -gate with inputs  $c_1, c_2, \dots$ , create countably many depth-1 circuits  $\neg z_i \vee c_1, \neg z_i \vee c_2, \dots$ , where any inputs  $G_j$  are replaced by  $z_j$ .

If we create an  $\wedge$ -gate and connect it to  $z_1$  and each of these depth-1 circuits created above, we obtain a depth-2 nondeterministic circuit which is equivalent to  $C$ .

□

Often, finite circuit complexity stands to benefit from this connection. Descriptive set theory is the older of the two fields, with many established results and techniques. This all carries over into the realm of countable circuits, and once we find a combinatorial proof for a fact about these circuits, it is often possible to adapt the argument to the finite case. We will see such an example in the next section.

## 4 The Borel hierarchy theorem

The Borel hierarchy theorem is a classical result from descriptive set theory, which claims the following:

**Theorem 4.1** (Borel hierarchy). *We have for every  $\alpha < \beta < \omega_1$  that  $\Sigma_\alpha \subsetneq \Sigma_\beta$ .*

In other words, the result is that the Borel hierarchy does not collapse. The standard proof of this fact is based on showing that  $\Sigma_\alpha \subsetneq \Pi_\alpha$  via universal sets and diagonalization, and such a proof is provided as Theorem 22.4 in [5]. Later in this section, we will provide a new, purely combinatorial proof of this fact.

This result ultimately led to the groundbreaking  $\text{AC}^0$  depth hierarchy theorem, and we describe the history of this development below.

### 4.1 The origins of $\text{AC}^0$ lower bounds

Recall that  $\text{AC}_d^0$  is the set of problems which can be computed by depth- $d$  polynomial-sized circuit families and  $\text{AC}^0 = \bigcup_{d=0}^{\infty} \text{AC}_d^0$ .

In 1981, Merrick Furst, James Saxe, and Michael Sipser found the first super-polynomial lower bound on constant depth circuits computing an explicit function when they showed in [2] that  $\text{PARITY} \notin \text{AC}^0$ . Even as early as in this paper, they describe connections to descriptive set theory, referencing a proof that there is no countable deterministic circuit computing an infinite parity function (a function whose output flips if any one input bit is flipped). The authors use the measurability of Borel sets to show this, and we will provide two alternative proofs later. They also describe an analogy between polynomial growth and countable sets: Loosely speaking, the power set operation is “forbidden” in both settings as it takes us to exponential growth in the former setting and uncountable sets in the latter. Most other operations, on the other hand, are “allowed” in both settings.

In 1983, Sipser established the full  $\text{AC}^0$  hierarchy in [6] by proving that  $\text{AC}_d^0 \subsetneq \text{AC}_{d+1}^0$  for every  $d \geq 0$ . His proof used probabilistic restrictions, which were the tool of choice in early circuit lower bounds. These techniques were later improved by Håstad in [3], where he developed his famous switching lemma and used it to prove sharp bounds on the size of depth- $d$  circuits computing PARITY. Probabilistic restrictions remain a common tool in circuit complexity, and many theorists are unaware of how Sipser actually came up with his proof technique.

## 4.2 From descriptive set theory to finite circuits

The Borel hierarchy theorem can also be interpreted as saying that depth- $\alpha + 1$  deterministic countable circuits are more powerful than depth- $\alpha$  circuits, and this connection inspired Sipser's  $\text{AC}^0$  depth hierarchy proof in the following manner:

1. Sipser first found a new combinatorial circuit-based proof of the Borel hierarchy theorem in the case where  $\alpha$  is finite (i.e. for finite-depth countable circuits).
2. Then, Sipser used probabilistic restrictions to adapt this proof to polynomial-sized circuit families to obtain an analogous result for the  $\text{AC}^0$  hierarchy.

Sipser outlines this process precisely in his paper.

This is perhaps the greatest success story of using analogies to descriptive set theory in order to derive results about polynomial-sized circuits. Even if probabilistic restrictions are the main ingredient in Sipser's proof, descriptive set theory was the primary inspiration. The Borel hierarchy theorem is just a single result in descriptive set theory which had a profound impact on circuit complexity. One naturally wonders whether other theorems have analogues for polynomial-sized circuits.

## 4.3 A combinatorial proof of the Borel hierarchy theorem

Sipser only proves the finite-depth case of the Borel hierarchy theorem, and it is a natural question whether the full result can be proven combinatorially. We now provide such a proof.

### 4.3.1 Setup and the main lemma

**Definition 4.1.** The *full alternating trees* of rank  $\alpha < \omega_1$  are the circuits defined recursively as follows:

- The full rank-0  $\vee$ -tree and  $\wedge$ -tree are both the identity circuit on a single bit.

- For any successor ordinal  $\alpha + 1$ , we define the full rank- $\alpha + 1 \vee$  (resp.  $\wedge$ )-tree to be an  $\vee$ -gate with countably many rank- $\alpha \wedge$  (resp.  $\vee$ )-trees as children.
- If  $\alpha$  is a limit ordinal, we define the full rank- $\alpha \vee$  (resp.  $\wedge$ )-tree to be an  $\vee$ -gate with a full rank- $\beta \wedge$  (resp.  $\vee$ )-tree child for every  $\beta < \alpha$  (note that there are countably many such  $\beta$ 's).

We identify the set of (countably many) leaves of each full alternating  $\vee$ -tree with  $x_1, x_2, \dots$ , and we let  $f_\alpha : \mathcal{P}(\{x_1, x_2, \dots\}) \rightarrow \{0, 1\}$  denote the function computed by each such tree.

Since each  $f_{\alpha+1}$  is computed by a circuit in  $\Sigma_{\alpha+1}$ , it suffices to show that each  $f_{\alpha+1}$  cannot be computed by a circuit in  $\Sigma_\alpha$ . We prove this using restrictions, functions  $\rho : \omega \rightarrow \{0, 1, *\}$  which, for every circuit  $C$  on  $\omega$ , induce a *restricted* circuit  $C^\rho$  whose inputs  $x_i$  are left untouched if  $\rho(x_i) = *$  and replaced with  $\rho(x_i)$  otherwise.

**Definition 4.2.** We call a circuit *forced* by  $\rho$  if it is equivalent to a constant 0- or 1-circuit. We call a circuit *suppressed* if its top gate is an  $\vee$ -gate and it is forced to 1 or if its top gate is an  $\wedge$ -gate and it is forced to 0. A forced circuit is *overriding* if it is not suppressed. We call a circuit *preserved* by  $\rho$  if it is equivalent to the identity circuit on a single literal.

We write “child of a circuit/tree” to refer to a child of the uppermost gate/root node of the circuit/tree. Notice that, in an alternating circuit, suppressed children do not affect the value of their parents and overriding children force their parents. Notice also that any depth-1 circuit can be suppressed by assigning a single literal, while it can only be made overriding if all of its literals are assigned. A circuit can be preserved by assigning one of its literals to \* and the rest to 0 or 1. The following lemma is the heart of our argument:

**Lemma 4.1** (The restriction lemma). *For any ordinal  $\alpha < \omega_1$ , countable disjoint collection of full rank- $\alpha$  alternating trees  $(T_{ij})_{i,j \in \mathbb{N}}$ , and at most countable collection of  $\Sigma_\alpha$ - or  $\Pi_\alpha$ -circuits  $(C_i)_{i \in \mathbb{N}}$  defined on the leaves of these trees, there exists a restriction  $\rho$  such that each  $C_i^\rho$  is equivalent to a finite circuit, each  $T_{ij}^\rho$  is either suppressed or preserved, and infinitely many trees  $T_{ij}^\rho$  are preserved for each fixed  $j$ .*

We will prove the lemma by transfinite induction. The claim is immediate for  $\alpha = 0$ , so we just need to address the successor and limit cases. Before this though, let us see how the lemma implies the full theorem:

*Proof of 4.1.* Suppose  $\alpha < \beta$ . The full alternating  $\vee$ -tree of rank  $\beta$  contains a full alternating tree of rank  $\alpha + 1$  as a subtree, and by applying a suitable restriction  $\rho$  and relabeling, we obtain a circuit equivalent to a full alternating tree of rank  $\alpha + 1$ . If we could compute  $f_\beta$  with a  $\Sigma_\alpha$ -circuit, the restriction of this circuit would be a  $\Sigma_\alpha$ -circuit computing the same function as this tree. The claim therefore reduces to proving that a full alternating tree of rank  $\alpha + 1$  is not equivalent to any  $\Sigma_\alpha$ -circuit.

To this end, suppose for the sake of contradiction that  $C$  is a  $\Sigma_\alpha$ -circuit computing the same function as a full alternating tree of rank  $\alpha + 1$ . We apply the restriction lemma to the rank- $\alpha$  children of the root node in this tree, labeled arbitrarily, and to the  $\Sigma_\alpha$ -circuit  $C$ . Applying the restriction we obtain gives us a finite circuit  $C^\rho$  equivalent to a full  $\vee$ - or  $\wedge$ -tree of depth 1. This is exactly our desired contradiction.

□

#### 4.3.2 The successor case

We now present the proof of the successor case, which is very similar to Sipser's original argument.

*Proof of the successor case.* Let  $(T_{ij})_{i,j \in \mathbb{N}}$  be full rank- $\alpha+1$  alternating trees and  $C_1, C_2, \dots$  be  $\Sigma_{\alpha+1}$ - or  $\Pi_{\alpha+1}$ -circuits defined on these leaves. We obtain a restriction from the inductive hypothesis, applied to the collection of all rank- $\alpha$  children of the root nodes of the  $T_{ij}$ 's and to the collection of all  $\Sigma_\alpha$ - or  $\Pi_\alpha$ -children of the uppermost gates in the  $C_i$ 's. After applying the resulting restriction, each  $T_{ij}$  is equivalent to a full rank-1 tree, and each  $C_i$  is equivalent to a  $\Sigma_1$ - or  $\Pi_1$ -circuit. We identify each  $T_{ij}$  and  $C_i$  with these equivalent circuits. Our goal is to find a further restriction  $\rho$  such that each  $T_{ij}^\rho$  is suppressed or preserved, infinitely many  $T_{ij}^\rho$ 's are preserved for each fixed  $j$ , and each  $C_i^\rho$  is equivalent to a finite circuit. Finding such a restriction proves the inductive step.

The challenge of constructing  $\rho$  is that we need to assign infinitely many \*'s in order to ensure that infinitely many  $T_{ij}^\rho$ 's are preserved for each fixed  $j$ , but not in a manner that makes any  $C_i^\rho$  depends on infinitely many \*'s. To address this difficulty, we define the *queue sequence*  $(q_n)_{n \in \mathbb{N}} = (1, 1, 2, 1, 2, 3, 1, 2, 3, 4, \dots)$  so that each  $n \in \mathbb{N}$  appears infinitely many times in  $(q_n)$ . We define  $\rho$  via a sequence of partial restrictions  $\rho_i$  such that each  $\rho_i$  assigns  $i$  \*'s and the circuit  $C_i$  depends only on these \*'s. Let the domain of  $\rho_0$  be empty. Then do the following for  $i = 1, 2, \dots$ :

1. Preserve some tree  $T_{q_{i-1}j}$  by extending  $\rho_{i-1}$  (assigning one \*).
2. For each of the  $2^i$  possible settings of the bits  $x_i$  with  $\rho_{i-1}(x_i) = *$  to 0 or 1, do the following:
  - (a) If  $C_i$  is unforced under this assignment, it must have an unforced  $\Sigma_0/\Pi_0$  child. Extend  $\rho_{i-1}$  to force this child to be overriding by assigning finitely many bits to 0 or 1.
  - (b) For each  $T_{ij}$  containing a bit so assigned, extend  $\rho_{i-1}$  to assign all other bits of  $T_{ij}$  such that  $T_{ij}$  is suppressed.

After all of these steps, we see that each  $C_i$  depends only on the finitely many bits  $x_i$  such that  $\rho_i(x_i) = *$  and is hence equivalent to a finite circuit. We also have that infinitely  $T_{ij}$ 's

are preserved for each fixed  $j$ . By assigning all remaining literals so that every other  $T_{ij}$  is preserved, we get our desired restriction  $\rho$ .

Finally, we obtain a new restriction by applying  $\rho$  to the preserved literals from our original restriction obtained from the inductive hypothesis. This combined restriction satisfies the conditions of the lemma, completing the induction in the successor case.

□

At this point, we have already proven the Borel hierarchy theorem for finite-depth circuits, matching Sipser. To obtain the full result, we just need to address the limit case.

#### 4.3.3 Tree decomposition

The proof of the limit case is much more delicate than that of the successor case, since each circuit can use as input leaves from trees with different heights. In order to apply the inductive hypothesis, we therefore need to develop a few properties of tree decomposition.

**Proposition 4.1** (Left subtraction). Given ordinals  $\alpha$  and  $\beta$  with  $\beta < \alpha$ , there exists a unique ordinal  $\gamma$  such that  $\beta + \gamma = \alpha$ .

**Proposition 4.2** (Right monotonicity). Given ordinals  $\beta$ ,  $\gamma$  and  $\delta$ , we have  $\beta + \delta < \beta + \gamma$  if and only if  $\delta < \gamma$ .

See [4] for a detailed treatment of ordinal arithmetic.

**Definition 4.3.** Given two full trees  $L$  and  $U$  we define the *grafted* tree  $L + U$  by replacing each leaf of  $U$  by a copy of  $L$ .

A simple transfinite induction verifies that  $\text{rank}(L + U) = \text{rank}(L) + \text{rank}(U)$ . We also have the following:

**Lemma 4.2.** let  $T_\alpha$  denote the full tree of rank  $\alpha$  for any  $\alpha < \omega_1$ . Then we have whenever  $\beta + \gamma = \alpha$  that  $T_\beta + T_\gamma$  is a subtree of  $T_\alpha$  rooted at the root node of  $T_\alpha$ , which we denote by  $T_\beta + T_\gamma \subseteq T_\alpha$ .

*Proof.* We proceed by transfinite induction on  $\gamma$ . If  $\gamma = 0$ , then the result is immediate as  $T_\beta + T_0 = T_\beta = T_\alpha$ . For the successor step, suppose  $\gamma = \delta + 1$  and that the claim holds for  $\delta$ . Then  $\alpha = \beta + \delta + 1$  is a successor ordinal, so the root node of  $T_\alpha$  has countably many  $T_{\beta+\delta} \supseteq T_\beta + T_\delta$  trees as children. Similarly, the root node of  $T_\gamma$  has countably many  $T_\delta$  trees as children, so the root node of  $T_\beta + T_\gamma$  has countably many  $T_\beta + T_\delta$  trees as children. Thus  $T_\beta + T_\gamma \subseteq T_\alpha$ , proving the successor case.

Now suppose  $\gamma$  is a limit ordinal and the claim holds for every  $\delta < \gamma$ . Then the root node of  $T_\gamma$  contains as children the trees  $T_\delta$  for each  $\delta < \gamma$ . Thus  $T_\beta + T_\gamma$  contains as children the trees  $T_\beta + T_\delta \subseteq T_{\beta+\delta}$  for each  $\delta < \gamma$ . Since each  $\beta + \delta < \beta + \gamma = \alpha$  by right monotonicity,

the trees  $T_{\beta+\delta}$  are all children of the root node of  $T_\alpha$ . Thus  $T_\beta + T_\gamma \subseteq T_\alpha$ , proving the limit case.  $\square$

#### 4.3.4 The limit case

With this lemma in hand, we are now ready to prove the limit case of the restriction lemma:

*Proof of the limit case.* Suppose  $\alpha$  is a limit ordinal, let  $(T_{ij})_{i,j \in \mathbb{N}}$  be full rank- $\alpha$  alternating trees, and suppose  $C_1, C_2, \dots$  are  $\Sigma_\alpha$ - or  $\Pi_\alpha$ -circuits defined on these leaves. Let  $D_1, D_2, \dots$  denote the children of the uppermost gates of the  $C_i$ 's. We write  $S_{ij1}, S_{ij2}, \dots$  to denote the children of the root nodes of the  $T_{ij}$ 's. We construct  $\rho$  via a series of nested restrictions, identifying the restricted circuits and trees with their simplified versions. At each stage, we maintain the invariant

$$\text{rank}(D_k) < \sup_{\ell \in \mathbb{N}} (\text{rank}(S_{ij\ell}))$$

for all  $i, j, k \in \mathbb{N}$ , which evidently holds before applying any restrictions since the right hand side is equal to  $\alpha$ . Define the queue sequence  $(q_n r_n)$  so that every pair of indices  $(q, r) \in \mathbb{N}^2$  appears infinitely many times, and do the following for  $s = 1, 2, \dots$ :

1. Choose a subtree  $S_{q_s r_s \ell}$  which has not been forced and permanently preserve it, assigning one  $*$ . This “permanent” assignment means that we consider the  $*$  fixed and cannot change it to a 0 or 1 in any subsequent step.
2. Let  $\beta_s = \text{rank}(D_s)$ , and suppress all subtrees  $S_{ij\ell}$  such that  $\text{rank}(S_{ij\ell}) < \beta_s$ . The invariant ensures that infinitely many subtrees of each  $T_{ij}$  remain.
3. Replace  $D_s$  with the  $\Sigma_{\beta_s+1}$ -circuit

$$\bigvee_{\sigma_1 \cdots \sigma_s \in \Sigma^s} \left( D_s^{\sigma_1 \cdots \sigma_s} \wedge \bigwedge_{i=1}^s x_i = \sigma_i \right),$$

where  $D_s^{\sigma_1 \cdots \sigma_s}$  denotes the circuit  $D_s$  with each starred literal  $x_i$  set to  $\sigma_i$ .

4. For each unforced  $S_{ij\ell}$ , let  $\gamma_{ij\ell}$  denote the unique ordinal such  $\beta_s + \gamma_{ij\ell} = \text{rank}(S_{ij\ell})$ . Using 4.2, we can restrict some nodes of  $S_{ij\ell}$  so that  $S_{ij\ell}$  is equivalent to an alternating tree  $T_{\beta_s} + T_{\gamma_{ij\ell}}$ .
5. Let  $\mathcal{F}$  denote the family of all gates  $G$  in some  $D_k$  which are the uppermost gate of a subcircuit with rank at most  $\beta_s$  and whose parents are the uppermost gate of a subcircuit with rank strictly greater than  $\beta_s$ . Extend the subcircuits rooted at each  $G \in \mathcal{F}$  to be  $\Sigma_{\beta_s}$ - or  $\Pi_{\beta_s}$ -circuits.

6. Now apply the inductive hypothesis to the  $\Sigma_{\beta_s}$ - or  $\Pi_{\beta_s}$ -circuits with uppermost gates in  $\mathcal{F}$  and to the subtrees  $T_{\beta_s}$  grouped so the lemma guarantees each node in  $T_{\gamma_{ij\ell}}$  with infinitely many trees  $T_{\beta_s}$  as children has infinitely many of those children preserved. Let  $\rho_s$  denote the restriction so obtained.
7. For each  $(S_{ij\ell})^{\rho_s}$ , apply a further restriction if needed so that we can identify the restricted tree with  $T_{\gamma_{ij\ell}}$ . (This is necessary because a direct descendant of a limit node might be suppressed instead of preserved, and a simple transfinite induction verifies that such a further restriction is possible.)
8. Replace all circuits and trees with their equivalent simplified versions.

We make a few observations about the resulting circuit at the end of each step. First, since each  $(D_s^{\sigma_1 \dots \sigma_s})^{\rho_s}$  depends on only finitely many preserved literals, the circuit

$$\left( \bigvee_{\sigma_1 \dots \sigma_s \in \Sigma^s} \left( D_s^{\sigma_1 \dots \sigma_s} \wedge \bigwedge_{i=1}^s x_i = \sigma_i \right) \right)^{\rho}$$

also depends on only finitely many preserved or permanently preserved literals and hence lies in  $\Sigma_0/\Pi_0$ . Each restricted  $(D_k)^{\rho_s}$  has rank  $\delta_k$ , where  $\delta_k$  is the unique ordinal such that  $\beta_s + \delta_k = \text{rank}(D_k)$ . Similarly, each restricted subtree  $(S_{ij\ell})^{\rho_s}$  has rank  $\gamma_{ij\ell}$  with  $\beta_s + \gamma_{ij\ell} = \text{rank}(S_{ij\ell})$ . Fix  $i, j \in \mathbb{N}$ . Then there exists some  $S_{ij\ell}$  with  $\text{rank}(D_k) < \text{rank}(S_{ij\ell})$ , and thus

$$\beta_s + \delta_k = \text{rank}(D_k) < \sup_{\ell \in \mathbb{N}} (\text{rank}(S_{ij\ell})) = \beta_s + \sup_{\ell \in \mathbb{N}} \gamma_{ij\ell}.$$

This means that  $\delta_k < \sup_{\ell \in \mathbb{N}}$  by right monotonicity, and this shows that the invariant is preserved after each step.

After all stages are complete, we can preserve any remaining subtrees and apply the resulting restriction  $\rho$ . After this application, each  $T_{ij}$  is equivalent to a full rank-1 tree, and each  $C_i$  is equivalent to a  $\Sigma_1$ - or  $\Pi_1$ -circuit. Thus we can apply the same construction as in the inductive step obtain one more restriction which gives us precisely the desired equivalences. This completes the induction in the limit case and proves the theorem. □

There does not seem to be a natural way to extend the class of rank- $\alpha$  circuits to the finite case, but perhaps there is some clever way to make this notion precise. If so, our combinatorial proof of the Borel hierarchy theorem or the ideas within could perhaps be adapted to provide a hierarchy theorem in this setting. The restriction lemma, however, gives us some elegant results, which we explore in the following section.

## 5 The Galvin-Prikry theorem

The Galvin-Prikry theorem is a Ramsey-like result in descriptive set theory which states the following:

**Theorem 5.1** (Galvin-Prikry). *For any Borel function  $f: \mathcal{P}(\mathbb{N}) \rightarrow \{0, 1\}$ , there exists an infinite set  $S \subseteq \mathbb{N}$  such that  $f$  is constant on every infinite subset of  $S$ .*

This theorem immediately implies that no Borel function computes an infinite parity function, since the restriction of such a parity function to an infinite set  $S$  is another infinite parity function.

Given the analogy between countable deterministic circuits and polynomial-sized circuit families, one might naively expect a similar result to hold for the class  $\text{P/poly}$ . However, the fact that  $\text{PARITY} \in \text{P/poly}$  implies that no nontrivial Ramsey-like result can be proven for these circuits. We will instead target the class  $\text{AC}^0$ . First, however, we discuss some similar results about countable circuits which can be obtained immediately from Lemma 4.1.

### 5.1 Consequences of the restriction lemma

The Galvin-Prikry theorem implies the following corollary, which is sufficient for many applications:

**Corollary 5.1.** *For any Borel function  $f: \mathcal{P}(\mathbb{N}) \rightarrow \{0, 1\}$ , there exists an infinite set  $S \subseteq \mathbb{N}$  and set  $R \subseteq \mathbb{N} \setminus S$  such that  $f$  is constant on every set of the form  $X \cup R$  with  $X \subseteq S$ .*

*Proof.* Using 5.1, we obtain  $S' \subseteq \mathbb{N}$  and  $y \in \{0, 1\}$  be such that  $S'$  is infinite and  $f(X) = y$  for all infinite subsets  $X$  of  $S'$ . Partition  $S'$  into two disjoint infinite sets  $S$  and  $R$ . Then  $S$  is infinite and  $f(X \cup R) = y$  for any  $X \subseteq S$ , as desired. □

The standard proof of the Galvin-Prikry theorem relies on a topological argument ([5]), but we can instead rephrase the corollary in terms of circuits and prove the result using the restriction lemma (4.1). This gives us a purely combinatorial proof of this fact:

**Corollary 5.2.** *For any countable, well-founded, deterministic circuit  $C$  defined on infinitely many variables, there exists a restriction  $\rho$  preserving infinitely many variables such that  $C^\rho$  is constant.*

*Proof.* Partition the variables  $x_1, x_2, \dots$  of  $C$  into countably many countably infinite sets  $S_1, S_2, \dots$ . Create countably many full rank- $\alpha$  alternating trees  $T_i$  with leaves  $S_i$ . Then the restriction lemma gives us a restriction  $\rho'$  such that  $C^{\rho'}$  depends on only finitely many variables and infinitely many trees are preserved. This implies that  $\rho'$  preserves infinitely

many variables. By extending  $\rho'$  to assign 0 or 1 to each of the finitely many variables  $C^{\rho'}$  depends on, we obtain a new restriction  $\rho'$  satisfying the conditions of the corollary.

□

**Corollary 5.3.** *No countable, well-founded, deterministic circuit  $C$  can compute an infinite parity function  $f$  (whose output flips when any input bit is flipped).*

*Proof.* Suppose for the sake of contradiction such a circuit  $C$  computes  $f$ . Then the previous corollary gives us a restriction  $\rho$  such that  $C^\rho$  computes  $f^\rho$ . This is impossible, since  $C^\rho$  is constant and  $f^\rho$  is another infinite parity function.

□

The above proof, unlike that presented in [2], does not rely on any external machinery from descriptive set theory. Furthermore, both the Ramsey-like result and the corollary about PARITY follow similar approaches to the finite case, where analogous results are proven using Håstad's switching lemma ([3], [1]). This approach in the infinite case therefore seems to be the most “compatible” with the finite case.

## 5.2 Current work

We are currently trying to prove a finite version of the Galvin-Prikry theorem, which would give us an easy method to prove that certain problems lie outside of this class.

## 6 The Lusin separation theorem

In [7], Michael Sipser provides a purely combinatorial proof of the foundational result from descriptive set theory that analytic sets are not closed under complement. Sipser observes that an analogous proof of this fact for polynomial-sized circuits would show that  $\text{NP/poly} \neq \text{coNP/poly}$  and thus  $\text{P} \neq \text{NP}$ . Sipser’s proof does not extend to the polynomial case, and he acknowledges that this approach seems unlikely to succeed.

We investigate a different foundational result, namely the Lusin separation theorem:

**Theorem 6.1** (Lusin separation). *For any two disjoint analytic sets  $A, C \subseteq \Sigma^\omega$ , there exists a Borel set  $B \subseteq \Sigma^\omega$  such that  $A \subseteq B$  and  $B \cap C = \emptyset$ .*

If we take  $C$  to be  $A^c$  in the above theorem, we see that any analytic set  $A$  whose complement is also analytic must actually be a Borel set. In other words, if a set and its complement can both be computed by countable nondeterministic circuits, then the set can be computed by a countable deterministic circuit. The polynomial analogue of this theorem is the claim that  $\text{P/poly} = \text{NP/poly} \cap \text{coNP/poly}$ .

## 6.1 Current work

There are constructive proofs of the Lusin separation theorem, and applying these proofs directly to the polynomial case gives us a circuit family that grows exponentially. However, we are searching for ways to control the “separation tree” ([5]) used in the construction to find polynomial-sized circuits for a suitable subclass of  $\text{NP/poly} \cap \text{coNP/poly}$ .

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