Signal Tap

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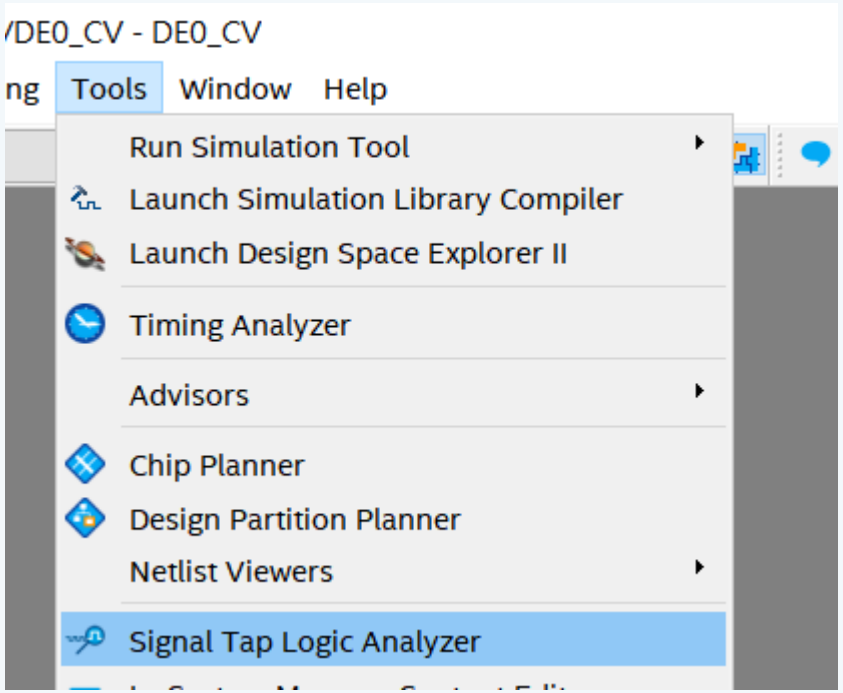
Signal Tap

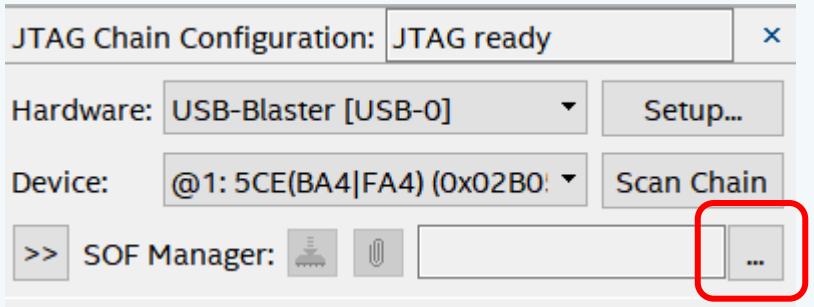
- Signal Tap是嵌入在FPGA裡的邏輯分析儀
- 透過JTAG connector即時擷取與顯示FPGA內部訊號狀態，並且可以設定多種觸發條件

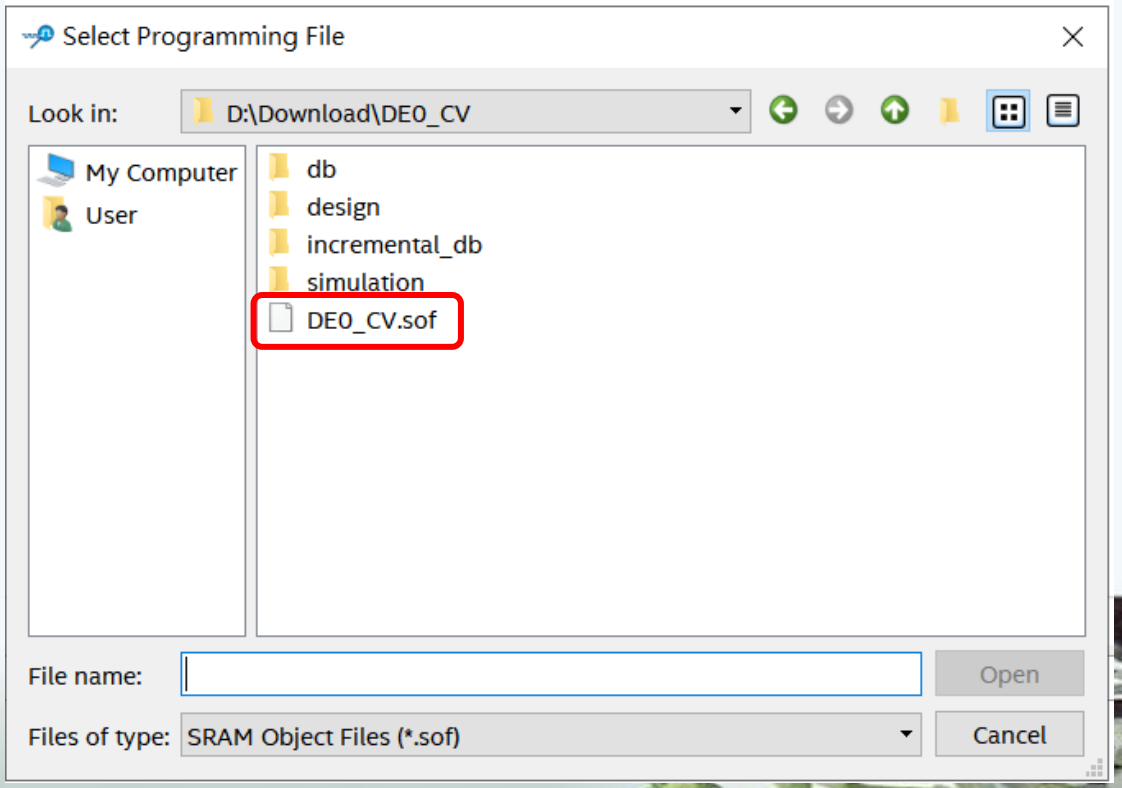
開啟Signal Tap

- Compile design
- Tools -> Signal Tap Logic Analyzer



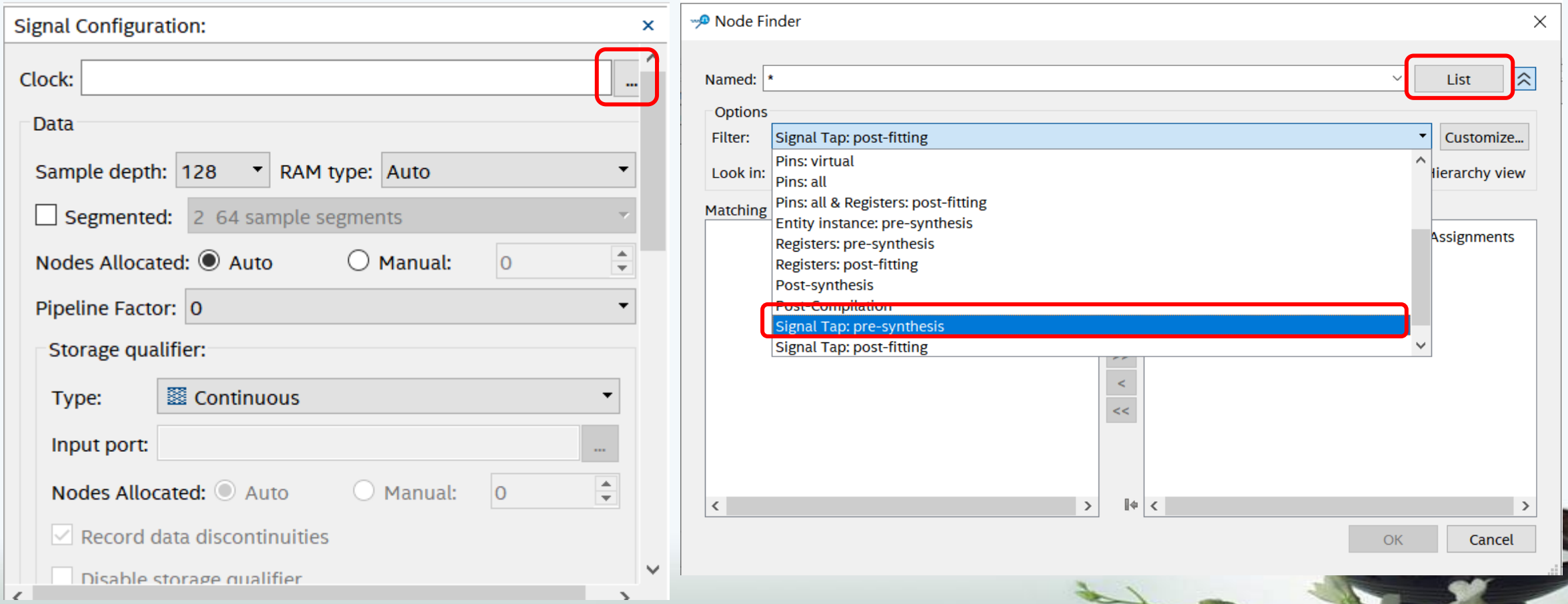
- 選取燒錄檔(.sof)


JTAG Chain Configuration:
JTAG ready
Hardware:
USB-Blaster [USB-0]
Setup...
Device:
@1: 5CE(BA4|FA4) (0x02B0
Scan Chain
>>
SOF Manager:
...


Select Programming File
Look in:
D:\Download\DE0_CV
My Computer
User
db
design
incremental_db
simulation
DE0_CV.sof
File name:
Open
Files of type:
SRAM Object Files (*.sof)
Cancel

訊號設定

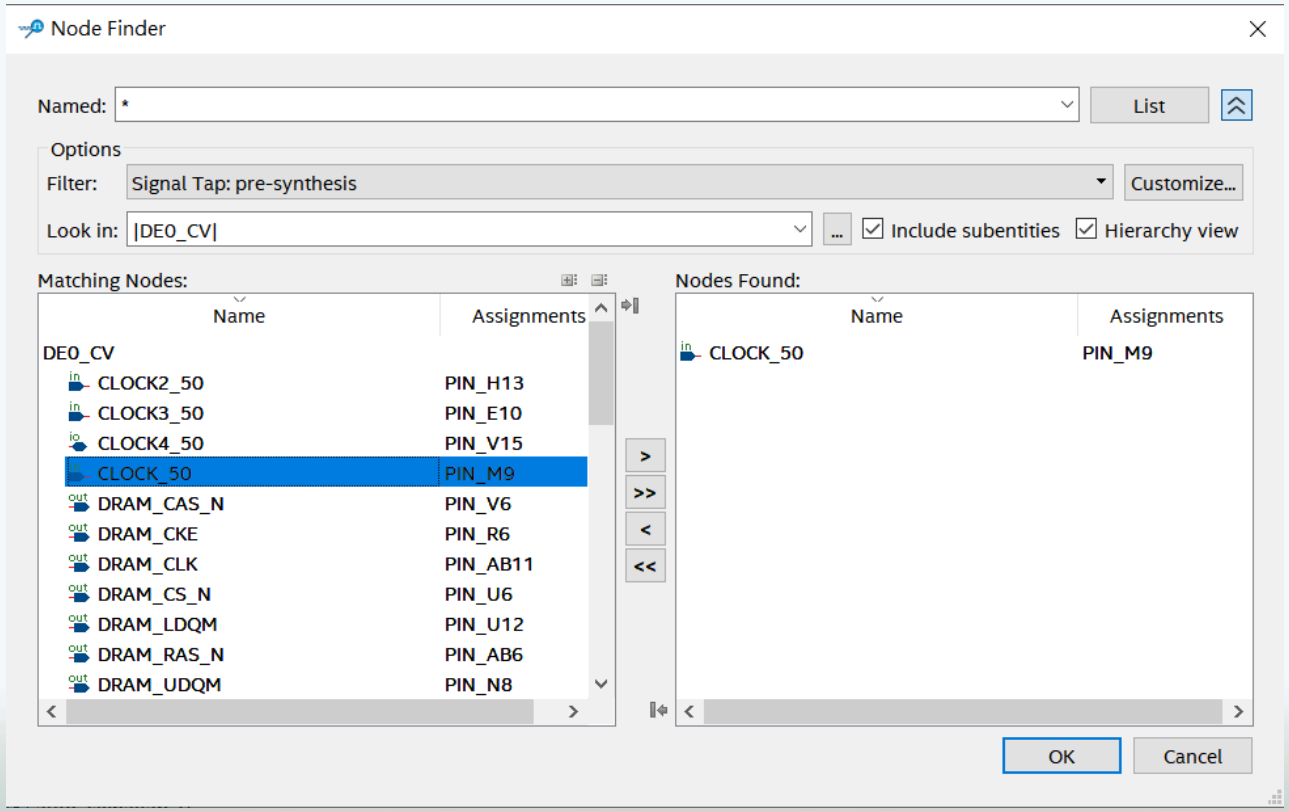
Signal Tap:pre-synthesis -> List

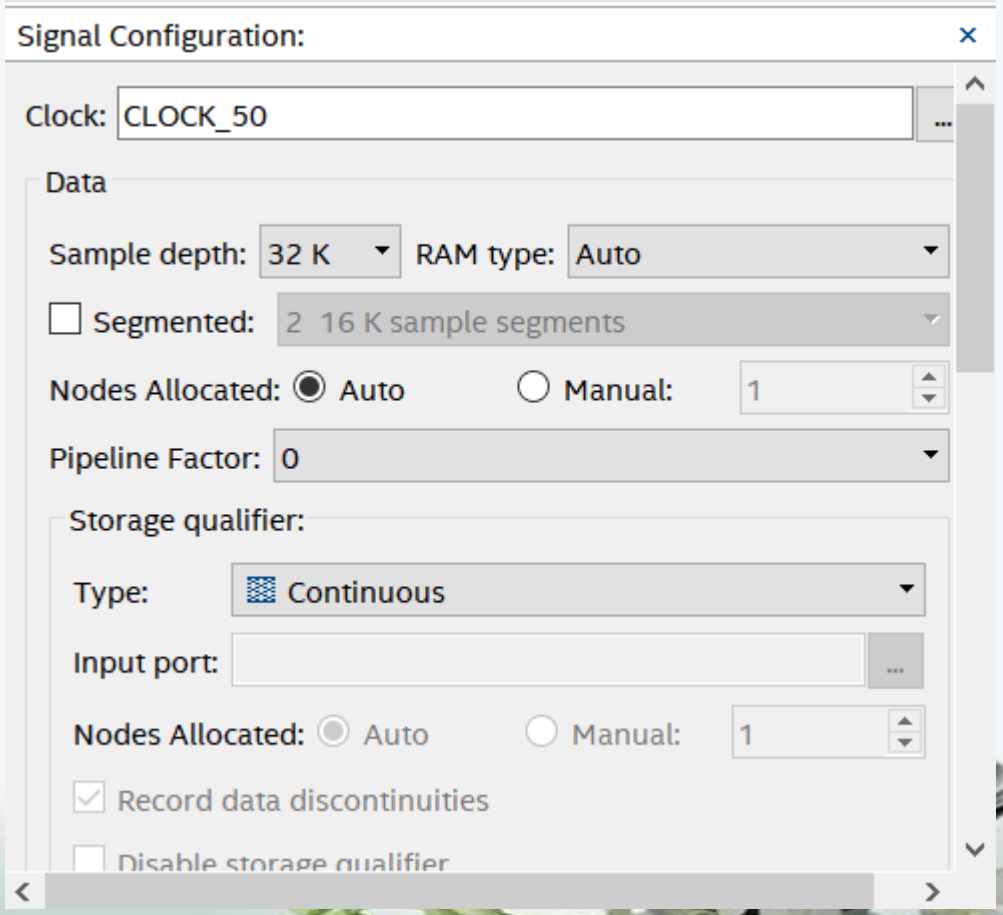


訊號設定

- 設定clk(clk正緣觸發時擷取訊號)
- 設定深度(32K次)

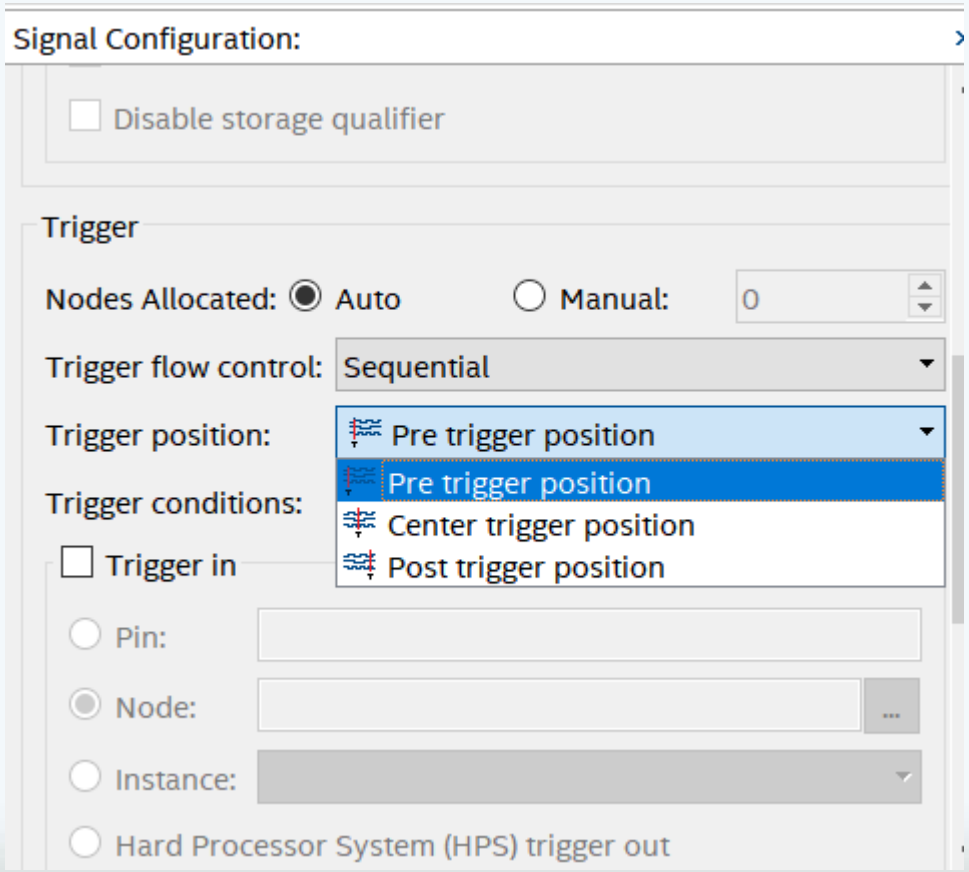
擷取頻率一定要大於觀察訊號的頻率





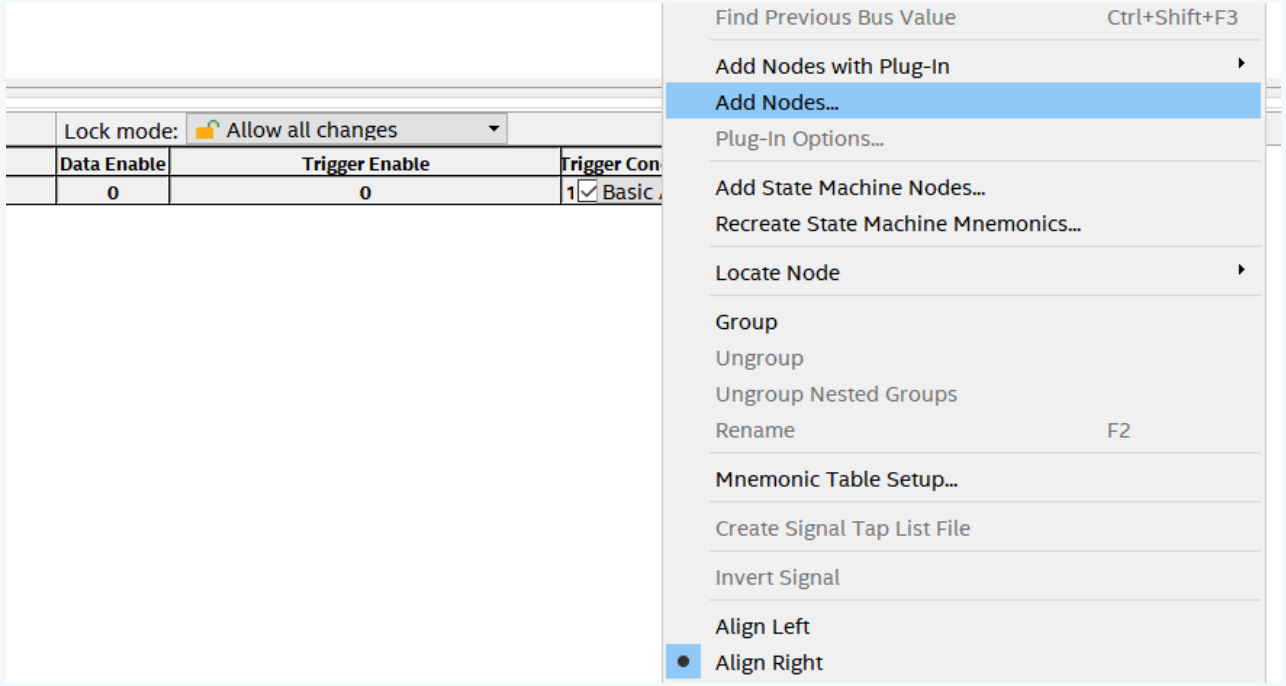
訊號設定

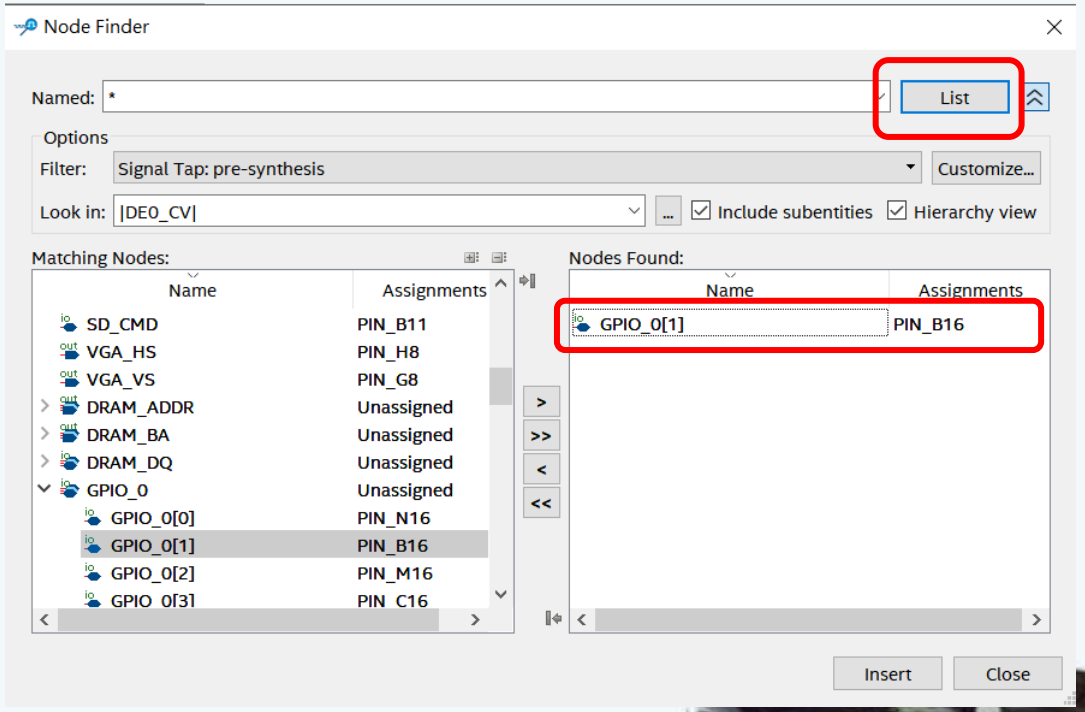
- 設定trigger位置



訊號設定

- 右鍵->add nodes 加入要觀看的信號跟觸發信號



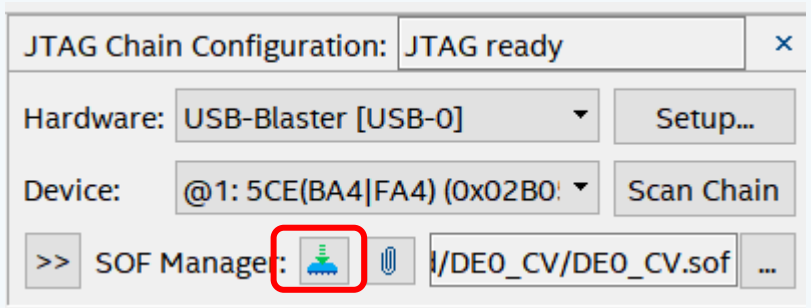


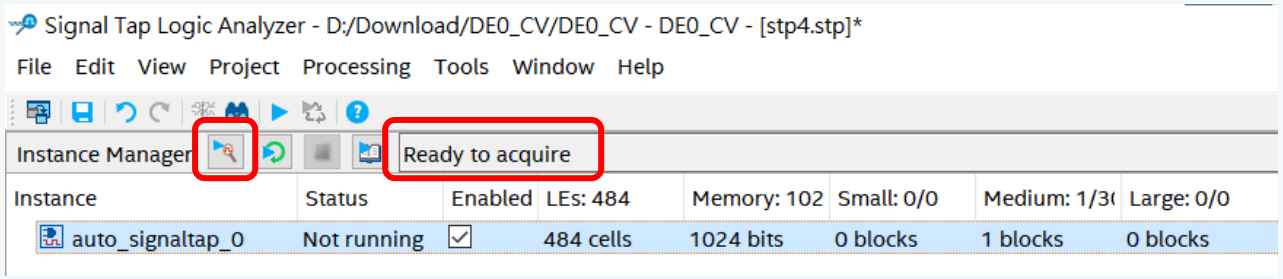
訊號設定

- 設定trigger觸發的條件(falling edge)

Node			Data Enable	Trigger Enable	Trigger Conditions
Type	Alias	Name	1	1	1 Basic AN
		GPIO_0[1]	☑	☑	↘

- 燒入sof檔
- 就緒後開始執行



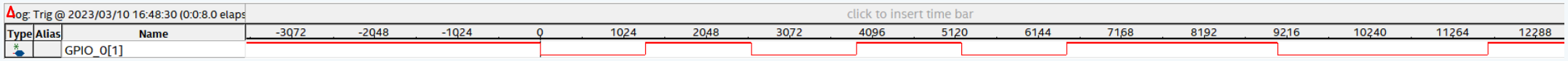


結果

- 測資為16進制35(RS-232, Baud Rate = 38400)

HEX	35
DEC	53
OCT	65
BIN	0011 0101

傳送順序



start bit

stop bit