PLL鎖相迴路實作

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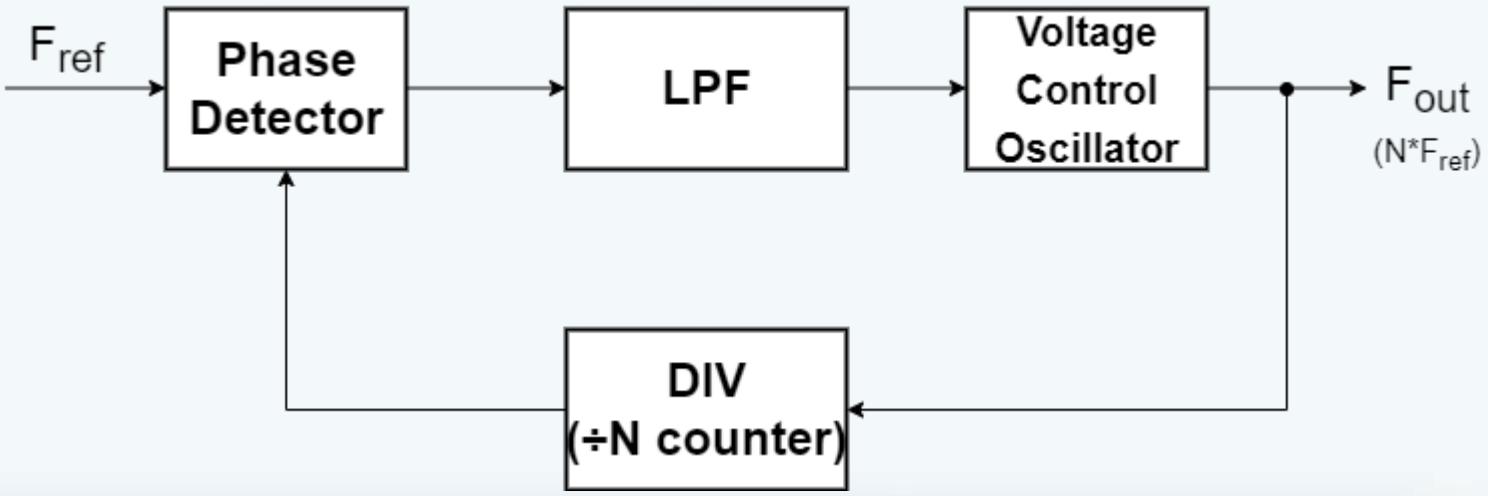
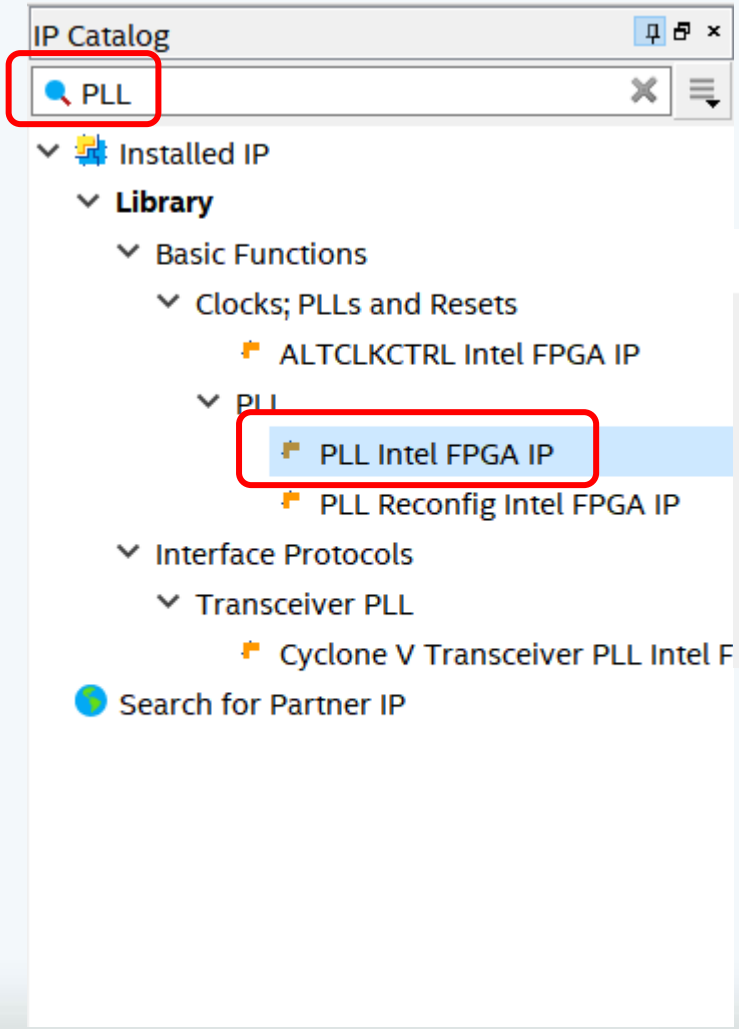
PLL鎖相迴路

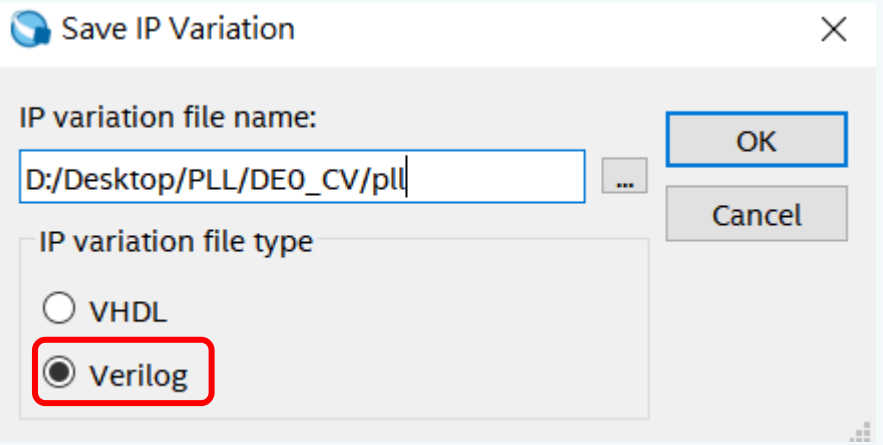
- 一個設計用於同步板子時脈與外部的時脈訊號的電路。



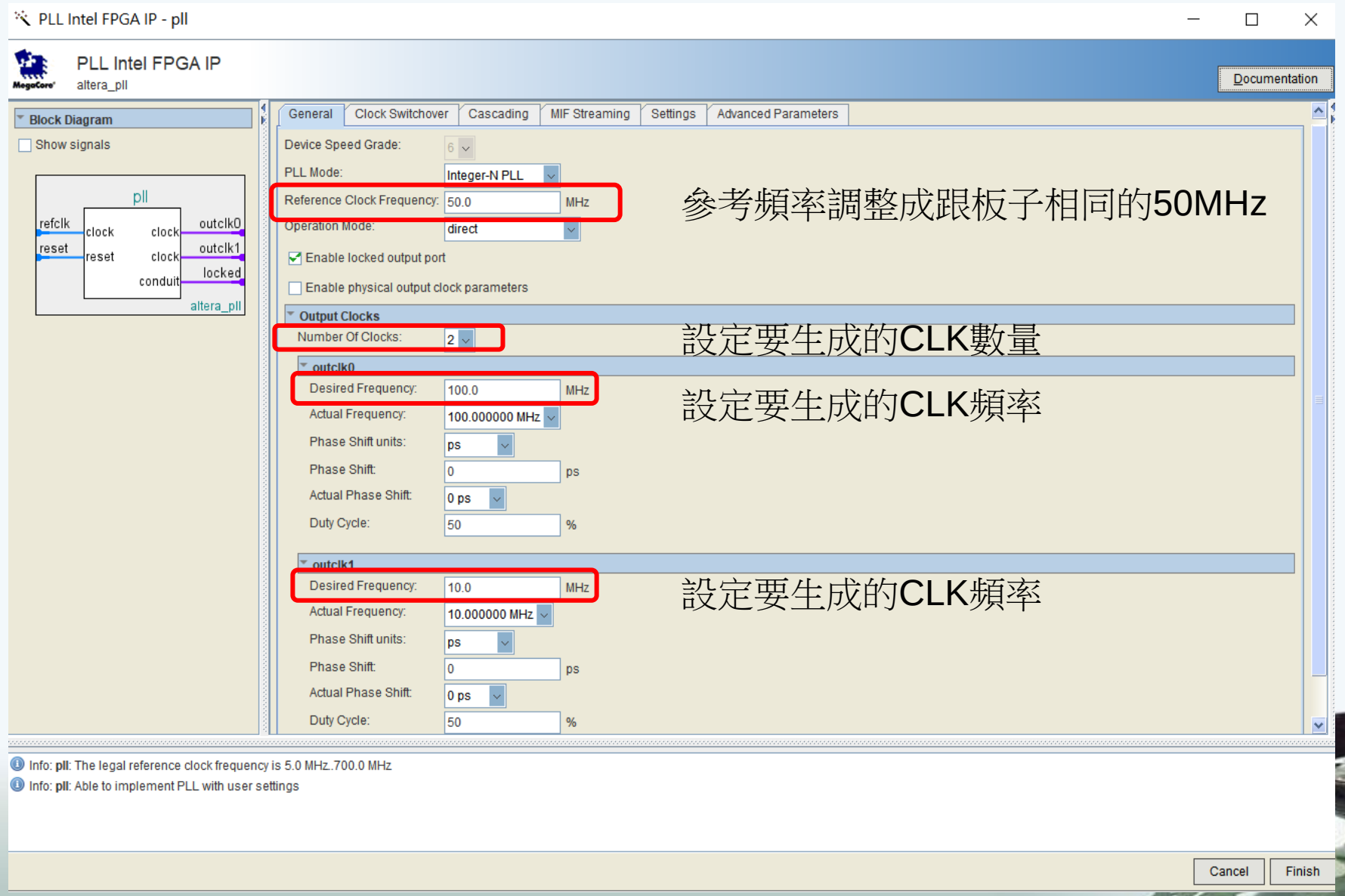
PLL實作

- 在IP Catalog搜尋PLL
- 開啟後選擇檔案類型並取名存檔





PLL實作



參考頻率調整成跟板子相同的50MHz

設定要生成的CLK數量

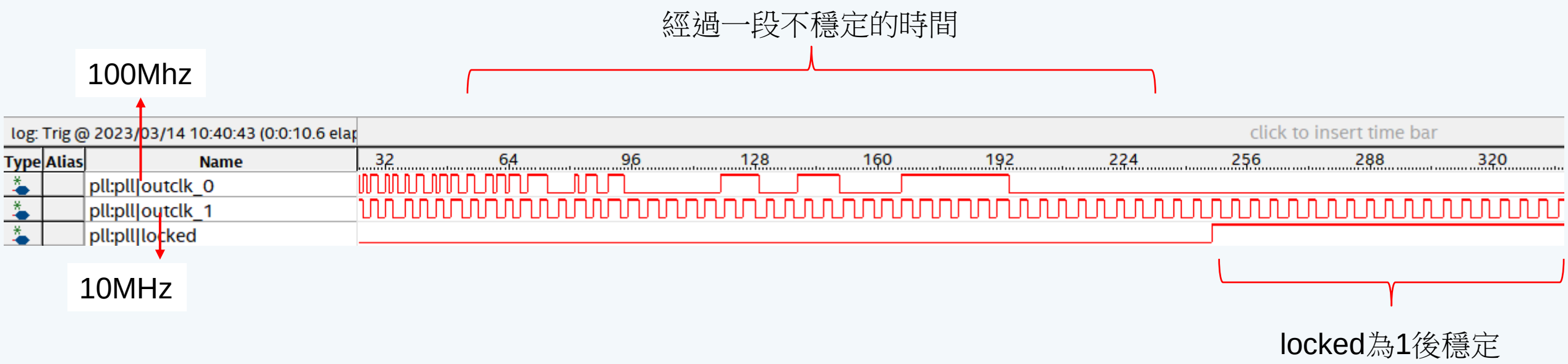
設定要生成的CLK頻率

設定要生成的CLK頻率

結果

- 以Signal Tap觀察:

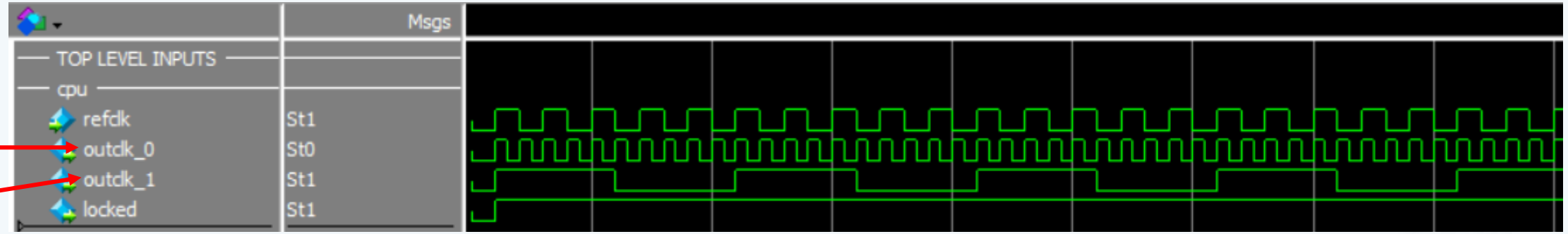
```
pll pll (
        .refclk(CLOCK_50),    //  refclk.clk
        .rst(KEY[0]),         //    reset.reset
        .outclk_0(), // outclk0.clk
        .outclk_1(), // outclk1.clk
        .locked()     //  locked.export
    );
```



結果

- **以modelsim模擬:**
  - 模擬IP時要在sim.do加入會用到的library

vsim -t 1ps -L altera_ver -L lpm_ver -L sgate_ver -L altera_mf_ver -L altera_lnsim_ver -L cyclonev_ver -L cyclonev_hssi_ver -L cyclonev_pcie_hip_ver -L rtl_work -L work -voptargs="+acc" testbench



Lock為1以後才穩定，只取用lock==1之後的訊號