

Signal Tap

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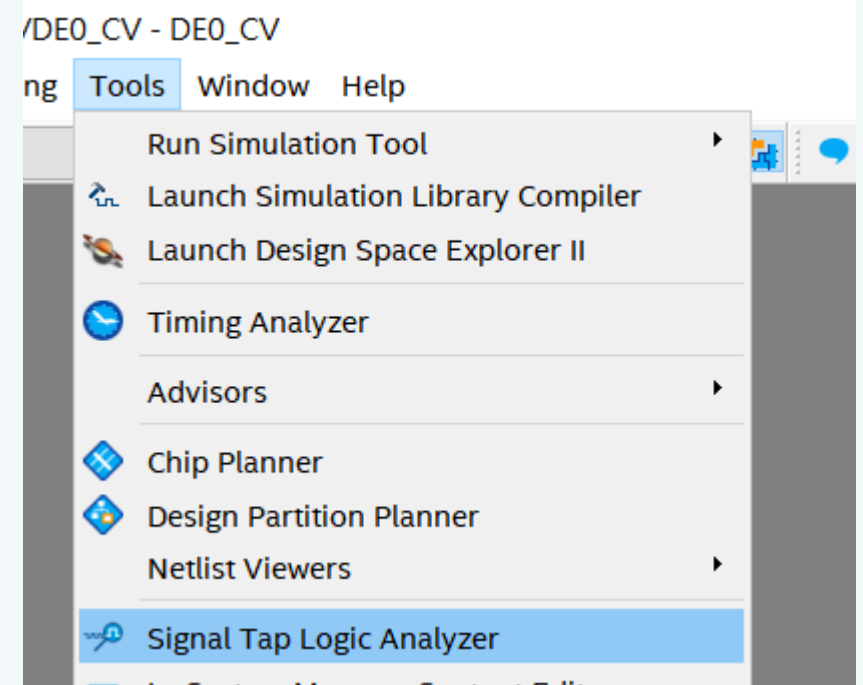
Signal Tap

- Signal Tap是嵌入在FPGA裡的邏輯分析儀
- 透過JTAG connector即時擷取與顯示FPGA內部訊號狀態，並且可以設定多種觸發條件

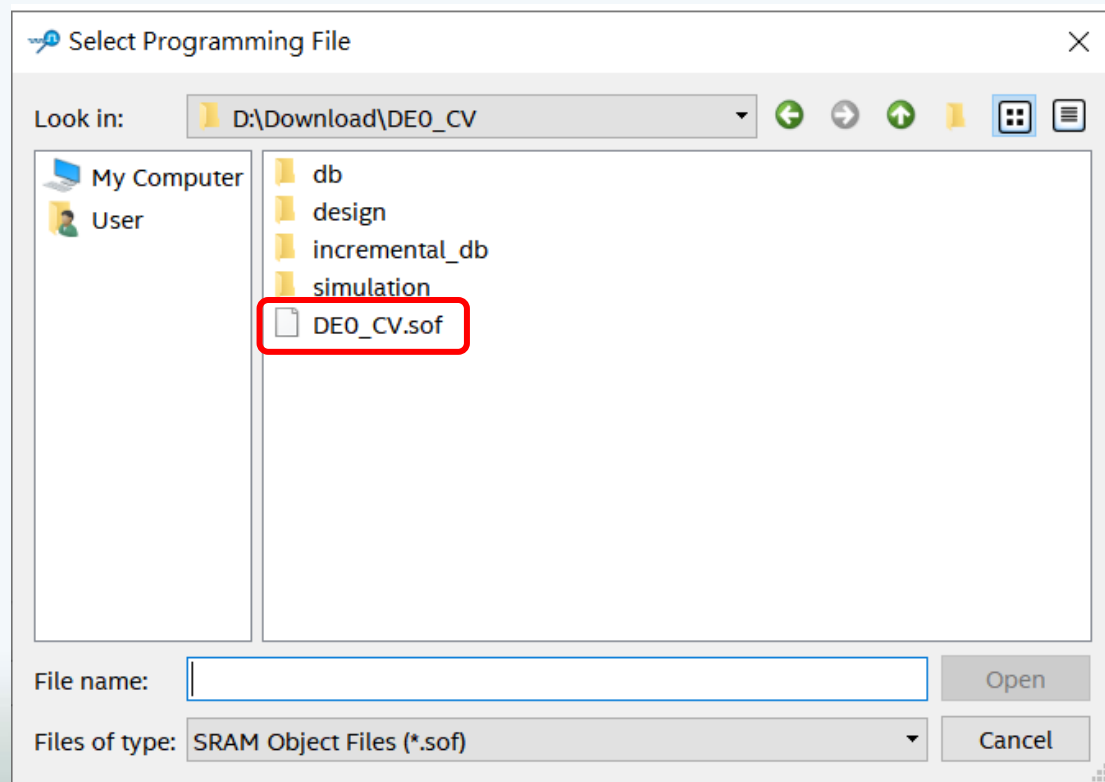
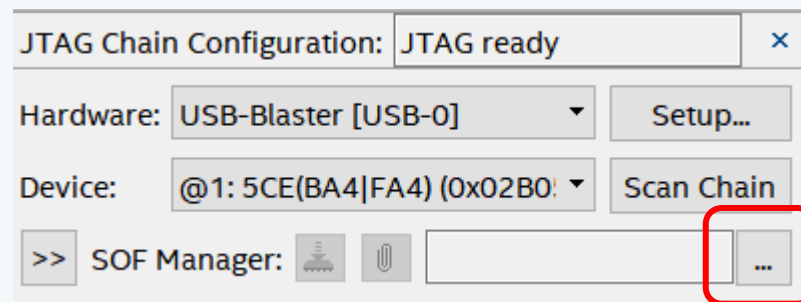


開啟Signal Tap

- Compile design
- Tools -> Signal Tap Logic Analyzer



- 選取燒錄檔(.sof)



訊號設定

Signal Tap:pre-synthesis -> List

Signal Configuration: ✕

Clock: ...

Data

Sample depth: 128 RAM type: Auto

☐ Segmented: 2 64 sample segments

Nodes Allocated: ☒ Auto ☐ Manual: 0

Pipeline Factor: 0

Storage qualifier:

Type: Continuous

Input port: ...

Nodes Allocated: ☒ Auto ☐ Manual: 0

☒ Record data discontinuities

☐ Disable storage qualifier

Node Finder ✕

Named: * List

Options

Filter: Signal Tap: post-fitting Customize...

Look in: Pins: virtual
Pins: all
Pins: all & Registers: post-fitting

Matching

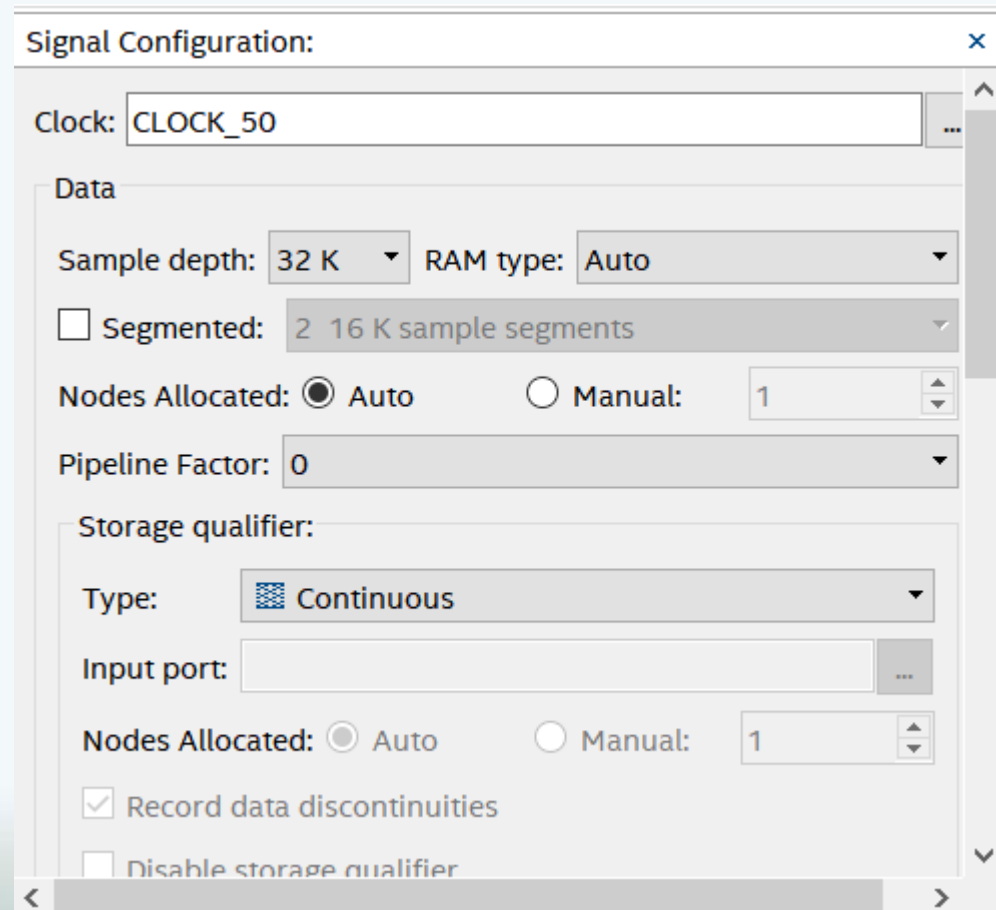
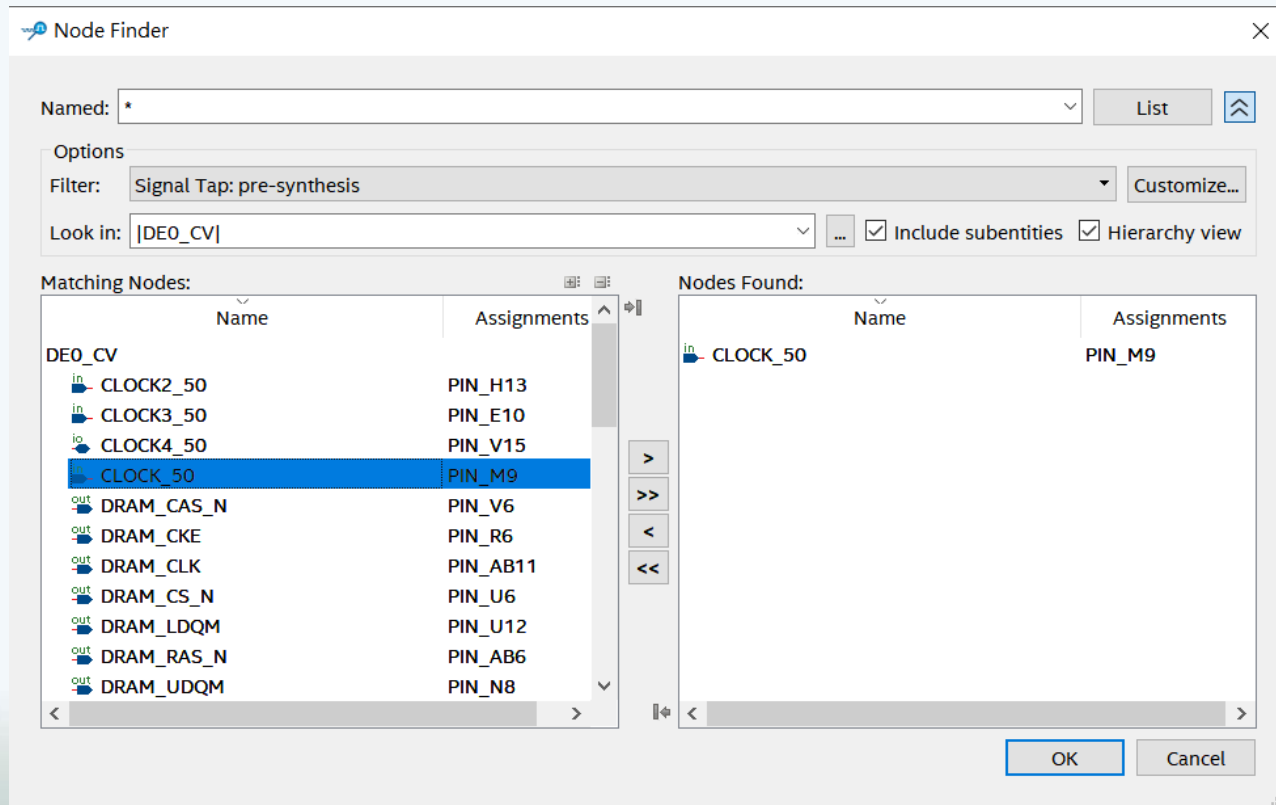
Entity instance: pre-synthesis
Registers: pre-synthesis
Registers: post-fitting
Post-synthesis
Post-Compilation
Signal Tap: pre-synthesis
Signal Tap: post-fitting

OK Cancel

訊號設定

- 設定clk(clk正緣觸發時擷取訊號)
- 設定深度(32K次)

擷取頻率一定要大於觀察訊號的頻率



訊號設定

- 設定trigger位置

Signal Configuration:

☐ Disable storage qualifier

Trigger

Nodes Allocated: ☒ Auto ☐ Manual:

Trigger flow control: Sequential

Trigger position: Pre trigger position

Trigger conditions:

☐ Trigger in

☐ Pin:

☒ Node:

☐ Instance:

☐ Hard Processor System (HPS) trigger out

Pre trigger position

Pre trigger position

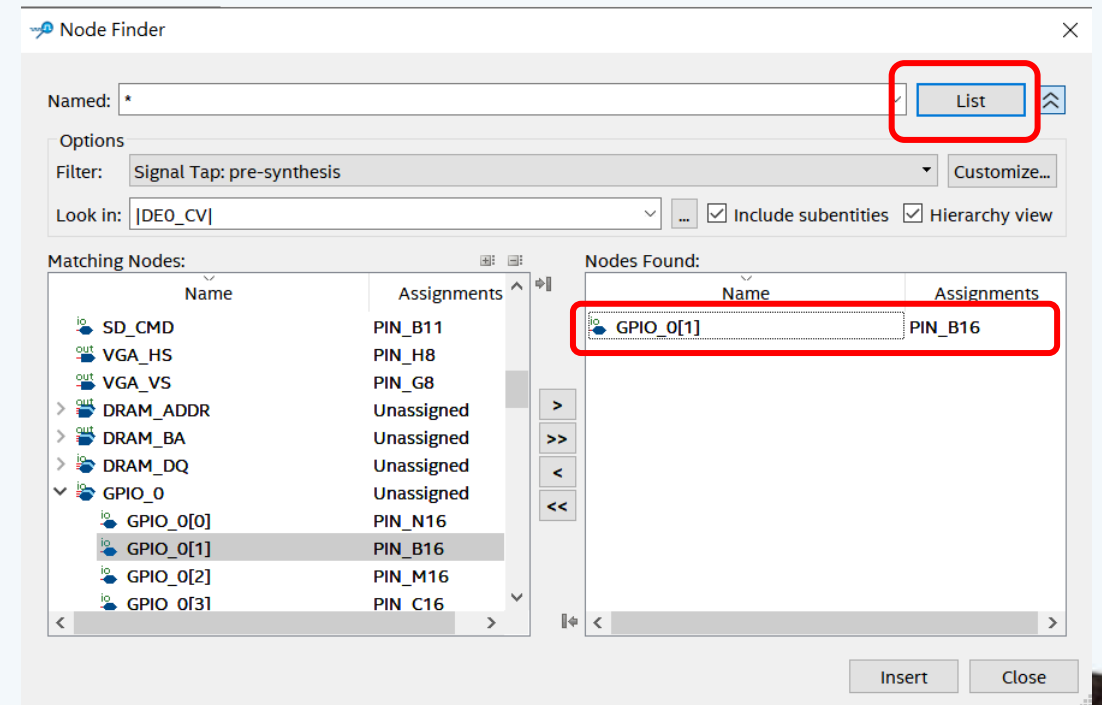
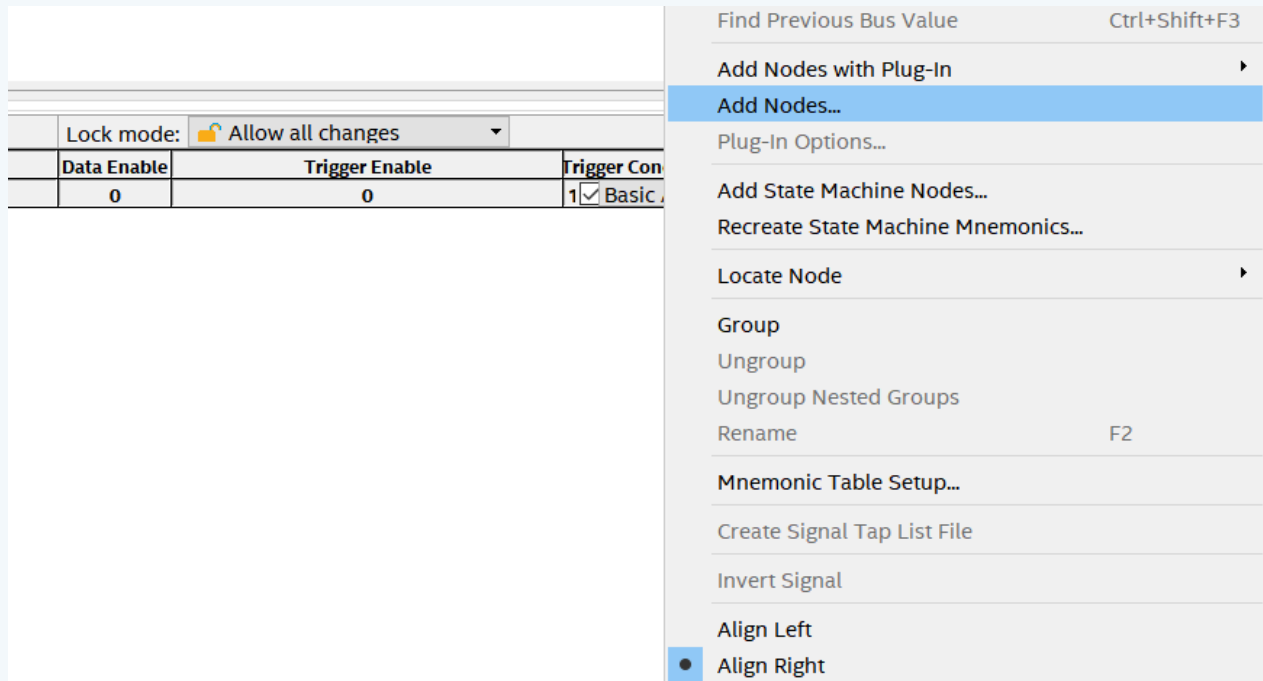
Center trigger position

Post trigger position





訊號設定

- 右鍵->add nodes 加入要觀看的信號跟觸發信號



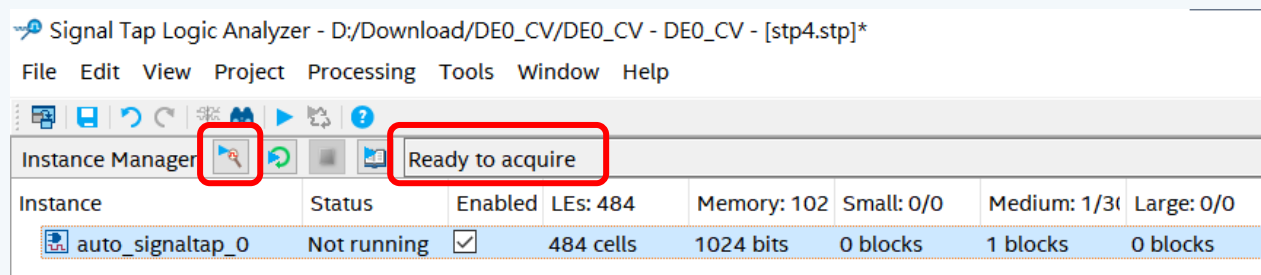
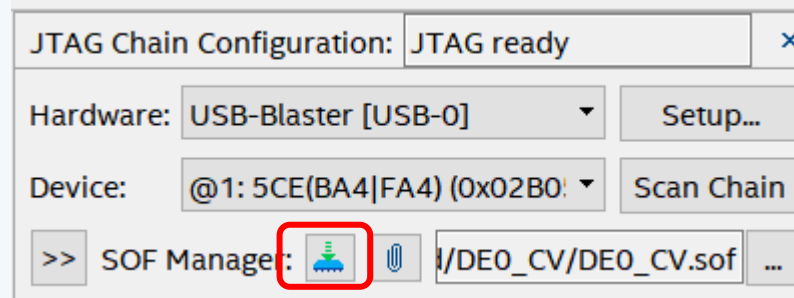
訊號設定

- 設定trigger觸發的條件(falling edge)

| Node | | | Data Enable | Trigger Enable | Trigger Conditions |
|---|-------|-----------|-------------------------------------|-------------------------------------|---|
| Type | Alias | Name | 1 | 1 | 1 <input checked="" type="checkbox"/> Basic AN ▾ |
|  | | GPIO_0[1] | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> |  |



- 燒入sof檔
- 就緒後開始執行

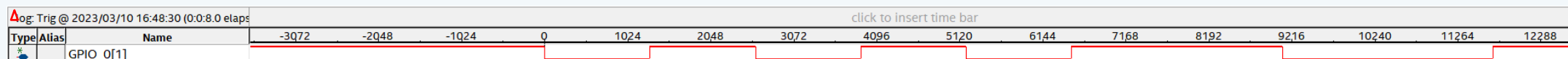


結果

- 測資為16進制35(RS-232, Baud Rate = 38400)

| | |
|-----|-----------|
| HEX | 35 |
| DEC | 53 |
| OCT | 65 |
| BIN | 0011 0101 |

← 傳送順序



↑
start bit

↑
stop bit

