

PLL鎖相迴路實作

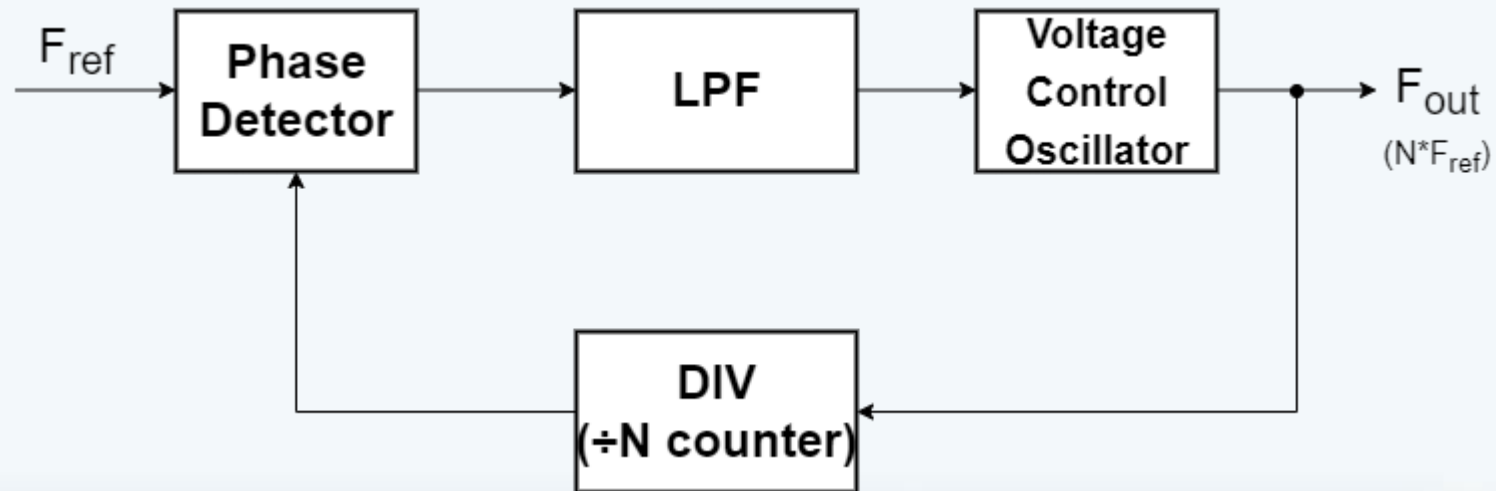
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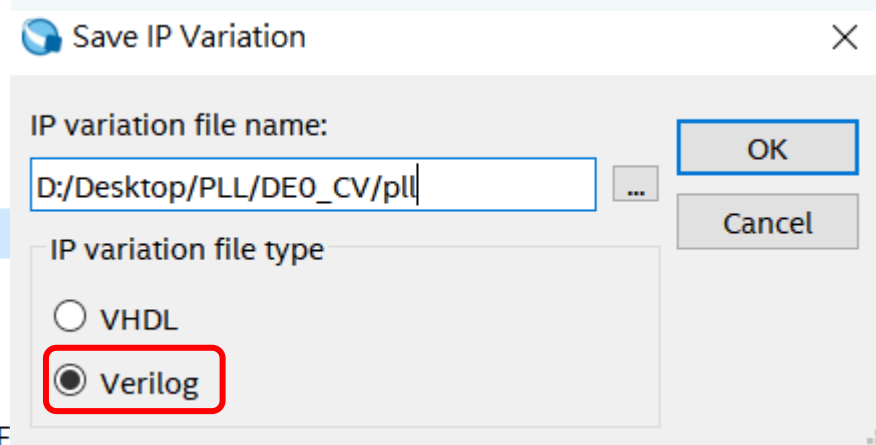
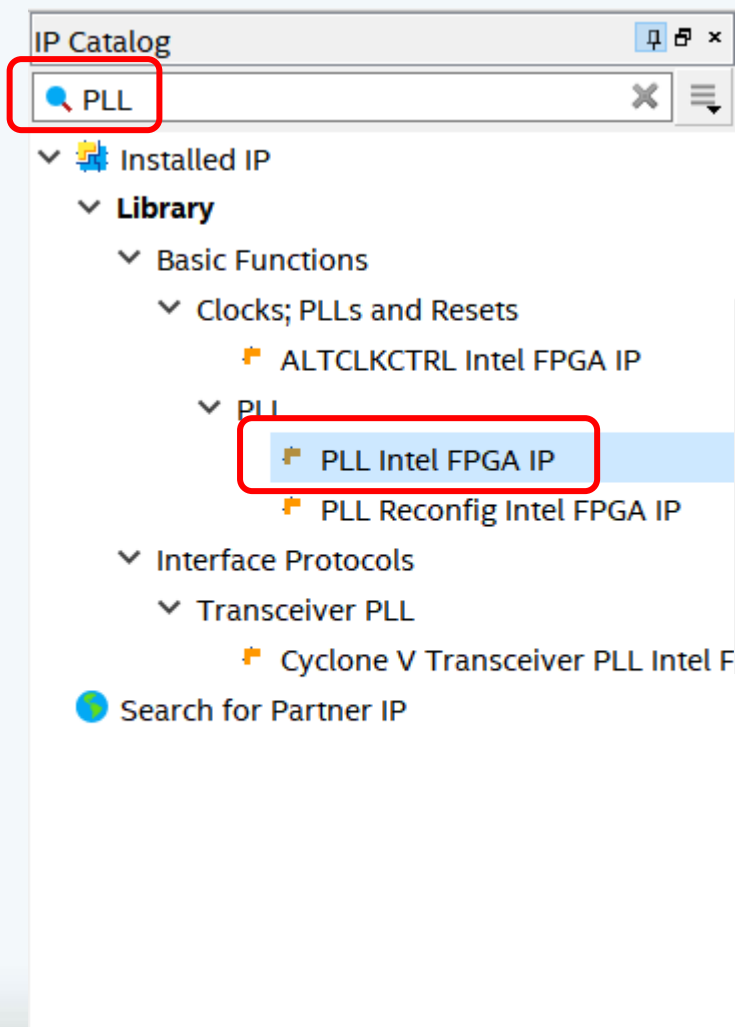
PLL鎖相迴路

- 一個設計用於同步板子時脈與外部的時脈訊號的電路。



PLL實作

- 在IP Catalog搜尋PLL
- 開啟後選擇檔案類型
並取名存檔



PLL實作

PLL Intel FPGA IP - pll

PLL Intel FPGA IP
altera_pll

Documentation

Block Diagram

Show signals

pll

refclk clock clock outclk0
reset reset clock outclk1
conduit locked
altera_pll

General Clock Switchover Cascading MIF Streaming Settings Advanced Parameters

Device Speed Grade: 6

PLL Mode: Integer-N PLL

Reference Clock Frequency: 50.0 MHz

Operation Mode: direct

☒ Enable locked output port

☐ Enable physical output clock parameters

Output Clocks

Number Of Clocks: 2

outclk0

Desired Frequency: 100.0 MHz

Actual Frequency: 100.000000 MHz

Phase Shift units: ps

Phase Shift: 0 ps

Actual Phase Shift: 0 ps

Duty Cycle: 50 %

outclk1

Desired Frequency: 10.0 MHz

Actual Frequency: 10.000000 MHz

Phase Shift units: ps

Phase Shift: 0 ps

Actual Phase Shift: 0 ps

Duty Cycle: 50 %

Info: pll: The legal reference clock frequency is 5.0 MHz..700.0 MHz

Info: pll: Able to implement PLL with user settings

Cancel Finish

參考頻率調整成跟板子相同的50MHz

設定要生成的CLK數量

設定要生成的CLK頻率

設定要生成的CLK頻率

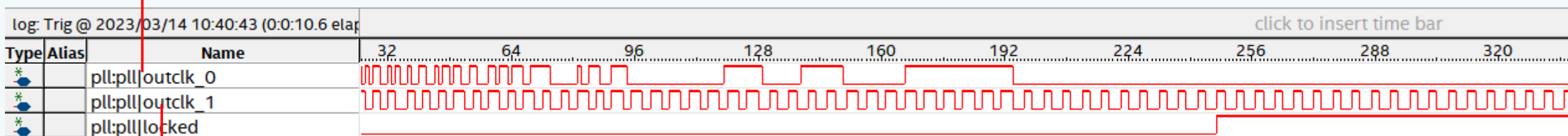
結果

- 以Signal Tap觀察：

```
2  p11 p11 (  
3      .refclk(CLOCK_50), // refclk.clk  
4      .rst(KEY[0]),      // reset.reset  
5      .outclk_0(),        // outclk0.clk  
6      .outclk_1(),        // outclk1.clk  
7      .locked()           // locked.export  
8  );  
9
```

經過一段不穩定的時間

100Mhz



10MHz

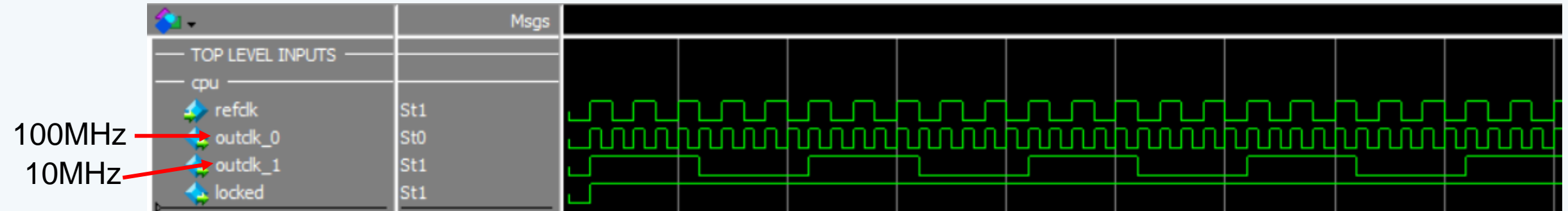
locked為1後穩定



結果

- 以modelsim模擬：
 - 模擬IP時要在sim.do加入會用到的library

```
vsim -t 1ps -L altera_ver -L lpm_ver -L sgate_ver -L  
altera_mf_ver -L altera_insim_ver -L cyclonev_ver -L  
cyclonev_hssi_ver -L cyclonev_pcie_hip_ver -L  
rtl_work -L work -voptargs="+acc" testbench
```



Lock為1以後才穩定，只取用lock==1之後的訊號

