Configuration-Bit Settings for PIC32MX250F128B

(Data Sheet # DS-60001168)

Usage:
#pragma config *SETTING = VALUE*

USERID	
USERID = 00000000	Range is from 0 to 0xffff

PMDL1WAY	Peripheral Module Disable Configuration
PMDL1WAY = ON	Allow only one reconfiguration
PMDL1WAY = OFF	Allow multiple reconfigurations

IOL1WAY	Peripheral Pin Select Configuration
IOL1WAY = ON	Allow only one reconfiguration
IOL1WAY = OFF	Allow multiple reconfigurations

FUSBIDIO	USB USID Selection
FUSBIDIO = OFF	Controlled by Port Function
FUSBIDIO = ON	Controlled by the USB Module

FVBUSONIO	USB VBUS ON Selection
FVBUSONIO = OFF	Controlled by Port Function
FVBUSONIO = ON	Controlled by USB Module

FPLLIDIV	PLL Input Divider
FPLLIDIV = DIV_1	1x Divider
FPLLIDIV = DIV_2	2x Divider
FPLLIDIV = DIV_3	3x Divider
FPLLIDIV = DIV_4	4x Divider
FPLLIDIV = DIV_5	5x Divider
FPLLIDIV = DIV_6	6x Divider
FPLLIDIV = DIV_10	10x Divider
FPLLIDIV = DIV_12	12x Divider

FPLLMUL	PLL Multiplier

FPLLMUL = MUL_15	15x Multiplier
FPLLMUL = MUL_16	16x Multiplier
FPLLMUL = MUL_17	17x Multiplier
FPLLMUL = MUL_18	18x Multiplier
FPLLMUL = MUL_19	19x Multiplier
FPLLMUL = MUL_20	20x Multiplier
FPLLMUL = MUL_21	21x Multiplier
FPLLMUL = MUL_24	24x Multiplier

UPLLIDIV	USB PLL Input Divider
UPLLIDIV = DIV_1	1x Divider
UPLLIDIV = DIV_2	2x Divider
UPLLIDIV = DIV_3	3x Divider
UPLLIDIV = DIV_4	4x Divider
UPLLIDIV = DIV_5	5x Divider
UPLLIDIV = DIV_6	6x Divider
UPLLIDIV = DIV_10	10x Divider
UPLLIDIV = DIV_12	12x Divider

UPLLEN	USB PLL Enable
UPLLEN = ON	Enabled
UPLLEN = OFF	Disabled and Bypassed

FPLLODIV	System PLL Output Clock Divider
FPLLODIV = DIV_1	PLL Divide by 1
FPLLODIV = DIV_2	PLL Divide by 2
FPLLODIV = DIV_4	PLL Divide by 4
FPLLODIV = DIV_8	PLL Divide by 8
FPLLODIV = DIV_16	PLL Divide by 16
FPLLODIV = DIV_32	PLL Divide by 32
FPLLODIV = DIV_64	PLL Divide by 64
FPLLODIV = DIV_256	PLL Divide by 256

FNOSC	Oscillator Selection Bits
FNOSC = FRC	Fast RC Osc (FRC)
FNOSC = FRCPLL	Fast RC Osc with PLL
FNOSC = PRI	Primary Osc (XT,HS,EC)
FNOSC = PRIPLL	Primary Osc w/PLL (XT+,HS+,EC+PLL)
FNOSC = SOSC	Low Power Secondary Osc (SOSC)

FNOSC = LPRC	Low Power RC Osc (LPRC)
FNOSC = FRCDIV16	Fast RC Osc w/Div-by-16 (FRC/16)
FNOSC = FRCDIV	Fast RC Osc w/Div-by-N (FRCDIV)

FSOSCEN	Secondary Oscillator Enable
FSOSCEN = OFF	Disabled
FSOSCEN = ON	Enabled

IESO	Internal/External Switch Over
IESO = OFF	Disabled
IESO = ON	Enabled

POSCMOD	Primary Oscillator Configuration
POSCMOD = EC	External clock mode
POSCMOD = XT	XT osc mode
POSCMOD = HS	HS osc mode
POSCMOD = OFF	Primary osc disabled

OSCIOFNC	CLKO Output Signal Active on the OSCO Pin
OSCIOFNC = OFF	Disabled
OSCIOFNC = ON	Enabled

FPBDIV	Peripheral Clock Divisor
FPBDIV = DIV_1	Pb_Clk is Sys_Clk/1
FPBDIV = DIV_2	Pb_Clk is Sys_Clk/2
FPBDIV = DIV_4	Pb_Clk is Sys_Clk/4
FPBDIV = DIV_8	Pb_Clk is Sys_Clk/8

FCKSM	Clock Switching and Monitor Selection
FCKSM = CSECME	Clock Switch Enable, FSCM Enabled
FCKSM = CSECMD	Clock Switch Enable, FSCM Disabled
FCKSM = CSDCMD	Clock Switch Disable, FSCM Disabled

WDTPS	Watchdog Timer Postscaler
WDTPS = PS1	1:1
WDTPS = PS2	1:2
WDTPS = PS4	1:4
WDTPS = PS8	1:8
WDTPS = PS16	1:16
WDTPS = PS32	1:32
WDTPS = PS64	1:64

WDTPS = PS128	1:128
WDTPS = PS256	1:256
WDTPS = PS512	1:512
WDTPS = PS1024	1:1024
WDTPS = PS2048	1:2048
WDTPS = PS4096	1:4096
WDTPS = PS8192	1:8192
WDTPS = PS16384	1:16384
WDTPS = PS32768	1:32768
WDTPS = PS65536	1:65536
WDTPS = PS131072	1:131072
WDTPS = PS262144	1:262144
WDTPS = PS524288	1:524288
WDTPS = PS1048576	1:1048576

WINDIS	Watchdog Timer Window Enable
WINDIS = ON	Watchdog Timer is in Window Mode
WINDIS = OFF	Watchdog Timer is in Non-Window Mode

FWDTEN	Watchdog Timer Enable
FWDTEN = OFF	WDT Disabled (SWDTEN Bit Controls)
FWDTEN = ON	WDT Enabled

FWDTWINSZ	Watchdog Timer Window Size
FWDTWINSZ = WINSZ_75	Window Size is 75%
FWDTWINSZ = WINSZ_50	Window Size is 50%
FWDTWINSZ = WINSZ_37	Window Size is 37.5%
FWDTWINSZ = WINSZ_25	Window Size is 25%

DEBUG	Background Debugger Enable
DEBUG = ON	Debugger is Enabled
DEBUG = OFF	Debugger is Disabled

JTAGEN	JTAG Enable
JTAGEN = ON	JTAG Port Enabled
JTAGEN = OFF	JTAG Disabled

ICESEL	ICE/ICD Comm Channel Select
ICESEL = ICS_PGx1	Communicate on PGEC1/PGED1
ICESEL = ICS_PGx2	Communicate on PGEC2/PGED2

ICESEL = ICS_PGx3	Communicate on PGEC3/PGED3
ICESEL = RESERVED	Reserved

PWP	Program Flash Write Protect
PWP = OFF	Disable
PWP = PWP1K	First 1K
PWP = PWP2K	First 2K
PWP = PWP3K	First 3K
PWP = PWP4K	First 4K
PWP = PWP5K	First 5K
PWP = PWP6K	First 6K
PWP = PWP7K	First 7K
PWP = PWP8K	First 8K
PWP = PWP9K	First 9K
PWP = PWP10K	First 10K
PWP = PWP11K	First 11K
PWP = PWP12K	First 12K
PWP = PWP13K	First 13K
PWP = PWP14K	First 14K
PWP = PWP15K	First 15K
PWP = PWP16K	First 16K
PWP = PWP17K	First 17K
PWP = PWP18K	First 18K
PWP = PWP19K	First 19K
PWP = PWP20K	First 20K
PWP = PWP21K	First 21K
PWP = PWP22K	First 22K
PWP = PWP23K	First 23K
PWP = PWP24K	First 24K
PWP = PWP25K	First 25K
PWP = PWP26K	First 26K
PWP = PWP27K	First 27K
PWP = PWP28K	First 28K
PWP = PWP29K	First 29K
PWP = PWP30K	First 30K
PWP = PWP31K	First 31K
PWP = PWP32K	First 32K

BWP	Boot Flash Write Protect bit

BWP = ON	Protection Enabled
BWP = OFF	Protection Disabled

CP	Code Protect
CP = ON	Protection Enabled
CP = OFF	Protection Disabled