BRADLEY UNIVERSITY (ECE Department)
ECE 120 - Intro to EE: Circuits & Digital Systems Laboratory
Lab #8 supplement: Robot Arm Position Control Implementation

ECE120 Lab8 Week #1 :

Prelab: (30%)

1. Clock divider:
   a) Please write VHDL codes to generate a 100 KHz signal from the 50MHz system clock. [What's the counter length used in the module? Show your work in your notebook if it is needed.]
   b) A reset is required in the clock divider.
   c) Simulate the clock divider using Xilinx ISIM.
2. PWM generator
   a) Please write VHDL codes to generate a PWM signal.
   b) A reset is required in the PWM generator.
   c) A 100 kHz clock signal is provided as an input of PWM generator.
   d) The duty cycle is determined by the clock cycle number represented by an input *PWM_CONST [N-1 downto 0]*.
   [Determine the value of N based on the system requirement of PWM in lab 8. Show your work in your notebook if it is needed.]
   e) The period of PWM output signal is 20 ms.
   f) The PWM generator will generate a one-clock-cycle tick signal every 20 ms.
   g) The PWM generator will generate a one-clock-cycle tick signal every 100 ms.
   h) Simulate the PWM generator using Xilinx ISIM.
3. Debouncer
   a) The deboucner is needed for a switch input.
   b) Please write VHDL codes to debounce an input for a 20ms time delay.
   c) A reset is required in the debouncer.
   d) Simulate the debouncer using Xilinx ISIM.

Lab work: (50%)

1. Clock divider
   a) Implement the clock divider on FPGA board. 'reset' is tied to an on-board ***BTN_SOUTH*** switch. The output of clock divider is redirected to an on-board LED. [*To show the design on the board, you may have to slow the clock so that it can be observed on the board.]*
2. Combine clock divider and PWM generator together using component instantiation (i.e., declaration and port map). The output of clock divider is fed as the input clock of PWM generator. PWM_CONST is set to a constant value. The *reset* is tied to BTN_SOUTH.
   a) Simulate the design using Xilinx ISIM.
   b) Provide +5V power supply to a robot arm (see Lab 8 document for layout of robot arm daughter board)
   c) Implement the VHDL design on FPGA board. The **pwm_out** from the FPGA board is used to control pan or tilt.
   d) Try different PWM_CONST values such that it will generate three different positions (45 degree, 90 degree, and 135 degree) on pan or tilt.
   e) Measure voltage, period, and duty cycle of the pan or tilt control signal which is connected to one of two HS-422 servos.
3. Show the simulation result of a debouncer to your instructor. Combine the debouncer together with clock divider and PWM generator. Implement the design on FPGA board.

Post lab: (20%)

10% for non-technical content. 10% is lumped to the 4-week final report.

ECE120 Lab 8 Week #2 :

Prelab: (30%)

1. 8-bit counter
    a) Please write VHDL codes to design an 8-bit counter.
    b) A reset is required in the counter design.
    c) The control signals include *inc*, *pause*, *load*.
    d) Simulate the counter design using Xilinx ISIM. [Test bench : 100 KHz clock]

2. Mode generator
    a) A reset is required in the mode generator. [Note: the pan/tilt is reset to 90 degree position]
    b) A 100 KHz clock signal is provided as an input of the mode generator.
    c) 4-bit switches are used as inputs.
    d) Please list all necessary control signals for different pan and tilt control modes.
    e) Please write VHDL codes and simulate the design using Xilinx ISIM.

Lab work: (55%)

1. Verify your 8-bit counter design on FPGA board. [The pre-load value of counter is tied to a constant in the VHDL code. Other inputs are tied to switches or pushbuttons. All outputs are tied to on-board LEDs.
2. Combine 8-bit counter with PWM generator (from week 1). The 100ms tick signal from PWM generator is tied to the *inc* input of 8-bit counter.
    a) Simulate the combined design using Xilinx ISIM.
    b) Verify the combined design on FPGA board and the robot arm daughter board.
3. Mode generator check
    a) Simulate the mode generator correctly.
    b) Combine the mode generator with two 8-bit counters (one for pan control, another for tilt control). Implement the design on FPGA board. 8-bit LEDs are used to probe one of 8-bit counters. Test different combinational inputs of 4 switches and record results in your notebook.

Post lab: (15%)

5% for non-technical content. 10% is lumped to the 4-week final report.

ECE120 Lab 8 Week #3 :

Prelab : (20%)

1. System block diagram
    a) Block diagram of robot arm position control system. (Follow lecture notes or use your own design idea).
    b) Label all input/output signals for all subsystems. If it is a data bus, please mark the data width.
    c) Mark corresponding FPGA pins for the input/output signals of top-level design.

2. Write VHDL codes to combine counters, PWM generators, mode generator and other necessary logics together as a whole system.

Lab work: (55%)

a) (Debugging) Verify your design on FPGA board and the robot arm daughter board.
b) (Extra credit) Write VHDL codes for user-defined advance modes.[For example: rotary pushbutton switch, different sweep pattern, an alarm circuit with mounted photo sensor etc.]

Post lab: (25%)
(5% is for non-technical content; 20% is lumped to the 4-week final report)

ECE120 Lab 8 Week #4 :

Demonstration Day:

Lab work (80%)
Debugging and demonstration

Postlab (20%)
20% is lumped to the 4-week final report.

VHDL Lab report:
(Total 60%: 10% from week 1, 10% from week 2, 20% from week 3, 20% from week 4)

Overall grading:

Prelab : 20% (30% + 30% + 20%) / 4
Lab work: 60% (50% + 55% + 55% + 80%) /4
Postlab: 20% (10%+ 5% + 5%+ 60%)/4

Report requirements:
A report is required per group. The report is submitted through Sakai as a .doc or .pdf file. It should include a brief description of lab 8, a system block diagram with necessary signals labeled, major simulation results, discussion (problems, debugging experience etc.) and conclusion. Please limit your report in 2-3 pages. List your final VHDL codes with necessary comments as appendix.

See ECE120_Lab7 week 2 notes for more other details.

Reports: Format requirements for next Lab #8 Report

1. Assume report will be printed for records
2. Title, Name, Partner name, Date
3. Narrative should refer to Fig numbers
4. Figures: Fig. Number and Title (just like notebook)
5. Graphs: Must be able to read hard-copy. Use descriptive names for multiple plots on same graph. Add text name to each plot is the best method.
6. Always do final check with spell/grammar checker
7. Report should be included in notebook. Recall notebook is the complete record of project.
8. All of the notebook format rules apply to the report.