MSX Dual Disk Drive Controller
HB720 DOS 2.X Version
Based on Memory Mapped I/O Registers

Super exceeds compatibility from:

EPCOM/SHARP HB-3600

SONY HBD-50

Based on MSXHans, 2001 PDF
By Evandro Souza 2024, January.

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CHAPTER 1

OPERATION

1-1. FEATURES

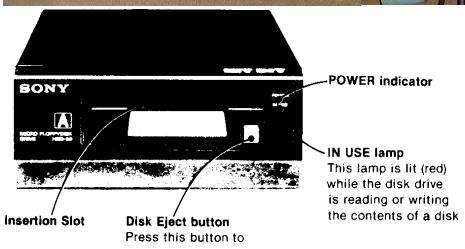
The HBD-50 floppy disk drive unit allows 3 1/2-inch micro floppy disks to be used with an MSX standard computer.
The 3 1/2-inch micro floppy disk is packaged in a hard case provided with a metal disk guard. 360K bytes of data can be recorded on a single disk and the contents can be easily retrieved and rewritten. This floppy disk drive unit will greatly extend the information-handling capabilities of your MSX computer.

1-2. SPECIFICATIONS

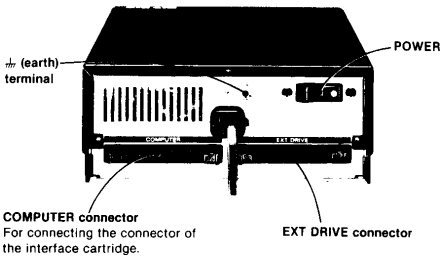
Interface Section	
Interface specifications	Fits to MSX slots
Internal ROM	64K bytes Standard I/O routines Enhanced DOS routines MSX-Disk BASIC 2 Utility routines
Power consumption	+ 5 V, 300 mA or less
Drive Section	
Disk used	5¼" and 3½" floppy disk
Disk type	Single and Double-sided
Recording capacity	Formatted: 360K / 720K bytes Bytes/sector: 512 Sectors/track: 9 Tracks/cylinder: 2 Tracks/disk: 80 Bytes/disk: 360K / 720K
Total no. of cylinders	40 / 80 cylinders
Total no. of tracks	40 / 80 / 160 tracks
Recording method	MFM (Modified-Frequency Modulation)
Disk rotation speed	300 rpm
Data transfer rate	250 K bits/sec
Average latency time	100 msec
Access time	Average: 350 msec Between tracks: 12 msec Setting time: 30 msec
Controller	WD2793-02
General	
Power requirements	United kingdom model 240V ac, 50Hz European model 220 V ac, 50 Hz Brazilian model 127/220V ac (switch selected) 60 Hz
Power consumption	United Kingdom model 25W European model 24 W Brazilian model 16W
Operating temperature	10°C-35°C (50°F-95°F) 160 x 67 x 260 mm (w/h/d)
Dimensions	For the drive unit only, including the projecting parts
Weight	Interface cartridge : 240 g Drive unit: 2.7 kg (excludes the disk)
Accessories	Blank disk (1) Disk labels (3)

1-3. PARTS IDENTIFICATION

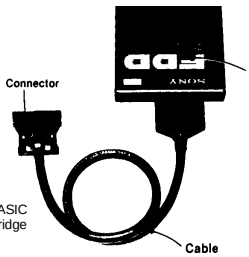
1-3-1. Drive Unit



Rear Panel



1-3-2. Interface Cartridge



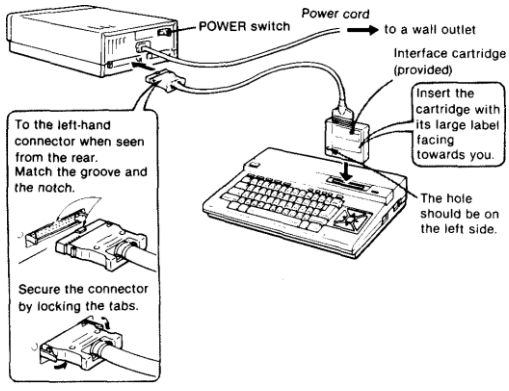
Interface cartridge
This cartridge contains MSX-Disk BASIC on ROM and is inserted into the cartridge slot of the computer.

1-4. CONNECTING THE UNIT

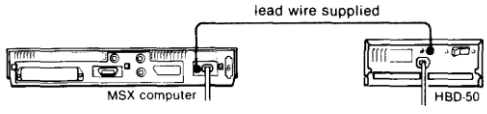
Notes on connection

Set the POWER switch of the device to be connected to OFF. Connecting the device while its power is ON may damage the internal circuitry. eWhen disconnecting the connector or cartridge, be sure to take hold of the plug or the cartridge. Pulling on the cord may break the wires.

•As a safety precaution, do not connect the power cord until all other connections have been completed.

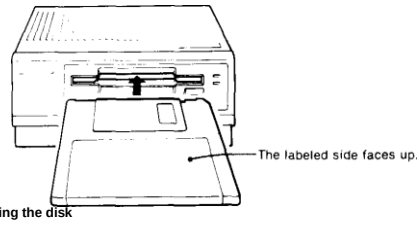


Earth wire connection

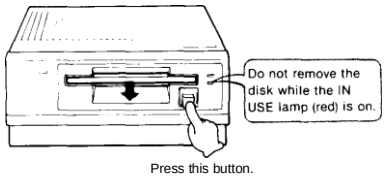


1-5. INSERTING A DISK

Without opening the metal disk guard, insert the floppydisk and gently push it *in until you hear* a click.



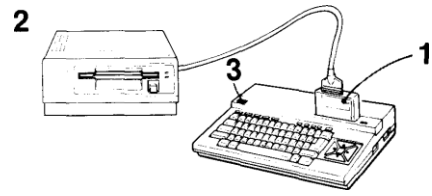
Removing the disk



1-6. STARTING UP MSX-DISK BASIC

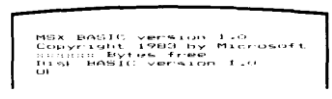
MSX-Disk BASIC is stored in ROM (read-only memory) within the interface cartridge of HBD-50.

When the interface cartridge is inserted into the cartridge slot of the computer, Disk BASIC is started up by simply switching on the power of the disk drive unit and the computer.



1 Insert the interface cartridge.
2 Set the POWER switch of HBD-50 to ON.
3 Set the POWER switch of the computer to ON.
When Disk-BASIC begins operating, the following message is displayed on the screen :

4 Enter the year, month, and date using two digits per entry (and connecting each entry by a hyphen) or simply press the [RETURN] key[1]). When the [RETURN] key is pressed, the screen will display the following message which indicates the Disk-BASIC has “signed on”.



Precautions

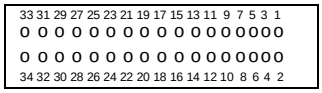
Be sure to switch on the power of the drive unit before that of the computer. If the computer has been turned on first, either press the RESET button of the computer or set the POWER switch of the computer to OFF, then to ON.

1) With MSX Disk-BASIC, date data set in this situation is not used.

1-7. PIN ASSIGNMENT OF THE CONNECTORS

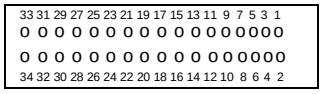
Pin Assignment of the Connectors

HB720 CARTRIDGE TO FDC: IDC 34 pins connector (BOTH SIDES)

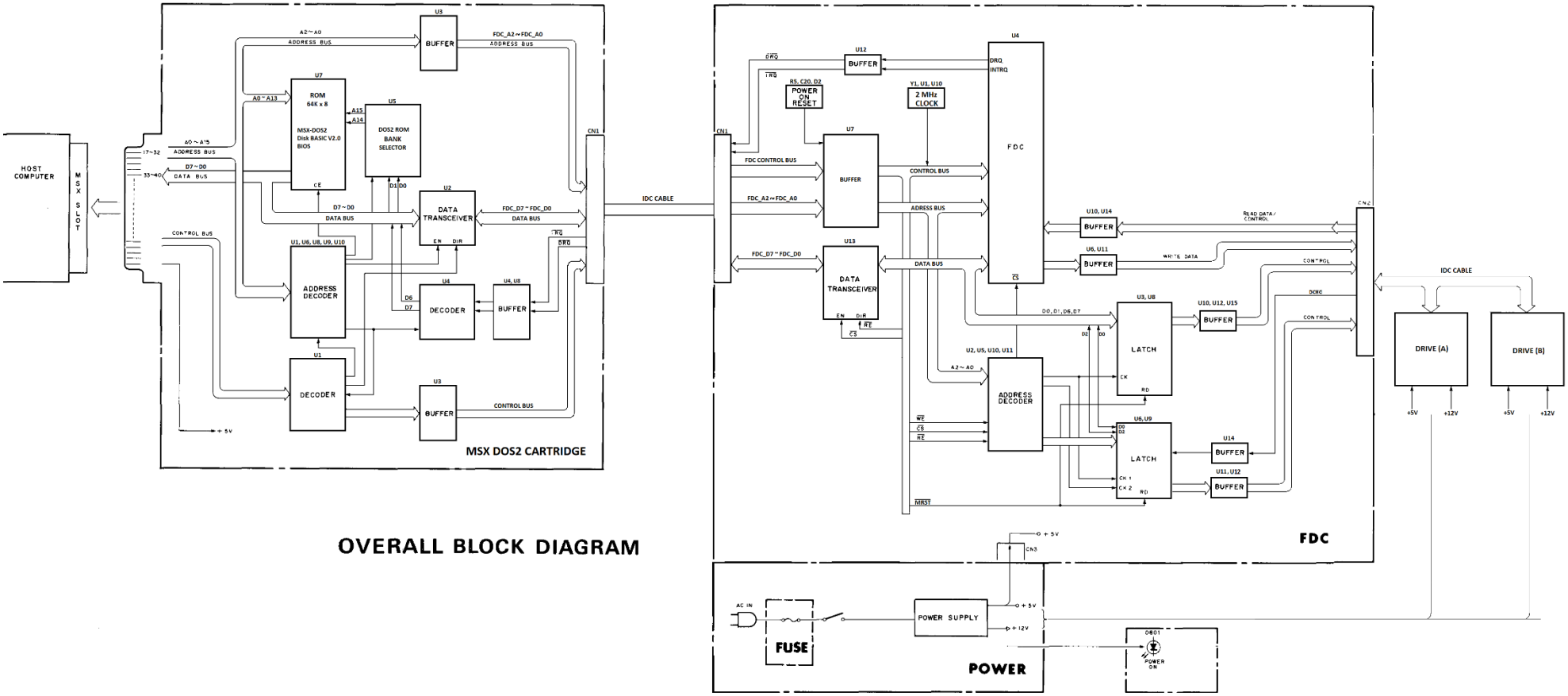


Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
1	GNDD (RETURN)	10	FDC_RE	19	GNDD (RETURN)	28	FDC_D5
2	DRQ	11	GNDD (RETURN)	20	FDC_D1	29	GNDD (RETURN)
3	N.C.	12	FDC_A0	21	GNDD (RETURN)	30	FDC_D6
4	IRQ	13	GNDD (RETURN)	22	FDC_D2	31	GNDD (RETURN)
5	GNDD (RETURN)	14	FDC_A1	23	GNDD (RETURN)	32	FDC_D7
6	FDC_WE	15	GNDD (RETURN)	24	FDC_D3	33	GNDD (RETURN)
7	N.C.	16	FDC_A2	25	GNDD (RETURN)	34	RESET
8	FDC_CS	17	GNDD (RETURN)	26	FDC_D4		
9	GNDD (RETURN)	18	FDC_D0	27	GNDD (RETURN)		

HB720 FDC TO EXT FLOPPPY DRIVE – Edge card connector (34 pins)
The pinout are the same for 5 ¼" and 3 ½" drives and the cable may have both options:
To use with 5 ¼", the connector is a card edge;
To use with 3 ½" the connector is a 34 pin female IDC.



Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
1	DISK CHANGE RESET	10	DRIVE SELECT 0	19	GNDD (RETURN)	28	WRITE PROTECT
2	DISK CHANGE	11	GNDD (RETURN)	20	STEP	29	GNDD (RETURN)
3	GNDD (RETURN)	12	DRIVE SELECT 1	21	GNDD (RETURN)	30	READ DATA
4	IN USE	13	GNDD (RETURN)	22	WRITE DATA	31	GNDD (RETURN)
5	GNDD (RETURN)	14	DRIVE SELECT 2	23	GNDD (RETURN)	32	(HEAD SELECT)
6	DRIVE SELECT 3	15	GNDD (RETURN)	24	WRITE GATE	33	GNDD (RETURN)
7	GNDD (RETURN)	16	MOTOR ON	25	GNDD (RETURN)	34	READY
8	INDEX	17	GNDD (RETURN)	26	TRACK 00	None	NONE
9	GNDD (RETURN)	18	DIRECTION	27	GNDD (RETURN)	None	NONE



OVERALL BLOCK DIAGRAM

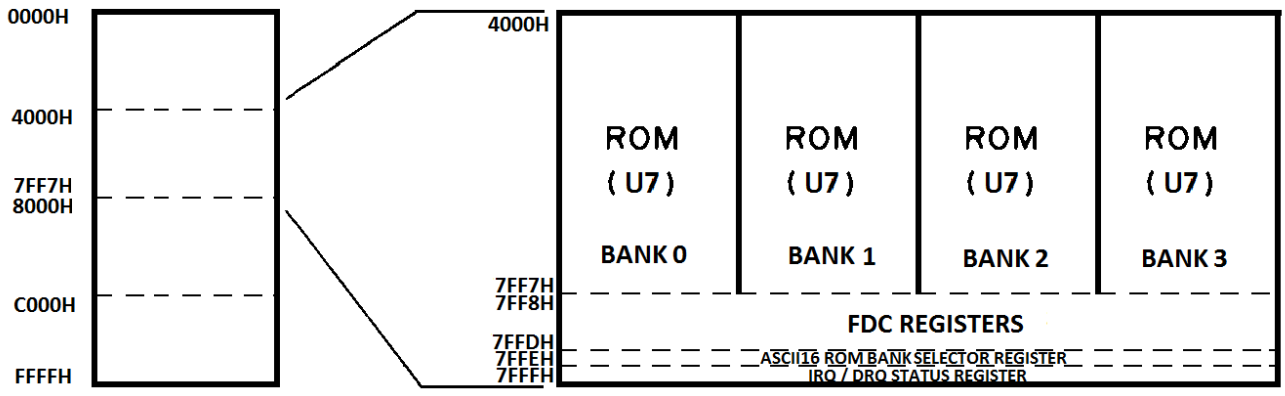
CHAPTER 3

3. THEORY OF OPERATION

3-1. Cartridge Board

3-1-1. Memory Map

This board cartridge uses the MSX computer cartridge slot. Addresses 4000H through 7FFFH on the memory map have been allocated to the HB720 cartridge.

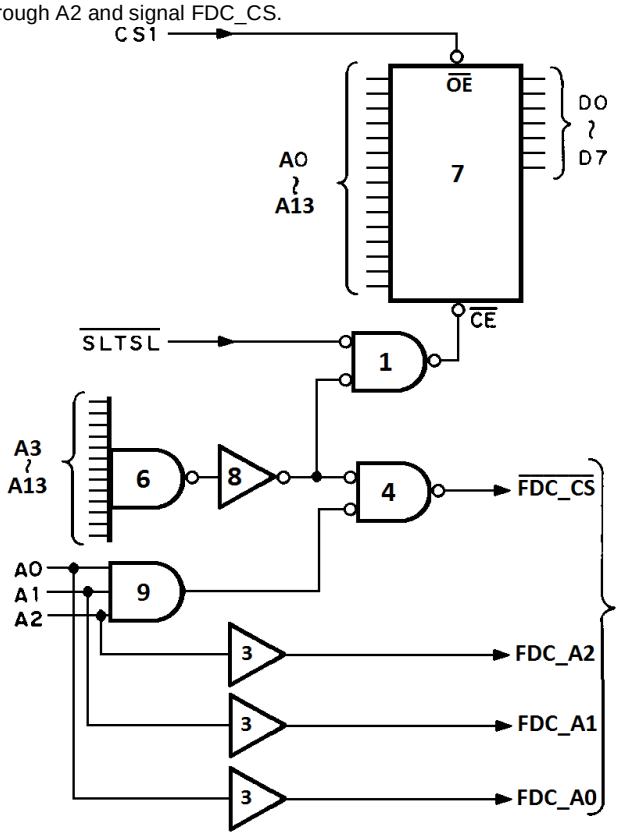


3-1-2. Selection by HB720 Cartridge

When the HB720 cartridge has been inserted into the MSX computer cartridge slot, addresses 4000H through 7FFFH will be selected by the cartridge connector signal CS1. In addition, U1 will AND signal SLTSL and the U6 (address decoder) output that has been inverted by U8, and will provide an output to U7 (ROM) pin CE for selection of the ROM.

3-1-3. Selection by FDC Controller

Individual registers of the FDC board have been allocated to the memory space for addresses 7FF8H through 7FFDH, and are selected by address signals A0 through A2 and signal FDC_CS.



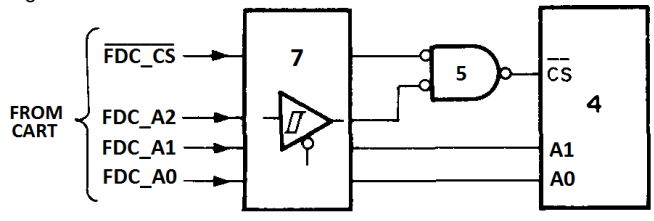
3-2. FDC Board

3-2-1. Memory Map of Control Ports in detail

Address Port	Write Mode of CPU	Read Mode of CPU
7FF8H	Command Register	Status Register
7FF9H	Track Register	Track Register
7FFAH	Sector Register	Sector Register
7FFBH	Data Register	Data Register
7FFCH	Side Select	Side Select
7FFDH	Drive Select	Drive Select
7FFEH	DOS2 ROM bank select	(Write only)
7FFFH	(Read only)	IRQ/DRQ Status

3-2-2. Selection of Individual FDC chip Registers

Individual registers of the FDC (U4) have been allocated to addresses 7FF8H through 7FFBH, and are selected by address signals AO through A2 and signal CS.



CR (COMMAND REGISTER
DR (DATA REGISTER
DSR (DATA SHIFT REGISTER
SCR (SECTOR REGISTER
TR (TRACK REGISTER
STR (STATUS REGISTER

REGISTER SELECTION

CS	A1	A0	RE = 0	WE = 0
1	X	X	NON SELECT	DAL=HI-Z
0	0	0	STR	CR
0	0	1	TR	TR
0	1	0	SCR	SCR
0	1	1	DR	DR

0 ; LOW LEVEL
1 ; HIGH LEVEL
HI-Z (HIGH IMPEDANCE)

3-2-3. Operation of Individual Registers

- Command Register (CR) - 7FF8H

This is an 8-bit write register, where the commands that correspond to the WD2793-02 operation will be written from the processor.
With the exception of a forced interrupt command, the command writing operation takes place after completion of the previous WD2793-02 command.

- Status Register (STR) - 7FF8H

This is an 8-bit read register. This register indicates the WD2793-02 internal status, the command execution processed status, and the disk drive status. The significance of individual bits will vary depending on whether the command is being executed or the command execution has already been concluded.

- Track Register (TR) - 7FF9H

This is an 8-bit read/write register. The low-high transition of MR (master reset) will set TR at FFH. When TR00 becomes low, TR will be made 00H.
The track number at which the head is located will usually be set in this register. At WD2793-02, this value may either be updated or not, depending on the command. In the case of a read data command or a write data command, the contents of this register will be compared with an ID field track number read of the disk, and when they coincide with each other, the read or write operation will duly be carried out.

- Sector Register (SCR) - 7FFAH

This is an 8-bit read/write register. In the case of a read data command or a write data command, the contents of this register will be compared with an ID field track number read of the disk, and when they coincide with each other, the read or write operation will duly be carried out.
When under a read address command, the ID field track number will be retained intact.

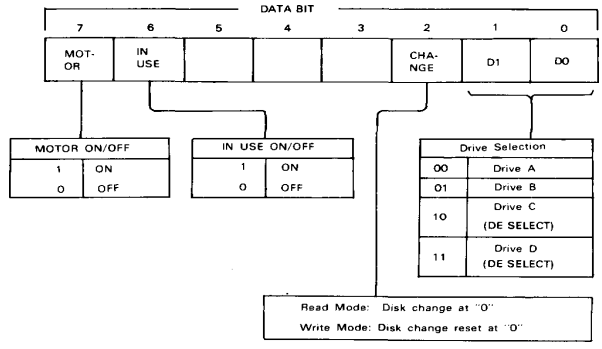
- Data Register (DR) - 7FFBH

This is a read/write register. In a disk reading mode, the data read of the disk will be loaded into this register. In a disk writing mode, the data that has been written earlier into this register will be written into the disk. In a seek mode, the target track address will be written this register

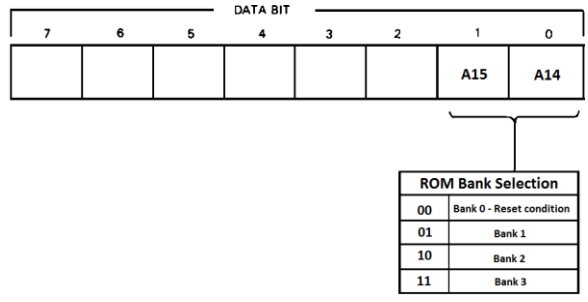
- Side Select - 7FFCH

At "0", side 0 will be selected, and at "", side 1 will be selected

- Drive Select -7FFDH

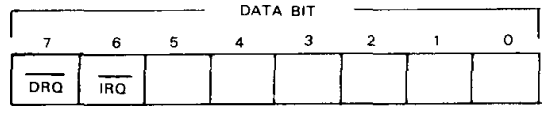


- ASCII16 - DOS2 ROM Bank Selector - 7FFEH



This is a write-only register.
It works as an ASCII16 mapper and selects each 16K bytes bank of ROM to be addressable by CPU.
Obs.: Programming technics of ASCII16 switching control are out of scope of this hardware explanation document.

- IRQ/DRQ Status - 7FFFH



IRQ will be made "0" when the completion of a command has been either concluded or terminated during process.
DRQ will be made "0" when the data write/read are being requested

Units for Capacitors and Resistors

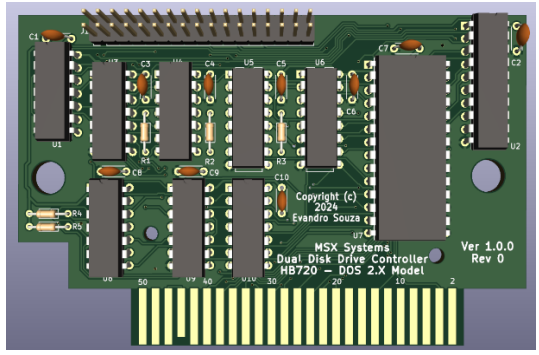
The following units are assumed in schematic diagrams, electrical parts list and exploded views unless otherwise specified:

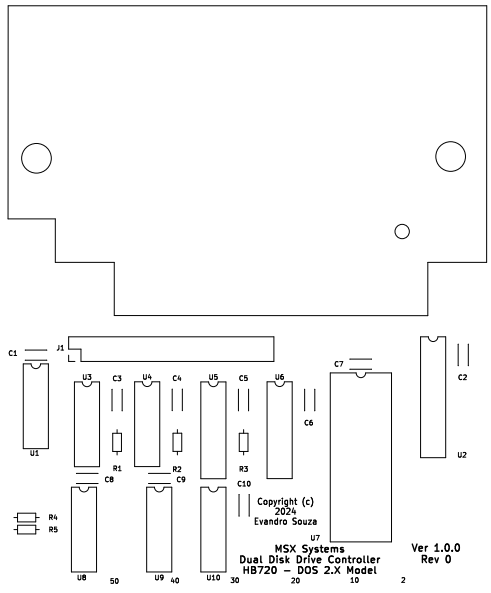
Capacitors:pF

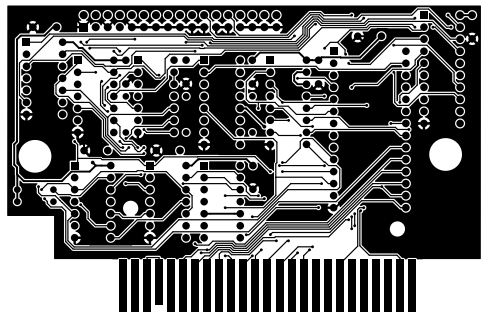
Resistors: ohm

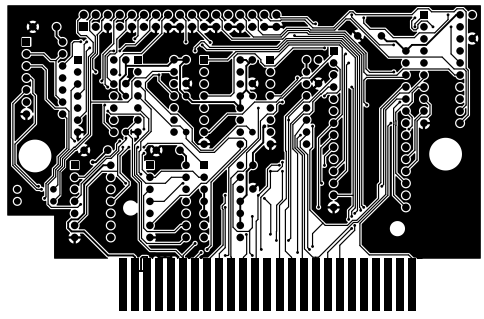
4. HB720 Boards

4.1. CARTRIDGE BOARD – DOS 2.X Model - PRINTED CIRCUIT BOARD & SCHEMATICS

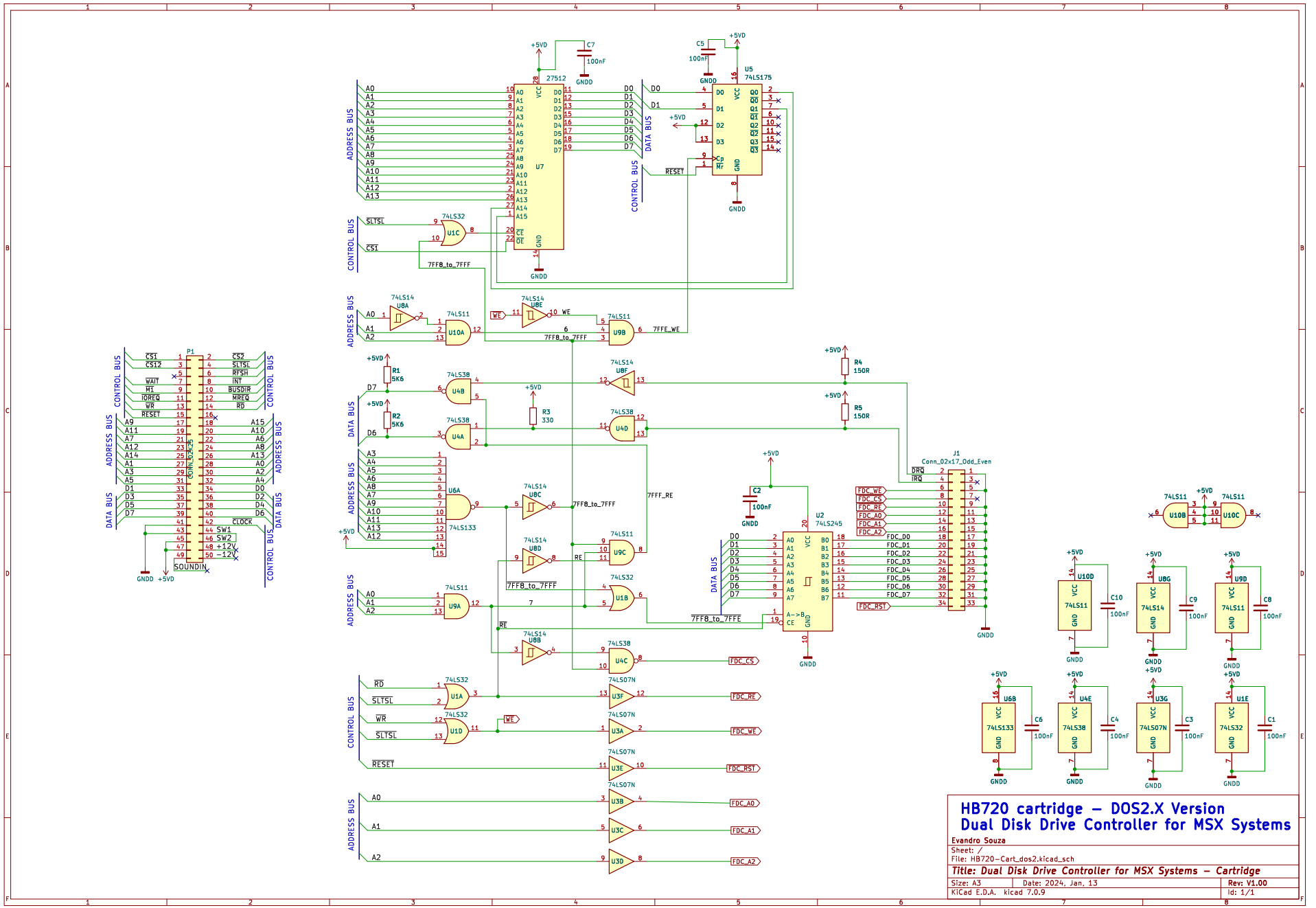




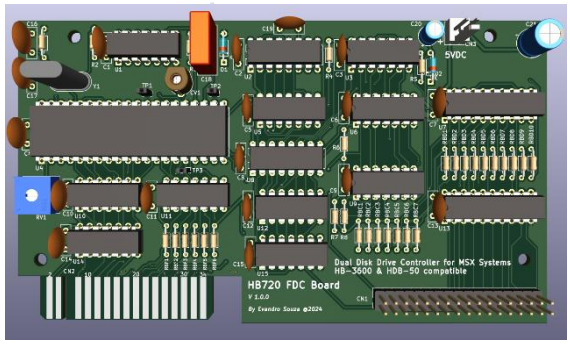


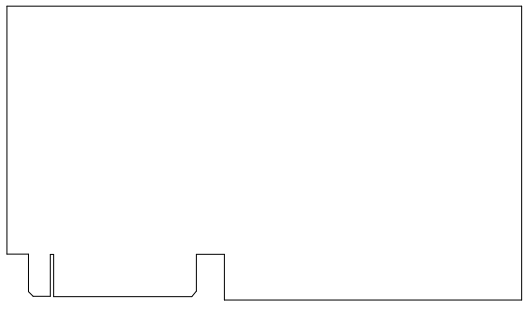


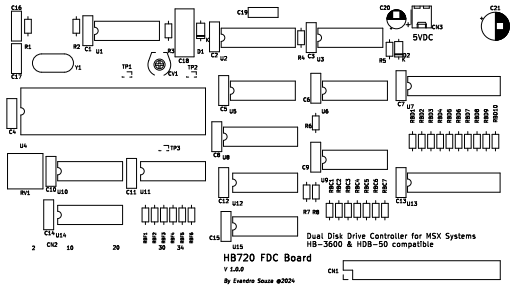
CHAPTER 4

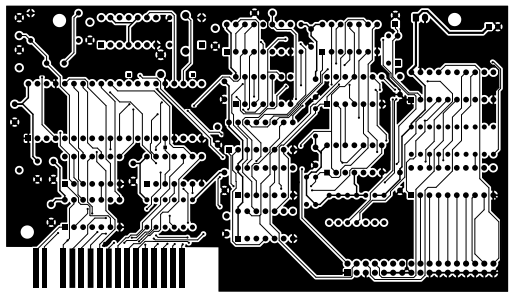

HB720 cartridge – DOS2.X Version
Dual Disk Drive Controller for MSX Systems
Evandro Souza
Sheet: /
File: HB720-Cart_dos2.kicad_sch
Title: Dual Disk Drive Controller for MSX Systems – Cartridge
Size: A3
Date: 2024, Jan, 13
Rev: V1.00
KiCad E.D.A. kicad 7.0.9
Id: 1/1

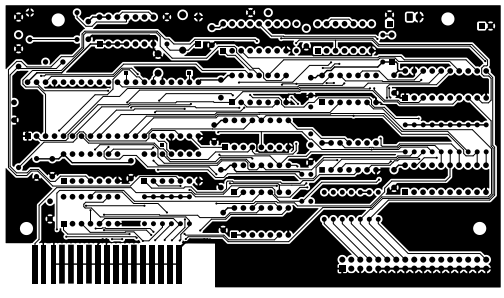
4.2. FDC Board - PRINTED CIRCUIT BOARD & SCHEMATICS



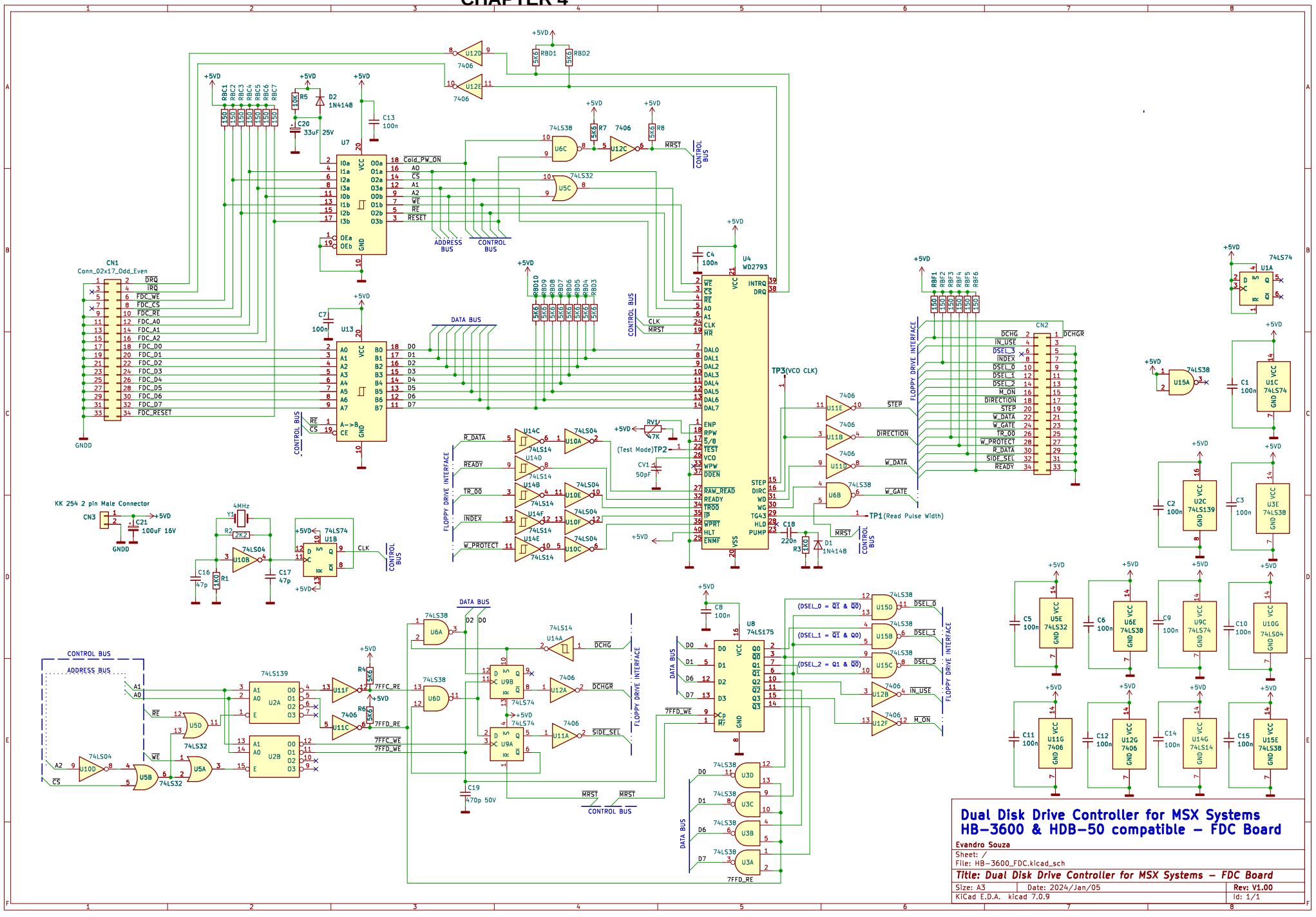






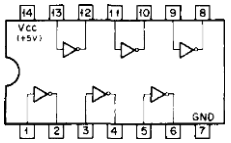


CHAPTER 4


Dual Disk Drive Controller for MSX Systems
HB-3600 & HDB-50 compatible - FDC Board
Evandro Souza
Sheet: /
File: HB-3600_FDC.kicad_sch
Title: Dual Disk Drive Controller for MSX Systems - FDC Board
Size: A3
Date: 2024/Jan/05
Rev: V1.00
KiCad E.D.A. kicad 7.0.9
Id: 1/1

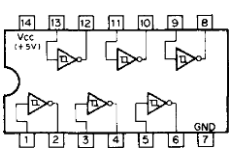
5. SEMICONDUCTOR PIN ASSIGNMENTS

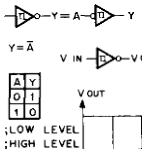
MB74LS04 (FUJITSU)
SN74LS04N ^TI) TTL
INVERTER — TOP VIEW
—



0; LOW LEVEL
UHIGH LEVEL

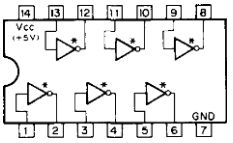
MB74LS14 (FUJITSU)
SN74LS14N (TI)
TTL SCHMITT TRIGGER INVERTER
— TOP VIEW —





»V IN
SN7414N .....0.9 1.7 V
SN74LS14N--0.8 1.6V

M532O6P (MITSUBISHI)
SN74O6N (TI)
TTL INVERTER BUFFER/DRIVER WITH OPEN-
COLLECTOR — TOP VIEW —

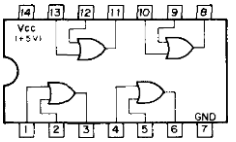


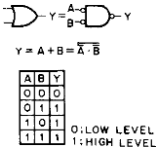
Y = A

HO;LOW LEVEL
1 ; HIGH LEVEL
*;OPEN COLLECTOR

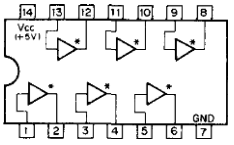
MB74LS32 (FUJITSU)
SN74LS32N (TI)

TTL 2-INPUT POSITIVE-OR GATE
— TOP VIEW —



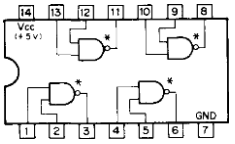


SN74O7N (TI)
TTL BUFFER/DRIVER WITH OPEN-COLLECTOR
— TOP VIEW —



0 LOW LEVEL
1 ; HIGH LEVEL
* ; OPEN COLLECTOR

MB74LS38 (FUJITSU)
SN7438N (TI)
SN74LS38N (TI)
TTL 2-INPUT POSITIVE-NAND GATE BUFFER
WITH OPEN-COLLECTOR — TOP VIEW —

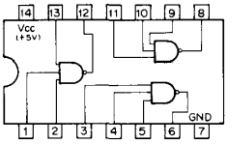


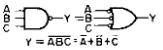
Y=AB=A+B

A _B Y.

0; LOW LEVEL
LÉ ± 1 ; HIGH LEVEL
¹ H I*! * ; OPEN COLLECTOR

SN74LS10N (TI)
TTL 3-INPUT POSITIVE NAND GATE
— TOP VIEW —



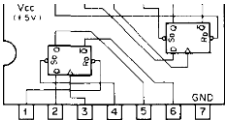


A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

0 : LOW LEVEL
1 : HIGH LEVEL

MB74LS74A (FUJITSU)
SN74LS74AN (TI)
TTL D-TYPE FLIP FLOP WITH DIRECT SET/RESET
— TOP VIEW —

[w] F?] [7;] H [ipl M lei

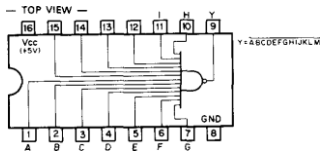


INPUTS				OUTPUTS	
S	RolC	D		On+1	On+1
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	1 *	1 *
1	1		1	1	0
1	1	J	0	0	
1	1	0	X	On	On

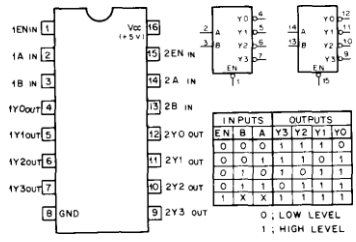
0;LOW LEVEL 1 ;
HIGH LEVEL X;
DON'T CARE 1*;
NONSTABLE

SN74LS133N (TI)
TTL 13-INPUT NAND GATE

— TOP VIEW —



MB74LS139 (FUJITSU)
SN74LS139N (TI)
TTL 2-T0-4-LINE DECOOER/DEMULTIPLEXER

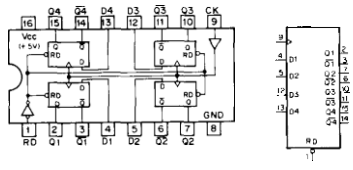


INPUTS			OUTPUTS			
EN	B	A	Y3	Y2	Y1	Y0
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1
1	X	X	1	1	1	1

0 ; LOW LEVEL
1 ; HIGH LEVEL

— TOP VIEW —

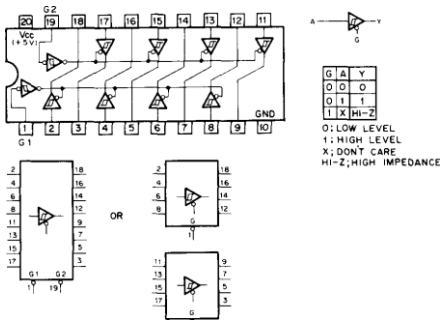
MB74LS1 75 (FUJITSU)
SN74LS175N (TI)
TTL O-TYPE FLIP-FLOP WITH CLEAR — TOP



RD	CK	D	Q	$\bar{Q}$
0	X	X	0	1
1	↑	1	1	0
1	↑	0	0	1
1	0	X	Q_0	$\bar{Q}_0$

0; LOW LEVEL
1; HIGH LEVEL
X; DON'T CARE

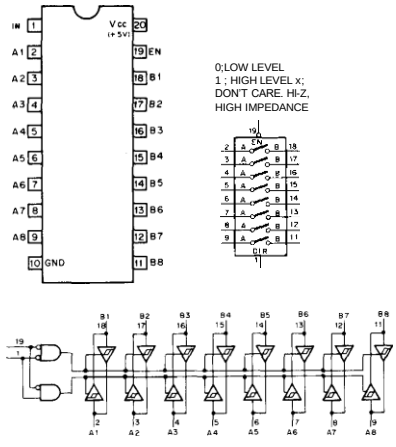
VIEW —
MB74LS244 (FUJITSU)
SN74LS244N (TI)
TTL 3-STATE SCHMITT TRIGGER
BUFFER/DRIVER — TOP VIEW —



G	A	Y
0	0	0
0	1	1
1	X	HI-Z

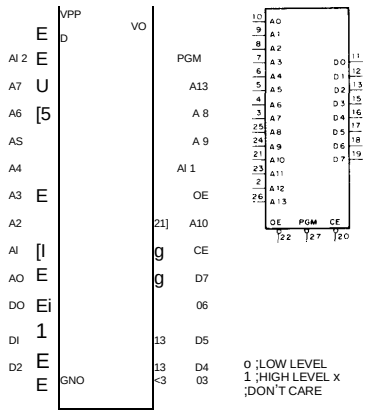
0; LOW LEVEL
1; HIGH LEVEL
X; DON'T CARE
HI-Z; HIGH IMPEDANCE

MB74LS245 (FUJITSU)
SN74LS245N (TI)
TTL BILATERAL SCHMITT TRIGGER BUS TRANSCEIVERS WITH 3-STATE OUTPUT — TOP VIEW —

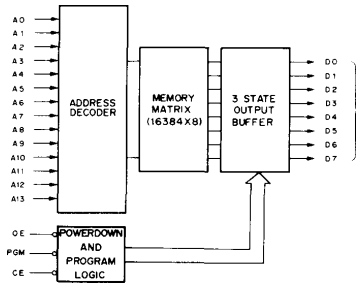


0;LOW LEVEL
1 ; HIGH LEVEL x; DON'T CARE. HI-Z, HIGH IMPEDANCE

HN48271 28G-25 (HITACHI) (ACCESS TIME = 250nS)
HN4827128G-30 (HITACHI) (ACCESS TIME = 300nS) HN4827128G-45 (HITACHI) (ACCESS TIME = 450nS) N-MOS ERASABLE AND PROGRAMMABLE ROM 128K-BIT <16384x8) — TOP VIEW —

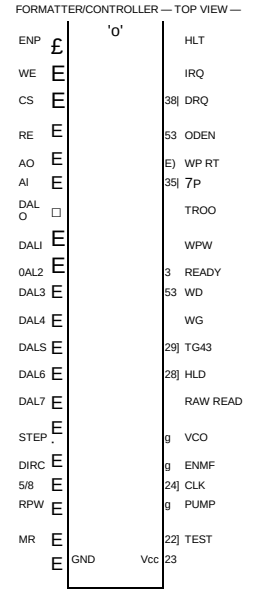


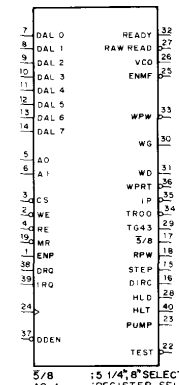
0 ;LOW LEVEL
1 ;HIGH LEVEL x
;DON'T CARE



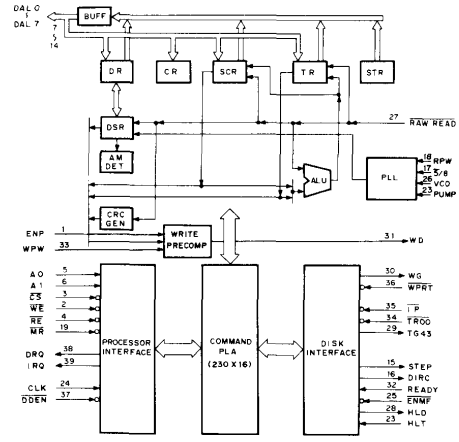
AO-13 ; ADDRESS INPUT
CE ; CHIP ENABLE DO-7 ; DATA
OE I OUTPUT ENABLE PGM ; PROGRAM

WD2793-02 (WESTERN DIGITAL)
N CHANNEL E/D MOS FLOPPY DISK FORMATTER/CONTROLLER — TOP VIEW —





5/8 ;5 1/4",8" SELECT
AO, 1 ;REGISTER SELECT LINES
CLK ;CLOCK
CS ;*CHIP* SELECT
DALO-7 JDATA ACCESS LINES DDEN iDOUBLE DENSITY
DIRC '.DIRECTION
DRQ ;DATA REQUEST
ENMF iENABLE MINI-FLOPPY
ENP J ENABLE PRECOMP
HLD » HEAD LOAD
HLT i HEAD LOAD TIMING
IP ;INDEX PULSE
IRQ :'INTERRUPT REQUEST
MR i MASTER RESET
RE I READ ENABLE
RPW ***! READ PULSE*** WIDTH
TG43 I TRACK GREATER THAN43
TROO : TRACK 00
VCO : VOLTAGE-CONTROLLED OSC
WD t WRITE DATA
WE i WRITE ENABLE
WG 'WRITE GATE
WPRT 1 WRITE PROTECT
WPW t WRITE PRECOMP WIDTH



CR COMMAND REGISTER
DR ;DATA REGISTER DSR iOATA SHIFT REGISTER SCR SECTOR REGISTER TR '.TRACK REGISTER STR '.STATUS REGISTER

REGISTER SELECTION

CS	A 1	AO	RE = 0	WE = 0
1	X	X	NON	OAL = HI-Z
0	0	0	STR	C R
0	0	1	TR	TR
0	1	0	SCR	SCR
0	1	1	DR	OR

0 :LOW LEVEL
1 I HIGH LEVEL X ; DON'T CARE HI-Z; HIGH IMPEDANCE

HB720