MSX Dual Disk Drive Controller
HB720 DOS 2.X Version
Based on Memory Mapped I/O Registers

Super exceeds compatibility from:

EPCOM/SHARP HB-3600

SONY HBD-50

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CHAPTER 1

OPERATION

1-1. FEATURES

The HBD-50 floppy disk drive unit allows 3 1/2-inch micro floppy disks to be used with an MSX standard computer.
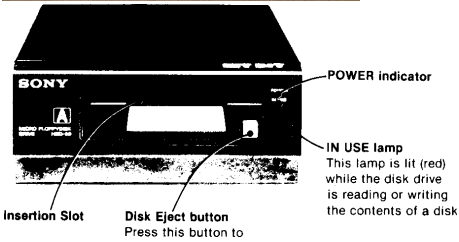
The 3 1/2-inch micro floppy disk is packaged in a hard case provided with a metal disk guard. 360K bytes of data can be recorded on a single disk and the contents can be easily retrieved and rewritten. This floppy disk drive unit will greatly extend the information-handling capabilities of your MSX computer.
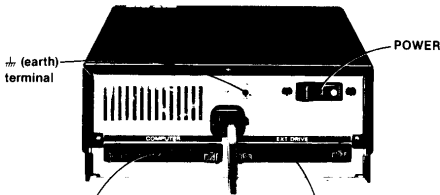
1-2. SPECIFICATIONS

Interface Section

Interface specifications	Fits to MSX slots
Internal ROM	64K bytes
	Standard I/O routines
	Enhanced DOS routines
	MSX-Disk BASIC 2 Utility routines
Power consumption	+ 5 V, 300 mA or less

Drive Section

Disk used	5¼" and 3$\frac{1}{2}$" floppy disk
Disk type	Single and Double-sided
Recording capacity	Formatted: 360K / 720K bytes
	Bytes/sector: 512
	Sectors/track: 9
	Tracks/cylinder: 2
	Tracks/disk: 80
	Bytes/disk: 360K / 720K
Total no. of cylinders	40 / 80 cylinders
Total no. of tracks	40 / 80 / 160 tracks
Recording method	MFM (Modified-Frequency Modulation)
Disk rotation speed	300 rpm
Data transfer rate	250 K bits/sec
Average latency time	100 msec
Access time	Average: 350 msec
	Between tracks: 12 msec
	Settling time: 30 msec
Controller	WD2793-02

General

Power requirements	United kingdom model 240V ac, 50Hz
	European model 220 V ac, 50 Hz
	Brazilian model 127/220V ac (switch selected) 60 Hz
Power consumption	United Kingdom model 25W
	European model 24 W
	Brazilian model 16W
Operating temperature	10°C-35°C (50°F-95°F) 160 x 67 x 260 mm (w/h/d)
Dimensions	For the drive unit only, including the projecting parts
Weight	Interface cartridge : 240 g
	Drive unit: 2.7 kg (excludes the disk)
Accessories	Blank disk (1)
	Disk labels (3)

1-3. PARTS IDENTIFICATION

1-3-1. Drive Unit

POWER indicator

IN USE lamp
This lamp is lit (red) while the disk drive is reading or writing the contents of a disk

Insertion Slot

Disk Eject button
Press this button to

Rear Panel

⏚ (earth) terminal

POWER

COMPUTER connector
For connecting the connector of the interface cartridge.

EXT DRIVE connector

1-3-2. Interface Cartridge
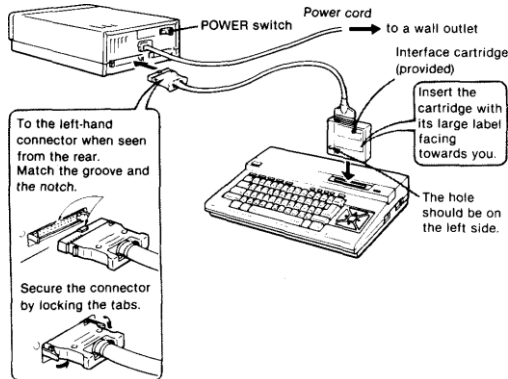

Connector

Cable

Interface cartridge
This cartridge contains MSX-Disk BASIC on ROM and is inserted into the cartridge slot of the computer.
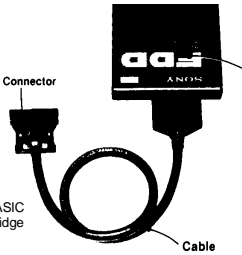
1-4. CONNECTING THE UNIT

Notes on connection

Set the POWER switch of the device to be connected to OFF. Connecting the device while its power is ON may damage the internal circuitry. eWhen disconnecting the connector or cartridge, be sure to take hold of the plug or the cartridge. Pulling on the cord may break the wires.

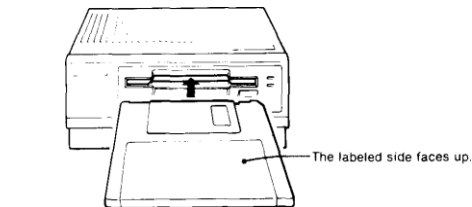•As a safety precaution, do not connect the power cord until all other connections have been completed.
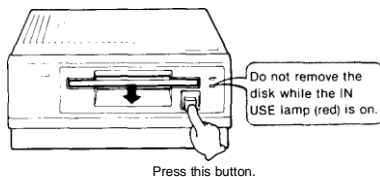

Earth wire connection
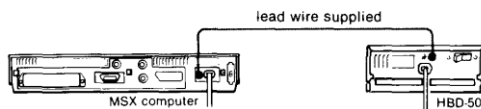
1-5. INSERTING A DISK

Without opening the metal disk guard, insert the floppydisk and gently push it *in until you hear* a click.

The labeled side faces up.

Removing the disk

Do not remove the disk while the IN USE lamp (red) is on.

Press this button.

1-6. STARTING UP MSX-DISK BASIC

MSX-Disk BASIC is stored in ROM (read-only memory) within the interface cartridge of HBD-50.

When the interface cartridge is inserted into the cartridge slot of the computer, Disk BASIC is started up by simply switching on the power of the disk drive unit and the computer.
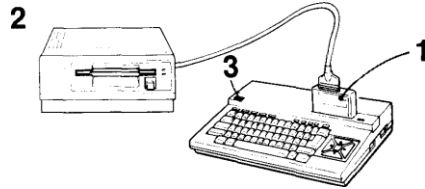
1   Insert the interface cartridge.
2   Set the POWER switch of HBD-50 to ON.
3   Set the POWER switch of the computer to ON.
    When Disk-BASIC begins operating, the following message is displayed on the screen :

4   Enter the year, month, and date using two digits per entry (and connecting each entry by a hyphen) or simply press the [RETURN] key[1]). When the [RETURN] key is pressed, the screen will display the following message which indicates the Disk-BASIC has "signed on".
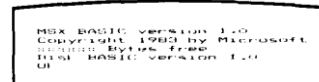
Precautions

Be sure to switch on the power of the drive unit before that of the computer. If the computer has been turned on first, either press the RESET button of the computer or set the POWER switch of the computer to OFF, then to ON.

1) With MSX Disk-BASIC, date data set in this situation is not used.

1-7. PIN ASSIGNMENT OF THE CONNECTORS

Pin Assignment of the Connectors

HB720 CARTRIDGE TO FDC: IDC 34 pins connector (BOTH SIDES)

```
33 31 29 27 25 23 21 19 17 15 13 11  9  7  5  3  1
 O  O  O  O  O  O  O  O  O  O  O  O  O  O  O  O  O

 O  O  O  O  O  O  O  O  O  O  O  O  O  O  O  O  O
34 32 30 28 26 24 22 20 18 16 14 12 10  8  6  4  2
```

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
1	GNDD (RETURN)	10	FDC_RE	19	GNDD (RETURN)	28	FDC_D5
2	DRQ	11	GNDD (RETURN)	20	FDC_D1	29	GNDD (RETURN)
3	N.C.	12	FDC_A0	21	GNDD (RETURN)	30	FDC_D6
4	IRQ	13	GNDD (RETURN)	22	FDC_D2	31	GNDD (RETURN)
5	GNDD (RETURN)	14	FDC_A1	23	GNDD (RETURN)	32	FDC_D7
6	FDC_WE	15	GNDD (RETURN)	24	FDC_D3	33	GNDD (RETURN)
7	N.C.	16	FDC_A2	25	GNDD (RETURN)	34	RESET
8	FDC_CS	17	GNDD (RETURN)	26	FDC_D4		
9	GNDD (RETURN)	18	FDC_D0	27	GNDD (RETURN)		

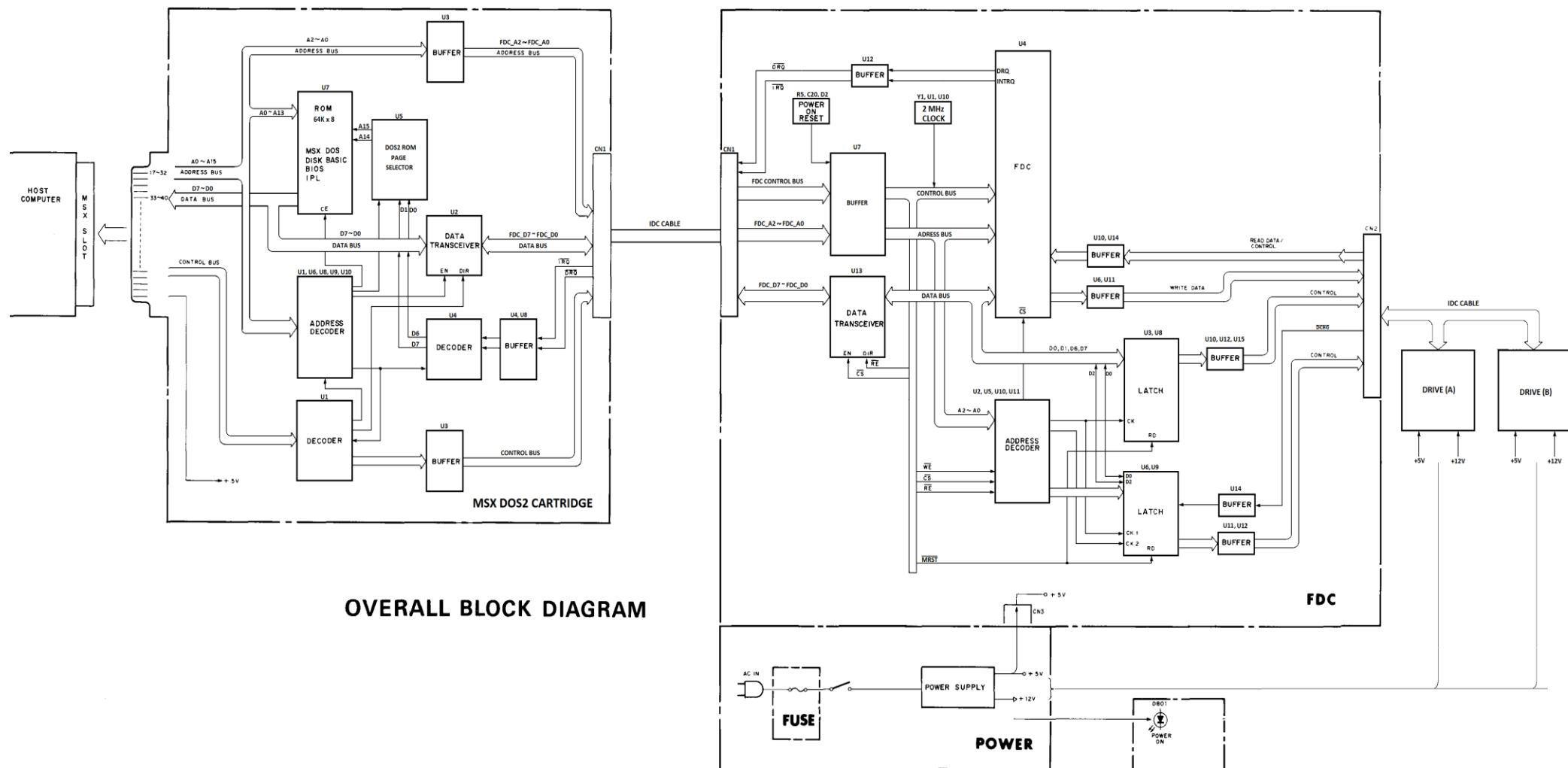HB720 FDC TO EXT FLOPPPY DRIVE – Edge card connector (34 pins)
The pinout are the same for 5 ¼" and 3 ½" drives and the cable may have both options:
To use with 5 ¼", the connector is a card edge;
To use with 3 ½" the connector is a 34 pin female IDC.

```
33 31 29 27 25 23 21 19 17 15 13 11  9  7  5  3  1
 O  O  O  O  O  O  O  O  O  O  O  O  O  O  O  O  O

 O  O  O  O  O  O  O  O  O  O  O  O  O  O  O  O  O
34 32 30 28 26 24 22 20 18 16 14 12 10  8  6  4  2
```

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
1	DISK CHANGE RESET	10	DRIVE SELECT 0	19	GNDD (RETURN)	28	WRITE PROTECT
2	DISK CHANGE	11	GNDD (RETURN)	20	STEP	29	GNDD (RETURN)
3	GNDD (RETURN)	12	DRIVE SELECT 1	21	GNDD (RETURN)	30	READ DATA
4	IN USE	13	GNDD (RETURN)	22	WRITE DATA	31	GNDD (RETURN)
5	GNDD (RETURN)	14	DRIVE SELECT 2	23	GNDD (RETURN)	32	(HEAD SELECT)
6	DRIVE SELECT 3	15	GNDD (RETURN)	24	WRITE GATE	33	GNDD (RETURN)
7	GNDD (RETURN)	16	MOTOR ON	25	GNDD (RETURN)	34	READY
8	INDEX	17	GNDD (RETURN)	26	TRACK 00	None	NONE
9	GNDD (RETURN)	18	DIRECTION	27	GNDD (RETURN)	None	NONE

OVERALL BLOCK DIAGRAM

MSX DOS2 CARTRIDGE

HOST COMPUTER — MSX SLOT

A2~A0 ADDRESS BUS — U3 BUFFER — FDC_A2~FDC_A0 ADDRESS BUS

U7 ROM 64K x 8 — MSX DOS DISK BASIC BIOS IPL — A0~A13, A0~A15 ADDRESS BUS, A15, A14, CE

U5 DOS2 ROM PAGE SELECTOR — D1 D0

D7~D0 DATA BUS

U2 DATA TRANSCEIVER — FDC_D7~FDC_D0 DATA BUS — EN DIR — ĪRQ, DRQ

U1, U6, U8, U9, U10 ADDRESS DECODER

U4 DECODER — D6, D7

U4, U8 BUFFER

U1 DECODER — U3 BUFFER — CONTROL BUS

CONTROL BUS

+5V

CN1

IDC CABLE

FDC

CN1

FDC CONTROL BUS — U7 BUFFER — CONTROL BUS

FDC_A2~FDC_A0 — ADRESS BUS

FDC_D7~FDC_D0 — U13 DATA TRANSCEIVER — DATA BUS — EN DIR RE, CS

ĪRQ, ĪRQ — U12 BUFFER — DRQ, INTRQ

R5, C20, D2 POWER ON RESET

Y1, U1, U10 2 MHz CLOCK

U4 FDC — CS

U10, U14 BUFFER — READ DATA/CONTROL

U6, U11 BUFFER — WRITE DATA — CONTROL

U3, U8 LATCH — CK, RD — U10, U12, U15 BUFFER — CONTROL, DCHG

D0, D1, D6, D7

U2, U5, U10, U11 ADDRESS DECODER — A2~A0 — WE, CS, RE

U6, U9 LATCH — D0, D2 — CK 1, CK 2, RD — U14 BUFFER — U11, U12 BUFFER

MRST

CN2 — IDC CABLE

DRIVE (A) +5V +12V — DRIVE (B) +5V +12V

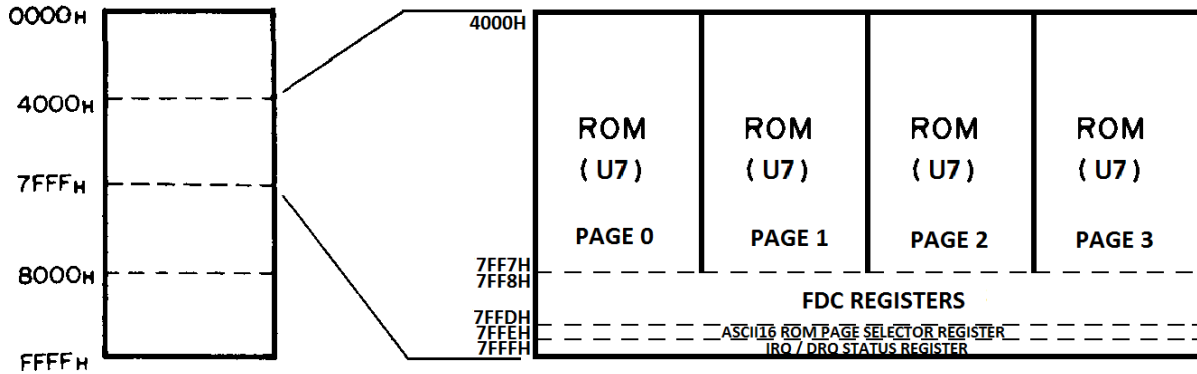**POWER**

AC IN — FUSE — POWER SUPPLY — +5V, +12V — CN3

DB01 POWER ON

3. THEORY OF OPERATION

3-1. Cartridge Board

3-1-1. Memory Map

This board cartridge uses the MSX computer cartridge slot. Addresses 4000H through 7FFFH on the memory map have been allocated to the HB720 cartridge.


3-1-2. Selection by HB720 Cartridge

When the HB720 cartridge has been inserted into the MSX computer cartridge slot, addresses 4000H through 7FFFH will be selected by the cartridge connector signal CS1. In addition, U1 will AND signal SLTSL and the U6 (address decoder) output that has been inverted by U8, and will provide an output to U7 (ROM) pin CE for selection of the ROM.

3-1-3. Selection by FDC Controller

Individual registers of the FDC board have been allocated to the memory space for addresses 7FF8H through 7FFDH, and are selected by address signals A0 through A2 and signal FDC_CS.
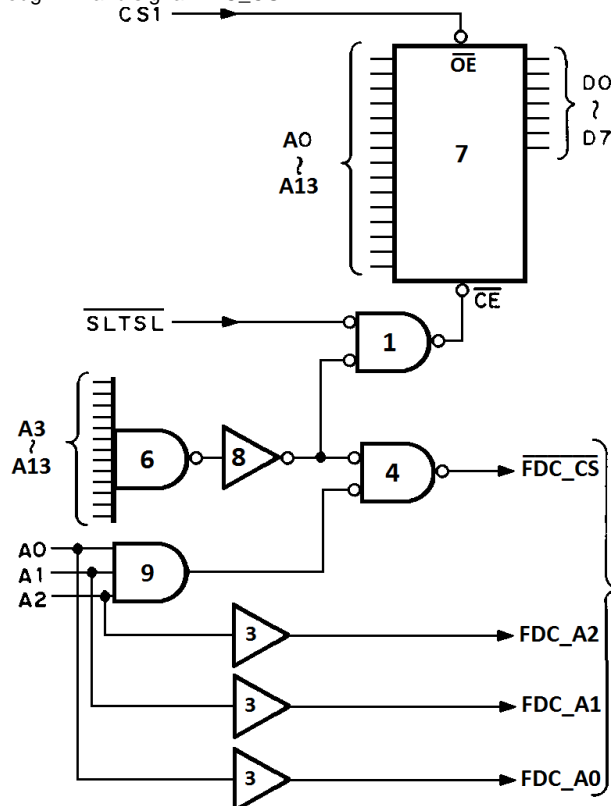
3-2. FDC Board

3-2-1. Memory Map of Control Ports in detail

Address Port	Write Mode of CPU	Read Mode of CPU
7FF8H	Command Register	Status Register
7FF9H	Track Register	Track Register
7FFAH	Sector Register	Sector Register
7FFBH	Data Register	Data Register
7FFCH	Side Select	Side Select
7FFDH	Drive Select	Drive Select
7FFEH	DOS2 ROM page select	(Write only)
7FFFH	(Read only)	IRQ/DRQ Status

3-2-2. Selection of Individual FDC chip Registers

Individual registers of the FDC (U4) have been allocated to addresses 7FF8H through 7FFBH, and are selected by address signals AO through A2 and signal CS.
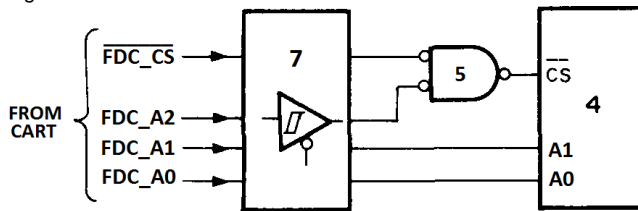
CR (COMMAND REGISTER
DR (DATA REGISTER
DSR (DATA SHIFT REGISTER
SCR (SECTOR REGISTER
TR (TRACK REGISTER
STR (STATUS REGISTER

REGISTER SELECTION

CS	A1	AO	RE = O	WE = O
1	X	X	NON SELECT	DAL = HI-Z
O	O	O	STR	CR
O	O	1	TR	TR
O	1	O	SCR	SCR
O	1	1	DR	DR

O ; LOW LEVEL
1 ; HIGH LEVEL
HI-Z (HIGH IMPEDANCE)

3-2-3. Operation of Individual Registers

➤ Command Register (CR) - 7FF8H

This is an 8-bit write register, where the commands that correspond to the WD2793-02 operation will be written from the processor.
With the exception of a forced interrupt command, the command writing operation takes place after completion of the previous WD2793-02 command.

➤ Status Register (STR) - 7FF8H

This is an 8-bit read register. This register indicates the WD2793-02 internal status, the command execution processed status, and the disk drive status. The significance of individual bits will vary depending on whether the command is being executed or the command execution has already been concluded.

➤ Track Register (TR) - 7FF9H

This is an 8-bit read/write register. The low-high transition of MR (master reset) will set TR at FFH. When TR00 becomes low, TR will be made 00H.
The track number at which the head is located will usually be set in this register. At WD2793-02, this value may either be updated or not, depending on the command. In the case of a read data command or a write data command, the contents of this register will be compared with an ID field track number read of the disk, and when they coincide with each other, the read or write operation will duly be carried out.

➤ Sector Register (SCR) - 7FFAH

This is an 8-bit read/write register. In the case of a read data command or a write data command, the contents of this register will be compared with an ID field track number read of the disk, and when they coincide with each other, the read or write operation will duly be carried out.
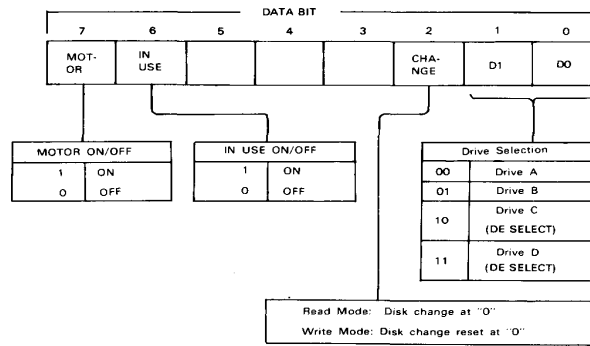When under a read address command, the ID field track number will be retained intact.

➢ Data Register (DR) - 7FFBH

This is a read/write register. In a disk reading mode, the data read of the disk will be loaded into this register. In a disk writing mode, the data that has been written earlier into this register will be written into the disk. In a seek mode, the target track address will be written this register
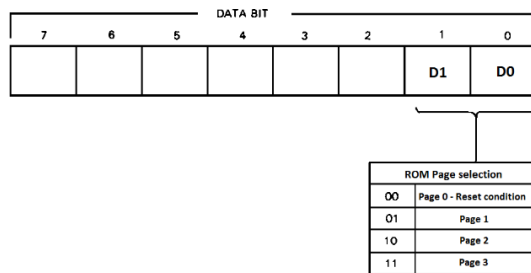
➢ Side Select - 7FFCH

DATA BIT							
7	6	5	4	3	2	1	0
							SIDE

➢ Drive Select -7FFDH

DATA BIT							
7	6	5	4	3	2	1	0
MOT-OR	IN USE				CHA-NGE	D1	D0

MOTOR ON/OFF	
1	ON
0	OFF

IN USE ON/OFF	
1	ON
0	OFF

Drive Selection	
00	Drive A
01	Drive B
10	Drive C (DE SELECT)
11	Drive D (DE SELECT)

Read Mode: Disk change at "0"

Write Mode: Disk change reset at "0"

➢ ASCII16 - DOS2 ROM Page Selector - 7FFEH

DATA BIT							
7	6	5	4	3	2	1	0
						D1	D0

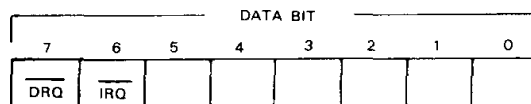| ROM Page selection	
00	Page 0 - Reset condition
01	Page 1
10	Page 2
11	Page 3

This is a write-only register.

It works as an ASCII16 mapper and selects each 16K bytes page of ROM to be addressable by CPU.

Obs.: Programming technics of ASCII16 switching control are out of scope of this hardware explanation document.

➢ IRQ/DRQ Status - 7FFFH

DATA BIT							
7	6	5	4	3	2	1	0
DRQ	IRQ						

IRQ will be made "0" when the completion of a command has been either concluded or terminated during process.

DRQ will be made "0" when the data write/read are being requested
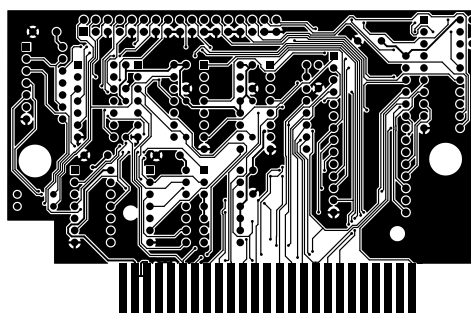
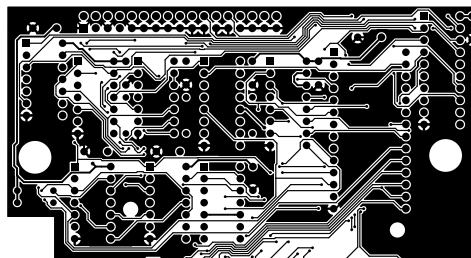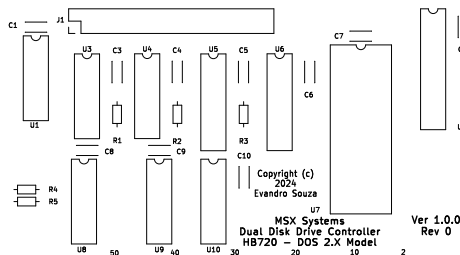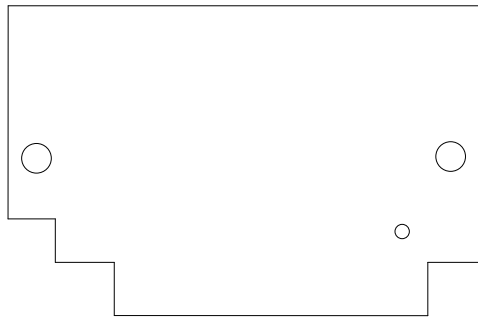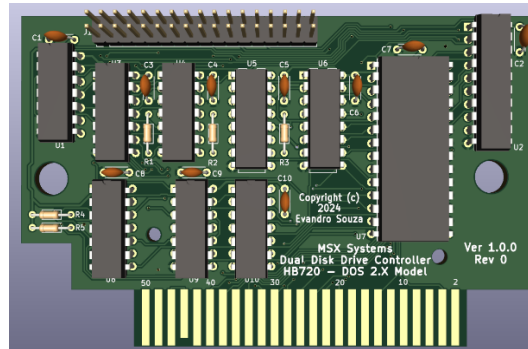Units for Capacitors and Resistors

The following units are assumed in schematic diagrams, electrical parts list and exploded views unless otherwise specified:

Capacitors: pF

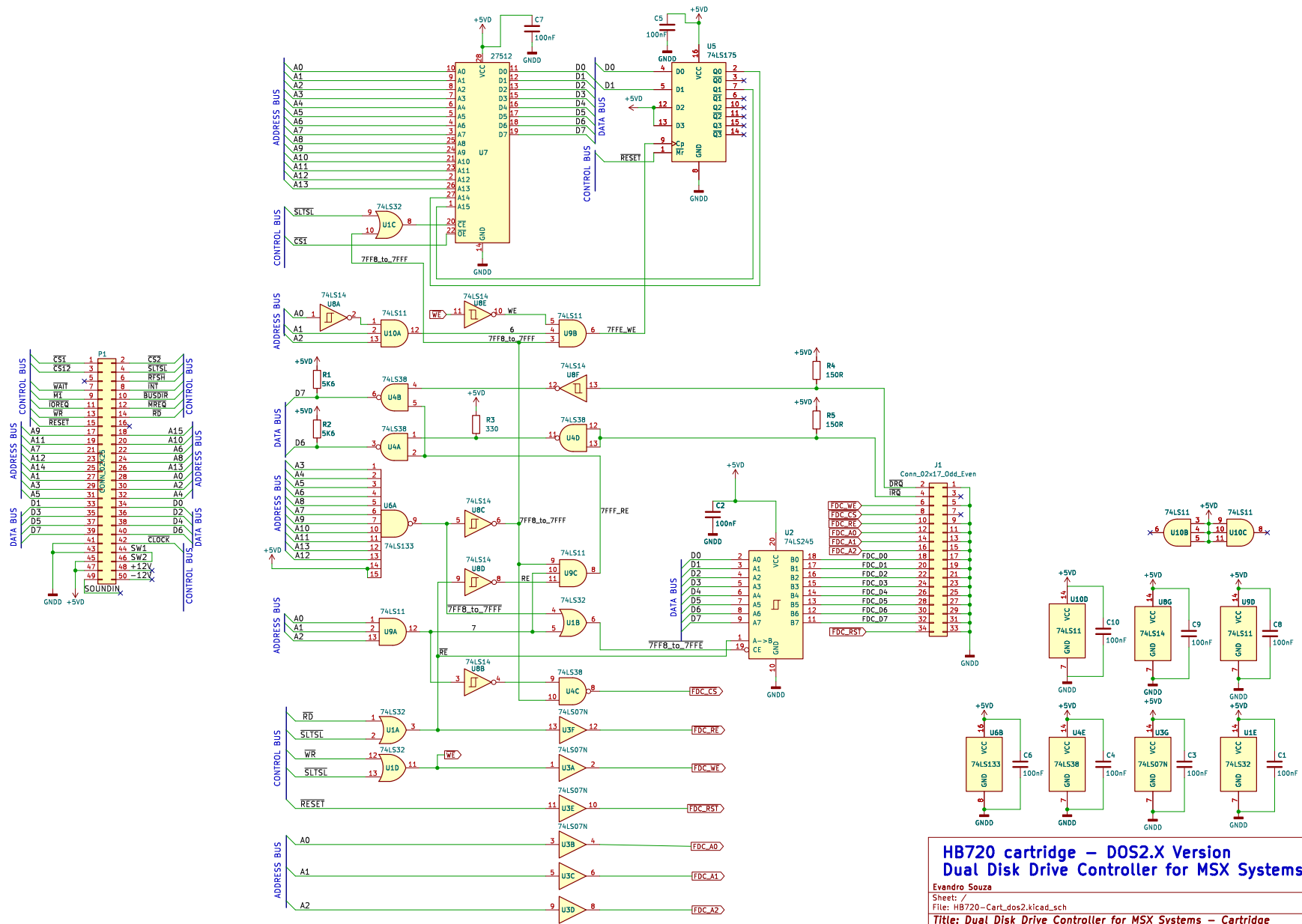Resistors: ohm

4. HB720 Boards

4.1. CARTRIDGE BOARD – DOS 2.X Model - PRINTED CIRCUIT BOARD & SCHEMATICS

HB720 cartridge – DOS2.X Version
Dual Disk Drive Controller for MSX Systems

Evandro Souza
Sheet: /
File: HB720-Cart_dos2.kicad_sch
Title: Dual Disk Drive Controller for MSX Systems – Cartridge

Size: A3	Date: 2024, Jan, 13	Rev: V1.00
KiCad E.D.A. kicad 7.0.9		Id: 1/1

4.2.   FDC Board - PRINTED CIRCUIT BOARD & SCHEMATICS

Dual Disk Drive Controller for MSX Systems
HB-3600 & HDB-50 compatible – FDC Board
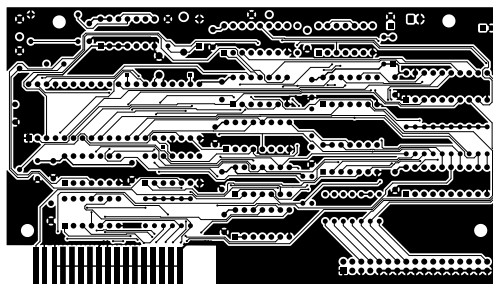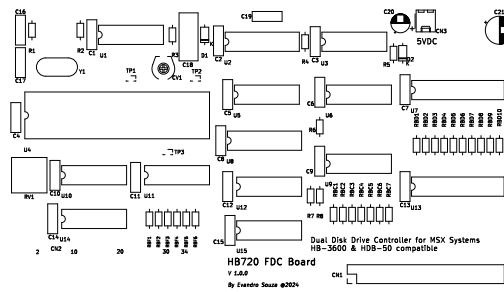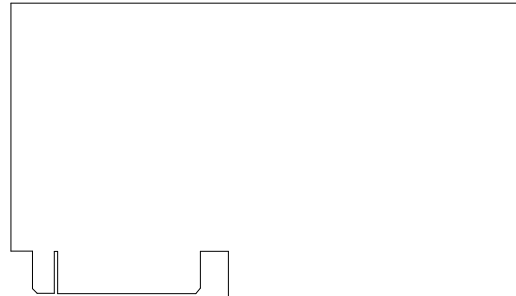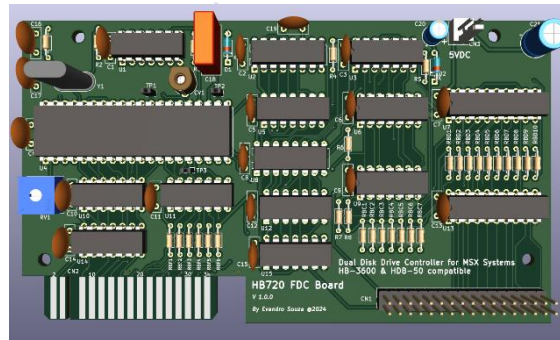
Evandro Souza
Sheet: /
File: HB-3600_FDC.kicad_sch

Title: Dual Disk Drive Controller for MSX Systems – FDC Board
Size: A3 | Date: 2024/Jan/05 | Rev: V1.00
KiCad E.D.A. kicad 7.0.9 | Id: 1/1

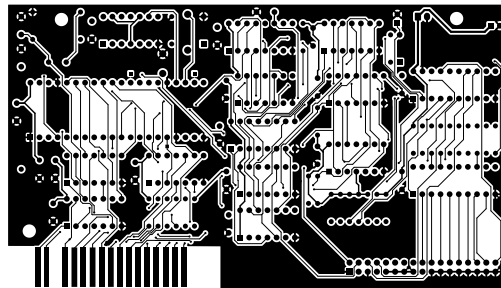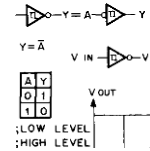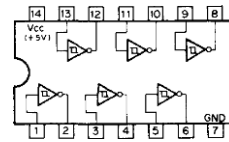# 5. SEMICONDUCTOR PIN ASSIGNMENTS

MB74LS04 (FUJITSU)
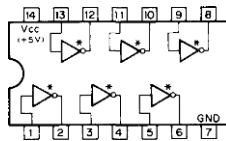SN74LS04N ^TI) TTL
INVERTER — TOP VIEW
—

0; LOW LEVEL
UHIGH LEVEL

MB74LS14 (FUJITSU)
SN74LS14N (TI)
TTL SCHMITT TRIGGER INVERTER
— TOP VIEW —

$Y = A$
$Y = \overline{A}$
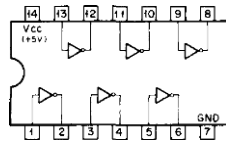
A	Y
0	1
1	0

; LOW LEVEL
; HIGH LEVEL

------- »V IN
SN7414N ......0.9 1.7 V
SN74LS14N--0.8 1.6V

M532O6P (MITSUBISHI)
SN74O6N (TI)
TTL INVERTER BUFFER/DRIVER WITH OPEN-
COLLECTOR — TOP VIEW —

$Y = A$

O;LOW LEVEL
1 ; HIGH LEVEL
*;OPEN COLLECTOR

MB74LS32 (FUJITSU)
SN74LS32N (TI)
TTL 2-INPUT POSITIVE-OR GATE
— TOP VIEW —

$Y = A + B = \overline{\overline{A} \cdot \overline{B}}$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

0:LOW LEVEL
1:HIGH LEVEL
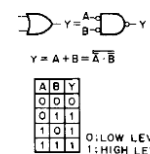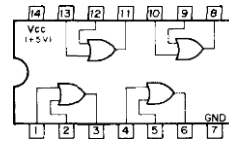
SN74O7N (TI)
TTL BUFFER/DRIVER WITH OPEN-COLLECTOR
— TOP VIEW —
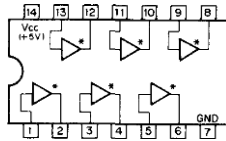
$Y = A$

0 LOW LEVEL
1 ; HIGH LEVEL
* ; OPEN COLLECTOR

MB74LS38 (FUJITSU)
SN7438N (TI)
SN74LS38N (TI)
TTL 2-INPUT POSITIVE-NAND GATE BUFFER
WITH OPEN-COLLECTOR — TOP VIEW —
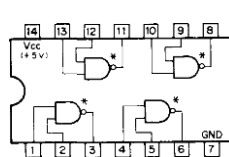
$Y=AB=A+B$

A _B Y.

0; LOW LEVEL
L£ ± 1 ; HIGH LEVEL
' H I'' * ; OPEN COLLECTOR

SN74LS10N (TI)
TTL 3-INPUT POSITIVE NAND GATE
— TOP VIEW —
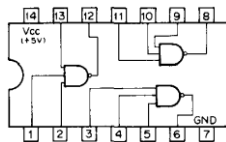
$Y = \overline{ABC} = \overline{A} + \overline{B} + \overline{C}$

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	0	0

0 : LOW LEVEL
1 : HIGH LEVEL

MB74LS74A (FUJITSU)
SN74LS74AN (TI)
TTL D-TYPE FLIP FLOP WITH DIRECT SET/RESET
— TOP VIEW —

[w] F?] [7;] H [ipl M lei
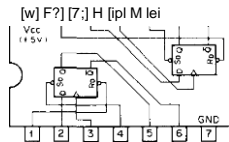
INPUTS				OUTPUTS	
S	RolC	D	Qn+1	Qn+1	
0	1	x	x	1	0
1	0	X	X	0	1
0	0	X	X	1*	1*
1	1	1		1	0
1	1	J	0	0	
1	1	0	X	On	On

0;LOW LEVEL 1 ;
HIGH LEVEL X;
DON'T CARE 1*;
NONSTABLE

HB720 Dual Disk Drive Controller

SN74LS133N (TI)
TTL 13-INPUT NAND GATE

— TOP VIEW —

Y = A̅B̅C̅D̅E̅F̅G̅H̅I̅J̅K̅L̅M̅

Vcc (+5V)

GND
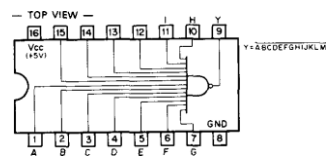
MB74LS139 (FUJITSU)
SN74LS139N (TI)
TTL 2-T0-4-LINE DECOOER/DEMULTIPLEXER

INPUTS			OUTPUTS			
EN	B	A	Y3	Y2	Y1	Y0
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1
1	X	X	1	1	1	1

0 ; LOW LEVEL
1 ; HIGH LEVEL
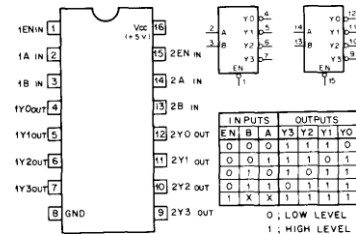
— TOP VIEW —

MB74LS1 75 (FUJITSU)
SN74LS175N (TI)
TTL O-TYPE FLIP-FLOP WITH CLEAR — TOP

RD	CK	D	Q	Q̅
0	X	X	0	1
1	⌐	1	1	0
1	⌐	0	0	1
1	0	X	Q0	Q̅0

0; LOW LEVEL
1 ; HIGH LEVEL
X; DON'T CARE
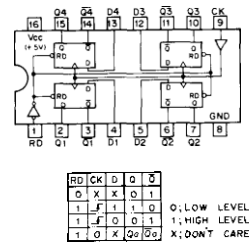
VIEW —
MB74LS244 (FUJITSU)
SN74LS244N (TI)
TTL   3-STATE   SCHMITT   TRIGGER
BUFFER/DRIVER — TOP VIEW —

G	A	Y
0	0	0
0	1	1
1	X	HI-Z

0; LOW LEVEL
1 ; HIGH LEVEL
X; DON'T CARE
HI-Z; HIGH IMPEDANCE

OR
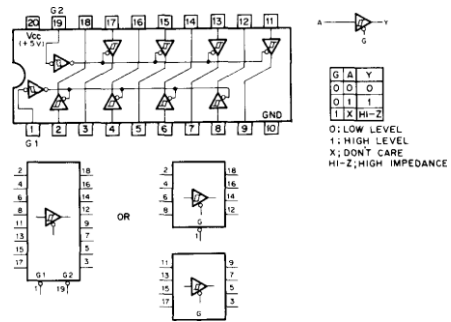
MB74LS245 (FUJITSU)
SN74LS245N (TI)
TTL BILATERAL SCHMITT TRIGGER BUS TRANSCEIVERS WITH 3-STATE
OUTPUT — TOP VIEW —

0;LOW LEVEL
1 ; HIGH LEVEL x;
DON'T CARE. HI-Z,
HIGH IMPEDANCE

HN48271 28G-25 (HITACHI) (ACCESS TIME = 250nS)
HN4827128G-30 (HITACHI) (ACCESS TIME = 300nS) HN4827128G-
45 (HITACHI) (ACCESS TIME = 450nS) N-MOS ERASABLE AND
PROGRAMMABLE ROM 128K-BIT <16384x8) — TOP VIEW —

VPP   VO
D

AI 2 E   PGM

A7 U   A13

A6 [5   A 8

AS   A 9

A4   AI 1

A3 E   OE

A2   21] A10

AI [I   g   CE

AO E   g   D7

DO Ei   06

DI   13   D5

D2 E   13   D4
       GNO <3   03

```
10  AO
9   A 1
8   A2
7   A3         D0  11
6   A4         D 1 12
5   A5         D2  13
4   A6         D3  15
3   A7         D4  16
25  A8         D5  17
24  A9         D6  18
21  A10        D7  19
2   A11
26  A12
    A13
   OE  PGM  CE
   22  27   20
```

o ;LOW LEVEL
1 ;HIGH LEVEL x
;DON'T CARE

AO ; ADDRESS INPUT
CE ; CHIP ENABLE DO-7 ;
DATA
OE I OUTPUT ENABLE PGM
; PROGRAM

HB720

WD2793-02 (WESTERN DIGITAL)
N CHANNEL E/D MOS FLOPPY DISK
FORMATTER/CONTROLLER — TOP VIEW —

ENP £   HLT

WE E   IRQ

CS E   38] DRQ

RE E   53   ODEN

AO E   E)   WP RT

AI E   35] 7P

DAL O □   TROO

DALI E   WPW

0AL2 E   3   READY

DAL3 E   53   WD

DAL4 E   WG

DALS E   29   TG43

DAL6 E   28   HLD

DAL7 E   RAW READ

STEP E   g   VCO

DIRC E   g   ENMF

5/8 E   24   CLK

RPW E   g   PUMP

MR E
      GND Vcc 23 22] TEST

```
7   DAL 0       READY  32
8   DAL 1     RAW READ 27
9   DAL 2       VCO    26
10  DAL 3      ENMF    25
11  DAL 4
12  DAL 5
13  DAL 6       WPW    33
14  DAL 7
                WG     30
5   AO
6   A 1         WD     31
                WPRT   36
   CS           I P    35
   WE           TROO   34
   RE           TG43   29
   MR           5/8    17
   ENP          RPW    18
   DRQ          STEP   15
   I RQ         DIRC   16
                HLD    28
                HLT    40
   ODEN         PUMP   23
                TEST   22
```

5/8   ; 5 1/4",8" SELECT
AO,1   : REGISTER SELECT LINES
CLK   ; CLOCK
CS   ; CHIP SELECT
DALO-7   JDATA ACCESS LINES DDEN
         iDOUBLE DENSITY
DIRC   '. DIRECTION
DRO   ; DATA REQUEST
ENMF   iENABLE MINI-FLOPPY
ENP   J ENABLE PRECOMP
HLD   » HEAD LOAD
HLT   i HEAD LOAD TIMING
IP   ; INDEX PULSE
IRQ   '. INTERRUPT REQUEST
MR   i MASTER RESET
RE   I READ ENABLE
RPW   ! READ PULSE WIDTH
TG43   I TRACK GREATER THAN43
TROO   : TRACK 00
VCO   : VOLTAGE-CONTROLLED OSC
WD   t WRITE DATA
WE   i WRITE ENABLE
WG   ' WRITE GATE
WPRT   1 WRITE PROTECT
WPW   t WRITE PRECOMP WIDTH

CR COMMAND REGISTER

DR ;DATA REGISTER DSR
iOATA SHIFT REGISTER SCR
SECTOR REGISTER TR '.TRACK
REGISTER STR '.STATUS
REGISTER

REGISTER SELECTION

CS	A 1	AO	RE = 0	WE = 0
1	X	X	NON	OAL = HI-Z
0	0	0	STR	C R
0	0	1	TR	TR
0	1	0	SCR	SCR
0	1	1	DR	OR

0 ;LOW LEVEL
1 I HIGH LEVEL X ; DON'T
CARE HI-Z; HIGH
IMPEDANCE