TTL and CMOS Logic Design

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Logic gates

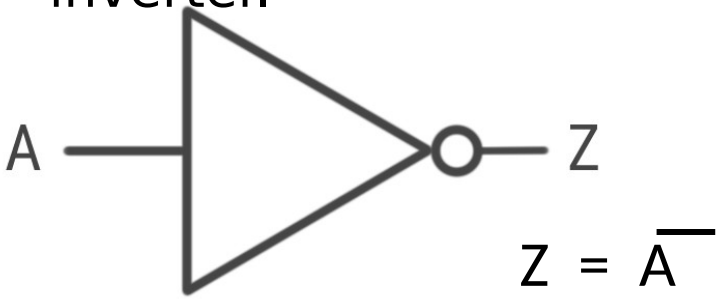
- A logic gate is the basic building block of digital circuits.
- A logic gate is an electronic circuit devices which makes a logical decision based on the different combination of inputs.

- Types of logic gates
  - NOT
  - AND
  - OR
  - NAND
  - NOR
  - Exclusive-OR (Ex-OR)
  - Exclusive-NOR (Ex-NOR)

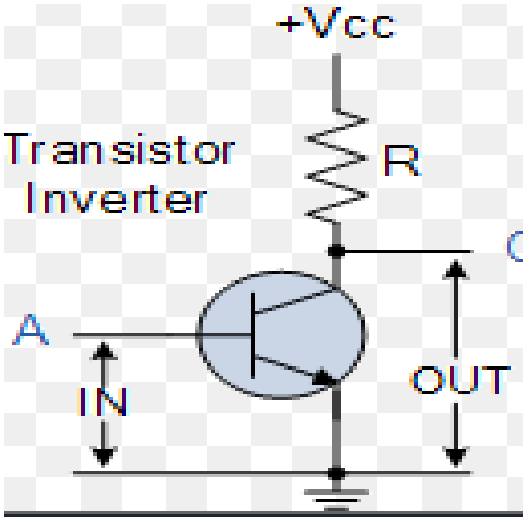
- Universal gates: NAND, NOR

NOT gate

- The NOT gate produces an inverted (complement) version of the input at its output. It is also known as an inverter.



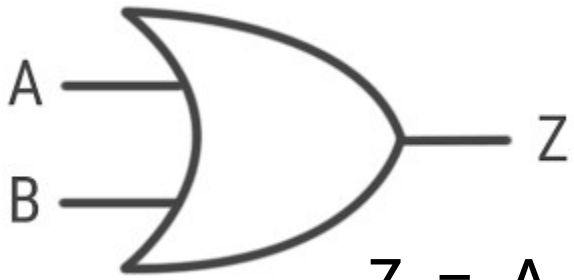
A	Z
0	1
1	0



NOT Gate using resistor

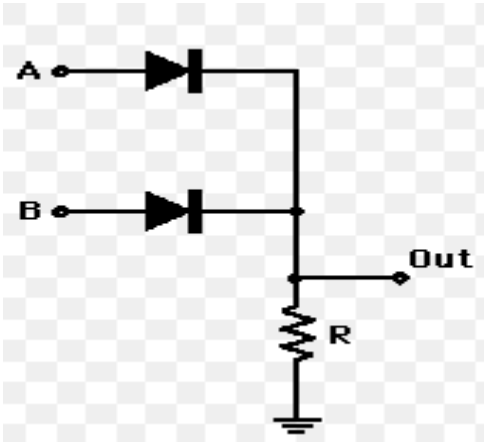
OR gate

- The OR gate gives a high output (1) if any one of its input is high. A plus (+) is used to show the OR operation.



$Z = A + B$

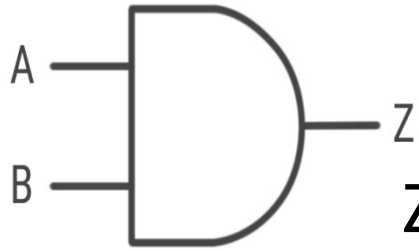
A	B	Z
0	0	0
0	1	1
1	0	1
1	1	1



OR Gate using diode

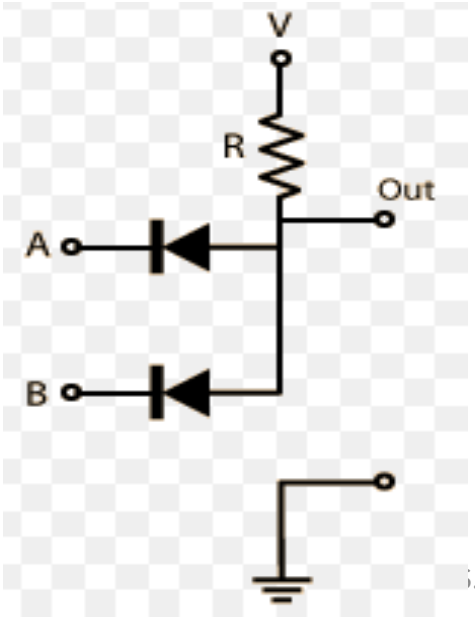
AND gate

- The AND gate gives a low output (0) if any one of its input is low. A dot (.) is used to show the AND operation.



$Z = A . B$

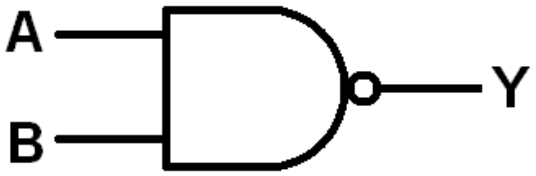
A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1



AND Gate using diode

NAND gate

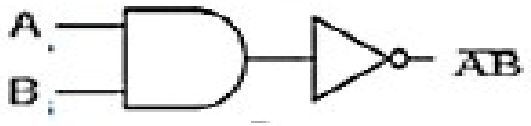
- The NAND gate gives a high output (1) if any one of its inputs is low (0). The NAND gate operation is inversion of AND gate operation.



$$Y = \overline{A \cdot B}$$

A	B	Y
0	0	1
1	0	1
0	1	1
1	1	0

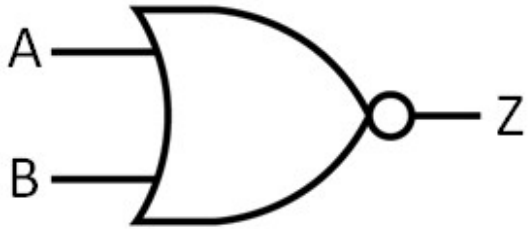
Equivalent gate circuit



NOR gate

- The NOR gate gives a low output (0) if any one of its input is high.

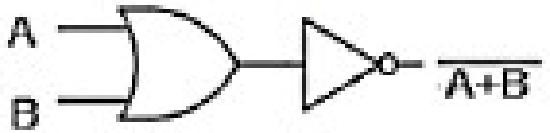
  The NOR gate operation is inversion of OR gate operation.



A	B	Z
0	0	1
1	0	0
0	1	0
1	1	0

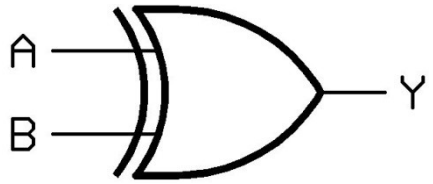
$$Z = \overline{A + B}$$

Equivalent gate circuit



EX-OR gate

- Exclusive-OR gate gives a high output (1), if the inputs are at different logic levels i.e either (0 and 1) or (1 and 0) and its output is low (0) if the inputs are at the same logic levels.
- An encircled plus sign (⊕) is used to show the XOR operation.

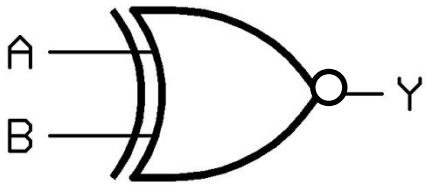


A	B	Y
0	0	0
1	0	1
0	1	1
1	1	0

$$Y = A \oplus B = A\bar{B} + \bar{A}B$$

EX-NOR gate

- The Exclusive-NOR gate gives a high (1) output only if both of its inputs are same and its output is low (0) if the inputs are at different logic levels, either (0 and 1) or (0 and 1).
- An encircled dot sign (⊙) is used to show the XNOR operation.



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

$$Y = \overline{A \odot B}$$

Digital Logic Family

- Digital logic family is referred to as a set of techniques used to implement the logic gates in the integrated circuits (IC's).

Integrated Circuits (IC)

- An IC is a small semiconductor crystal called chip, containing electronic components (transistors, diodes, resistors) that are interconnected to build a required circuit.

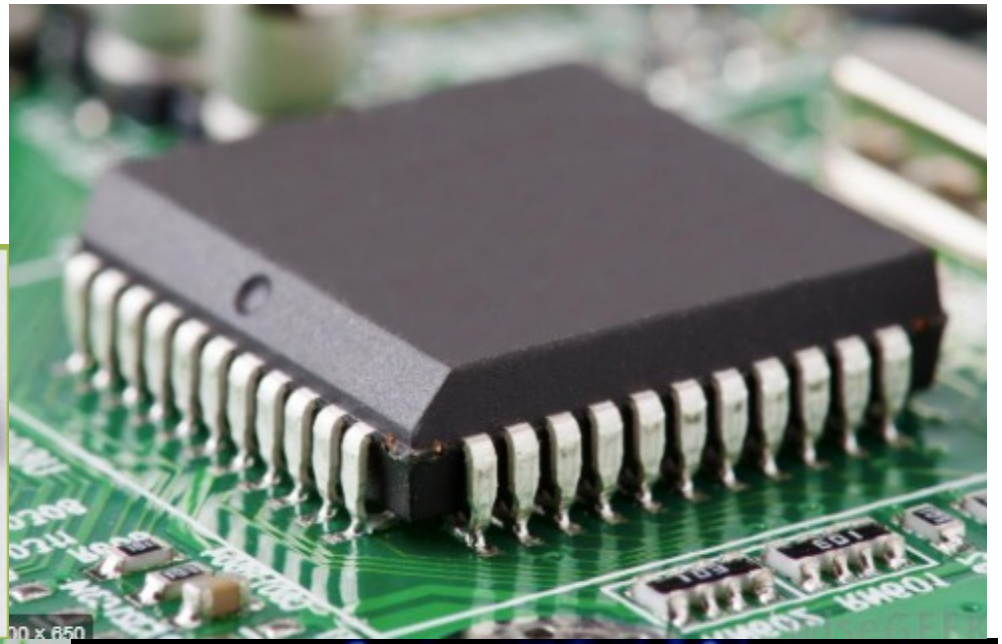
Types of IC:

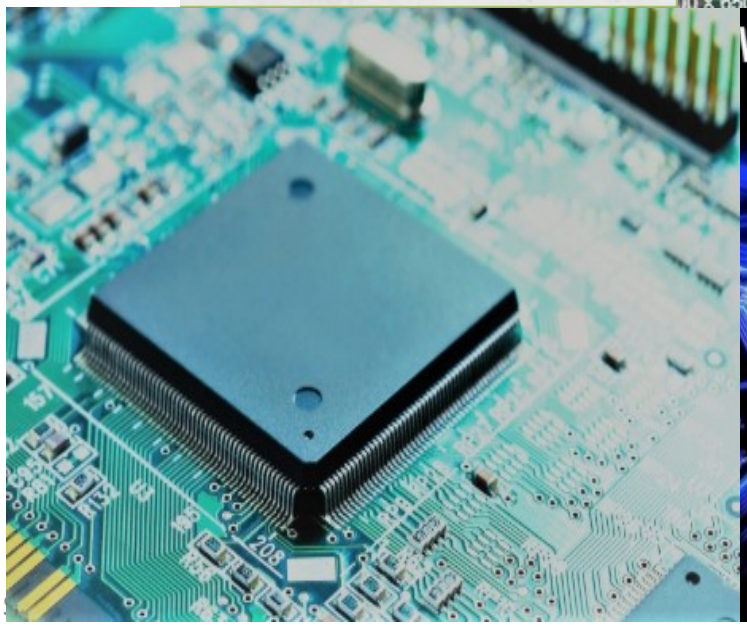
- Linear IC (Analog IC)
  - Linear ICs have continuously variable output that depends on the input signal level
- Digital IC
  - Digital ICs operate at only a few defined levels or states, rather than over a continuous range of signal.

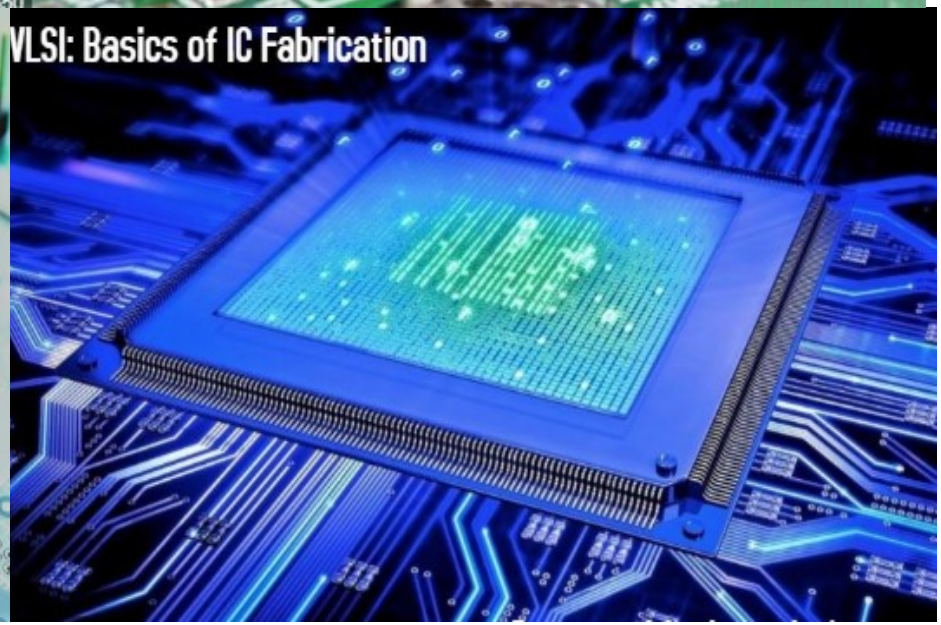
Levels of Integration

- Based on the complexity of the circuit, digital IC's are further classified as 4 basic types:
- Small Scale Integration (SSI)
  - Number of logic gates in 10's e.g. (Basic gates)
- Medium Scale Integration (MSI)
  - Number of logic gates between 10's to 100's e.g. (Decoder, Encoder, Multiplexer)
- Large Scale Integration (LSI)
  - Number of logic gates between 100's to 1000's e.g. (Third generation processors)
- Very Large Scale Integration (VLSI)
  - Number of logic gates greater than 10,000 e.g. (Digital computers, processors)


HD74LS74AP
3L26






VLSI: Basics of IC Fabrication

Characteristics of Digital ICs

- Propagation delay
- Power dissipation
- Fan in
- Fan out
- Noise Margin
- Noise immunity
- Operating temperature

Positve logic and Negative logic

Positive logic: H is set to be binary 1

Negative logic: L is set to be binary 1

Inputs		Output
x	*y*	*z*
L	*L*	*H*
L	*H*	*H*
H	*L*	*H*
H	*H*	*L*

Fig. 10-1 Positive Logic NAND Gate

Propagation delay

- The time taken for the output of a gate to change after the inputs have changed.

Average propagation delay =

- - time required for the output to go from logical 0 to logical 1 (low to high)
- - time required for the output to go from logical 1 to logical 0 (high to low)

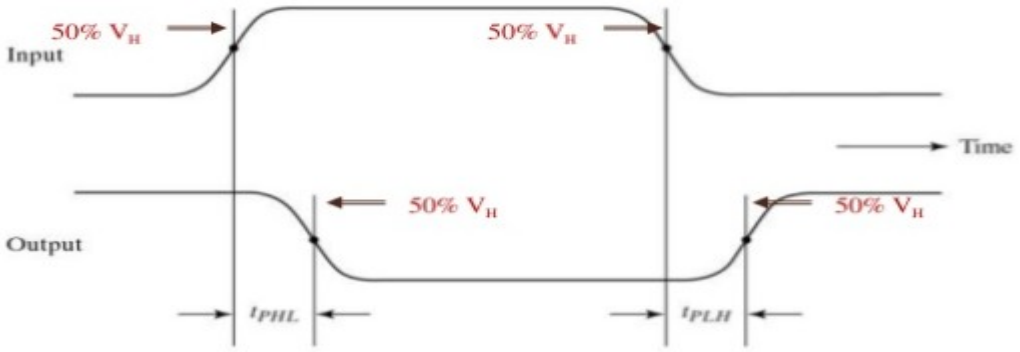


Fig. 10-4 Measurement of Propagation Delay

For standard TTL $t_{PHL} = 7ns, t_{PLH} = 11ns$

$t_P(avg) = ?$

Power dissipation

- Power consumed by the logic gates when fully driven by all its inputs.
  - It is expressed in milli-watts or nano-watts
- It is determined by the current Icc, that is drawn fr

$$I_{CC}(avg) = \frac{I_{CCH} + I_{CCL}}{2}$$

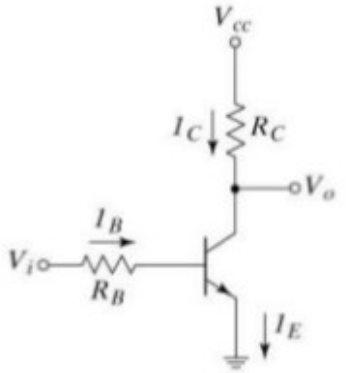
$$P_D(avg) = I_{CC}(avg) \times V_{CC}$$

For standard TTL

$$I_{CCH} = 1mA, \quad I_{CCL} = 3mA$$

$$P_D(avg) = ?$$

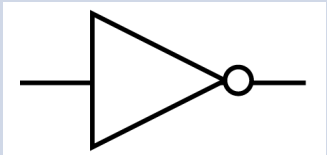
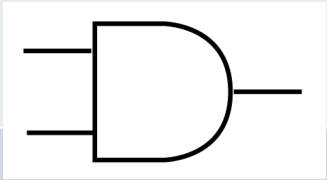
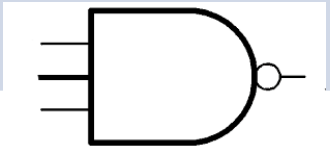
$$Total\ P_D(avg)\ in\ IC7400 = ?$$



Vcc – supply voltage of the circuit
Icc – total current drawn in the circuit

Fan in

- The maximum number of input which can be given to logic gates, without any degradation the input voltage level.

Gates	Fan in
	1
	2
	3

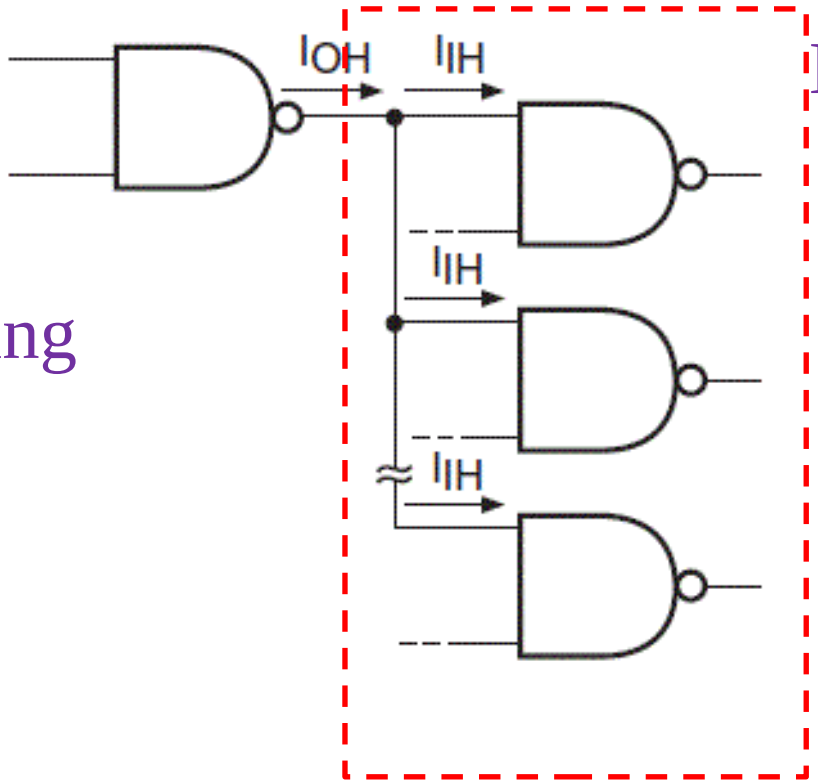
Fan out

- Fan out of a gate specifies the number of loads that can be connected to the output of the gate without degrading the voltage levels
- The driving gate must be capable of supplying certain amount of current to the load gates to maintain the required voltage level.

Definition:

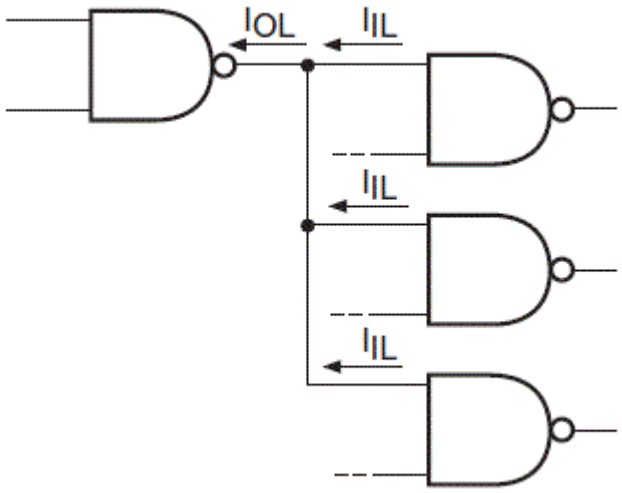
- Fan out is calculated from the amount of the current available at the output of the gate & the amount of the current needed in each input of the gate

Current sourcing logic



Fan out =

Current sinking logic



- Fan out =

Noise Margin

- Undesirable voltages induced on the connecting wires between the logical circuits
  - Ex(Glitches)
- Two noise
  - **AC Noise**
    - AC noise is caused by random pulse created by other switching signals
  - **DC Noise**
    - DC noise is caused by drift in voltage level

Noise immunity

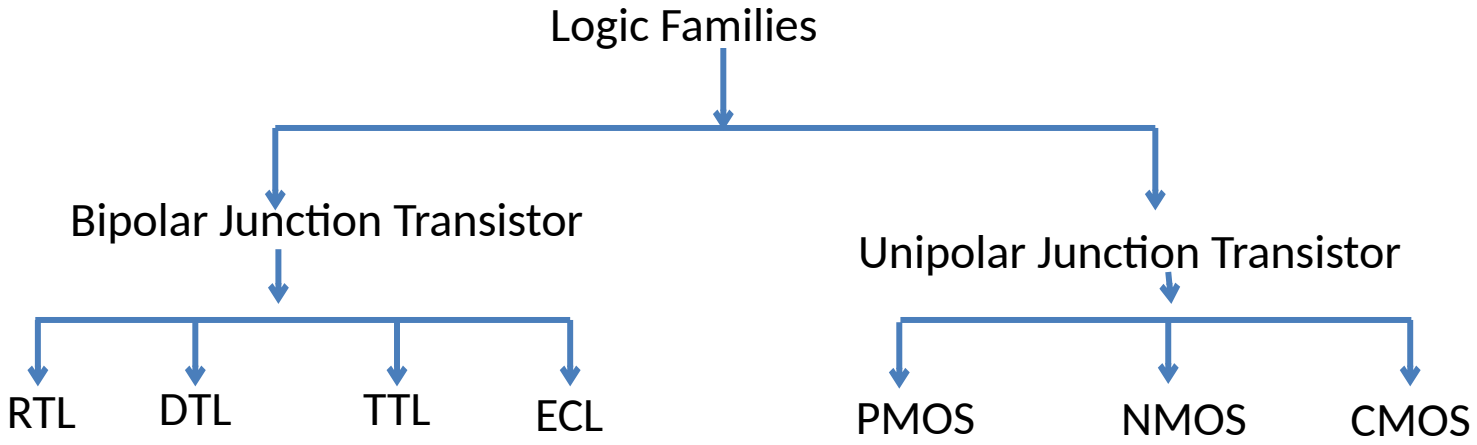
- The maximum noise voltage that may appear in the input logic gates without changing the logical state of its output.
- The quantitative measure of noise immunity is called as Noise Margin
- The difference between the operating input voltage level and threshold voltage is called as Noise Margin

Operating temperature

- ICs are semiconductor devices that are temperature sensitive by nature.
- Operating temperature ranges for an ICs
    - for consumer and Industrial applications
    - for military applications

Logic Families

- The important components of logic families are Diodes, Resistors, and Transistors, MOSFET's.



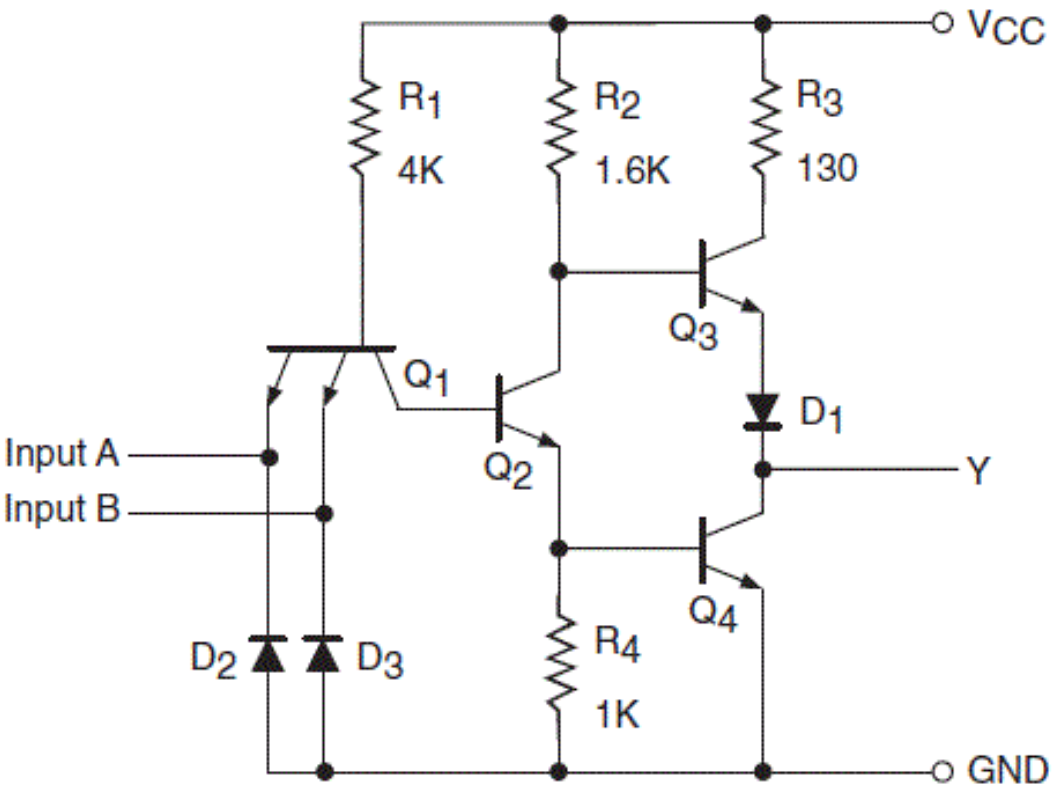
  - Resistor-Transistor Logic (RTL)
  - Diode-Transistor Logic (DTL)
  - Transistor-Transistor Logic (TTL)
  - Emitter-Coupled Logic (ECL)
  - CMOS Families

Transistor Transistor Logic (TTL)

- The full form of **TTL** is **Transistor Transistor Logic**
- This is a logic family which is mainly build up of NPN transistors, PN junction diodes and diffused resistors
- The basic building block of this logic family is NAND gate
- Subfamilies of this logic are
- Standard TTL, advanced Schottky TTL, schottky TTL, low power TTL, high power TTL, fast TTL

Transistor Transistor Logic (TTL)

- TTL NAND



Transistor Transistor Logic (TTL)

- When both inputs A and B are low, both the diodes are forward biased. So the current due to the supply voltage $+V_{CC}$ = 5 V will go to the ground through R_1 and the two diodes D_A and D_B

- The supply voltage gets dropped in the resistor R_1 and it will not be sufficient to turn ON the transistor Q_2. With Q_2 open, the transistor Q_4 will also cut off. But the transistor Q_3 is pulled high. Since Q_3 is an emitter follower, the output at the terminal will also be HIGH, which is at logic 1

- When any one input, either A or B is low, the diode with low input will be forward biased. The same operation will take place as explained above. In this case, the output will be HIGH

- When both the inputs A and B are high, both the diodes at the emitter-base junction will be reverse biased. The diode D_C at the collector-base junction is forward biased. It will turn on the transistor Q_2. With Q_2 turned ON, transistor Q_4 will also be turned ON

- Both the transistors at the output side will conduct and so the output at terminal will have LOW value, which is considered as logic 0.

Transistor Transistor Logic (TTL)

- **NOR Gate**
- Suppose input A is at logic high, the corresponding transistor's emitter-base junction is reverse biased, and base-collector junction is forward biased
- Transistor Q3 gets base current from supply voltage Vcc and goes to saturation
- As a result of the low collector voltage from Q3, transistor Q5 goes to cut off and on the other hand, if another input is low, Q4 is cut off and correspondingly Q5 is cut off and output is connected directly to the ground through transistor Q3
- Similarly, when both inputs are logic low, the output will be at logic high.

Transistor Transistor Logic (TTL)

- **NOR Gate**

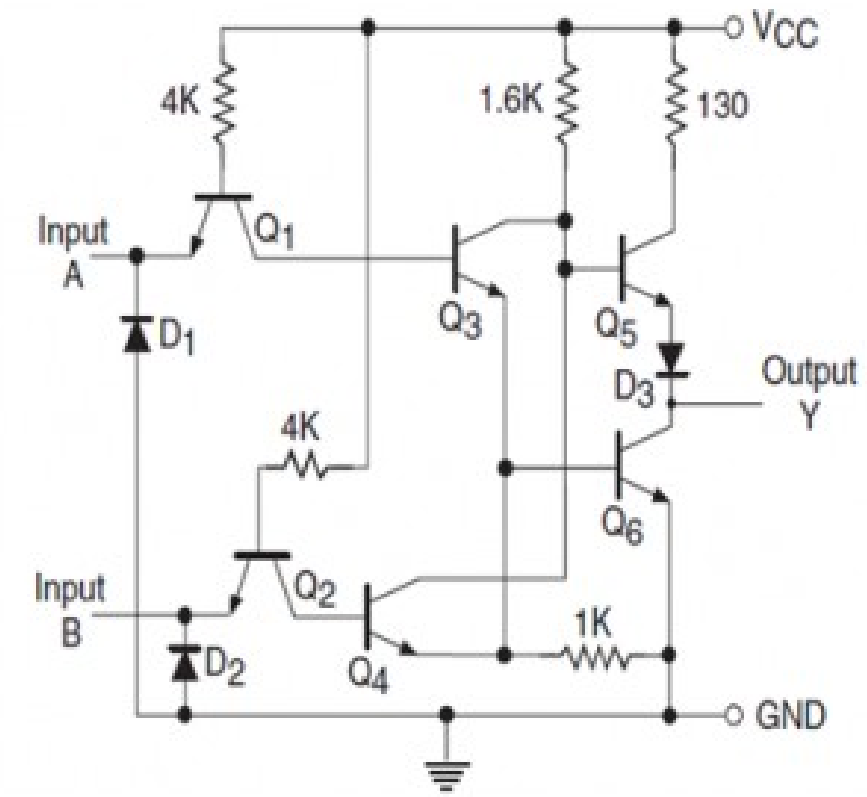
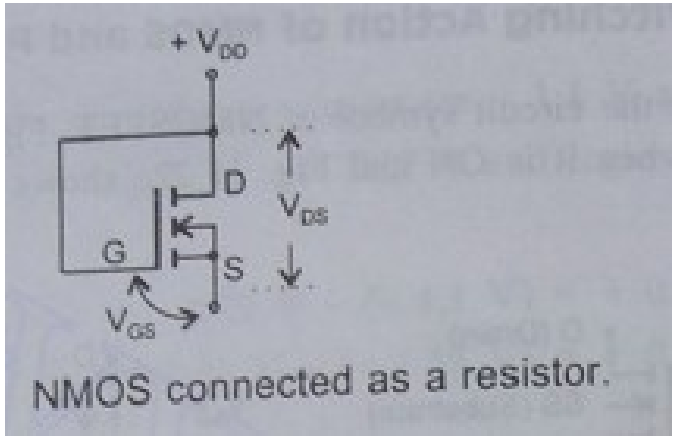


Table 11.1 Comparison of logic families

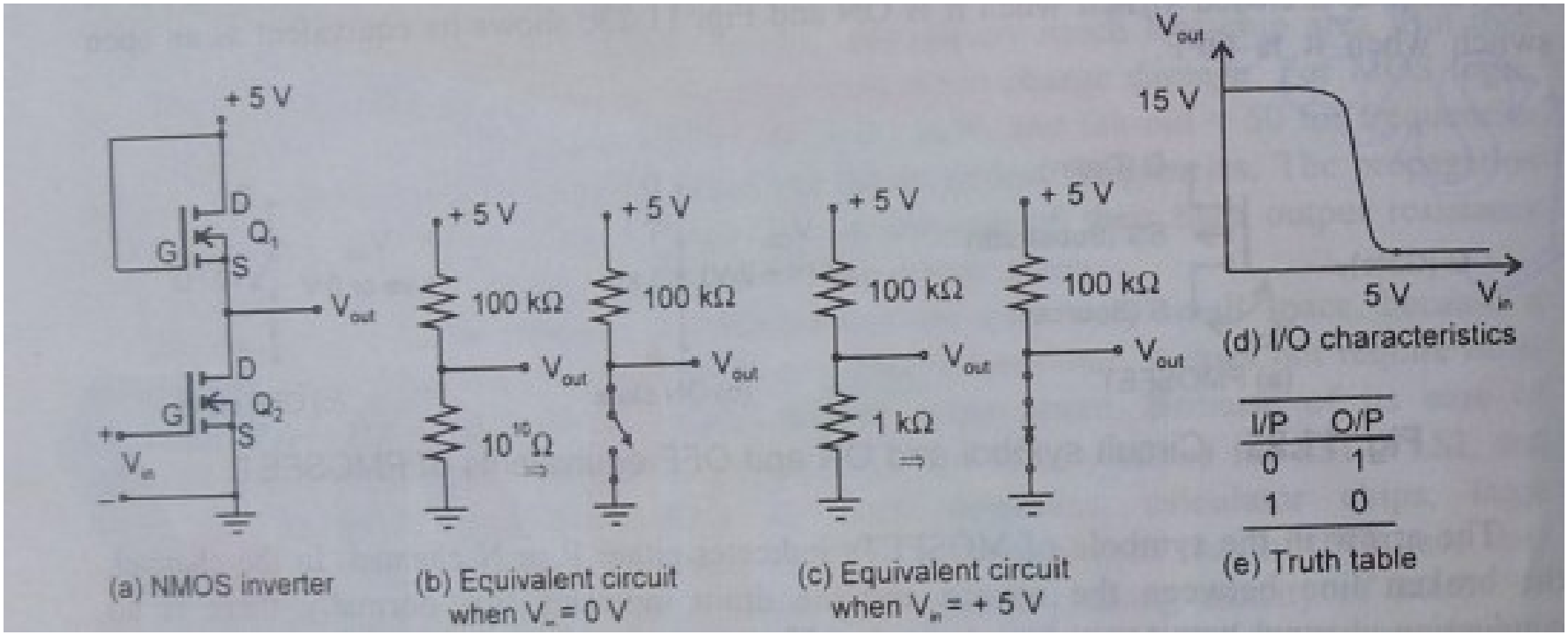
Logic family	Propagation delay time (ns)	Power dissipation per gate (mW)	Noise margin (V)	Fan-in	Fan-out	Cost
TTL	9	10	0.4	8	10	Low
ECL	1	50	0.25	5	10	High
MOS	50	0.1	1.5		10	Low
CMOS	< 50	0.01	5	10	50	Low
IIL	1	0.1	0.35	5	8	Very low



NMOS connected as a resistor.

NMOS Inverter

Q1= Load MOSFET
Q2=Switch MOSFET



(a) NMOS inverter

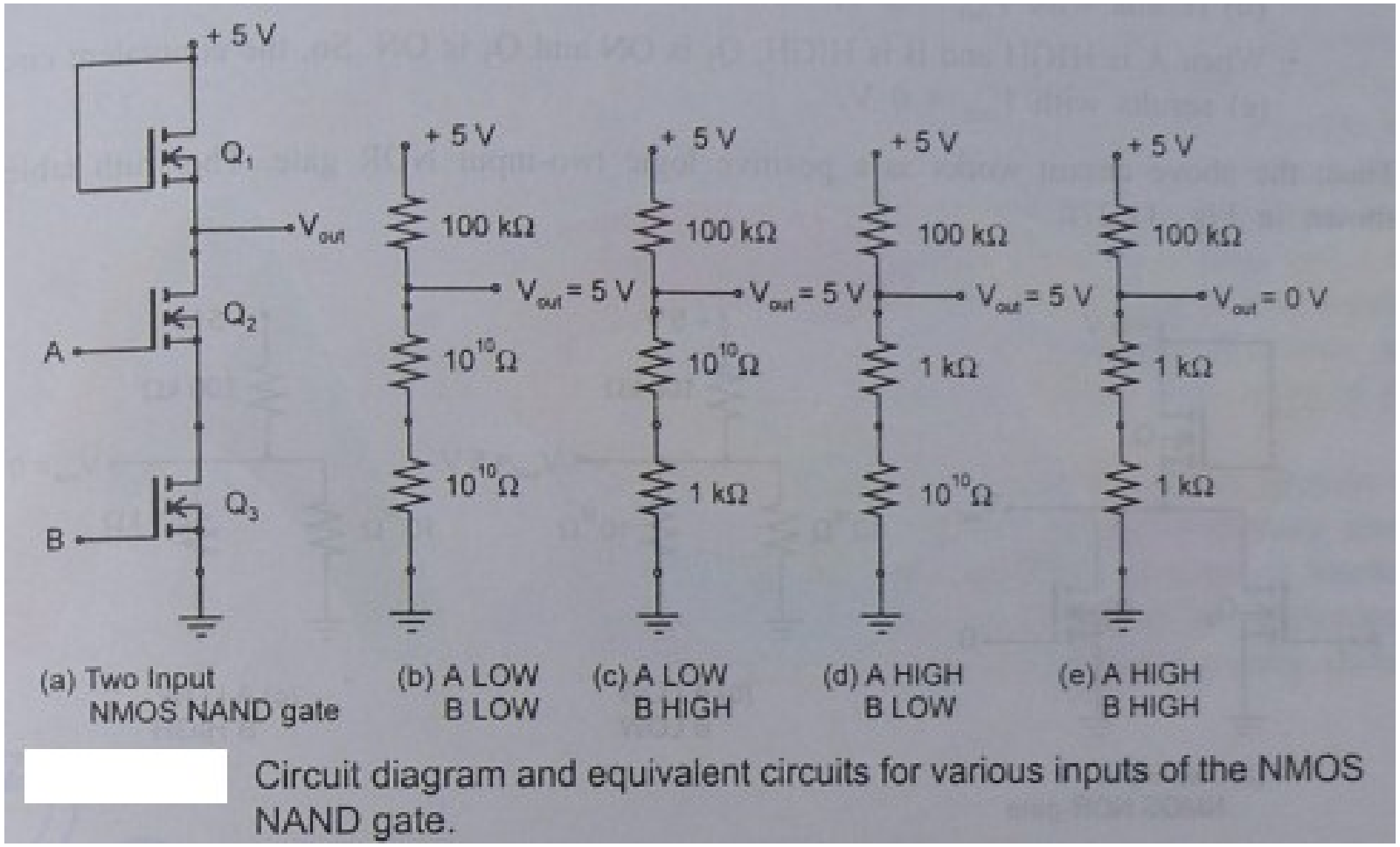
(b) Equivalent circuit when V_{in} = 0 V

(c) Equivalent circuit when V_{in} = + 5 V

(d) I/O characteristics

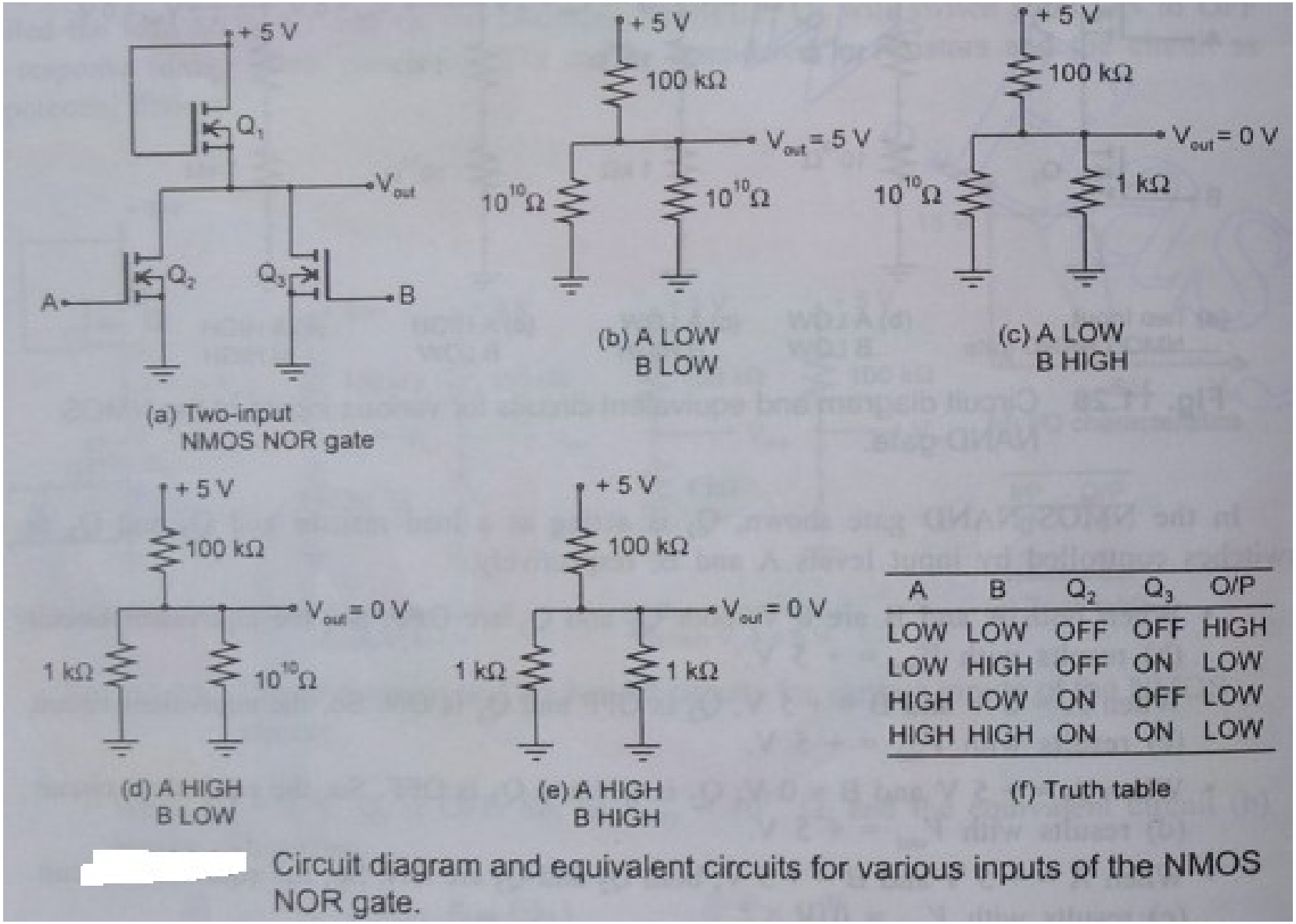
(e) Truth table

NMOS NAND Gate



Circuit diagram and equivalent circuits for various inputs of the NMOS NAND gate.

NMOS NOR Gate



A	B	Q_2	Q_3	O/P
LOW	LOW	OFF	OFF	HIGH
LOW	HIGH	OFF	ON	LOW
HIGH	LOW	ON	OFF	LOW
HIGH	HIGH	ON	ON	LOW

(f) Truth table

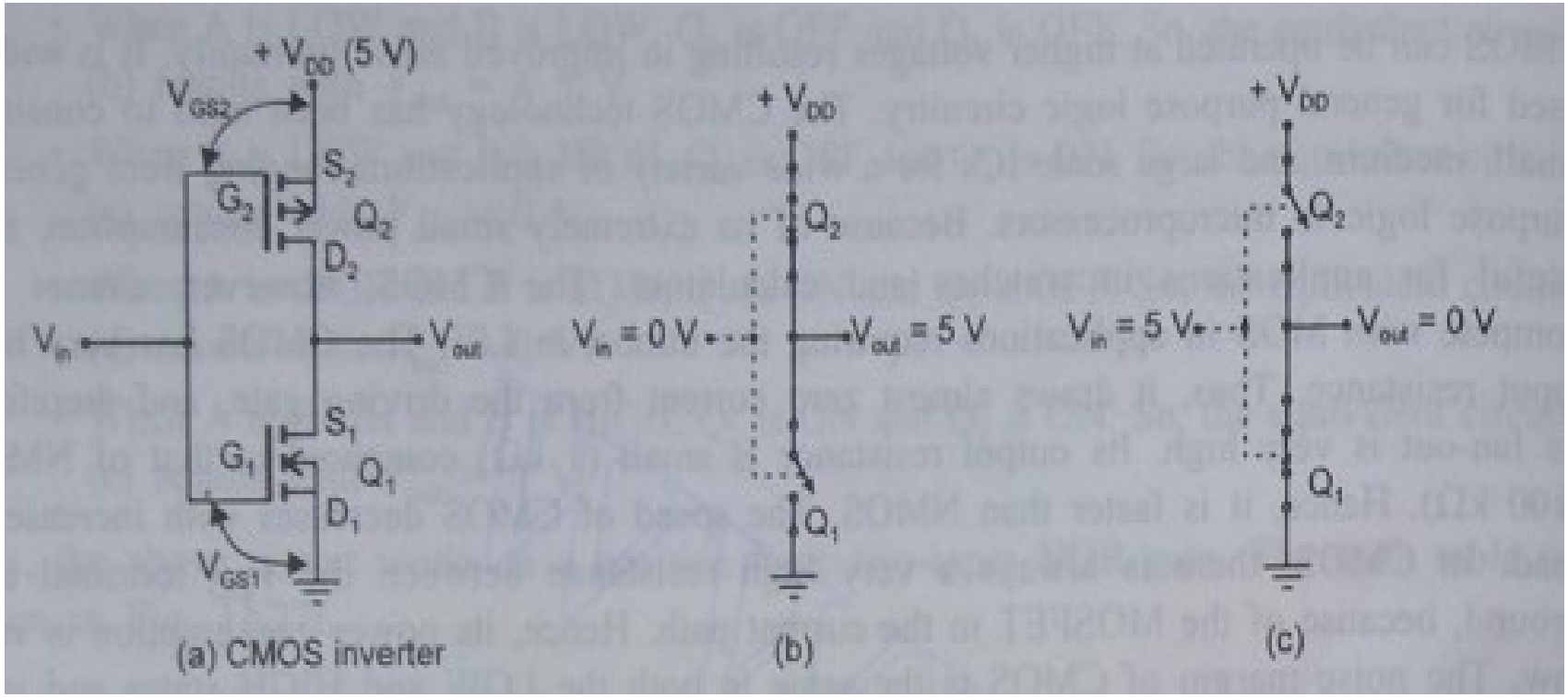
Circuit diagram and equivalent circuits for various inputs of the NMOS NOR gate.

Complementary Metal-oxide-semiconductor (CMOS)

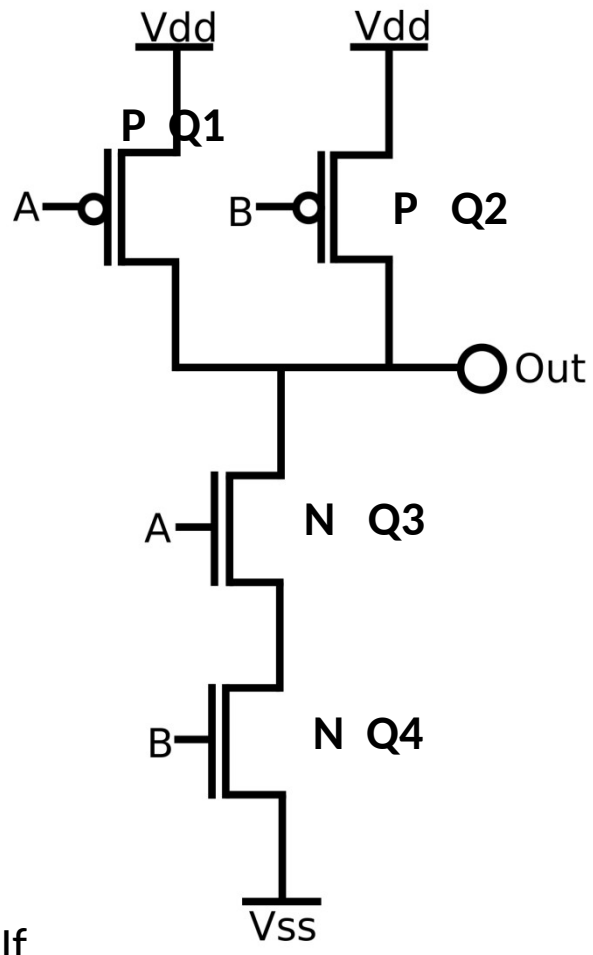
- CMOS IC's are fabricated using MOSFET (both PMOS and NMOS)
- Uses a supply voltage between 3v to 15v
- Consumes less power than TTL IC's
- Higher number of logic gates are integrated in a single IC
- Found in electronic components, including microprocessors, batteries, and digital camera image sensors
- CMOS Inverter –

A	Q1	Q2	Output
0	ON	OFF	1
1	OFF	ON	0

CMOS Inverter



CMOS NAND Gate

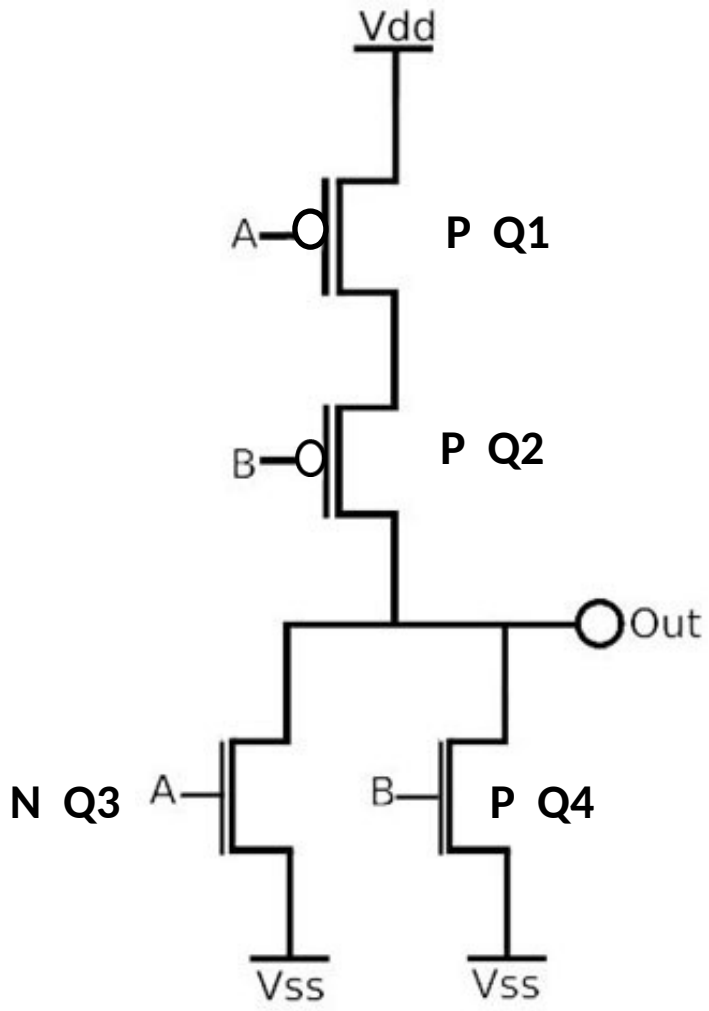


A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

If,

- A=B=1, Both P channel are OFF, Both N channel are turned ON, Out =0
- A or B=0,1, associated N channel is OFF and associated P channel is ON, Out =1
- A=B=0, Both P channel are ON, Both N channel are turned OFF, Out =1 (Vdd)

CMOS NOR Gate

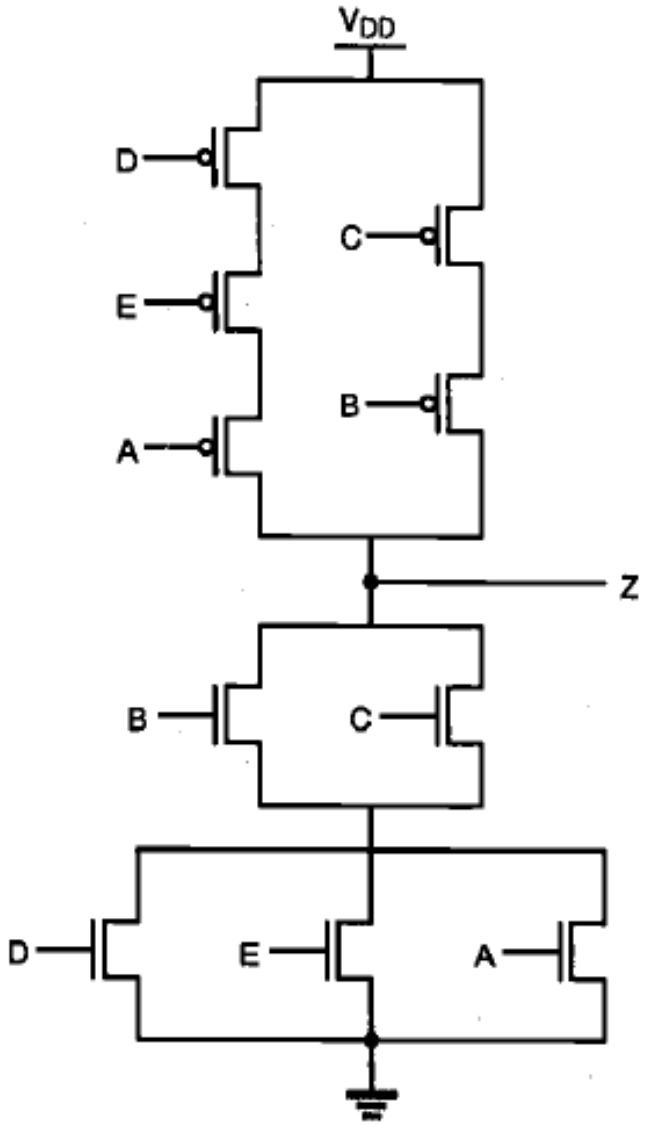


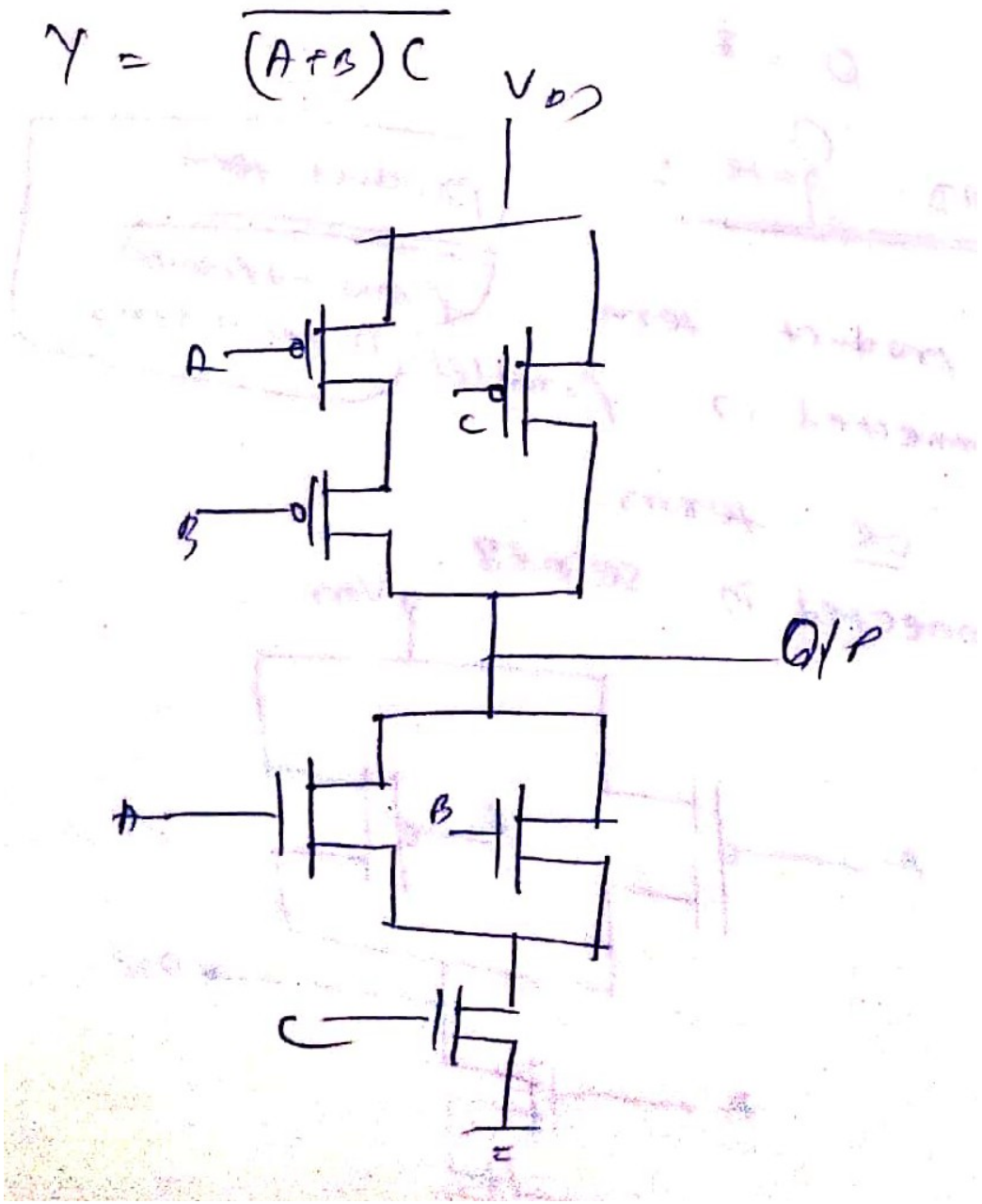
A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

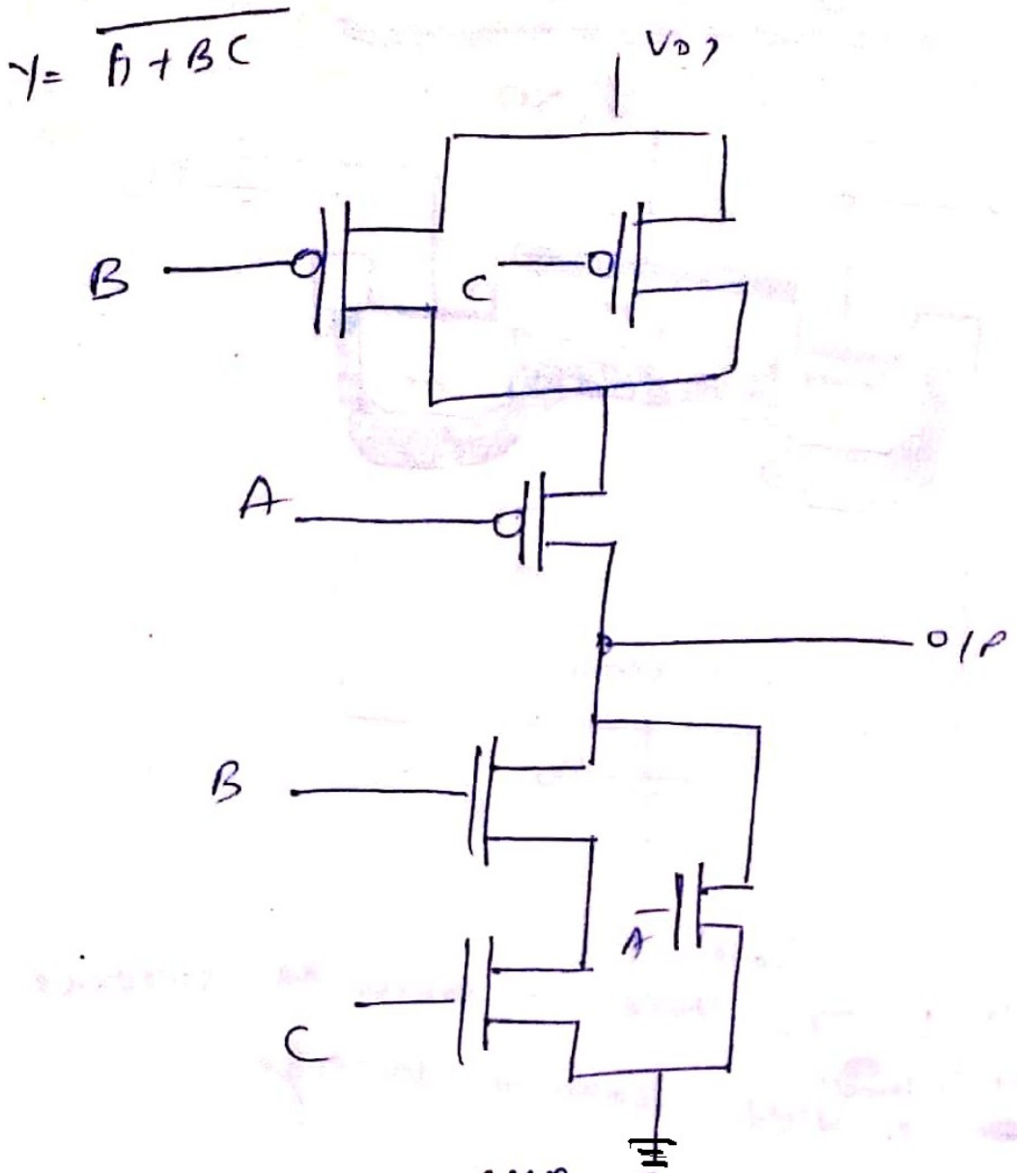
If,

- A=B=1, Both P channel are OFF, Both N channel are turned ON, Out =0
- A or B=0,1, associated N channel is ON and associated P channel is OFF, Out =0 (Vss)
- A=B=0, Both P channel are ON, Both N channel are turned OFF, Out =1 (Vdd)

$$Z = \overline{(D + E + A)(B + C)}$$




Y = $\overline{(A+B)C}$
V_{DD}
A
B
C
O/P
A
B
C


Y = $\overline{A + BC}$
VDD
B
C
A
O/P
B
A
C

Thank you