Hello!

I do not have a cover page yet. But I will implement one further down the line, as I know they are professional.

I just want to heavily note; everything here is not finalized.

As of 11/18/2025 the board was submitted for manufacturing.

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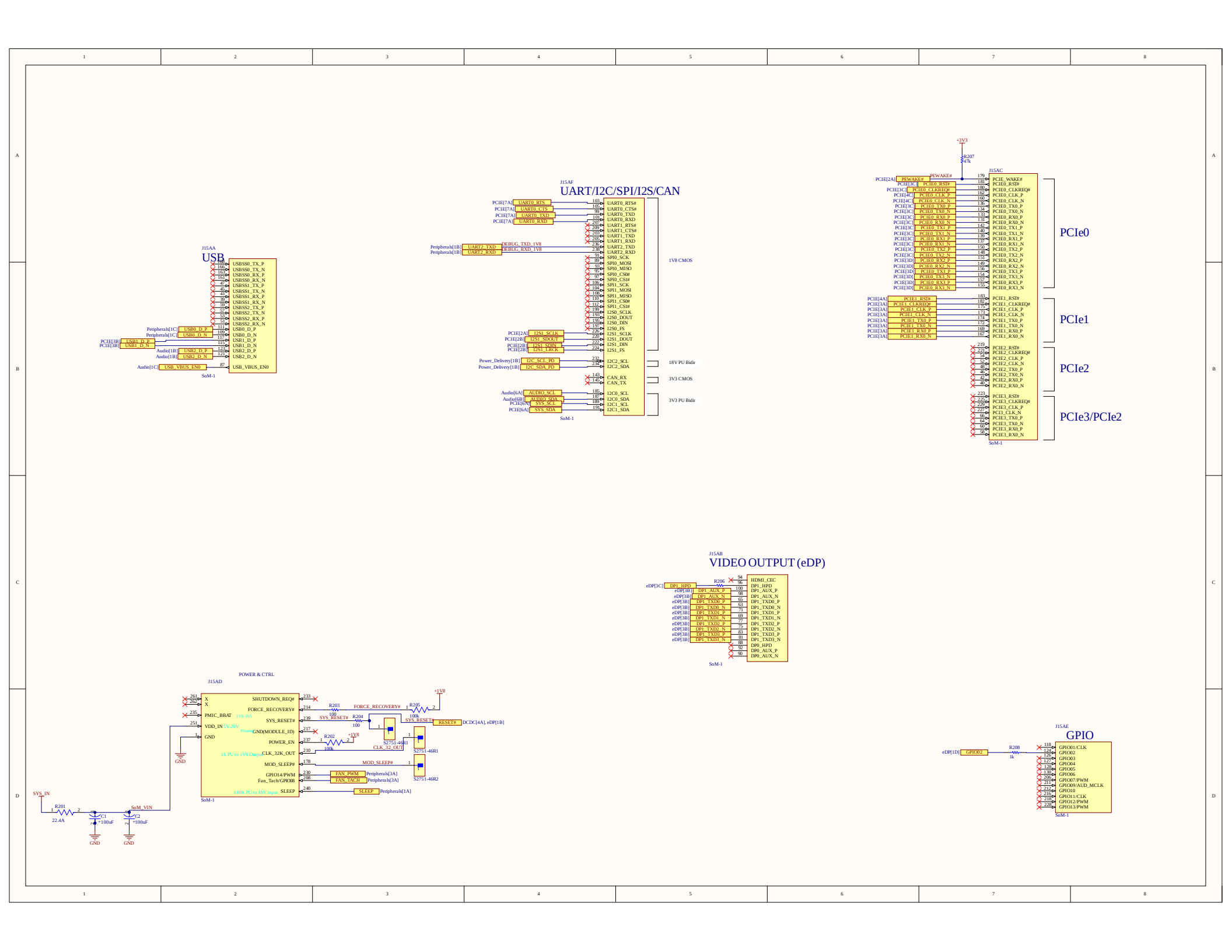
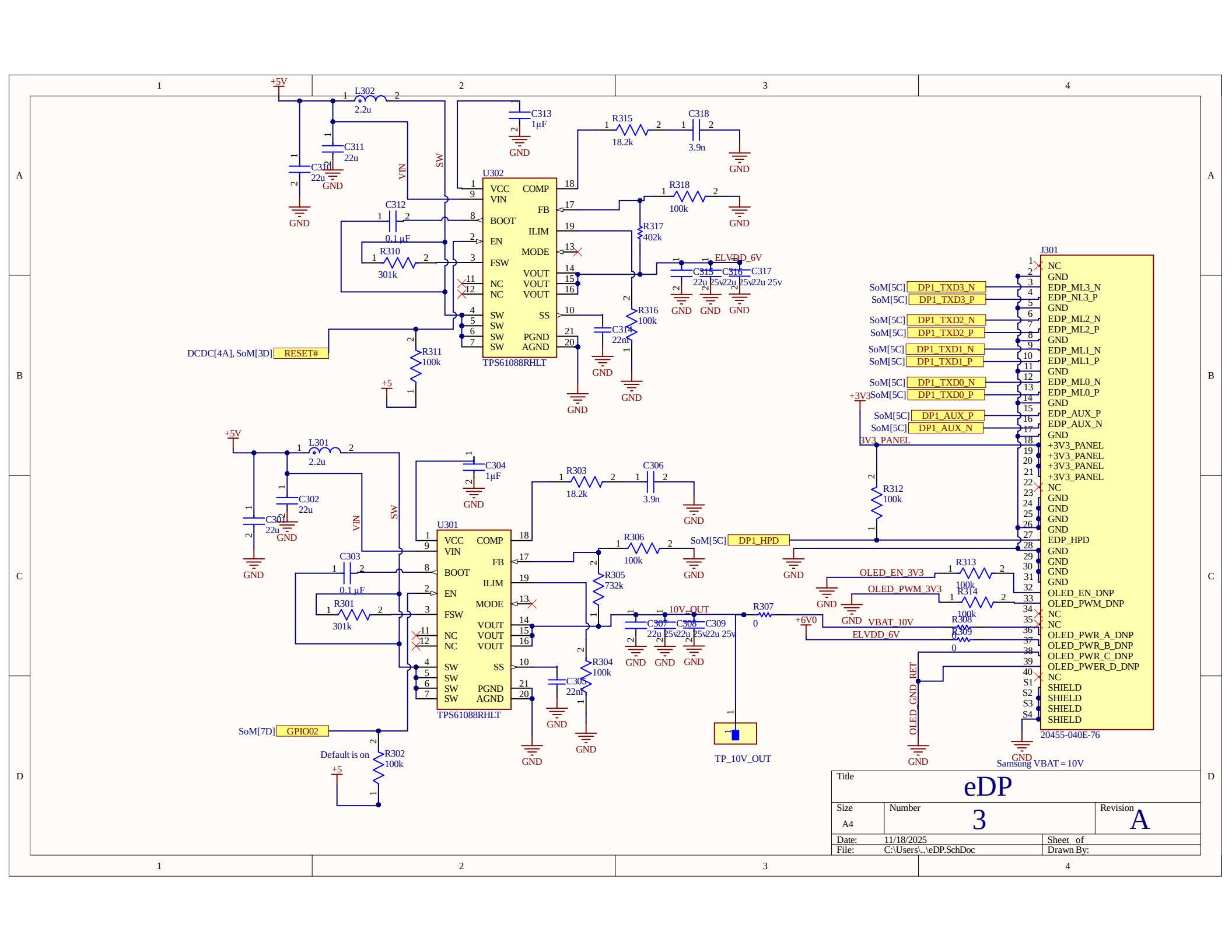
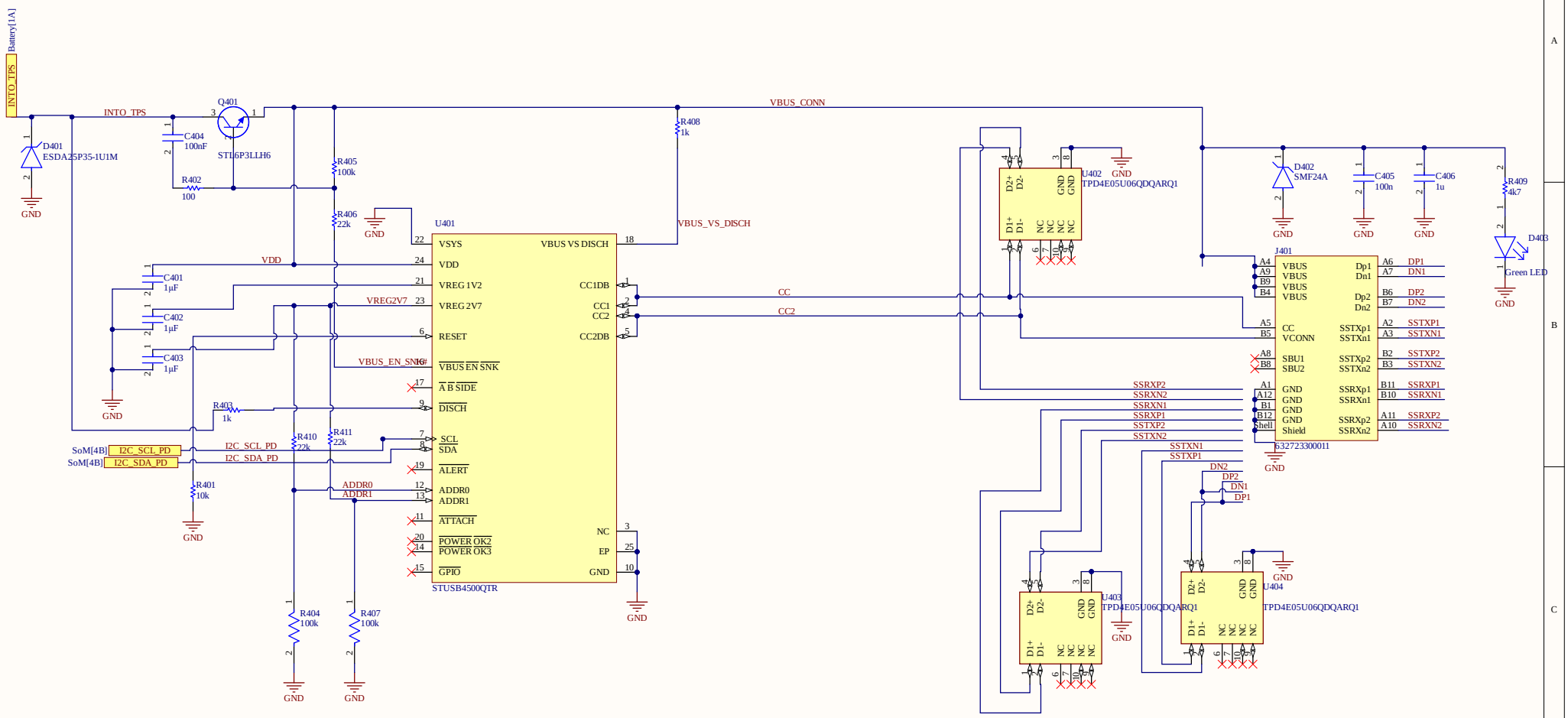
Size A	Number		Revision
Date:	11/18/2025	Sheet of	
File:	C:\Users\..\COVER PAGE.SchDoc	Drawn By:	


J15AA
USB
USBSS0_TX_P
USBSS0_TX_N
USBSS0_RX_P
USBSS0_RX_N
USBSS1_TX_P
USBSS1_TX_N
USBSS1_RX_P
USBSS1_RX_N
USBSS2_TX_P
USBSS2_TX_N
USBSS2_RX_P
USBSS2_RX_N
USB0_D_P
USB0_D_N
USB1_D_P
USB1_D_N
USB2_D_P
USB2_D_N
USB_VBUS_EN0
Peripherals[1C]
PCIE[3B]
Audio[1B]
Audio[1C]
SoM-1
J15AF
UART/I2C/SPI/I2S/CAN
UART0_RTS
UART0_CTS
UART0_TXD
UART0_RXD
UART1_RTS#
UART1_CTS#
UART1_TXD
UART1_RXD
UART2_TXD
UART2_RXD
SPI0_SCK
SPI0_MOSI
SPI0_MISO
SPI0_CS0#
SPI0_CS1#
SPI1_SCK
SPI1_MOSI
SPI1_MISO
SPI1_CS0#
SPI1_CS1#
I2S0_SCLK
I2S0_DOUT
I2S0_DIN
I2S0_FS
I2S1_SCLK
I2S1_DOUT
I2S1_DIN
I2S1_FS
I2C2_SCL
I2C2_SDA
CAN_RX
CAN_TX
I2C0_SCL
I2C0_SDA
I2C1_SCL
I2C1_SDA
DEBUG_TXD_1V8
DEBUG_RXD_1V8
1V8 CMOS
18V PU Bidir
3V3 CMOS
3V3 PU Bidir
J15AC
PCIE_WAKE#
PCIE0_RST#
PCIE0_CLKREQ#
PCIE0_CLK_P
PCIE0_CLK_N
PCIE0_TX0_P
PCIE0_TX0_N
PCIE0_RX0_P
PCIE0_RX0_N
PCIE0_TX1_P
PCIE0_TX1_N
PCIE0_RX1_P
PCIE0_RX1_N
PCIE0_TX2_P
PCIE0_TX2_N
PCIE0_RX2_P
PCIE0_RX2_N
PCIE0_TX3_P
PCIE0_TX3_N
PCIE0_RX3_P
PCIE0_RX3_N
PCIe0
PCIE1_RST#
PCIE1_CLKREQ#
PCIE1_CLK_P
PCIE1_CLK_N
PCIE1_TX0_P
PCIE1_TX0_N
PCIE1_RX0_P
PCIE1_RX0_N
PCIe1
PCIE2_RST#
PCIE2_CLKREQ#
PCIE2_CLK_P
PCIE2_CLK_N
PCIE2_TX0_P
PCIE2_TX0_N
PCIE2_RX0_P
PCIE2_RX0_N
PCIe2
PCIE3_RST#
PCIE3_CLKREQ#
PCIE3_CLK_P
PCI3_CLK_N
PCIE3_TX0_P
PCIE3_TX0_N
PCIE3_RX0_P
PCIE3_RX0_N
PCIe3/PCIe2
+3V3
R207
47k
J15AB
VIDEO OUTPUT (eDP)
DP1_HPD
DP1_AUX_P
DP1_AUX_N
DP1_TXD0_P
DP1_TXD0_N
DP1_TXD1_P
DP1_TXD1_N
DP1_TXD2_P
DP1_TXD2_N
DP1_TXD3_P
DP1_TXD3_N
DP0_HPD
DP0_AUX_P
DP0_AUX_N
HDMI_CEC
R206
POWER & CTRL
J15AD
SHUTDOWN_REQ#
FORCE_RECOVERY#
SYS_RESET#
PMIC_BBAT
VDD_IN
GND
POWER_EN
CLK_32K_OUT
MOD_SLEEP#
GPIO14/PWM
Fan_Tach/GPIO08
SLEEP
1V8/3V3
5V-20V
Floating
1k PU to 1V8 Output
100k PU to 1V8V input
R203
R204
R205
R202
100k
FORCE_RECOVERY#
SYS_RESET#
RESET#
DCDC[4A], eDP[1B]
CLK_32_OUT1
S2751-46R1
S2751-46R2
FAN_PWM
FAN_TACH
Peripherals[3A]
SLEEP
Peripherals[1A]
+1V8
SYS_IN
SoM_VIN
R201
22.4A
C1
C2
*100uF
J15AE
GPIO
GPIO01/CLK
GPIO02
GPIO03
GPIO04
GPIO05
GPIO06
GPIO07/PWM
GPIO09/AUD_MCLK
GPIO10
GPIO11/CLK
GPIO12/PWM
GPIO13/PWM
R208
1k


+5V
L302
2.2u
C313
1µF
R315
18.2k
C318
3.9n
C311
22u
C310
22u
VIN
SW
U302
VCC
VIN
BOOT
EN
FSW
NC
NC
SW
SW
SW
SW
COMP
FB
ILIM
MODE
VOUT
VOUT
VOUT
SS
PGND
AGND
TPS61088RHLT
R318
100k
C312
0.1 µF
R317
402k
R310
301k
ELVDD_6V
C315
22u 25v
C316
22u 25v
C317
22u 25v
R316
100k
C314
22nF
DCDC[4A], SoM[3D]
RESET#
R311
100k
L301
2.2u
C304
1µF
R303
18.2k
C306
3.9n
C302
22u
C301
22u
C303
0.1 µF
R301
301k
U301
R306
100k
SoM[5C]
DP1_HPD
R305
732k
10V_OUT
R307
0
C307
22u 25v
C308
22u 25v
C309
22u 25v
R304
100k
C305
22nF
+6V0
TP_10V_OUT
SoM[7D]
GPIO02
Default is on
R302
100k
R312
100k
+3V3
3V3_PANEL
J301
NC
GND
EDP_ML3_N
EDP_NL3_P
EDP_ML2_N
EDP_ML2_P
EDP_ML1_N
EDP_ML1_P
EDP_ML0_N
EDP_ML0_P
EDP_AUX_P
EDP_AUX_N
+3V3_PANEL
EDP_HPD
OLED_EN_DNP
OLED_PWM_DNP
OLED_PWR_A_DNP
OLED_PWR_B_DNP
OLED_PWR_C_DNP
OLED_PWER_D_DNP
SHIELD
20455-040E-76
DP1_TXD3_N
DP1_TXD3_P
DP1_TXD2_N
DP1_TXD2_P
DP1_TXD1_N
DP1_TXD1_P
DP1_TXD0_N
DP1_TXD0_P
DP1_AUX_P
DP1_AUX_N
OLED_EN_3V3
OLED_PWM_3V3
VBAT_10V
ELVDD_6V
OLED_GND_RET
R313
100k
R314
100k
R308
R309
0
Samsung VBAT = 10V
Title
eDP
Size
A4
Number
3
Revision
A
Date:
11/18/2025
File:
C:\Users\..\eDP.SchDoc
Sheet of
Drawn By:



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Date: 11/18/2025		Sheet of	
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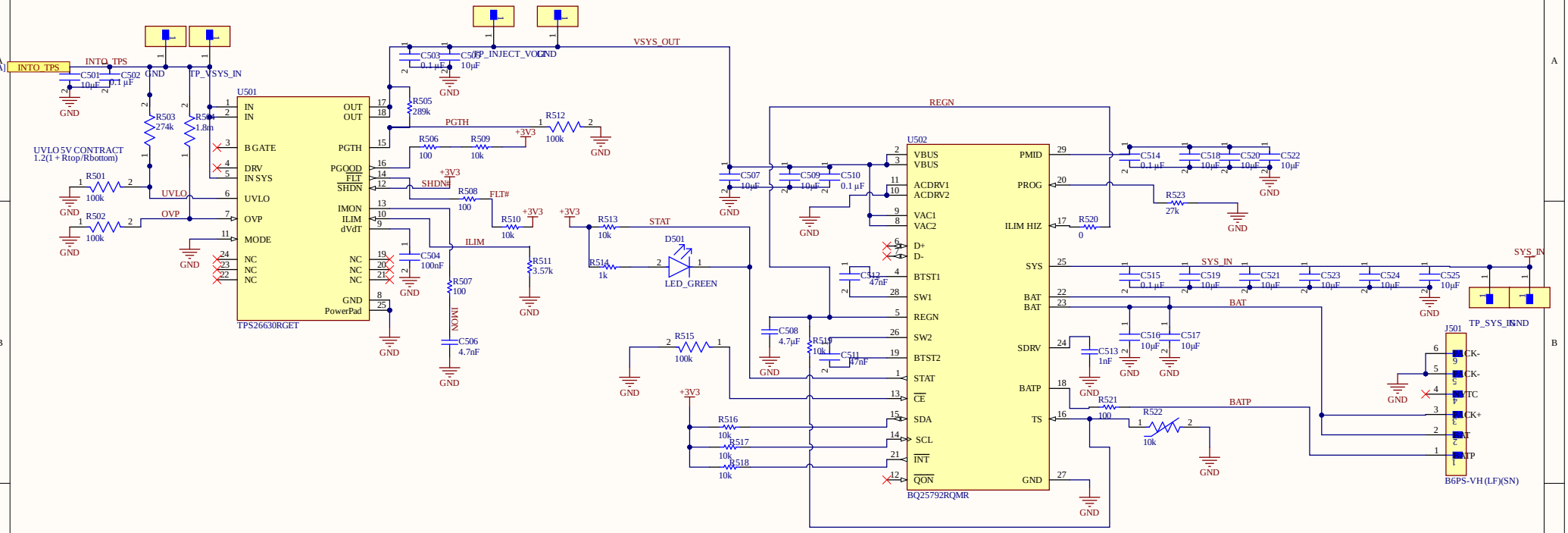

BATTERY: 4-CELL (4S2P)

Title	BATTERY		
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Date: 11/18/2025		Sheet of	
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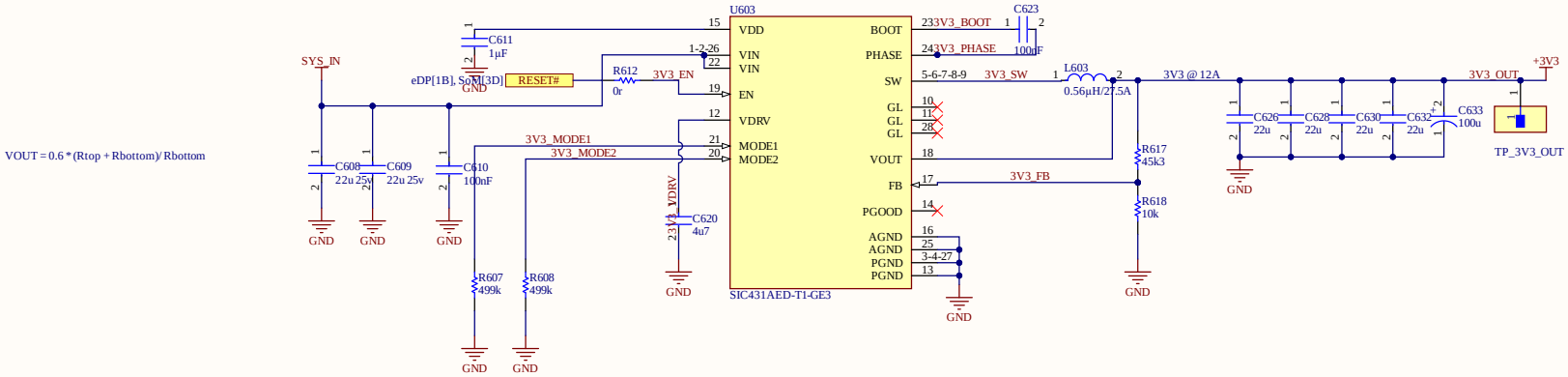
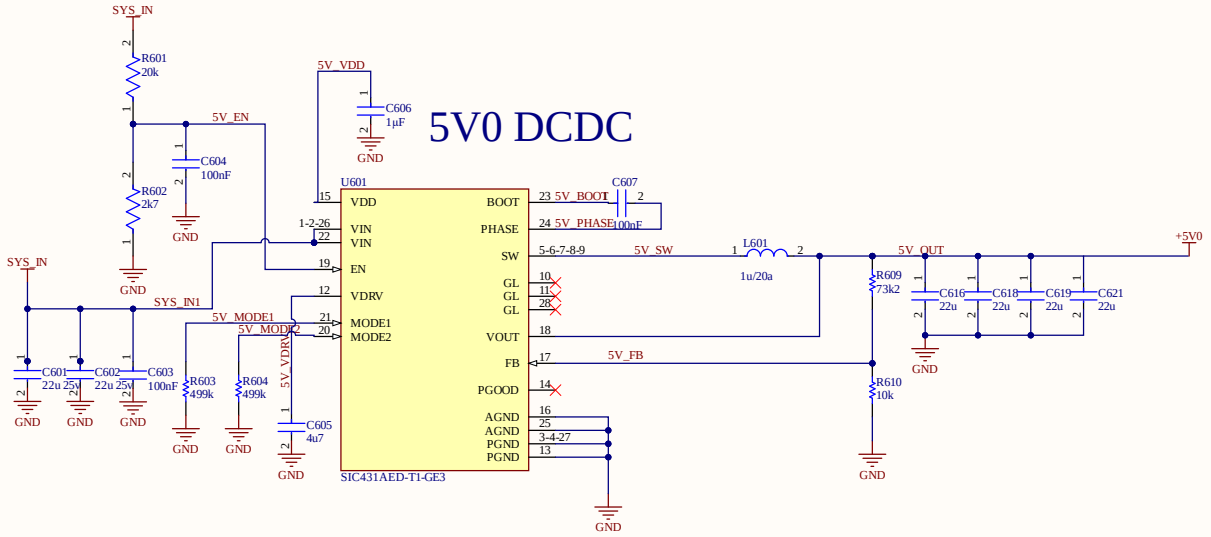
3V3 DCDC



5V0 DCDC

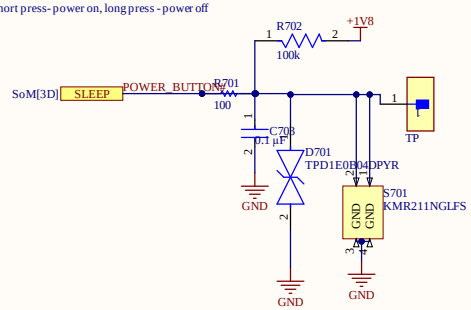


Title: DCDC Schematic		
Size: A3	Number: 6	Revision: A
Date: 11/18/2025		Sheet of
File: C:\Users\..\DCDC.SchDoc		Drawn By:

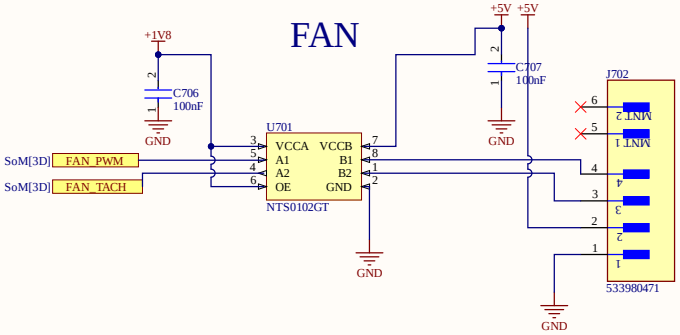
POWER ON

Power button

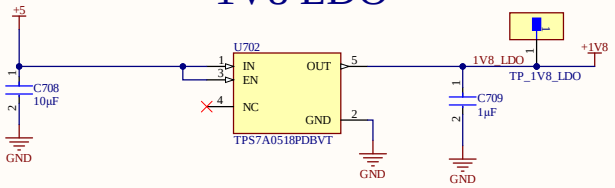
Short press- power on, long press - power off



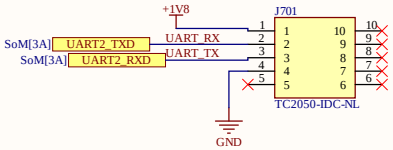
FAN



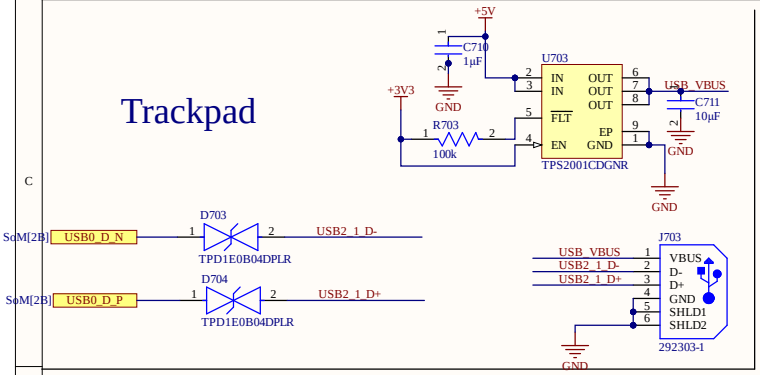
1V8 LDO



UART_DEBUGGER



Trackpad



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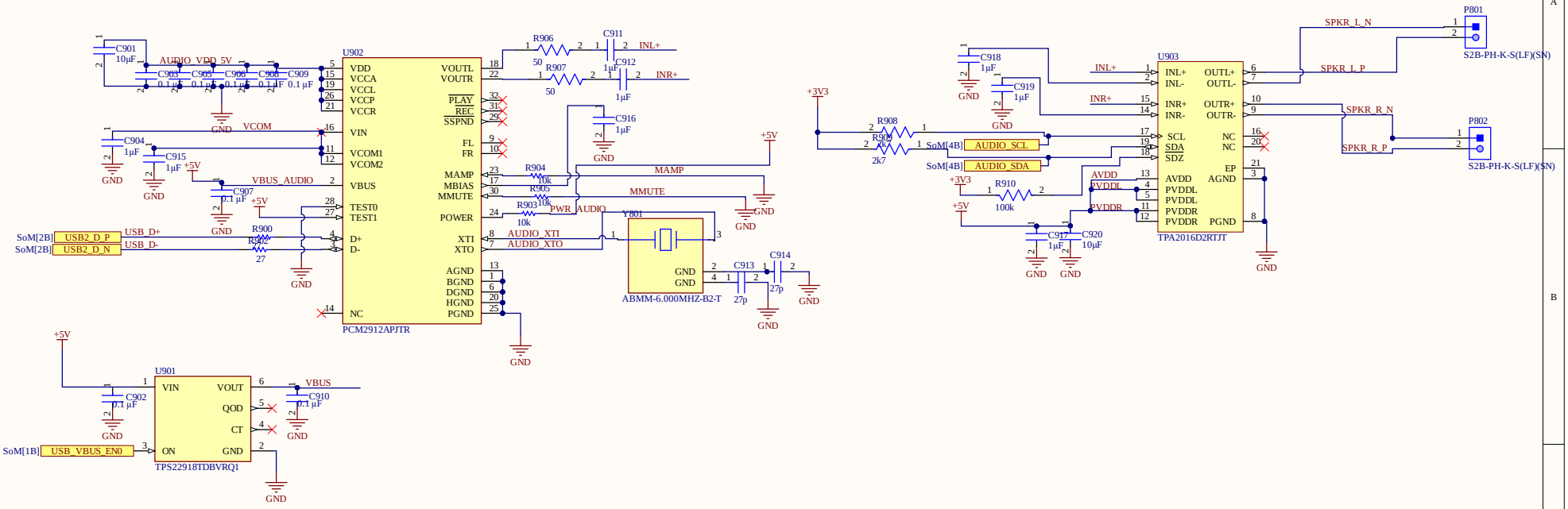
Date: 11/18/2025		Sheet of
File: C:\Users\..\Peripherals.SchDoc		Drawn By:

AUDIO



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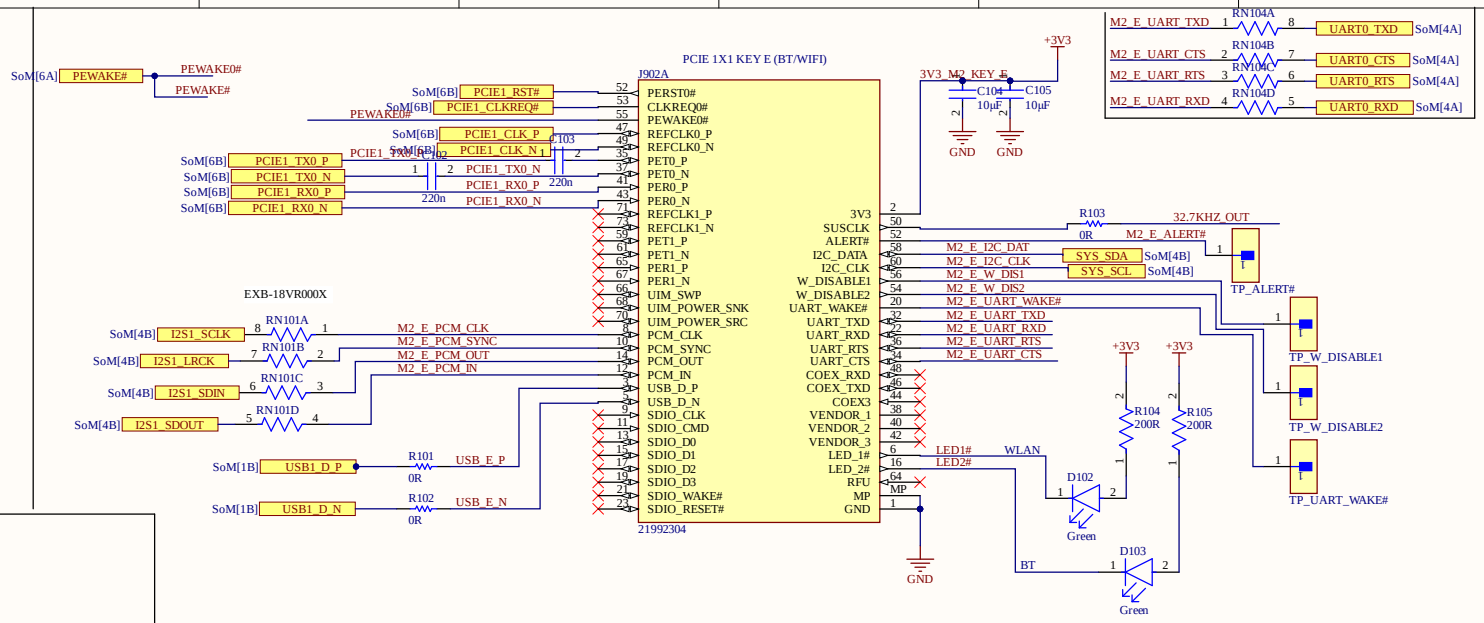
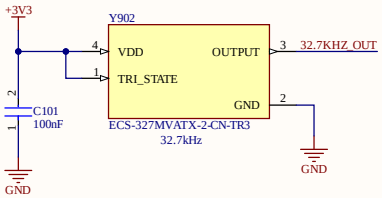
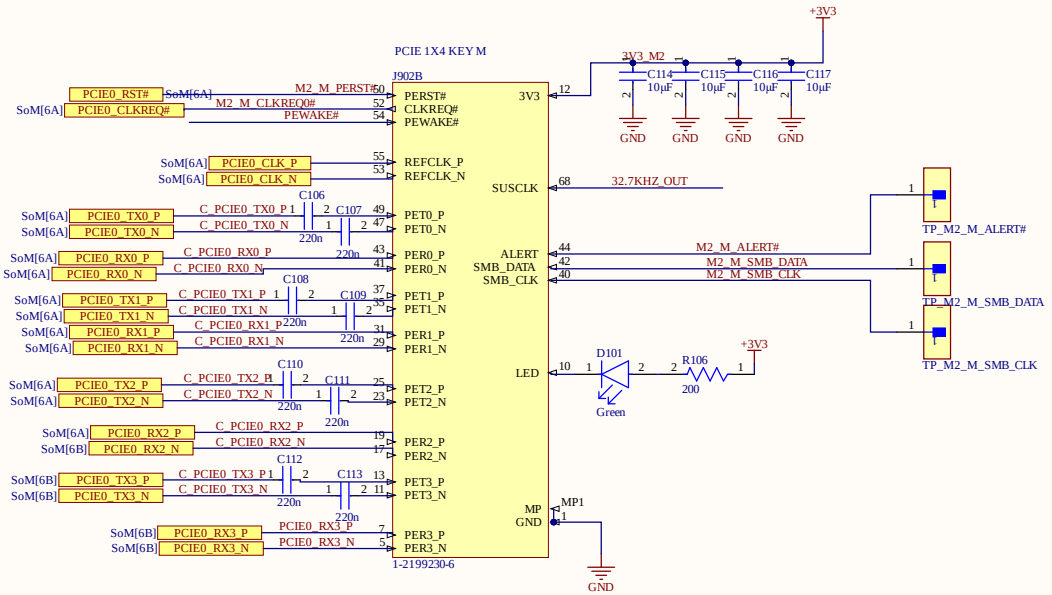


SUSCLK





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