

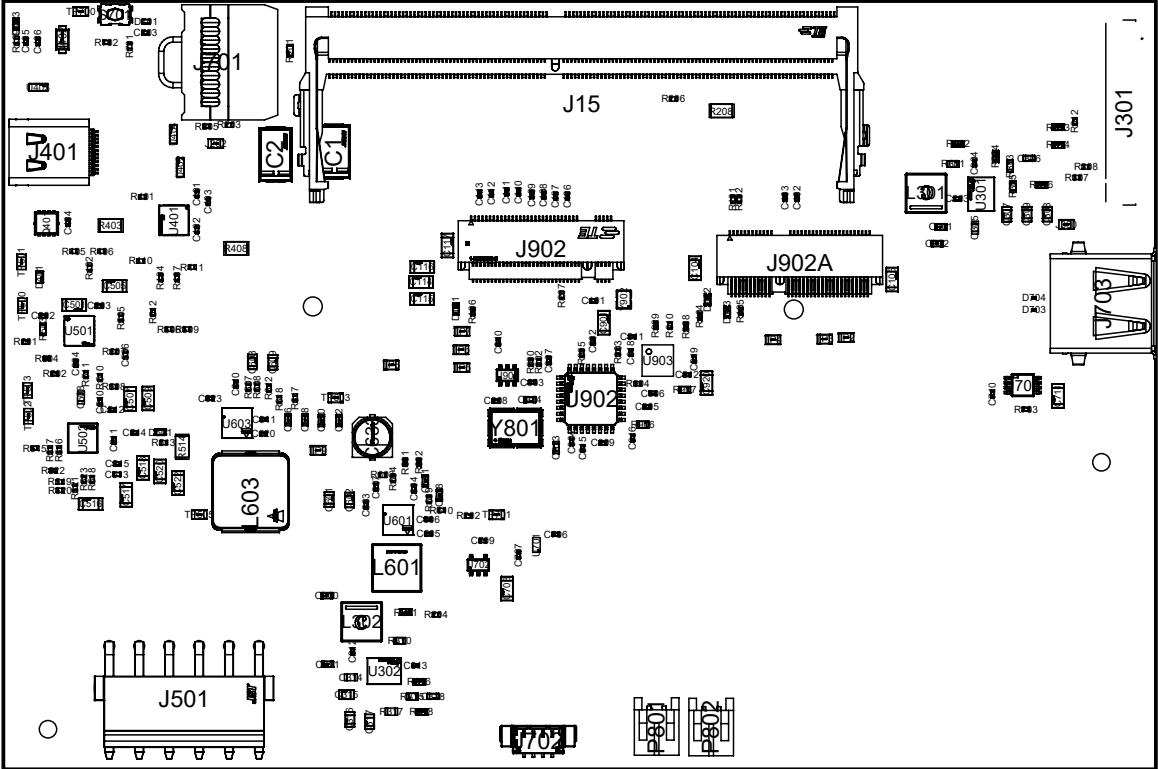
Length = 152.4mm

Width = 101.6mm

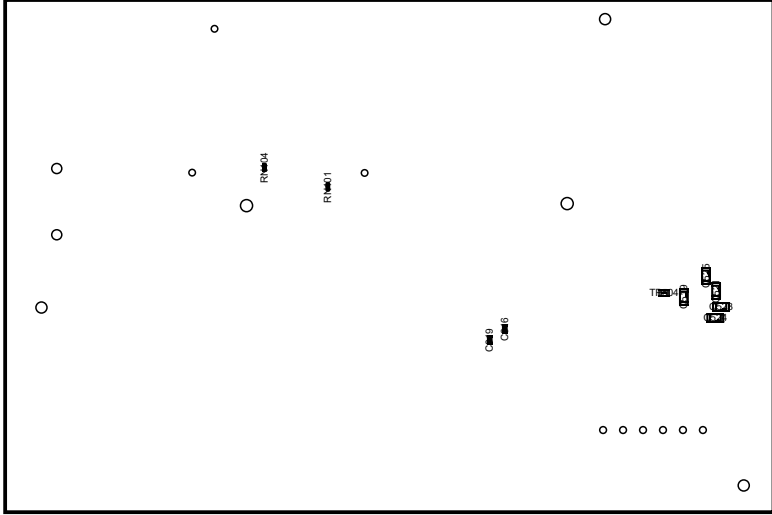
Thickness = 1.54 mm

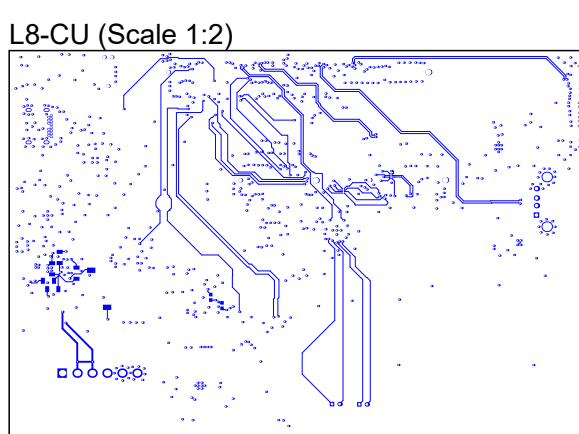
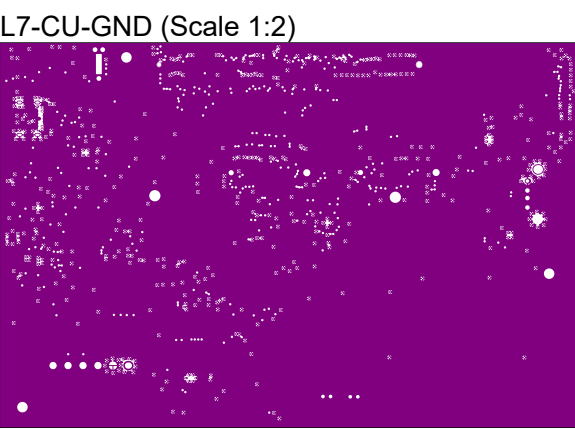
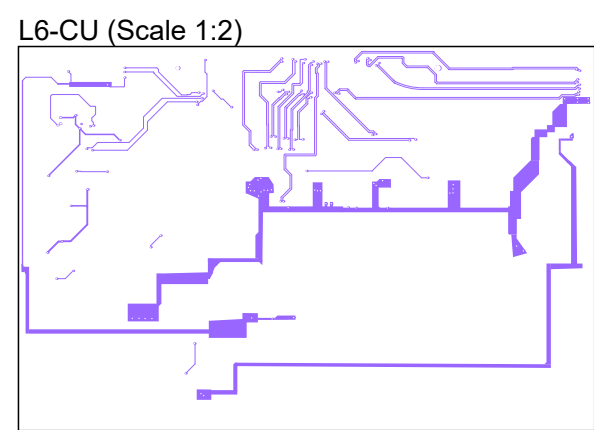
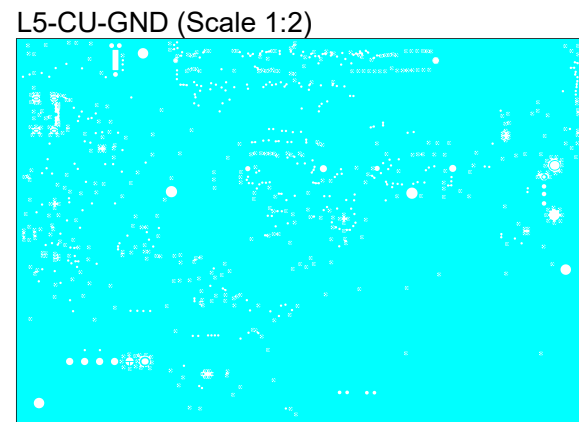
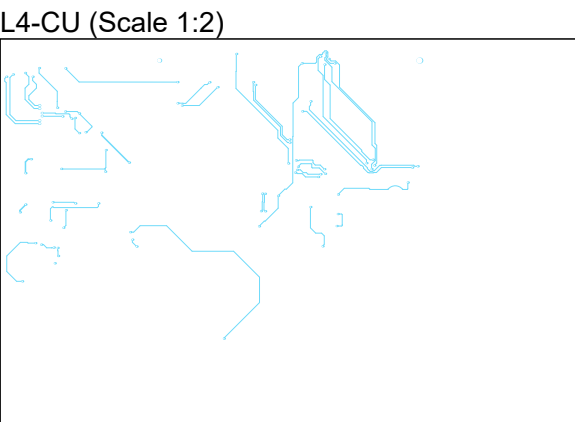
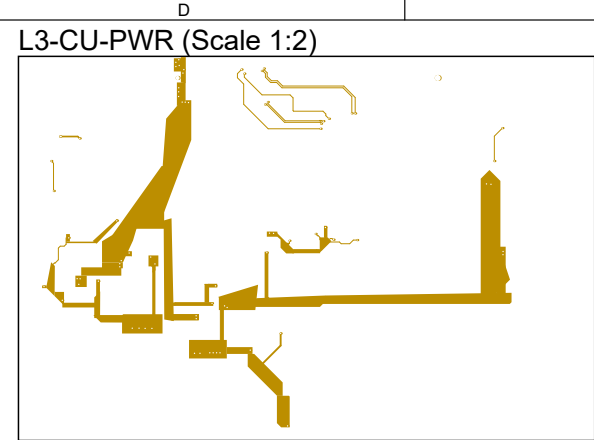
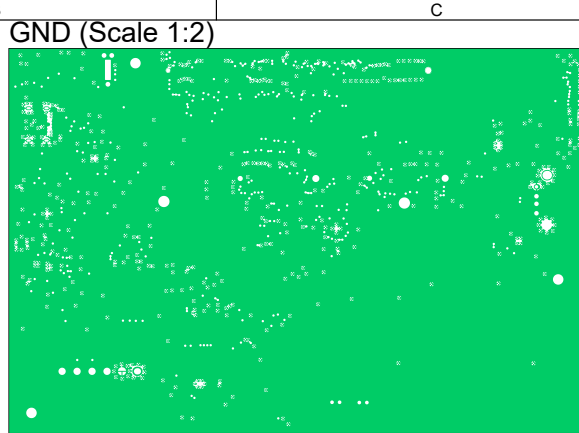
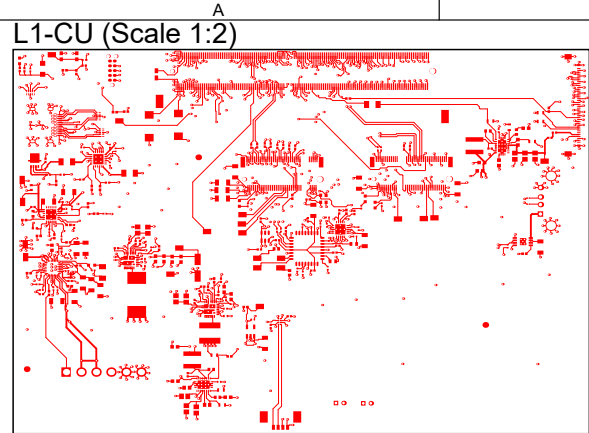
Layers = 8

View from Top side (Scale 1:1)



View from Bottom side (Scale 2:3)







Transmission Line Structure Table											
Impedance Id	Transmission Line	Target Impedance	Calculated Impedance	Trace layer	Wide Trace Width	Narrow Trace Width	Gap	Reference layers	Substack	Clearance	Target Tolerance
1	Coated Microstrip	50	49.99	L1-CU	0.21mm	0.21mm		GND	Board Layer Stack	0.13mm	10%
2	Edge-Coupled Coated Microstrip	90	85.14	L1-CU	0.25mm	0.25mm	0.30mm	GND	Board Layer Stack	0.13mm	10%
3	Edge-Coupled Coated Microstrip	85	88.03	L1-CU	0.25mm	0.25mm	0.30mm	GND	Board Layer Stack	0.00mm	10%
4	Coated Microstrip	45	45.00	L1-CU	0.25mm	0.25mm		GND	Board Layer Stack	0.13mm	10%
5	Edge-Coupled Coated Microstrip	100	94.63	L1-CU	0.21mm	0.21mm	0.30mm	GND	Board Layer Stack	0.13mm	10%
6	Coated Microstrip	42.5	42.49	L1-CU	0.27mm	0.27mm		GND	Board Layer Stack	0.13mm	10%
7	Offset Stripline	50	50.01	L3-CU-PWR	0.13mm	0.13mm		GND,L4-CU	Board Layer Stack	0.00mm	10%
8	Edge-Coupled Offset Stripline	90	85.23	L3-CU-PWR	0.17mm	0.17mm	0.30mm	GND,L4-CU	Board Layer Stack	0.00mm	10%
9	Edge-Coupled Offset Stripline	85	85.23	L3-CU-PWR	0.17mm	0.17mm	0.30mm	GND,L4-CU	Board Layer Stack	0.00mm	10%
10	Offset Stripline	45	44.99	L3-CU-PWR	0.17mm	0.17mm		GND,L4-CU	Board Layer Stack	0.13mm	10%
11	Edge-Coupled Offset Stripline	100	94.30	L3-CU-PWR	0.13mm	0.13mm	0.30mm	GND,L4-CU	Board Layer Stack	0.13mm	10%
12	Offset Stripline	42.5	42.49	L3-CU-PWR	0.19mm	0.19mm		GND,L4-CU	Board Layer Stack	0.13mm	10%
13	Offset Stripline	50	50.01	L4-CU	0.13mm	0.13mm		L3-CU-PWR,L5-CU-GND	Board Layer Stack	0.00mm	10%
14	Edge-Coupled Offset Stripline	90	85.23	L4-CU	0.17mm	0.17mm	0.30mm	L3-CU-PWR,L5-CU-GND	Board Layer Stack	0.00mm	10%
15	Edge-Coupled Offset Stripline	85	85.23	L4-CU	0.17mm	0.17mm	0.30mm	L3-CU-PWR,L5-CU-GND	Board Layer Stack	0.13mm	10%
16	Offset Stripline	45	44.99	L4-CU	0.17mm	0.17mm		L3-CU-PWR,L5-CU-GND	Board Layer Stack	0.13mm	10%
17	Edge-Coupled Offset Stripline	100	94.30	L4-CU	0.13mm	0.13mm	0.30mm	L3-CU-PWR,L5-CU-GND	Board Layer Stack	0.13mm	10%
18	Offset Stripline	42.5	42.49	L4-CU	0.19mm	0.19mm		L3-CU-PWR,L5-CU-GND	Board Layer Stack	0.13mm	10%
19	Offset Stripline	50	50.01	L6-CU	0.13mm	0.13mm		L5-CU-GND,L7-CU-GND	Board Layer Stack	0.00mm	10%
20	Edge-Coupled Offset Stripline	90	85.23	L6-CU	0.17mm	0.17mm	0.30mm	L5-CU-GND,L7-CU-GND	Board Layer Stack	0.00mm	10%
21	Edge-Coupled Offset Stripline	85	85.23	L6-CU	0.17mm	0.17mm	0.30mm	L5-CU-GND,L7-CU-GND	Board Layer Stack	0.00mm	10%
22	Offset Stripline	45	44.99	L6-CU	0.17mm	0.17mm		L5-CU-GND,L7-CU-GND	Board Layer Stack	0.13mm	10%
23	Edge-Coupled Offset Stripline	100	94.30	L6-CU	0.13mm	0.13mm	0.30mm	L5-CU-GND,L7-CU-GND	Board Layer Stack	0.13mm	10%
24	Offset Stripline	42.5	42.49	L6-CU	0.19mm	0.19mm		L5-CU-GND,L7-CU-GND	Board Layer Stack	0.13mm	10%
25	Coated Microstrip	50	49.99	L8-CU	0.22mm	0.22mm		L7-CU-GND	Board Layer Stack	0.00mm	10%
26	Edge-Coupled Coated Microstrip	90	88.02	L8-CU	0.25mm	0.25mm	0.30mm	L7-CU-GND	Board Layer Stack	0.00mm	10%
27	Edge-Coupled Coated Microstrip	85	88.02	L8-CU	0.25mm	0.25mm	0.30mm	L7-CU-GND	Board Layer Stack	0.00mm	10%
28	Coated Microstrip	45	45.01	L8-CU	0.25mm	0.25mm		L7-CU-GND	Board Layer Stack	0.13mm	10%
29	Edge-Coupled Coated Microstrip	100	94.60	L8-CU	0.21mm	0.21mm	0.30mm	L7-CU-GND	Board Layer Stack	0.13mm	10%
30	Coated Microstrip	42.5	42.50	L8-CU	0.28mm	0.28mm		L7-CU-GND	Board Layer Stack	0.13mm	10%

Impedance Control Notes

Provide controlled impedance for all high-speed interfaces according to the "Transmission Line Structure Table" in this drawing.

Target impedances by interface:

eDP

50 Ω single-ended

100 Ω differential

PCIe

42.5 Ω single-ended (half-impedance of 85 Ω diff)

85 Ω differential

USB (USB2)

45 Ω single-ended (half-impedance of 90 Ω diff)

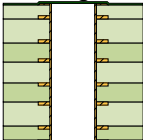
90 Ω differential

Impedance tolerance: ±10% for all controlled-impedance structures.

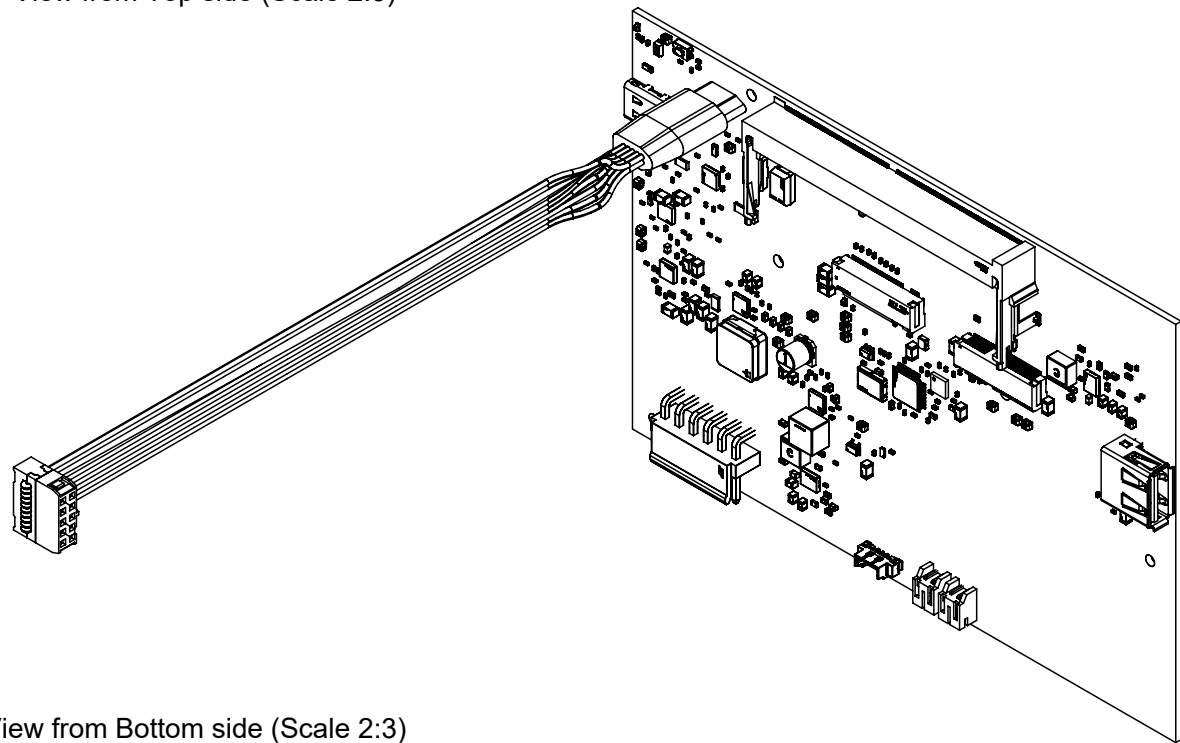
Trace widths and spacings shown in the design are nominal; the PCB manufacturer may adjust them as required to achieve the target impedances on the specified layers.

Through-Vias only

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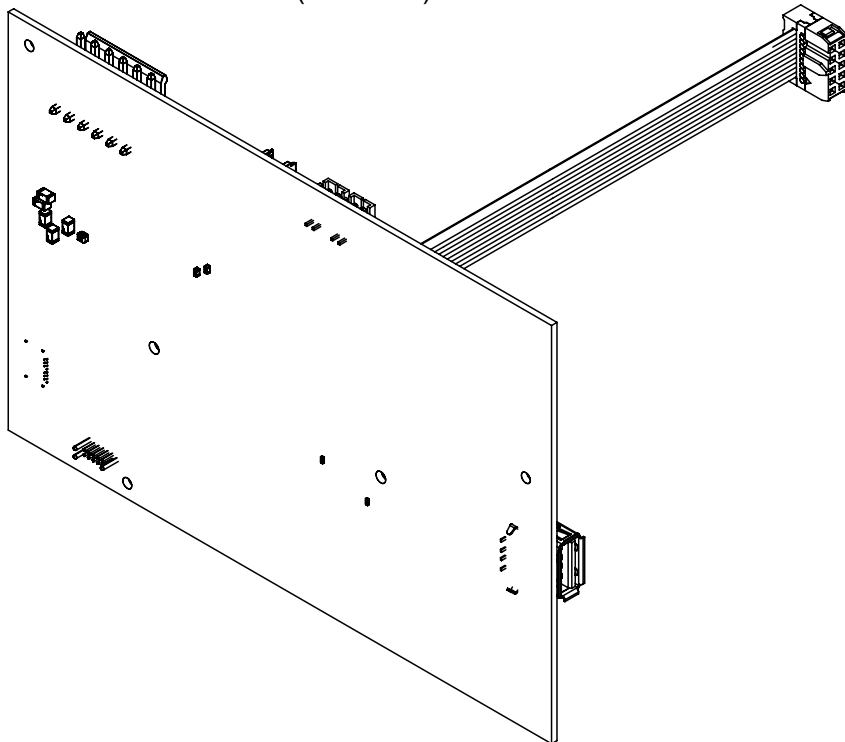


View from Top side (Scale 2:3)

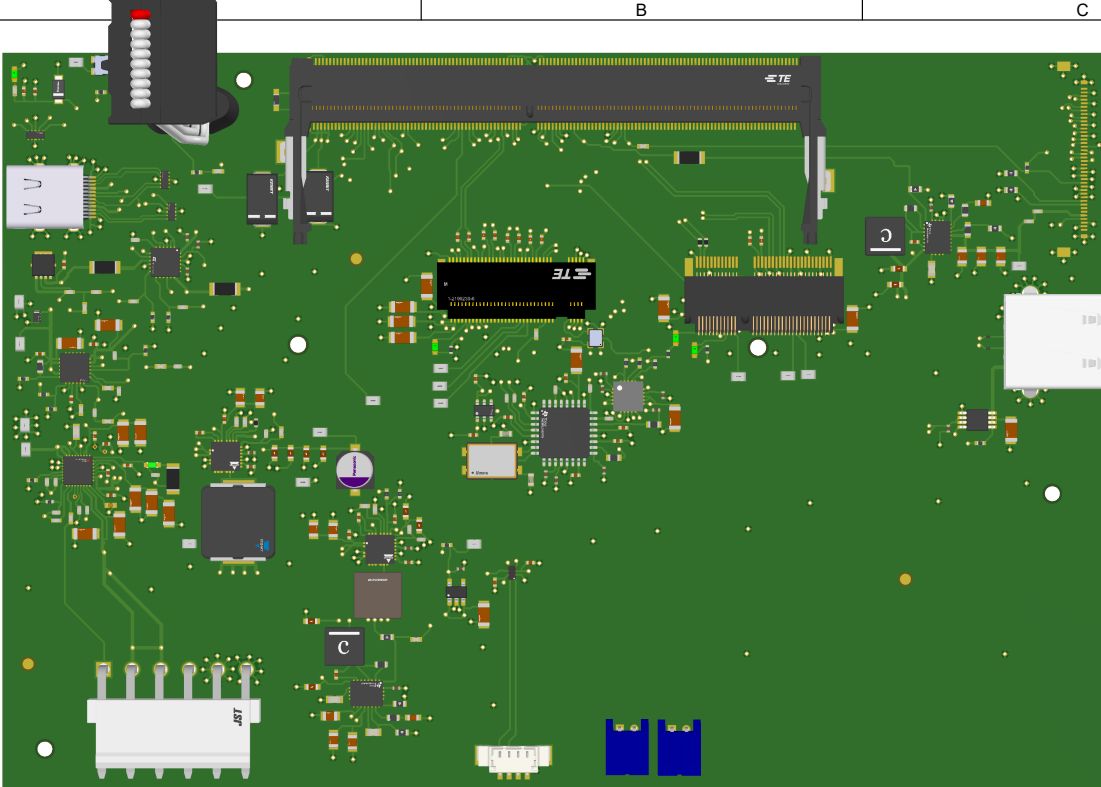


Top

View from Bottom side (Scale 2:3)

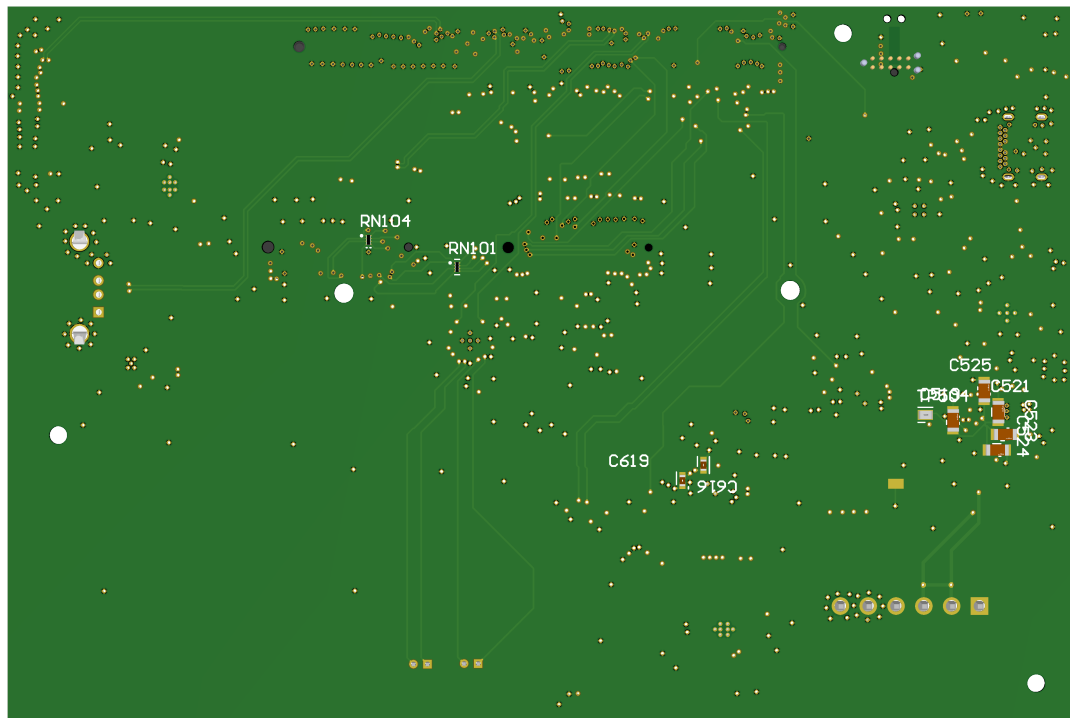


Bottom



Top

Realistic View



Bottom

