國 立 中 山 大 學

資 訊 工 程 學 系 所

Introduction to EDA&Testing – Spring, 2024

Homework Assignment #2
Due Date: April 03, 2024

1. (25%) For ECL NOR gates as shown, if the outputs of two NOR gates short together, analyze electrically the resultant output behavior (wired AND? wired OR). Explain why?

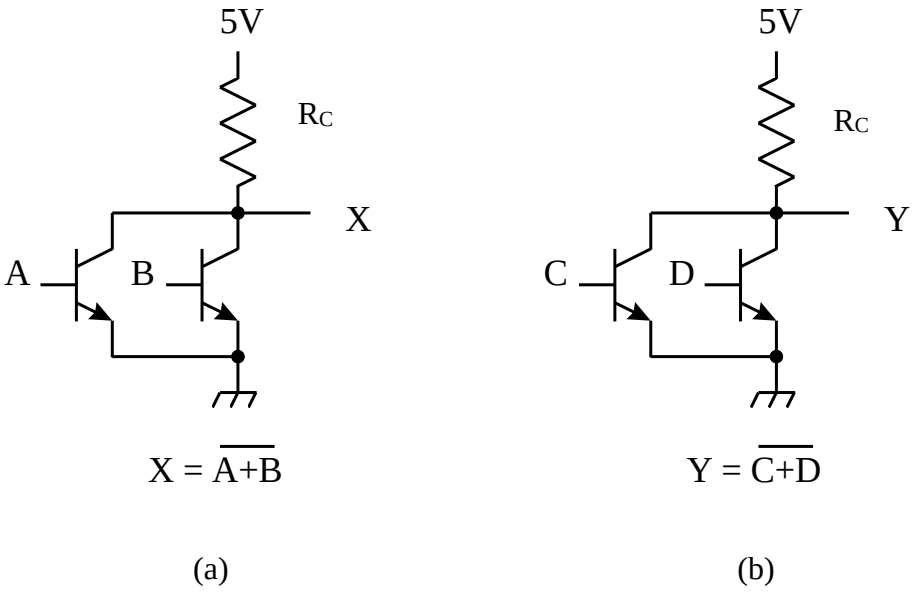

Figure 1. NOR Gates

2. (25%) In Problem 1, if there is a defect that the value of R_C of the gate $X = \overline{A+B}$ is increased by 100 times. If the patterns can be applied to A, B and the output can be observed at X, derive a test pattern to detect this defect.

3. (25%) Derive test patterns to detect the transistor M1 stuck-open fault

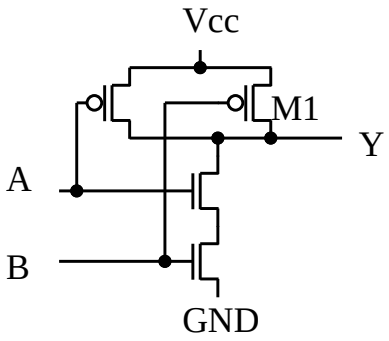

Figure 2. NAND Gate

4. （25%）

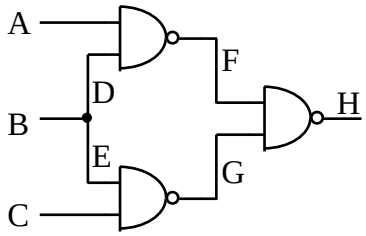

Figure 3.

For the above circuit, try to derive test pattern for the fault F(sa0). For the derived pattern, try to identify what other multiple faults of multipliticity = 2 can be detected.