s0_r →
s0_inv_r
s1_r→
s1_inv_r
s0_s
s0_inv_s
s1_s →
s1_inv_s
→ oe inv_s
→ d0 data inv_r
→ d3 data su_alu
a nins(if1) su_inv_aiu
4 pinc(a[]) SI_alu
1 nins(h[]) SI_inv_aiu
→ 4 nins(f[1]) s0_q
4_pins(c[],) s0_q 4_pins(c[],) s0_inv_q 4_pins(c[],) s1_q
→ 4 nins(v data[]) 51_111v_q
→ ram0 SU_re
×ram3 s0_inv_re →
s1_re →
×u3 ST_INV_re→
\rightarrow 4 nins(v tri[]) S_y
S_IIIV_y
g_lo →
p_lo >
ovr→
z→
reg_wr
en_q
16_pins(select_a_hi[],)
16_pins(select_b_hi[]) →