```
#####################################################################
#  Generated by:      Cadence Encounter 14.28-s033_1
#  OS:                Linux x86_64(Host ID linux-32.ews.illinois.edu)
#  Generated on:      Sat May  2 06:54:44 2020
#  Design:            controller
#  Command:           summaryReport -noHtml -outfile summaryReport.rpt
#####################################################################


==============================
General Design Information
==============================
Design Status: Routed
Design Name: controller
# Instances: 320
# Hard Macros: 0
# Std Cells: 320
    ------------------------------
    Standard Cells in Netlist
    ------------------------------
               Cell Type   Instance Count  Area (um^2)
                   ABorC                1        130.6368
                  and2_1                1         81.6480
                  filler              168       2743.3728
                   inv_1               59       2890.3392
                   inv_2                4        195.9552
                   inv_4                8        391.9104
                 invzp_1                8        653.1840
                  mux2_1                4        457.2288
                 nand2_1                5        326.5920
                 nand2_2               12        783.8208
                 nand4_1                3        244.9440
                  nor2_1               41       2008.5408
                  nor2_4                4        457.2288
                  nor3_1                1         65.3184
                  nor4_1                1         81.6480
# Pads: 0
# Net: 209
# Special Net: 125
# IO Pins:
    ------------------------------
    Issued IO Information
    ------------------------------
    # Unplaced IO Pin  0
    # Floating IO
        ------------------------------
        Floating IO
        ------------------------------
            Floating IO Name
                        c[0]
                        c[1]  2
    # IO Connected to Non-IO Inst
        ------------------------------
        IO Connected to Non-IO Inst
        ------------------------------
                     IO Name      Non-IO Inst Name
               write_en_inv                 U149
                   Q_en_inv                 U179
                       Q_en                 U179
                      inv_r                 U220
                      inv_s                 U275
        regfile_selecter[0]                 U146
        regfile_selecter[1]               drvqshl
          regfile_select[0]                 U146
          regfile_select[1]                 U207
        Q_mux_select_bar[0]                 U206
        Q_mux_select_bar[1]                 U203
```

Q_mux_select[0]	U205
Q_mux_select[1]	U202
s_select_bar[0]	U199
s_select_bar[1]	U147
s_select[0]	U200
s_select[1]	U197
r_select_bar[0]	U196
r_select_bar[1]	U194
r_select[0]	U195
r_select[1]	U148
mux_input_bar[0]	U191
mux_input_bar[1]	U189
mux_input[0]	U192
mux_input[1]	U190
y_select_bar	U184
y_select	U185
reg_wr	U149
q3_data	U178
q0_data	U209
q3	drvqshl
q0	drvqshr
ram3	drvraml
ram0	drvramr
oe	U216
y_data[0]	U215
y_data[1]	U214
y_data[2]	U212
y_data[3]	U211
y_tri[0]	drvy0
y_tri[1]	drvy1
y_tri[2]	drvy2
y_tri[3]	drvy3
z	U180
ovr	U218
p_lo	U217
g_lo	U150
p[0]	U217
p[1]	U217
p[2]	U217
p[3]	U217
c[2]	U218
c[3]	U150
f[0]	U180
f[1]	U180
f[2]	U180
f[3]	U180
select_b_low[0]	U221
select_b_low[1]	U260
select_b_low[2]	U262
select_b_low[3]	U223
select_b_low[4]	U228
select_b_low[5]	U244
select_b_low[6]	U246
select_b_low[7]	U230
select_b_low[8]	U232
select_b_low[9]	U248
select_b_low[10]	U250
select_b_low[11]	U234
select_b_low[12]	U225
select_b_low[13]	U264
select_b_low[14]	U266
select_b_low[15]	U133
select_a_low[0]	U222
select_a_low[1]	U268
select_a_low[2]	U270
select_a_low[3]	U224
select_a_low[4]	U236

```
             select_a_low[5]                 U252
             select_a_low[6]                 U254
             select_a_low[7]                 U238
             select_a_low[8]                 U240
             select_a_low[9]                 U256
            select_a_low[10]                 U258
            select_a_low[11]                 U242
            select_a_low[12]                 U226
            select_a_low[13]                 U272
            select_a_low[14]                 U274
            select_a_low[15]                 U134
              select_b_hi[0]                 U151
              select_b_hi[1]                 U259
              select_b_hi[2]                 U261
              select_b_hi[3]                 U152
              select_b_hi[4]                 U227
              select_b_hi[5]                 U243
              select_b_hi[6]                 U245
              select_b_hi[7]                 U229
              select_b_hi[8]                 U231
              select_b_hi[9]                 U247
             select_b_hi[10]                 U249
             select_b_hi[11]                 U233
             select_b_hi[12]                 U153
             select_b_hi[13]                 U263
             select_b_hi[14]                 U265
             select_b_hi[15]                 U182
              select_a_hi[0]                 U154
              select_a_hi[1]                 U267
              select_a_hi[2]                 U269
              select_a_hi[3]                 U155
              select_a_hi[4]                 U235
              select_a_hi[5]                 U251
              select_a_hi[6]                 U253
              select_a_hi[7]                 U237
              select_a_hi[8]                 U239
              select_a_hi[9]                 U255
             select_a_hi[10]                 U257
             select_a_hi[11]                 U241
             select_a_hi[12]                 U156
             select_a_hi[13]                 U271
             select_a_hi[14]                 U273
             select_a_hi[15]                 U181
                        b[0]                 U133
                        b[1]                 U133
                        b[2]                 U133
                        b[3]                 U133
                        a[0]                 U134
                        a[1]                 U134
                        a[2]                 U134
                        a[3]                 U134
                        i[0]                 U147
                        i[1]                 U143
                        i[2]                 U147
                        i[3]                 U177
                        i[4]                 U144
                        i[5]                 U186
                        i[6]                 U184
                        i[7]                 U145
                        i[8]                 U183  138  140
# Pins:
    ------------------------------
    Correctness of Pin Connectivity     All Instances
    ------------------------------
    # Floating Terms  0
    # Output Term Marked Tie Hi/Lo  0
    # Output Term Shorted to PG Net  0  399
```

```
# PG Pins:
    ------------------------------
    Correctness of PG Pin Connectivity     All Instances
    ------------------------------
    # Instances that No Net Defined for Any PG Pin
        ------------------------------
        The Instances that No Net Defined     any PG Pin
        ------------------------------
               Instance Name
                  FILLER_168
                  FILLER_167
                  FILLER_166
                  FILLER_165
                  FILLER_164
                  FILLER_163
                  FILLER_162
                  FILLER_161
                  FILLER_160
                  FILLER_159
                  FILLER_158
                  FILLER_157
                  FILLER_156
                  FILLER_155
                  FILLER_154
                  FILLER_153
                  FILLER_152
                  FILLER_151
                  FILLER_150
                  FILLER_149
                  FILLER_148
                  FILLER_147
                  FILLER_146
                  FILLER_145
                  FILLER_144
                  FILLER_143
                  FILLER_142
                  FILLER_141
                  FILLER_140
                  FILLER_139
                  FILLER_138
                  FILLER_137
                  FILLER_136
                  FILLER_135
                  FILLER_134
                  FILLER_133
                  FILLER_132
                  FILLER_131
                  FILLER_130
                  FILLER_129
                  FILLER_128
                  FILLER_127
                  FILLER_126
                  FILLER_125
                  FILLER_124
                  FILLER_123
                  FILLER_122
                  FILLER_121
                  FILLER_120
                  FILLER_119
                  FILLER_118
                  FILLER_117
                  FILLER_116
                  FILLER_115
                  FILLER_114
                  FILLER_113
                  FILLER_112
                  FILLER_111
```

FILLER_110
FILLER_109
FILLER_108
FILLER_107
FILLER_106
FILLER_105
FILLER_104
FILLER_103
FILLER_102
FILLER_101
FILLER_100
FILLER_99
FILLER_98
FILLER_97
FILLER_96
FILLER_95
FILLER_94
FILLER_93
FILLER_92
FILLER_91
FILLER_90
FILLER_89
FILLER_88
FILLER_87
FILLER_86
FILLER_85
FILLER_84
FILLER_83
FILLER_82
FILLER_81
FILLER_80
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FILLER_46
FILLER_45
FILLER_44

FILLER_43
FILLER_42
FILLER_41
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FILLER_32
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FILLER_10
FILLER_9
FILLER_8
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FILLER_6
FILLER_5
FILLER_4
FILLER_3
FILLER_2
FILLER_1
U276
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U186

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                      U185
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                      U172
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                      U170
                      U169
                      U168
                      U167
                      U166
                      U165
                      U164
                      U163
                      U162
                      U161
                      U160
                      U159
                      U158
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                      U156
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                      U154
                      U153
                      U152
                      U151
                      U150
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                      U145
                      U144
                      U143
                      U142
                      U141
                      U140
                      U139
                      U138
                      U137
                      U136
                      U135
                      U134
                      U133
                   drvraml
                   drvqshl
                   drvramr
                   drvqshr
                     drvy3
                     drvy2
                     drvy1
                     drvy0  320
    # Floating PG Terms  0
    # PG Pins Connect to Non-PG Net  0
    # Power Pins Connect Ground Net  0
    # Ground Pins Connect Power Net  0  640
Average Pins Per Net(Signal): 1.909
```

```
==============================
General Library Information
==============================
# Routing Layers: 5
# Masterslice Layers: 12
# Pin Layers:
    General Caution:
        1) Library have metal1, metal2, metal3, metal4 and metal5 pins, you should setPreRouteAsObs {1 2
3}                                  to ensure these pins are accessible after placement

    ------------------------------
    Pin Layers
    ------------------------------
    metal5
    metal4
    metal3
    metal2
    metal1  5
# Layers:
    ------------------------------
    Layer metal5 Information
    ------------------------------
    Type  Routing
    Wire Pitch X  2.160 um
    Wire Pitch Y  2.160 um
    Wire Width  0.480 um
    Spacing  0.480 um
    ------------------------------
    Layer via4 Information
    ------------------------------
    Type  Cut
    Vias
        ------------------------------
        Via list in layer via4
        ------------------------------
                Vias in via4  Default
                       M5_M4      Yes  For complete list click here
    Multiple Orientation Vias  CAUTION: There is only one default via in this layer
    ------------------------------
    Layer metal4 Information
    ------------------------------
    Type  Routing
    Wire Pitch X  1.080 um
    Wire Pitch Y  1.080 um
    Wire Width  0.360 um
    Spacing  0.480 um
    ------------------------------
    Layer via3 Information
    ------------------------------
    Type  Cut
    Vias
        ------------------------------
        Via list in layer via3
        ------------------------------
                Vias in via3  Default
                       M4_M3      Yes  For complete list click here
    Multiple Orientation Vias  CAUTION: There is only one default via in this layer
    ------------------------------
    Layer metal3 Information
    ------------------------------
    Type  Routing
    Wire Pitch X  1.080 um
    Wire Pitch Y  1.080 um
    Wire Width  0.360 um
    Spacing  0.480 um
    ------------------------------
    Layer via2 Information
```

```
------------------------------
Type  Cut
Vias
    ------------------------------
    Via list in layer via2
    ------------------------------
            Vias in via2  Default
                  M3_M2      Yes  For complete list click here
Multiple Orientation Vias  CAUTION: There is only one default via in this layer
------------------------------
Layer metal2 Information
------------------------------
Type  Routing
Wire Pitch X  1.080 um
Wire Pitch Y  1.080 um
Wire Width  0.360 um
Spacing  0.480 um
------------------------------
Layer via Information
------------------------------
Type  Cut
Vias
    ------------------------------
    Via list in layer via
    ------------------------------
             Vias in via  Default
                   M2_M1      Yes  For complete list click here
Multiple Orientation Vias  CAUTION: There is only one default via in this layer
------------------------------
Layer metal1 Information
------------------------------
Type  Routing
Wire Pitch X  1.080 um
Wire Pitch Y  1.080 um
Wire Width  0.360 um
Spacing  0.360 um
------------------------------
Layer cc Information
------------------------------
Type  Cut
Vias
    ------------------------------
    Via list in layer cc
    ------------------------------
              Vias in cc  Default
                 M1_POLY       No
                    NTAP       No
                    M1_N       No
                    M1_P       No  For complete list click here
------------------------------
Layer nodrc Information
------------------------------
Type  Masterslice
------------------------------
Layer metalcap Information
------------------------------
Type  Masterslice
------------------------------
Layer cap_id Information
------------------------------
Type  Masterslice
------------------------------
Layer res_id Information
------------------------------
Type  Masterslice
------------------------------
Layer text Information
```

```
    ------------------------------
    Type  Masterslice
    ------------------------------
    Layer sblock Information
    ------------------------------
    Type  Masterslice
    ------------------------------
    Layer pad Information
    ------------------------------
    Type  Masterslice
    ------------------------------
    Layer glass Information
    ------------------------------
    Type  Masterslice
    ------------------------------
    Layer poly Information
    ------------------------------
    Type  Masterslice
    ------------------------------
    Layer pactive Information
    ------------------------------
    Type  Masterslice
    ------------------------------
    Layer nactive Information
    ------------------------------
    Type  Masterslice
    ------------------------------
    Layer nwell Information
    ------------------------------
    Type  Masterslice  22
# Pins without Physical Port: 0
# Pins in Library without Timing Lib:
    ------------------------------
    Pins in Library without timing lib
    ------------------------------
               Cell Name      List of Pin Name
                  ABnorC                   ip1
                  ABnorC                   ip2
                  ABnorC                   ip3
                  ABnorC                    op
                   ABorC                   ip1
                   ABorC                   ip2
                   ABorC                   ip3
                   ABorC                    op
            ab_or_c_or_d                   ip1
            ab_or_c_or_d                   ip2
            ab_or_c_or_d                   ip3
            ab_or_c_or_d                   ip4
            ab_or_c_or_d                    op
                  and2_1                   ip1
                  and2_1                   ip2
                  and2_1                    op
                  and2_2                   ip1
                  and2_2                   ip2
                  and2_2                    op
                  and2_4                   ip1
                  and2_4                   ip2
                  and2_4                    op
                  and3_1                   ip1
                  and3_1                   ip2
                  and3_1                   ip3
                  and3_1                    op
                  and3_2                   ip1
                  and3_2                   ip2
                  and3_2                   ip3
                  and3_2                    op
                  and3_4                   ip1
```

and3_4	ip2
and3_4	ip3
and3_4	op
and4_1	ip1
and4_1	ip2
and4_1	ip3
and4_1	ip4
and4_1	op
and4_2	ip1
and4_2	ip2
and4_2	ip3
and4_2	ip4
and4_2	op
and4_4	ip1
and4_4	ip2
and4_4	ip3
and4_4	ip4
and4_4	op
buf_1	ip
buf_1	op
buf_2	ip
buf_2	op
buf_4	ip
buf_4	op
bufzp_2	c
bufzp_2	ip
bufzp_2	op
cd_12	ip
cd_12	op
cd_16	ip
cd_16	op
cd_8	ip
cd_8	op
dksp_1	ck
dksp_1	ip
dksp_1	q
dksp_1	qb
dksp_1	sb
dp_1	ck
dp_1	ip
dp_1	q
dp_2	ck
dp_2	ip
dp_2	q
dp_4	ck
dp_4	ip
dp_4	q
drp_1	ck
drp_1	ip
drp_1	q
drp_1	rb
drp_2	ck
drp_2	ip
drp_2	q
drp_2	rb
drp_4	ck
drp_4	ip
drp_4	q
drp_4	rb
drsp_1	ck
drsp_1	ip
drsp_1	q
drsp_1	rb
drsp_1	s
drsp_2	ck
drsp_2	ip
drsp_2	q

```
    drsp_2                  rb
    drsp_2                   s
    drsp_4                  ck
    drsp_4                  ip
    drsp_4                   q
    drsp_4                  rb
    drsp_4                   s
   dtrsp_2                  ck
   dtrsp_2                  ip
   dtrsp_2                   q
   dtrsp_2                  rb
   dtrsp_2                   s
   dtrsp_2                 sip
   dtrsp_2                  sm
 fulladder                   a
 fulladder                   b
 fulladder                  ci
 fulladder                  co
 fulladder                   s
     inv_1                  ip
     inv_1                  op
     inv_2                  ip
     inv_2                  op
     inv_4                  ip
     inv_4                  op
   invzp_1                   c
   invzp_1                  ip
   invzp_1                  op
   invzp_2                   c
   invzp_2                  ip
   invzp_2                  op
   invzp_4                   c
   invzp_4                  ip
   invzp_4                  op
    jkrp_2                  ck
    jkrp_2                   j
    jkrp_2                   k
    jkrp_2                   q
    jkrp_2                  qb
    jkrp_2                  rb
      lp_1                  ck
      lp_1                  ip
      lp_1                   q
      lp_2                  ck
      lp_2                  ip
      lp_2                   q
     lrp_1                  ck
     lrp_1                  ip
     lrp_1                   q
     lrp_1                  rb
     lrp_2                  ck
     lrp_2                  ip
     lrp_2                   q
     lrp_2                  rb
     lrp_4                  ck
     lrp_4                  ip
     lrp_4                   q
     lrp_4                  rb
    lrsp_1                  ck
    lrsp_1                  ip
    lrsp_1                   q
    lrsp_1                  rb
    lrsp_1                   s
    lrsp_2                  ck
    lrsp_2                  ip
    lrsp_2                   q
    lrsp_2                  rb
```

lrsp_2	s
lrsp_4	ck
lrsp_4	ip
lrsp_4	q
lrsp_4	rb
lrsp_4	s
mux2_1	ip1
mux2_1	ip2
mux2_1	op
mux2_1	s
mux2_2	ip1
mux2_2	ip2
mux2_2	op
mux2_2	s
mux2_4	ip1
mux2_4	ip2
mux2_4	op
mux2_4	s
mux3_2	ip1
mux3_2	ip2
mux3_2	ip3
mux3_2	op
mux3_2	s0
mux3_2	s1
mux4_2	ip1
mux4_2	ip2
mux4_2	ip3
mux4_2	ip4
mux4_2	op
mux4_2	s0
mux4_2	s1
nand2_1	ip1
nand2_1	ip2
nand2_1	op
nand2_2	ip1
nand2_2	ip2
nand2_2	op
nand2_4	ip1
nand2_4	ip2
nand2_4	op
nand3_1	ip1
nand3_1	ip2
nand3_1	ip3
nand3_1	op
nand3_2	ip1
nand3_2	ip2
nand3_2	ip3
nand3_2	op
nand3_4	ip1
nand3_4	ip2
nand3_4	ip3
nand3_4	op
nand4_1	ip1
nand4_1	ip2
nand4_1	ip3
nand4_1	ip4
nand4_1	op
nand4_2	ip1
nand4_2	ip2
nand4_2	ip3
nand4_2	ip4
nand4_2	op
nand4_4	ip1
nand4_4	ip2
nand4_4	ip3
nand4_4	ip4
nand4_4	op

```
            nor2_1                  ip1
            nor2_1                  ip2
            nor2_1                   op
            nor2_2                  ip1
            nor2_2                  ip2
            nor2_2                   op
            nor2_4                  ip1
            nor2_4                  ip2
            nor2_4                   op
            nor3_1                  ip1
            nor3_1                  ip2
            nor3_1                  ip3
            nor3_1                   op
            nor3_2                  ip1
            nor3_2                  ip2
            nor3_2                  ip3
            nor3_2                   op
            nor3_4                  ip1
            nor3_4                  ip2
            nor3_4                  ip3
            nor3_4                   op
            nor4_1                  ip1
            nor4_1                  ip2
            nor4_1                  ip3
            nor4_1                  ip4
            nor4_1                   op
            nor4_2                  ip1
            nor4_2                  ip2
            nor4_2                  ip3
            nor4_2                  ip4
            nor4_2                   op
            nor4_4                  ip1
            nor4_4                  ip2
            nor4_4                  ip3
            nor4_4                  ip4
            nor4_4                   op
not_ab_or_c_or_d                    ip1
not_ab_or_c_or_d                    ip2
not_ab_or_c_or_d                    ip3
not_ab_or_c_or_d                    ip4
not_ab_or_c_or_d                     op
             or2_1                  ip1
             or2_1                  ip2
             or2_1                   op
             or2_2                  ip1
             or2_2                  ip2
             or2_2                   op
             or2_4                  ip1
             or2_4                  ip2
             or2_4                   op
             or3_1                  ip1
             or3_1                  ip2
             or3_1                  ip3
             or3_1                   op
             or3_2                  ip1
             or3_2                  ip2
             or3_2                  ip3
             or3_2                   op
             or3_4                  ip1
             or3_4                  ip2
             or3_4                  ip3
             or3_4                   op
             or4_1                  ip1
             or4_1                  ip2
             or4_1                  ip3
             or4_1                  ip4
             or4_1                   op
```

```
                  or4_2                   ip1
                  or4_2                   ip2
                  or4_2                   ip3
                  or4_2                   ip4
                  or4_2                    op
                  or4_4                   ip1
                  or4_4                   ip2
                  or4_4                   ip3
                  or4_4                   ip4
                  or4_4                    op
                xnor2_1                   ip1
                xnor2_1                   ip2
                xnor2_1                    op
                xnor2_2                   ip1
                xnor2_2                   ip2
                xnor2_2                    op
                 xor2_1                   ip1
                 xor2_1                   ip2
                 xor2_1                    op
                 xor2_2                   ip1
                 xor2_2                   ip2
                 xor2_2                    op
                 padgnd                   pad
          padbidirhe_025                    di
          padbidirhe_025                   dib
          padbidirhe_025
          padbidirhe_025                   oeb
          padbidirhe_025                   pad
                 padinc                    di
                 padinc                   dib
                 padinc                   pad
                  padio                  data
                  padio                   pad
                 padout                    di
                 padout                   dib
                 padout
                 padout                   pad
                 padvdd                   pad
             padnoconnect                 pad  338
# Pins Missing Direction: 0
Antenna Summary Report:
    General Caution:
        1) All Antenna Constructs are absent     the layer section of LEF.
        2) All Antenna Constructs are absent     the macro section of LEF.For more information click
here
# Cells Missing LEF Info: 0
# Cells with Dimension Errors: 0

==============================
Netlist Information
==============================
# HFO (>200) Nets: 0
# No-driven Nets: 19
    General Caution:
        1) TODO
    No-driven Nets
    gnd!
    vdd!
    d[3]
    d[2]
    d[1]
    d[0]
    f3_in
    f0_in
    cin
    y[0]
    y[1]
```

```
    y[2]
    y[3]
    q0_out
    q0_in
    q3_in
    q3_out
    cp
    clock_inv
# Multi-driven Nets: 0
# Assign Statements: 0
Is Design Uniquified: YES
# Pins in Netlist without timing lib:
    ------------------------------
    Pins in Netlist without timing lib
    ------------------------------
    Cell Name  List of Pin Name
    ABorC  ip1
    ABorC  ip2
    ABorC  ip3
    ABorC  op
    and2_1  ip1
    and2_1  ip2
    and2_1  op
    inv_1  ip
    inv_1  op
    inv_2  ip
    inv_2  op
    inv_4  ip
    inv_4  op
    invzp_1  c
    invzp_1  ip
    invzp_1  op
    mux2_1  ip1
    mux2_1  ip2
    mux2_1  op
    mux2_1  s
    nand2_1  ip1
    nand2_1  ip2
    nand2_1  op
    nand2_2  ip1
    nand2_2  ip2
    nand2_2  op
    nand4_1  ip1
    nand4_1  ip2
    nand4_1  ip3
    nand4_1  ip4
    nand4_1  op
    nor2_1  ip1
    nor2_1  ip2
    nor2_1  op
    nor2_4  ip1
    nor2_4  ip2
    nor2_4  op
    nor3_1  ip1
    nor3_1  ip2
    nor3_1  ip3
    nor3_1  op
    nor4_1  ip1
    nor4_1  ip2
    nor4_1  ip3
    nor4_1  ip4
    nor4_1  op  46

==============================

==============================
: Internal  External
```

```
No of Nets:        186           0
No of Connections:        351           0
Total Net Length (X): 3.5577e+03  0.0000e+00
Total Net Length (Y): 2.6397e+03  0.0000e+00
Total Net Length: 6.1974e+03  0.0000e+00

==============================
Timing Information
==============================
# Clocks in design: 0
# Generated clocks: 0
# "dont_use" cells from .libs: 0
# "dont_touch" cells from .libs: 0
# Cells in .lib with max_tran: 0
# Cells in .lib with max_cap: 0
# Cells in .lib with max_fanout: 0
SDC max_cap: N/A
SDC max_tran: N/A
SDC max_fanout: N/A
Default Ext. Scale Factor: 1.000
Detail Ext. Scale Factor: 1.000

==============================
Floorplan/Placement Information
==============================
Total area of Standard cells: 11512.368 um^2
Total area of Standard cells(Subtracting Physical Cells): 8768.995 um^2
Total area of Macros: 0.000 um^2
Total area of Blockages: 0.000 um^2
Total area of Pad cells: 0.000 um^2
Total area of Core: 11554.099 um^2
Total area of Chip: 11554.099 um^2
Effective Utilization: 1.0444e+00
Number of Cell Rows: 3
% Pure Gate Density #1 (Subtracting BLOCKAGES): 99.639%
% Pure Gate Density #2 (Subtracting BLOCKAGES and Physical Cells): 75.895%
% Pure Gate Density #3 (Subtracting MACROS): 99.639%
% Pure Gate Density #4 (Subtracting MACROS and Physical Cells): 75.895%
% Pure Gate Density #5 (Subtracting MACROS and BLOCKAGES): 99.639%
% Pure Gate Density #6 (Subtracting MACROS and BLOCKAGES and Physical Cells): 75.895%
% Core Density (Counting Std Cells and MACROs): 99.639%
% Core Density #2(Subtracting Physical Cells): 75.895%
% Chip Density (Counting Std Cells and MACROs and IOs): 99.639%
% Chip Density #2(Subtracting Physical Cells): 75.895%
# Macros within 5 sites of IO pad: No
Macro halo defined?: No

==============================
Wire Length Distribution
==============================
Total metal1 wire length: 444.4800 um
Total metal2 wire length: 2099.0400 um
Total metal3 wire length: 2987.5800 um
Total metal4 wire length: 239.8200 um
Total metal5 wire length: 400.2600 um
Total wire length: 6171.1800 um
Average wire length/net: 29.5272 um
Area of Power Net Distribution:
    ------------------------------
    Area of Power Net Distribution
    ------------------------------
    Layer Name  Area of Power Net  Routable Area  Percentage
    metal1  1005.0480  11554.0992  8.6986%
    metal2  146.9664  11554.0992  1.2720%
    metal3  0.0000  11554.4380  0.0000%
    metal4  0.0000  11554.0992  0.0000%
    metal5  0.0000  11554.0992  0.0000%  For more information click here
```