

1. Description

1.1. Project

Project Name	Sonus DSP Subsystem
Board Name	STM32H745I-DISCO
Generated with:	STM32CubeMX 6.10.0
Date	02/02/2024

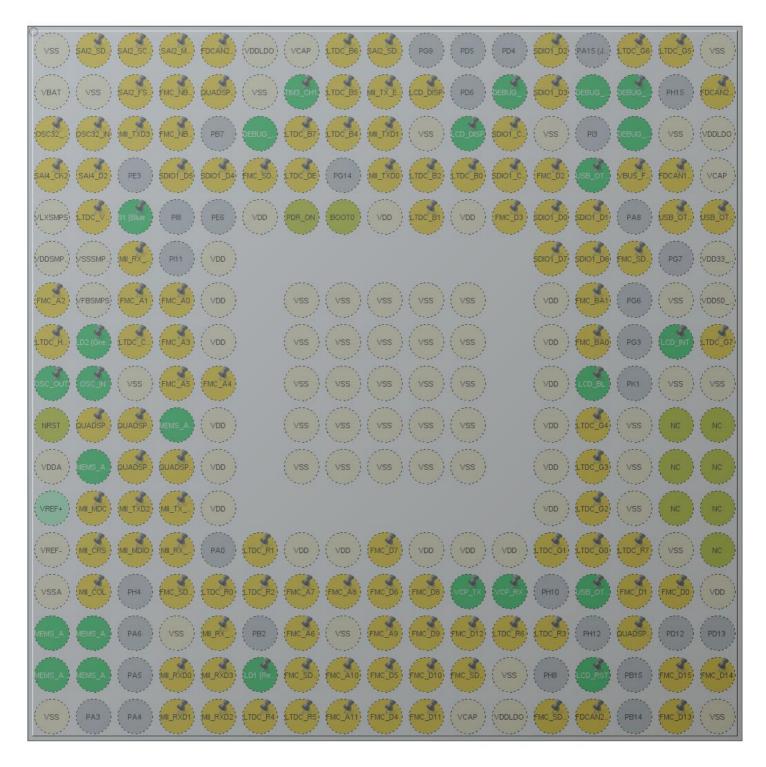
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H745/755
MCU name	STM32H745XIHx
MCU Package	TFBGA240
MCU Pin number	265

1.3. Core(s) information

Core(s)	ARM Cortex-M7
	ARM Cortex-M4

2. Pinout Configuration



TFBGA240 +25 (Top view)

3. Pins Configuration

Pin Number TFBGA240	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A1	VSS	Power		
A2	PI6 *	I/O	SAI2_SD_A	
А3	PI5 *	I/O	SAI2_SCK_A	
A4	PI4 *	I/O	SAI2_MCLK_A	
A5	PB5 *	I/O	FDCAN2_RX	FDCAN2_RX
A6	VDDLDO	Power		
A7	VCAP	Power		
A8	PK5 *	I/O	LTDC_B6	
A9	PG10 *	I/O	SAI2_SD_B	
A13	PC10 *	I/O	SDMMC1_D2	SDIO1_D2
A15	PI1 *	I/O	LTDC_G6	
A16	PIO *	I/O	LTDC_G5	
A17	VSS	Power		
B1	VBAT	Power		
B2	VSS	Power		
В3	PI7 *	I/O	SAI2_FS_A	
B4	PE1 *	I/O	FMC_NBL1	
B5	PB6 *	I/O	QUADSPI_BK1_NCS	
В6	VSS	Power		
В7	PB4 (NJTRST)	I/O	TIM3_CH1	
B8	PK4 *	I/O	LTDC_B5	
В9	PG11 *	I/O	ETH_TX_EN	MII_TX_EN
B10	PJ15 *	I/O	LTDC_B3	LCD_DISP
B12	PD3 **	I/O	GPIO_Input	DEBUG_EN_IN
B13	PC11 *	I/O	SDMMC1_D3	SDIO1_D3
B14	PA14 (JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
B15	Pl2 **	I/O	GPIO_Output	DEBUG_GPIO_0
B17	PH14 *	I/O	FDCAN1_RX	FDCAN2_RX
C1	PC15-OSC32_OUT (OSC32_OUT) *	I/O	RCC_OSC32_OUT	OSC32_OUT
C2	PC14-OSC32_IN (OSC32_IN) *	I/O	RCC_OSC32_IN	OSC32_IN
C3	PE2 *	I/O	ETH_TXD3	MII_TXD3
C4	PE0 *	I/O	FMC_NBL0	
C6	PB3 (JTDO/TRACESWO)	I/O	DEBUG_JTDO-SWO	
C 7	PK6 *	I/O	LTDC_B7	

Pin Number	Pin Name	Pin Type	Alternate	Label
TFBGA240	(function after		Function(s)	
	reset)		,	
C8	PK3 *	I/O	LTDC_B4	
C9	PG12 *	I/O	ETH_TXD1	MII_TXD1
C10	VSS	Power	_	_
C11	PD7 **	I/O	GPIO_Input	LCD_DISP
C12	PC12 *	I/O	SDMMC1_CK	SDIO1_CK
C13	VSS	Power		
C15	PA13 (JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
C16	VSS	Power		
C17	VDDLDO	Power		
D1	PE5 *	I/O	SAI4_CK2	
D2	PE4 *	I/O	SAI4_D2	
D4	PB9 *	I/O	SDMMC1_D5	SDIO1_D5
D5	PB8 *	I/O	SDMMC1_D4	SDIO1_D4
D6	PG15 *	I/O	FMC_SDNCAS	
D7	PK7 *	I/O	LTDC_DE	
D9	PG13 *	I/O	ETH_TXD0	MII_TXD0
D10	PJ14 *	I/O	LTDC_B2	
D11	PJ12 *	I/O	LTDC_B0	
D12	PD2 *	I/O	SDMMC1_CMD	SDIO1_CMD
D13	PD0 *	I/O	FMC_D2	
D14	PA10 **	I/O	GPIO_Input	USB_OTG_FS2_ID
D15	PA9 *	I/O	USB_OTG_FS_VBUS	VBUS_FS2
D16	PH13 *	I/O	FDCAN1_TX	FDCAN1_TX
D17	VCAP	Power		
E1	VLXSMPS	Power		
E2	PI9 *	I/O	LTDC_VSYNC	
E3	PC13 **	I/O	GPIO_Input	B1 [Blue PushButton]
E6	VDD	Power		
E7	PDR_ON	Reset		
E8	воото	Boot		
E9	VDD	Power		
E10	PJ13 *	I/O	LTDC_B1	
E11	VDD	Power		
E12	PD1 *	I/O	FMC_D3	
E13	PC8 *	I/O	SDMMC1_D0	SDIO1_D0
E14	PC9 *	I/O	SDMMC1_D1	SDIO1_D1
E16	PA12 *	I/O	USB_OTG_FS_DP	USB_OTG_FS2_P
E17	PA11 *	I/O	USB_OTG_FS_DM	USB_OTG_FS2_N
F1	VDDSMPS	Power		

TEDC A 2.40		Pin Type	Alternate	Label
TFBGA240	(function after		Function(s)	
	reset)		,	
F2	VSSSMPS	Power		
F3	PI10 *	I/O	ETH_RX_ER	MII_RX_ER
F5	VDD	Power		
F13	PC7 *	I/O	SDMMC1_D7	SDIO1_D7
F14	PC6 *	I/O	SDMMC1_D6	SDIO1_D6
F15	PG8 *	I/O	FMC_SDCLK	
F17	VDD33_USB	Power		
G1	PF2 *	I/O	FMC_A2	
G2	VFBSMPS	Power		
G3	PF1 *	I/O	FMC_A1	
G4	PF0 *	I/O	FMC_A0	
G5	VDD	Power		
G7	VSS	Power		
G8	VSS	Power		
G9	VSS	Power		
G10	VSS	Power		
G11	VSS	Power		
G13	VDD	Power		
G14	PG5 *	I/O	FMC_BA1	
G16	VSS	Power		
G17	VDD50_USB	Power		
H1	PI12 *	I/O	LTDC_HSYNC	
H2	PI13 **	I/O	GPIO_Output	LD2 [Green Led]
H3	PI14 *	I/O	LTDC_CLK	
H4	PF3 *	I/O	FMC_A3	
H5	VDD	Power		
H7	VSS	Power		
H8	VSS	Power		
H9	VSS	Power		
H10	VSS	Power		
H11	VSS	Power		
H13	VDD	Power		
H14	PG4 *	I/O	FMC_BA0	
H16	PG2	I/O	GPIO_EXTI2	LCD_INT
H17	PK2 *	I/O	LTDC_G7	
J1	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	OSC_OUT
J2	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	OSC_IN
J3	VSS	Power		
J4	PF5 *	I/O	FMC_A5	

Pin Number	Pin Name	Pin Type	Alternate	Label
TFBGA240	(function after		Function(s)	
	reset)			
J5	PF4 *	I/O	FMC_A4	
J7	VSS	Power		
J8	VSS	Power		
J9	VSS	Power		
J10	VSS	Power		
J11	VSS	Power		
J13	VDD	Power		
J14	PK0 **	I/O	GPIO_Input	LCD_BL
J16	VSS	Power		
J17	VSS	Power		
K1	NRST	Reset		
K2	PF6 *	I/O	QUADSPI_BK1_IO3	
K3	PF7 *	I/O	QUADSPI_BK1_IO2	
K4	PF8	I/O	ADC3_INP7	MEMS_AIN_2
K5	VDD	Power		
K7	VSS	Power		
K8	VSS	Power		
K 9	VSS	Power		
K10	VSS	Power		
K11	VSS	Power		
K13	VDD	Power		
K14	PJ11 *	I/O	LTDC_G4	
K15	VSS	Power		
K16	NC	NC		
K17	NC	NC		
L1	VDDA	Power		
L2	PC0	I/O	ADC1_INP10	MEMS_AIN_1
L3	PF10 *	I/O	QUADSPI_CLK	
L4	PF9 *	I/O	QUADSPI_BK1_IO1	
L5	VDD	Power		
L7	VSS	Power		
L8	VSS	Power		
L9	VSS	Power		
L10	VSS	Power		
L11	VSS	Power		
L13	VDD	Power		
L14	PJ10 *	I/O	LTDC_G3	
L15	VSS	Power		
L16	NC	NC		

Pin Number	Pin Name	Pin Type	Alternate	Label
TFBGA240	(function after		Function(s)	
	reset)		()	
L17	NC	NC		
M2	PC1 *	I/O	ETH_MDC	MII_MDC
M3	PC2 *	I/O	ETH_TXD2	MII_TXD2
M4	PC3 *	I/O	ETH_TX_CLK	MII_TX_CLK
M5	VDD	Power		
M13	VDD	Power		
M14	PJ9 *	I/O	LTDC_G2	
M15	VSS	Power		
M16	NC	NC		
M17	NC	NC		
N1	VREF-	Power		
N2	PH2 *	I/O	ETH_CRS	MII_CRS
N3	PA2 *	I/O	ETH_MDIO	MII_MDIO
N4	PA1 *	I/O	ETH_RX_CLK	MII_RX_CLK
N6	PJ0 *	I/O	LTDC_R1	
N7	VDD	Power		
N8	VDD	Power		
N9	PE10 *	I/O	FMC_D7	
N10	VDD	Power		
N11	VDD	Power		
N12	VDD	Power		
N13	PJ8 *	I/O	LTDC_G1	
N14	PJ7 *	I/O	LTDC_G0	
N15	PJ6 *	I/O	LTDC_R7	
N16	VSS	Power		
N17	NC	NC		
P1	VSSA	Power		
P2	PH3 *	I/O	ETH_COL	MII_COL
P4	PH5 *	I/O	FMC_SDNWE	
P5	PI15 *	I/O	LTDC_R0	
P6	PJ1 *	I/O	LTDC_R2	
P7	PF13 *	I/O	FMC_A7	
P8	PF14 *	I/O	FMC_A8	
P9	PE9 *	I/O	FMC_D6	
P10	PE11 *	I/O	FMC_D8	
P11	PB10	I/O	USART3_TX	VCP_TX
P12	PB11	I/O	USART3_RX	VCP_RX
P14	PH11	I/O	GPIO_EXTI11	USB_OTG_FS2_OverCurre nt

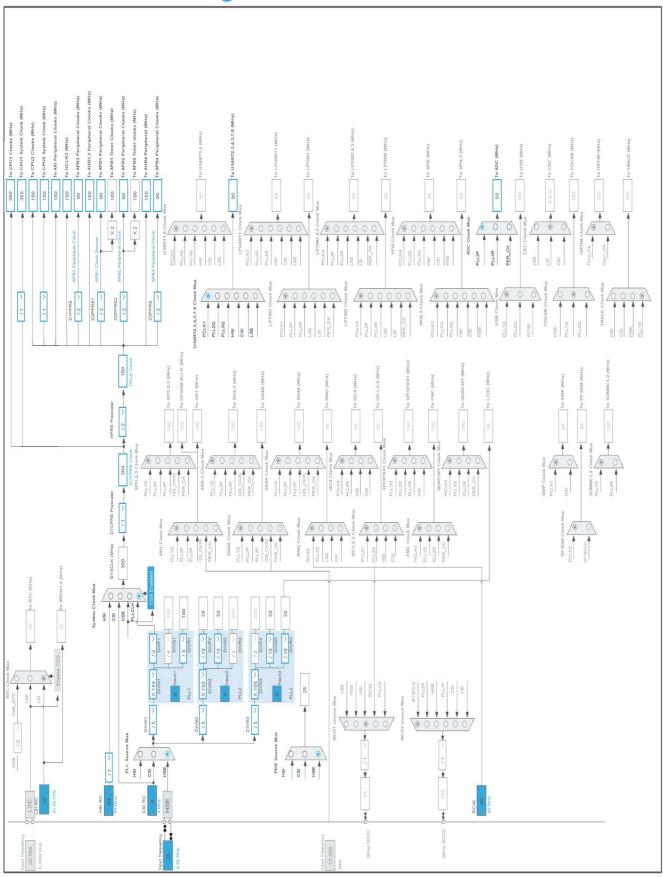
Pin Number	Pin Name	Pin Type	Alternate	Label
TFBGA240	(function after		Function(s)	
	reset)			
P15	PD15 *	I/O	FMC_D1	
P16	PD14 *	I/O	FMC_D0	
P17	VDD	Power		
R1	PC2_C	I/O	ADC3_INP0	MEMS_AIN_5
R2	PC3_C	I/O	ADC3_INP1	MEMS_AIN_6
R4	VSS	Power		
R5	PA7 *	I/O	ETH_RX_DV	MII_RX_DV
R7	PF12 *	I/O	FMC_A6	
R8	VSS	Power		
R9	PF15 *	I/O	FMC_A9	
R10	PE12 *	I/O	FMC_D9	
R11	PE15 *	I/O	FMC_D12	
R12	PJ5 *	I/O	LTDC_R6	
R13	PH9 *	I/O	LTDC_R3	
R15	PD11 *	I/O	QUADSPI_BK1_IO0	
T1	PA0_C	I/O	ADC1_INP0	MEMS_AIN_3
T2	PA1_C	I/O	ADC1_INP1	MEMS_AIN_4
T4	PC4 *	I/O	ETH_RXD0	MII_RXD0
T5	PB1 *	I/O	ETH_RXD3	MII_RXD3
T6	PJ2 **	I/O	GPIO_Output	LD1 [Red Led]
T7	PF11 *	I/O	FMC_SDNRAS	
T8	PG0 *	I/O	FMC_A10	
T 9	PE8 *	I/O	FMC_D5	
T10	PE13 *	I/O	FMC_D10	
T11	PH6 *	I/O	FMC_SDNE1	
T12	VSS	Power		
T14	PB12 **	I/O	GPIO_Output	LCD_RST
T16	PD10 *	I/O	FMC_D15	
T17	PD9 *	I/O	FMC_D14	
U1	VSS	Power		
U4	PC5 *	I/O	ETH_RXD1	MII_RXD1
U5	PB0 *	I/O	ETH_RXD2	MII_RXD2
U6	PJ3 *	I/O	LTDC_R4	
U7	PJ4 *	I/O	LTDC_R5	
U8	PG1 *	I/O	FMC_A11	
U9	PE7 *	I/O	FMC_D4	
U10	PE14 *	I/O	FMC_D11	
U11	VCAP	Power		
U12	VDDLDO	Power		

Pin Number TFBGA240	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
U13	PH7 *	I/O	FMC_SDCKE1	
U14	PB13 *	I/O	FDCAN2_TX	FDCAN2_TX
U16	PD8 *	I/O	FMC_D13	
U17	VSS	Power		

^{**} The pin is affected with an I/O function

^{*} The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	Sonus DSP Subsystem
Project Folder	C:\Users\Owner\MegaMachineSTM32Work\PhononsPhotons-
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.9.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	M4-0x200
Minimum Stack Size	M4-0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls ARM Cortex-M7

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC

5.4. Advanced Settings - Generated Function Calls ARM Cortex-M4

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	MX_ADC1_Init	ADC1

Rank	Function Name	Peripheral Instance Name
4	MX_ADC3_Init	ADC3
5	MX_USART3_UART_Init	USART3
6	MX_TIM3_Init	TIM3

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32H7
Line	STM32H745/755
MCU	STM32H745XIHx
Datasheet	DS12923_Rev1

1.2. Parameter Selection

Temperature	25
Vdd	3.0

1.3. Battery Selection

Battery	Li-SOCL2(DD36000)
Capacity	36000.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	450.0 mA
Max Pulse Current	1000.0 mA
Cells in series	1
Cells in parallel	1

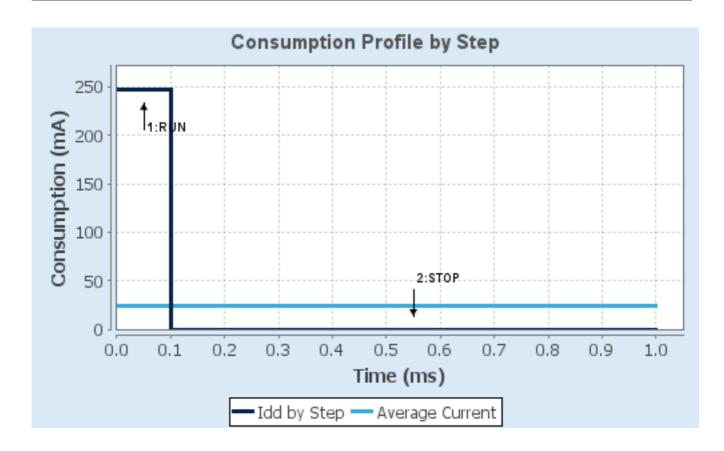
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0: Scale0	SVOS5: System-Scale5
D1 Mode	DRUN/CRUN	DSTANDBY
D2 Mode	DRUN/CRUN	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	CM7: ITCM/Cache / CM4: FLASH B/ART	CM7: NA / CM4: NA
CM7 Frequency	480 MHz	0 Hz
Clock Configuration	HSE BYP PLL ALL IPs ON	LSE Flash-ON
CM4 Frequency	240 MHz	0 Hz
Clock Source Frequency	25 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	247 mA	145 µA
Duration	0.1 ms	0.9 ms
DMIPS	1027.0	0.0
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	24.83 mA
Battery Life	1 month, 29 days,	Average DMIPS	1027.2001
	21 hours	_	DMIPS

1.6. Chart



2. Peripherals and Middlewares Configuration

2.1. ADC1 mode: IN0

IN1: IN1 Single-ended IN10: IN10 Single-ended 2.1.1. Parameter Settings:

Core(s) Settings:

Context(s): Cortex-M4

Initialized Context: Cortex-M4

Power Domain: D2

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler Asynchronous clock mode divided by 2

Resolution ADC 16-bit resolution

Scan Conversion Mode Enabled
Continuous Conversion Mode Disabled
Discontinuous Conversion Mode Disabled

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data overwritten *

Left Bit Shift No bit shift

Conversion Data Management Mode * DMA Circular Mode *

Low Power Auto Wait Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions Enable
Enable Regular Oversampling Disable
Number Of Conversion 3 *

External Trigger Conversion Source

Timer 3 Trigger Out event *

External Trigger Conversion Edge

Trigger detection on the rising edge

Rank

Channel 10 *

Sampling Time 16.5 Cycles *

Offset Number No offset
Offset Signed Saturation Disable
Rank 2 *

Channel Channel 0

Sampling Time

16.5 Cycles *

Offset Number No offset
Offset Signed Saturation Disable
Rank 3 *

Channel 1 *
Sampling Time Channel 1 *

Offset Number No offset
Offset Signed Saturation Disable

ADC_Injected_ConversionMode:

Enable Injected Conversions Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode false

2.2. ADC3 mode: IN0

IN1: IN1 Single-ended

mode: IN7

2.2.1. Parameter Settings:

Core(s) Settings:

Context(s): Cortex-M4

Initialized Context: Cortex-M4

Power Domain: D3

ADC_Settings:

Clock Prescaler Asynchronous clock mode divided by 2

Resolution ADC 16-bit resolution

Scan Conversion Mode Enabled
Continuous Conversion Mode Disabled
Discontinuous Conversion Mode Disabled

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data overwritten *

Left Bit Shift No bit shift

Low Power Auto Wait Disabled ADC_Regular_ConversionMode: Enable **Enable Regular Conversions** Disable **Enable Regular Oversampling Number Of Conversion** 3 * External Trigger Conversion Source Timer 3 Trigger Out event * External Trigger Conversion Edge Trigger detection on the rising edge 1 Rank Channel Channel 7 * Sampling Time 16.5 Cycles * No offset Offset Number Disable Offset Signed Saturation Rank 2 * Channel Channel 0 Sampling Time 16.5 Cycles * Offset Number No offset Offset Signed Saturation Disable Rank 3 * Channel Channel 1 * Sampling Time 16.5 Cycles * No offset Offset Number Offset Signed Saturation Disable ADC_Injected_ConversionMode: **Enable Injected Conversions** Disable **Analog Watchdog 1:** Enable Analog WatchDog1 Mode false **Analog Watchdog 2:** Enable Analog WatchDog2 Mode false **Analog Watchdog 3:** Enable Analog WatchDog3 Mode false **2.3. DEBUG Debug: Trace Asynchronous Sw** 2.3.1. Core(s) Settings: Context(s):

Cortex-M7
Cortex-M4

Initialized Context: Cortex-M7

Power Domain:

2.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

2.4.1. Parameter Settings:

Core(s) Settings:

Context(s): Cortex-M7

Cortex-M4

Initialized Context: Cortex-M7

Power Domain: D3

Power Parameters:

SupplySource PWR_DIRECT_SMPS_SUPPLY
Power Regulator Voltage Scale Power Regulator Voltage Scale 1

RCC Parameters:

TIM Prescaler Selection Disabled
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000
CSI Calibration Value 16
HSI Calibration Value 32

System Parameters:

VDD voltage (V) 3.3

Flash Latency(WS) 2 WS (3 CPU cycle)

Product revision rev.Y

PLL range Parameters:

PLL1 clock Input range

PLL2 input frequency range

Between 4 and 8 MHz

PLL1 clock Output range

Wide VCO range

PLL2 clock Output range

Wide VCO range

2.5. SYS

Timebase Source: SysTick

2.5.1. Core(s) Settings:

Context(s):

Cortex-M7

Initialized Context: Cortex-M7

Power Domain:

2.6. SYS_M4

Timebase Source: SysTick

2.6.1. Core(s) Settings:

Context(s): Cortex-M4

Initialized Context: Cortex-M4

Power Domain:

2.7. TIM3

Clock Source: Internal Clock
Channel1: PWM Generation CH1

Channel4: PWM Generation No Output

2.7.1. Parameter Settings:

Core(s) Settings:

Context(s): Cortex-M4

Initialized Context: Cortex-M4

Power Domain: D2

Counter Settings:

Internal Clock Division (CKD)

Prescaler (PSC - 16 bits value) 0
Counter Mode Up
Counter Period (AutoReload Register - 16 bits value) 750 *

auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

No Division

Trigger Event Selection TRGO Update Event *

Clear Input:

Clear Input Source Disable

PWM Generation Channel 1:

Mode PWM mode 2 *

Pulse (16 bits value)

Output compare preload

Fast Mode

CH Polarity

400 *

Disable

High

PWM Generation Channel 4:

Mode PWM mode 2 *

Pulse (16 bits value)

Output compare preload

Fast Mode

CH Polarity

400 *

Disable

High

2.8. **USART3**

Mode: Asynchronous

2.8.1. Parameter Settings:

Core(s) Settings:

Context(s): Cortex-M4

Initialized Context: Cortex-M4

Power Domain: D2

Basic Parameters:

Baud Rate 4000000 *

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable
ClockPrescaler 1
Fifo Mode Disable

Txfifo Threshold 1 eighth full configuration
Rxfifo Threshold 1 eighth full configuration

Advanced Features:

Auto Baudrate Disable

TX Pin Active Level Inversion Disable

RX Pin Active Level Inversion Disable

Data Inversion Disable

TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

^{*} User modified value

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max	User Label	Context	Power
				down	Speed			Domain
ADC1	PC0	ADC1_INP10	Analog mode	No pull-up and no pull- down	n/a	MEMS_AIN_1	Cortex-M4	D2
	PA0_C	ADC1_INP0	Analog mode	No pull-up and no pull- down	n/a	MEMS_AIN_3	Cortex-M4	D2
	PA1_C	ADC1_INP1	Analog mode	No pull-up and no pull- down	n/a	MEMS_AIN_4	Cortex-M4	D2
ADC3	PF8	ADC3_INP7	Analog mode	No pull-up and no pull- down	n/a	MEMS_AIN_2	Cortex-M4	D3
	PC2_C	ADC3_INP0	Analog mode	No pull-up and no pull- down	n/a	MEMS_AIN_5	Cortex-M4	D3
	PC3_C	ADC3_INP1	Analog mode	No pull-up and no pull- down	n/a	MEMS_AIN_6	Cortex-M4	D3
DEBUG	PA14 (JTCK/S WCLK)	DEBUG_JTC K-SWCLK	n/a	n/a	n/a		Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PB3 (JTDO/TR ACESWO	DEBUG_JTD O-SWO	n/a	n/a	n/a		Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PA13 (JTMS/S WDIO)	DEBUG_JTM S-SWDIO	n/a	n/a	n/a		Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
RCC	PH1- OSC_OU T (PH1)	RCC_OSC_ OUT	n/a	n/a	n/a	OSC_OUT	Cortex-M7* Cortex-M4	D3
	PH0- OSC_IN (PH0)	RCC_OSC_I N	n/a	n/a	n/a	OSC_IN	Cortex-M7* Cortex-M4	D3
TIM3	PB4 (NJTRST)	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull- down	Low		Cortex-M4	D2
USART3	PB10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull- down	Low	VCP_TX	Cortex-M4	D2
	PB11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull- down	Low	VCP_RX	Cortex-M4	D2
Single Mapped	PI6	SAI2_SD_A	Alternate Function Push Pull	No pull-up and no pull- down	Low			
Signals	PI5	SAI2_SCK_A	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PI4	SAI2_MCLK_ A	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PB5	FDCAN2_RX	Alternate Function Push Pull	No pull-up and no pull- down	Low	FDCAN2_RX		

IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max Speed	User Label	Context	Power Domain
	PK5	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PG10	SAI2_SD_B	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PC10	SDMMC1_D 2	Alternate Function Push Pull	No pull-up and no pull- down	Very High	SDIO1_D2		
	PI1	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PI0	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PI7	SAI2_FS_A	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PB6	QUADSPI_B K1_NCS	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PK4	LTDC_B5	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull- down	Low	MII_TX_EN		
	PJ15	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull- down	Low	LCD_DISP		
	PC11	SDMMC1_D	Alternate Function Push Pull	No pull-up and no pull- down	Very High	SDIO1_D3		
	PH14	FDCAN1_RX	Alternate Function Push Pull	No pull-up and no pull- down	Low	FDCAN2_RX		
	PC15- OSC32_ OUT	RCC_OSC32 _OUT	n/a	n/a	n/a	OSC32_OUT		
	PC14- OSC32_I N	RCC_OSC32 _IN	n/a	n/a	n/a	OSC32_IN		
	PE2	ETH_TXD3	Alternate Function Push Pull	No pull-up and no pull- down	Low	MII_TXD3		
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PK6	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PK3	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PG12	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull- down	Low	MII_TXD1		
	PC12	SDMMC1_C K	Alternate Function Push Pull	No pull-up and no pull- down	Very High	SDIO1_CK		
	PE5	SAI4_CK2	Alternate Function	No pull-up and no pull-	Low			

IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max Speed	User Label	Context	Power Domain
			Push Pull	down	Opoda			201110111
	PE4	SAI4_D2	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PB9	SDMMC1_D 5	Alternate Function Push Pull	No pull-up and no pull- down	Very High	SDIO1_D5		
	PB8	SDMMC1_D 4	Alternate Function Push Pull	No pull-up and no pull- down	Very High	SDIO1_D4		
	PG15	FMC_SDNC AS	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PK7	LTDC_DE	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull- down	Low	MII_TXD0		
	PJ14	LTDC_B2	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PJ12	LTDC_B0	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PD2	SDMMC1_C MD	Alternate Function Push Pull	No pull-up and no pull- down	Very High	SDIO1_CMD		
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PA9	USB_OTG_F S_VBUS	n/a	n/a	n/a	VBUS_FS2		
	PH13	FDCAN1_TX	Alternate Function Push Pull	No pull-up and no pull- down	Low	FDCAN1_TX		
	PI9	LTDC_VSYN C	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PJ13	LTDC_B1	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PC8	SDMMC1_D 0	Alternate Function Push Pull	No pull-up and no pull- down	Very High	SDIO1_D0		
	PC9	SDMMC1_D 1	Alternate Function Push Pull	No pull-up and no pull- down	Very High	SDIO1_D1		
	PA12	USB_OTG_F S_DP	Alternate Function Push Pull	No pull-up and no pull- down	Low	USB_OTG_FS2_P		
	PA11	USB_OTG_F S_DM	Alternate Function Push Pull	No pull-up and no pull- down	Low	USB_OTG_FS2_N		
	PI10	ETH_RX_ER	Alternate Function Push Pull	No pull-up and no pull- down	Low	MII_RX_ER		
	PC7	SDMMC1_D 7	Alternate Function Push Pull	No pull-up and no pull- down	Very High	SDIO1_D7		
	PC6	SDMMC1_D 6	Alternate Function Push Pull	No pull-up and no pull- down	Very High	SDIO1_D6		

IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max Speed	User Label	Context	Power Domain
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PG5	FMC_BA1	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PI12	LTDC_HSYN C	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PI14	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PK2	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PF6	QUADSPI_B K1_IO3	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PF7	QUADSPI_B K1_IO2	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PJ11	LTDC_G4	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PF10	QUADSPI_C LK	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PF9	QUADSPI_B K1_IO1	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PJ10	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull- down	Low	MII_MDC		
	PC2	ETH_TXD2	Alternate Function Push Pull	No pull-up and no pull- down	Low	MII_TXD2		
	PC3	ETH_TX_CL K	Alternate Function Push Pull	No pull-up and no pull- down	Low	MII_TX_CLK		
	PJ9	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PH2	ETH_CRS	Alternate Function	No pull-up and no pull-	Low	MII_CRS		

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
			Push Pull	down				
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull- down	Low	MII_MDIO		
	PA1	ETH_RX_CL K	Alternate Function Push Pull	No pull-up and no pull- down	Low	MII_RX_CLK		
	PJ0	LTDC_R1	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PJ8	LTDC_G1	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PJ7	LTDC_G0	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PJ6	LTDC_R7	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PH3	ETH_COL	Alternate Function Push Pull	No pull-up and no pull- down	Low	MII_COL		
	PH5	FMC_SDNW E	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PI15	LTDC_R0	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PJ1	LTDC_R2	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PA7	ETH_RX_DV	Alternate Function Push Pull	No pull-up and no pull- down	Low	MII_RX_DV		
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull- down	Very High			

IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max Speed	User Label	Context	Power Domain
	PJ5	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PH9	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PD11	QUADSPI_B K1_IO0	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull- down	Low	MII_RXD0		
	PB1	ETH_RXD3	Alternate Function Push Pull	No pull-up and no pull- down	Low	MII_RXD3		
	PF11	FMC_SDNR AS	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PH6	FMC_SDNE1	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull- down	Low	MII_RXD1		
	PB0	ETH_RXD2	Alternate Function Push Pull	No pull-up and no pull- down	Low	MII_RXD2		
	PJ3	LTDC_R4	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PJ4	LTDC_R5	Alternate Function Push Pull	No pull-up and no pull- down	Low			
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PH7	FMC_SDCK E1	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
	PB13	FDCAN2_TX	Alternate Function Push Pull	No pull-up and no pull- down	Low	FDCAN2_TX		
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull- down	Very High			
GPIO	PD3	GPIO_Input	Input mode	Pull-up *	n/a	DEBUG_EN_IN	Cortex-M4	Cortex-M4

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
	PI2	GPIO_Output	Output Push Pull	No pull-up and no pull- down	Low	DEBUG_GPIO_0	Cortex-M4	Cortex-M4
	PD7	GPIO_Input	Input mode	No pull-up and no pull- down	n/a	LCD_DISP		
	PA10	GPIO_Input	Input mode	No pull-up and no pull- down	n/a	USB_OTG_FS2_ID		
	PC13	GPIO_Input	Input mode	No pull-up and no pull- down	n/a	B1 [Blue PushButton]	Cortex-M4	Cortex-M4
	PI13	GPIO_Output	Output Push Pull	No pull-up and no pull- down	Low	LD2 [Green Led]	Cortex-M4	Cortex-M4
	PG2	GPIO_EXTI2	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull- down	n/a	LCD_INT		
	PK0	GPIO_Input	Input mode	No pull-up and no pull- down	n/a	LCD_BL		
	PH11	GPIO_EXTI1	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull- down	n/a	USB_OTG_FS2_Ov erCurrent		
	PJ2	GPIO_Output	Output Push Pull	No pull-up and no pull- down	Low	LD1 [Red Led]	Cortex-M4	Cortex-M4
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull- down	Low	LCD_RST		

^{*} Initialized context

3.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Stream0	Peripheral To Memory	High *
ADC3	DMA1_Stream1	Peripheral To Memory	High *
USART3 TX	DMA1_Stream7	Memory To Peripheral	Low

ADC1: DMA1_Stream0 DMA request Settings:

Mode: Circular *
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Half Word
Memory Data Width: Half Word

ADC3: DMA1_Stream1 DMA request Settings:

Mode: Circular *
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Half Word
Memory Data Width: Half Word

USART3_TX: DMA1_Stream7 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Byte
Memory Data Width: Byte

3.3. BDMA configuration

nothing configured in DMA service

3.4. MDMA configuration

nothing configured in DMA service

3.5. NVIC configuration

3.5.1. NVIC1

Interrupt Table	Enable	Preenmption Priority	SubPriority		
Non maskable interrupt	true	0	0		
Hard fault interrupt	true	0	0		
Memory management fault	true	0	0		
Pre-fetch fault, memory access fault	true	0	0		
Undefined instruction or illegal state	true	0	0		
System service call via SWI instruction	true	0	0		
Debug monitor	true	0	0		
Pendable request for system service	true	0	0		
System tick timer	true	0	0		
PVD and AVD interrupts through EXTI line 16	unused				
Flash global interrupt	unused				
RCC global interrupt		unused			
EXTI line2 interrupt		unused			
EXTI line[15:10] interrupts		unused			
CM4 send event interrupt for CM7	unused				
FPU global interrupt	unused				
HSEM1 global interrupt	unused				
RAM ECC diagnostic global interrupt	unused				
Hold core interrupt	unused				

3.5.2. NVIC1 Code generation

Enabled interrupt Table	Select for init Sequence ordering Generate IRQ handler		Call HAL handler	
	sequence ordering	Hariotei		
Non maskable interrupt	false	true	true	
Hard fault interrupt	false	true	false	
Memory management fault	false	true	false	
Pre-fetch fault, memory access fault	false	true	false	
Undefined instruction or illegal state	false	true	false	
System service call via SWI instruction	false	true	false	
Debug monitor	false	true	false	
Pendable request for system service	false	true	false	
System tick timer	false	true	true	

3.5.3. NVIC2

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0

Interrupt Table	Enable	Preenmption Priority	SubPriority		
Hard fault interrupt	true	0	0		
Memory management fault	true	0	0		
Pre-fetch fault, memory access fault	true	0	0		
Undefined instruction or illegal state	true	0	0		
System service call via SWI instruction	true	0	0		
Debug monitor	true	0	0		
Pendable request for system service	true	0	0		
System tick timer	true	0	0		
DMA1 stream0 global interrupt	true	0	0		
DMA1 stream1 global interrupt	true	0	0		
USART3 global interrupt	true	0	0		
DMA1 stream7 global interrupt	true	0	0		
PVD and AVD interrupts through EXTI line 16	unused				
Flash global interrupt		unused			
EXTI line2 interrupt		unused			
ADC1 and ADC2 global interrupts		unused			
TIM3 global interrupt		unused			
EXTI line[15:10] interrupts		unused			
CM7 send event interrupt for CM4		unused			
FPU global interrupt		unused			
HSEM2 global interrupt		unused			
ADC3 global interrupt	unused				
RAM ECC diagnostic global interrupt	unused				
Hold core interrupt	unused				

3.5.4. NVIC2 Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	true
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false true		false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 stream0 global interrupt	false	true	true
DMA1 stream1 global interrupt	false	true	true
USART3 global interrupt	false	true	true
DMA1 stream7 global interrupt	false	true	true

Sonus DSP Subsystem	Project
Configuration	Report

User modified value			

4. System Views

4.1. Category view

4.1.1. Current

4. 1.Z. WILLIOUL HILEIS	4.1.2.	Without	filters
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4.2. Context Execution view		

4.3. Context Initialization view	

4.4. Power Domain view	
4.4. I Ower Domain view	

5. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl_model/stm32h7_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip

System View https://www.st.com/resource/en/svd/stm32h7-svd.zip

Description

Presentations https://www.st.com/resource/en/product_presentation/microcontrollers_st

m32h7_series_product_overview.pdf

Presentations https://www.st.com/resource/en/product_presentation/stm32-

stm8_embedded_software_solutions.pdf

Presentations https://www.st.com/resource/en/product_presentation/stm32_eval-

tools_portfolio.pdf

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onal-safety-packages.pdf

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Brochures https://www.st.com/resource/en/brochure/brstm32h7.pdf
Brochures https://www.st.com/resource/en/brochure/brstm32h7vl.pdf

Brochures https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-

and-smart-i-os.pdf

Flyers https://www.st.com/resource/en/flyer/flstm32nucleo.pdf

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discharge-sensitivity-measurement-stmicroelectronics.pdf

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guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf

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- Application Notes https://www.st.com/resource/en/application_note/an2867-oscillator-design-guide-for-stm8afals-stm32-mcus-and-mpus-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an3126-audio-and-waveform-generation-using-the-dac-in-stm32-products-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an3155-usart-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an3156-usb-dfu-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4013-stm32-crossseries-timer-overview-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4221-i2c-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4229-how-to-implement-a-vocoder-solution-using-stm32-microcontrollers-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4277-using-stm32-device-pwm-shutdown-features-for-motor-control-and-digital-power-conversion-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4286-spi-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4539-hrtim-cookbook-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4566-extending-the-dac-performance-of-stm32-microcontrollers-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4635-minimization-of-power-consumption-using-lpuart-for-stm32-microcontrollers-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4655-virtually-increasing-the-number-of-serial-communication-peripherals-in-stm32-applications-stmicroelectronics.pdf

- Application Notes https://www.st.com/resource/en/application_note/an4750-handling-of-soft-errors-in-stm32-applications-stmicroelectronics.pdf
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- Application Notes https://www.st.com/resource/en/application_note/an4776-generalpurpose-timer-cookbook-for-stm32-microcontrollers-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4803-highspeed-si-simulations-using-ibis-and-boardlevel-simulations-using-hyperlynx-si-on-stm32-mcus-and-mpus-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4839-level-1-cache-on-stm32f7-series-and-stm32h7-series-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4861-lcdtft-display-controller-ltdc-on-stm32-mcus-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4908-stm32-usart-automatic-baud-rate-detection-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4989-stm32-microcontroller-debug-toolbox-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4990-getting-started-with-sigmadelta-digital-interface-on-applicable-stm32-microcontrollers-stmicroelectronics.pdf
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