
STM32
CubeMX

1. Description

1.1. Project

Project Name	PhonPhot_Complete_System
Board Name	custom
Generated with:	STM32CubeMX 6.10.0
Date	02/02/2024

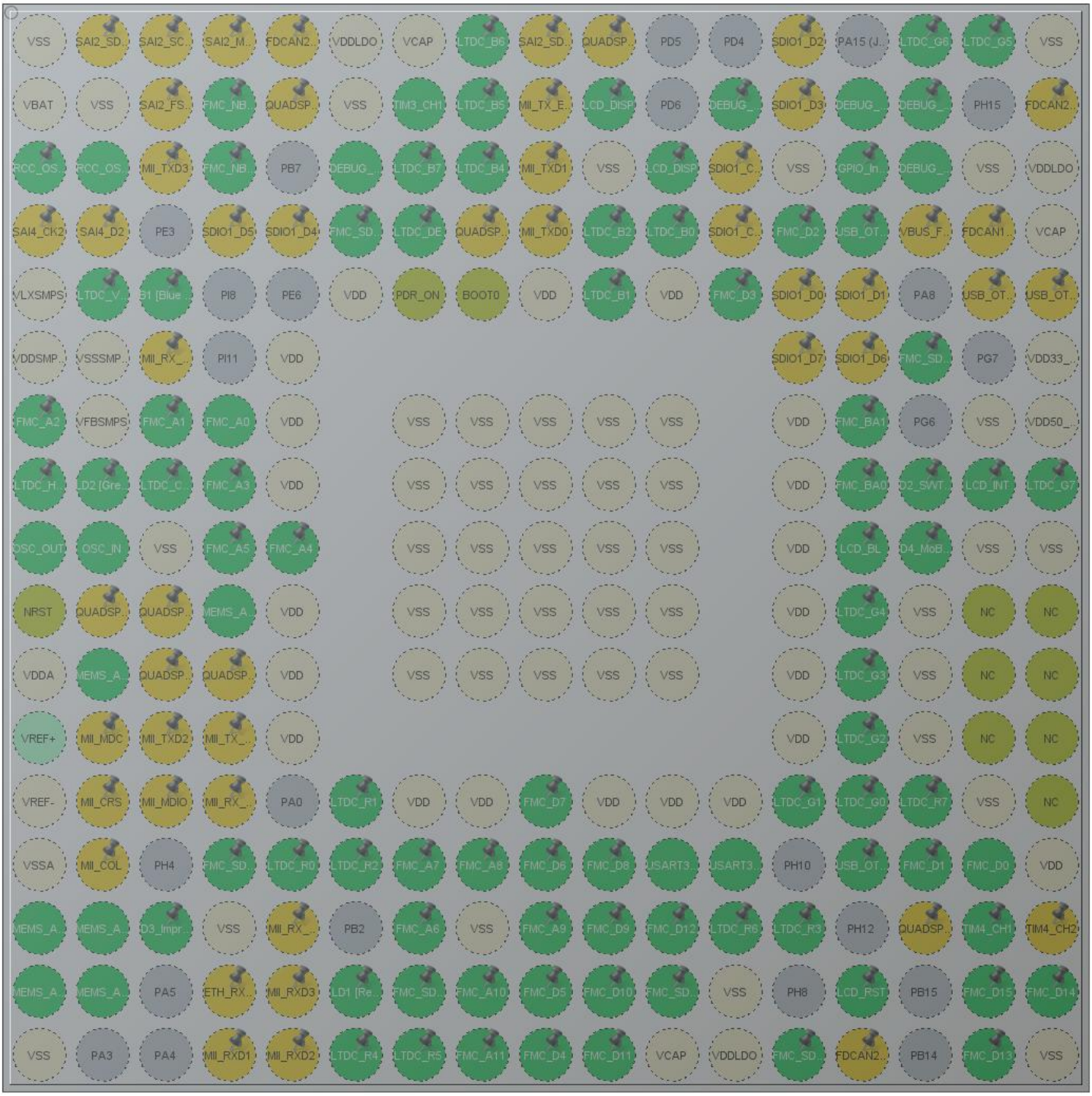
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H745/755
MCU name	STM32H745XIHx
MCU Package	TFBGA240
MCU Pin number	265

1.3. Core(s) information

Core(s)	ARM Cortex-M7 ARM Cortex-M4

2. Pinout Configuration



TFBGA240 +25 (Top view)

3. Pins Configuration

Pin Number TFBGA240	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A1	VSS	Power		
A2	PI6 *	I/O	SAI2_SD_A	
A3	PI5 *	I/O	SAI2_SCK_A	
A4	PI4 *	I/O	SAI2_MCLK_A	
A5	PB5 *	I/O	FDCAN2_RX	FDCAN2_RX
A6	VDDLDO	Power		
A7	VCAP	Power		
A8	PK5	I/O	LTDC_B6	
A9	PG10 *	I/O	SAI2_SD_B	
A10	PG9 *	I/O	QUADSPI_BK2_IO2	
A13	PC10 *	I/O	SDMMC1_D2	SDIO1_D2
A15	PI1	I/O	LTDC_G6	
A16	PI0	I/O	LTDC_G5	
A17	VSS	Power		
B1	VBAT	Power		
B2	VSS	Power		
B3	PI7 *	I/O	SAI2_FS_A	
B4	PE1	I/O	FMC_NBL1	
B5	PB6 *	I/O	QUADSPI_BK1_NCS	
B6	VSS	Power		
B7	PB4 (NJTRST)	I/O	TIM3_CH1	
B8	PK4	I/O	LTDC_B5	
B9	PG11 *	I/O	ETH_TX_EN	MII_TX_EN
B10	PJ15	I/O	LTDC_B3	LCD_DISP
B12	PD3 **	I/O	GPIO_Input	DEBUG_EN_IN
B13	PC11 *	I/O	SDMMC1_D3	SDIO1_D3
B14	PA14 (JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
B15	PI2 **	I/O	GPIO_Output	DEBUG_GPIO_0
B17	PH14 *	I/O	FDCAN1_RX	FDCAN2_RX
C1	PC15-OSC32_OUT (OSC32_OUT)	I/O	RCC_OSC32_OUT	
C2	PC14-OSC32_IN (OSC32_IN)	I/O	RCC_OSC32_IN	
C3	PE2 *	I/O	ETH_TXD3	MII_TXD3
C4	PE0	I/O	FMC_NBL0	
C6	PB3 (JTDO/TRACESWO)	I/O	DEBUG_JTDO-SWO	

Pin Number TFBGA240	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
C7	PK6	I/O	LTDC_B7	
C8	PK3	I/O	LTDC_B4	
C9	PG12 *	I/O	ETH_TXD1	MII_TXD1
C10	VSS	Power		
C11	PD7 **	I/O	GPIO_Input	LCD_DISP
C12	PC12 *	I/O	SDMMC1_CK	SDIO1_CK
C13	VSS	Power		
C14	PI3 **	I/O	GPIO_Input	
C15	PA13 (JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
C16	VSS	Power		
C17	VDDLDO	Power		
D1	PE5 *	I/O	SAI4_CK2	
D2	PE4 *	I/O	SAI4_D2	
D4	PB9 *	I/O	SDMMC1_D5	SDIO1_D5
D5	PB8 *	I/O	SDMMC1_D4	SDIO1_D4
D6	PG15	I/O	FMC_SDNCAS	
D7	PK7	I/O	LTDC_DE	
D8	PG14 *	I/O	QUADSPI_BK2_IO3	
D9	PG13 *	I/O	ETH_TXD0	MII_TXD0
D10	PJ14	I/O	LTDC_B2	
D11	PJ12	I/O	LTDC_B0	
D12	PD2 *	I/O	SDMMC1_CMD	SDIO1_CMD
D13	PD0	I/O	FMC_D2	
D14	PA10 **	I/O	GPIO_Input	USB_OTG_FS2_ID
D15	PA9 *	I/O	USB_OTG_FS_VBUS	VBUS_FS2
D16	PH13 *	I/O	FDCAN1_TX	FDCAN1_TX
D17	VCAP	Power		
E1	VLXSMPS	Power		
E2	PI9	I/O	LTDC_VSYNC	
E3	PC13 **	I/O	GPIO_Input	B1 [Blue PushButton]
E6	VDD	Power		
E7	PDR_ON	Reset		
E8	BOOT0	Boot		
E9	VDD	Power		
E10	PJ13	I/O	LTDC_B1	
E11	VDD	Power		
E12	PD1	I/O	FMC_D3	
E13	PC8 *	I/O	SDMMC1_D0	SDIO1_D0
E14	PC9 *	I/O	SDMMC1_D1	SDIO1_D1

Pin Number TFBGA240	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
E16	PA12 *	I/O	USB_OTG_FS_DP	USB_OTG_FS2_P
E17	PA11 *	I/O	USB_OTG_FS_DM	USB_OTG_FS2_N
F1	VDDSMPS	Power		
F2	VSSSMPS	Power		
F3	PI10 *	I/O	ETH_RX_ER	MII_RX_ER
F5	VDD	Power		
F13	PC7 *	I/O	SDMMC1_D7	SDIO1_D7
F14	PC6 *	I/O	SDMMC1_D6	SDIO1_D6
F15	PG8	I/O	FMC_SDCLK	
F17	VDD33_USB	Power		
G1	PF2	I/O	FMC_A2	
G2	VFBSMPS	Power		
G3	PF1	I/O	FMC_A1	
G4	PF0	I/O	FMC_A0	
G5	VDD	Power		
G7	VSS	Power		
G8	VSS	Power		
G9	VSS	Power		
G10	VSS	Power		
G11	VSS	Power		
G13	VDD	Power		
G14	PG5	I/O	FMC_BA1	
G16	VSS	Power		
G17	VDD50_USB	Power		
H1	PI12	I/O	LTDC_HSYNC	
H2	PI13 **	I/O	GPIO_Output	LD2 [Green Led]
H3	PI14	I/O	LTDC_CLK	
H4	PF3	I/O	FMC_A3	
H5	VDD	Power		
H7	VSS	Power		
H8	VSS	Power		
H9	VSS	Power		
H10	VSS	Power		
H11	VSS	Power		
H13	VDD	Power		
H14	PG4	I/O	FMC_BA0	
H15	PG3 **	I/O	GPIO_Input	D2_SWToggle
H16	PG2	I/O	GPIO_EXTI2	LCD_INT
H17	PK2	I/O	LTDC_G7	

Pin Number TFBGA240	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
J1	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	OSC_OUT
J2	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	OSC_IN
J3	VSS	Power		
J4	PF5	I/O	FMC_A5	
J5	PF4	I/O	FMC_A4	
J7	VSS	Power		
J8	VSS	Power		
J9	VSS	Power		
J10	VSS	Power		
J11	VSS	Power		
J13	VDD	Power		
J14	PK0 **	I/O	GPIO_Input	LCD_BL
J15	PK1 **	I/O	GPIO_Input	D4_MoButton
J16	VSS	Power		
J17	VSS	Power		
K1	NRST	Reset		
K2	PF6 *	I/O	QUADSPI_BK1_IO3	
K3	PF7 *	I/O	QUADSPI_BK1_IO2	
K4	PF8	I/O	ADC3_INP7	MEMS_AIN_2
K5	VDD	Power		
K7	VSS	Power		
K8	VSS	Power		
K9	VSS	Power		
K10	VSS	Power		
K11	VSS	Power		
K13	VDD	Power		
K14	PJ11	I/O	LTDC_G4	
K15	VSS	Power		
K16	NC	NC		
K17	NC	NC		
L1	VDDA	Power		
L2	PC0	I/O	ADC1_INP10	MEMS_AIN_1
L3	PF10 *	I/O	QUADSPI_CLK	
L4	PF9 *	I/O	QUADSPI_BK1_IO1	
L5	VDD	Power		
L7	VSS	Power		
L8	VSS	Power		
L9	VSS	Power		
L10	VSS	Power		

Pin Number TFBGA240	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
L11	VSS	Power		
L13	VDD	Power		
L14	PJ10	I/O	LTDC_G3	
L15	VSS	Power		
L16	NC	NC		
L17	NC	NC		
M2	PC1 *	I/O	ETH_MDC	MII_MDC
M3	PC2 *	I/O	ETH_TXD2	MII_TXD2
M4	PC3 *	I/O	ETH_TX_CLK	MII_TX_CLK
M5	VDD	Power		
M13	VDD	Power		
M14	PJ9	I/O	LTDC_G2	
M15	VSS	Power		
M16	NC	NC		
M17	NC	NC		
N1	VREF-	Power		
N2	PH2 *	I/O	ETH_CRS	MII_CRS
N3	PA2 *	I/O	ETH_MDIO	MII_MDIO
N4	PA1 *	I/O	ETH_RX_CLK	MII_RX_CLK
N6	PJ0	I/O	LTDC_R1	
N7	VDD	Power		
N8	VDD	Power		
N9	PE10	I/O	FMC_D7	
N10	VDD	Power		
N11	VDD	Power		
N12	VDD	Power		
N13	PJ8	I/O	LTDC_G1	
N14	PJ7	I/O	LTDC_G0	
N15	PJ6	I/O	LTDC_R7	
N16	VSS	Power		
N17	NC	NC		
P1	VSSA	Power		
P2	PH3 *	I/O	ETH_COL	MII_COL
P4	PH5	I/O	FMC_SDNWE	
P5	PI15	I/O	LTDC_R0	
P6	PJ1	I/O	LTDC_R2	
P7	PF13	I/O	FMC_A7	
P8	PF14	I/O	FMC_A8	
P9	PE9	I/O	FMC_D6	

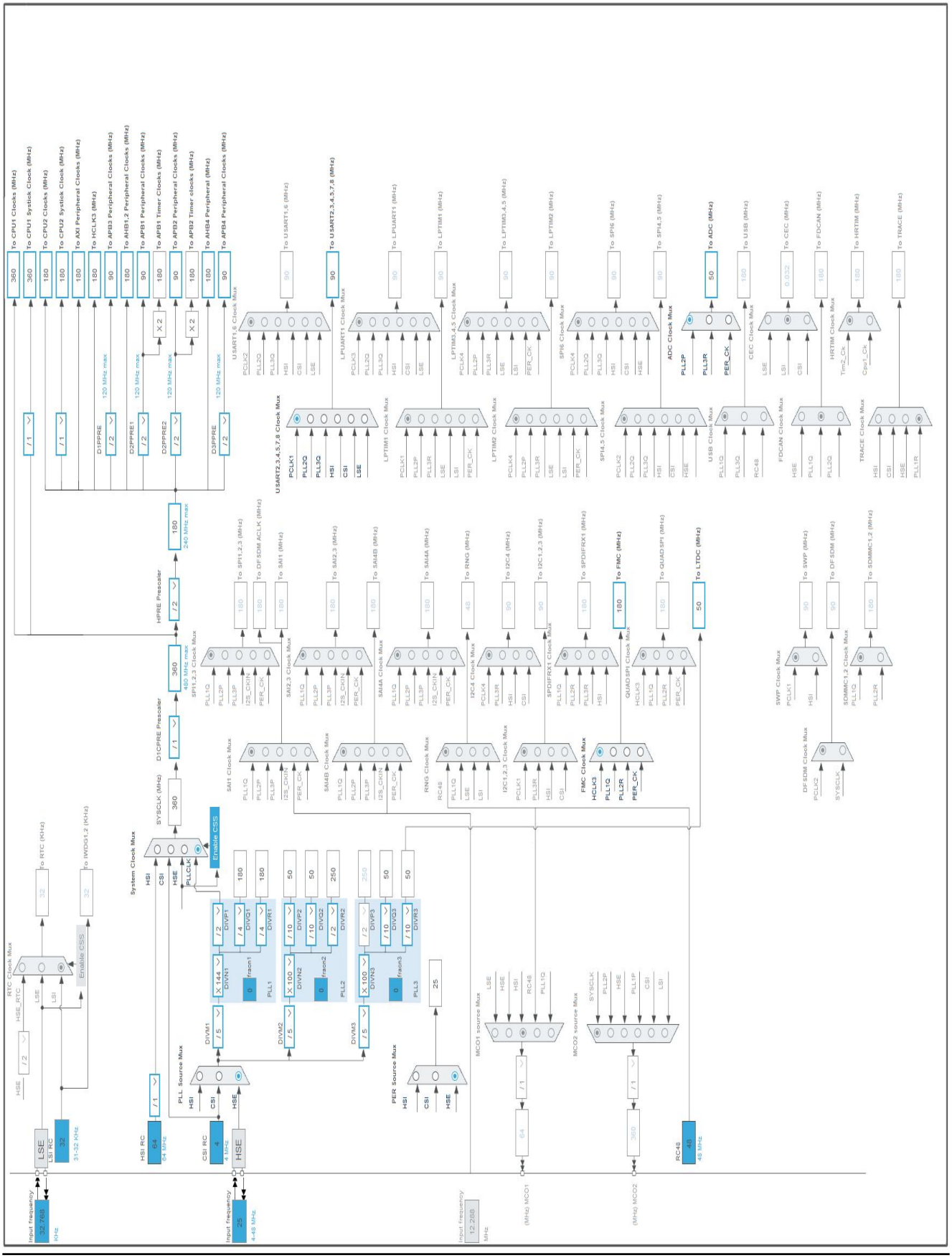
Pin Number TFBGA240	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
P10	PE11	I/O	FMC_D8	
P11	PB10	I/O	USART3_TX	
P12	PB11	I/O	USART3_RX	
P14	PH11	I/O	GPIO_EXTI11	USB_OTG_FS2_OverCurrent
P15	PD15	I/O	FMC_D1	
P16	PD14	I/O	FMC_D0	
P17	VDD	Power		
R1	PC2_C	I/O	ADC3_INP0	MEMS_AIN_5
R2	PC3_C	I/O	ADC3_INP1	MEMS_AIN_6
R3	PA6 **	I/O	GPIO_Output	D3_ImprGnD
R4	VSS	Power		
R5	PA7 *	I/O	ETH_RX_DV	MII_RX_DV
R7	PF12	I/O	FMC_A6	
R8	VSS	Power		
R9	PF15	I/O	FMC_A9	
R10	PE12	I/O	FMC_D9	
R11	PE15	I/O	FMC_D12	
R12	PJ5	I/O	LTDC_R6	
R13	PH9	I/O	LTDC_R3	
R15	PD11 *	I/O	QUADSPI_BK1_IO0	
R16	PD12	I/O	TIM4_CH1	
R17	PD13 *	I/O	TIM4_CH2	
T1	PA0_C	I/O	ADC1_INP0	MEMS_AIN_3
T2	PA1_C	I/O	ADC1_INP1	MEMS_AIN_4
T4	PC4 *	I/O	ETH_RXD0	ETH_RXD0
T5	PB1 *	I/O	ETH_RXD3	MII_RXD3
T6	PJ2 **	I/O	GPIO_Output	LD1 [Red Led]
T7	PF11	I/O	FMC_SDNRAS	
T8	PG0	I/O	FMC_A10	
T9	PE8	I/O	FMC_D5	
T10	PE13	I/O	FMC_D10	
T11	PH6	I/O	FMC_SDNE1	
T12	VSS	Power		
T14	PB12 **	I/O	GPIO_Output	LCD_RST
T16	PD10	I/O	FMC_D15	
T17	PD9	I/O	FMC_D14	
U1	VSS	Power		
U4	PC5 *	I/O	ETH_RXD1	MII_RXD1

Pin Number TFBGA240	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
U5	PB0 *	I/O	ETH_RXD2	MII_RXD2
U6	PJ3	I/O	LTDC_R4	
U7	PJ4	I/O	LTDC_R5	
U8	PG1	I/O	FMC_A11	
U9	PE7	I/O	FMC_D4	
U10	PE14	I/O	FMC_D11	
U11	VCAP	Power		
U12	VDDLDO	Power		
U13	PH7	I/O	FMC_SDCKE1	
U14	PB13 *	I/O	FDCAN2_TX	FDCAN2_TX
U16	PD8	I/O	FMC_D13	
U17	VSS	Power		

** The pin is affected with an I/O function

* The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	PhonPhot_Complete_System
Project Folder	C:\Users\Owner\MegaMachineSTM32Work\PhononsPhotons-
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.11.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x1000
Minimum Stack Size	0x1000

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls ARM Cortex-M7

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_DMA_Init	DMA
4	MX_LTDC_Init	LTDC
5	MX_CRC_Init	CRC
6	MX_DMA2D_Init	DMA2D
7	MX_FREERTOS_Init	FREERTOS_M7
8	MX_TIM4_Init	TIM4
9	MX_FMC_Init	FMC
11	MX_TouchGFX_Init	STMicroelectronics.X-CUBE-TOUCHGFX.4.18.1_M7
12	MX_TouchGFX_Process	STMicroelectronics.X-CUBE-TOUCHGFX.4.18.1_M7

5.4. Advanced Settings - Generated Function Calls ARM Cortex-M4

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	MX_TIM3_Init	TIM3
4	MX_USART3_UART_Init	USART3
5	MX_ADC3_Init	ADC3
6	MX_ADC1_Init	ADC1

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32H7
Line	STM32H745/755
MCU	STM32H745XIHx
Datasheet	DS12923_Rev1

1.2. Parameter Selection

Temperature	25
Vdd	3.0

1.3. Battery Selection

Battery	Li-SOCL2(DD36000)
Capacity	36000.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	450.0 mA
Max Pulse Current	1000.0 mA
Cells in series	1
Cells in parallel	1

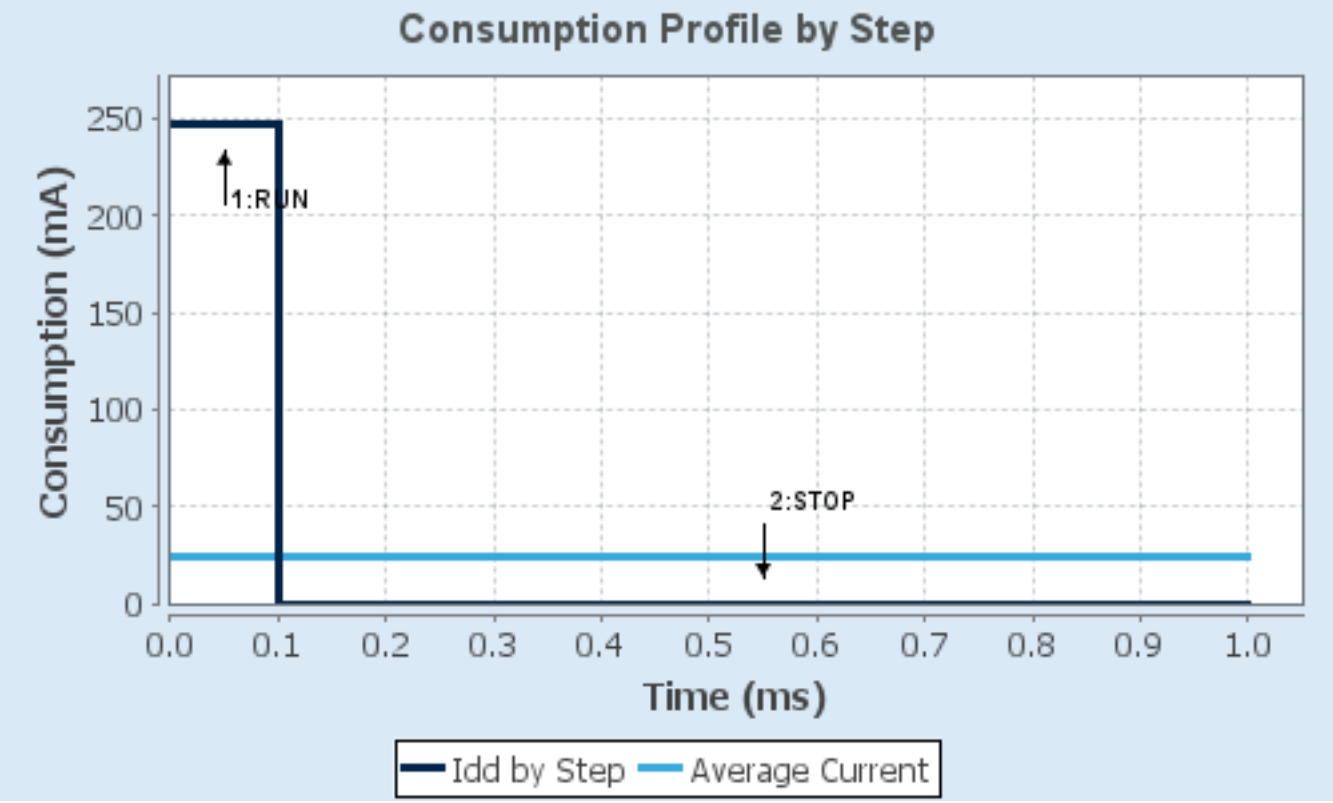
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0: Scale0	SVOS5: System-Scale5
D1 Mode	DRUN/CRUN	DSTANDBY
D2 Mode	DRUN/CRUN	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	CM7: ITCM/Cache / CM4: FLASH_B/ART	CM7: NA / CM4: NA
CM7 Frequency	480 MHz	0 Hz
Clock Configuration	HSE BYP PLL ALL_IPs_ON	LSE Flash-ON
CM4 Frequency	240 MHz	0 Hz
Clock Source Frequency	25 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	247 mA	145 µA
Duration	0.1 ms	0.9 ms
DMIPS	1027.0	0.0
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	24.83 mA
Battery Life	1 month, 29 days, 21 hours	Average DMIPS	1027.2001 DMIPS

1.6. Chart


Consumption Profile by Step
Consumption (mA)
250
200
150
100
50
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

2. Peripherals and Middlewares Configuration

2.1. ADC1

mode: IN0

IN1: IN1 Single-ended

IN10: IN10 Single-ended

2.1.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D2

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Asynchronous clock mode divided by 2 ***
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	**Overrun data overwritten ***
Left Bit Shift	No bit shift
Conversion Data Management Mode	**DMA Circular Mode ***
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	**3 ***
External Trigger Conversion Source	**Timer 3 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	**Channel 10 ***
Sampling Time	**16.5 Cycles ***
Offset Number	No offset
Offset Signed Saturation	Disable
Rank	**2 ***
Channel	Channel 0

Sampling Time	**16.5 Cycles ***
Offset Number	No offset
Offset Signed Saturation	Disable
Rank	**3 ***
Channel	**Channel 1 ***
Sampling Time	**16.5 Cycles ***
Offset Number	No offset
Offset Signed Saturation	Disable

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

2.2. ADC3
mode: IN0
IN1: IN1 Single-ended
mode: IN7

2.2.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D3

ADC_Settings:

Clock Prescaler	**Asynchronous clock mode divided by 2 ***
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	**Overrun data overwritten ***
Left Bit Shift	No bit shift
Conversion Data Management Mode	**DMA Circular Mode ***

Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	**3 ***
External Trigger Conversion Source	**Timer 3 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	**Channel 7 ***
Sampling Time	**16.5 Cycles ***
Offset Number	No offset
Offset Signed Saturation	Disable
Rank	**2 ***
Channel	Channel 0
Sampling Time	**16.5 Cycles ***
Offset Number	No offset
Offset Signed Saturation	Disable
Rank	**3 ***
Channel	**Channel 1 ***
Sampling Time	**16.5 Cycles ***
Offset Number	No offset
Offset Signed Saturation	Disable

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

2.3. CORTEX_M7

2.3.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7

Power Domain:	D1

Speculation default mode Settings:

Speculation default mode	Disabled

Cortex Interface Settings:

CPU ICache	**Enabled ***
CPU DCache	**Enabled ***

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	**Background Region Privileged accesses only + MPU Disabled during hard fault, NMI and FAULTMASK handlers ***

Cortex Memory Protection Unit Region 0 Settings:

MPU Region	**Enabled ***
MPU Region Base Address	**0xD0000000 ***
MPU Region Size	**1MB ***
MPU SubRegion Disable	**0x0 ***
MPU TEX field level	level 0
MPU Access Permission	**ALL ACCESS PERMITTED ***
MPU Instruction Access	**DISABLE ***
MPU Shareability Permission	DISABLE
MPU Cacheable Permission	**ENABLE ***
MPU Bufferable Permission	**ENABLE ***

Cortex Memory Protection Unit Region 1 Settings:

MPU Region	**Enabled ***
MPU Region Base Address	**0x90000000 ***
MPU Region Size	**128MB ***
MPU SubRegion Disable	**0x0 ***
MPU TEX field level	level 0
MPU Access Permission	**ALL ACCESS PERMITTED ***
MPU Instruction Access	**DISABLE ***
MPU Shareability Permission	DISABLE
MPU Cacheable Permission	**ENABLE ***
MPU Bufferable Permission	**ENABLE ***

Cortex Memory Protection Unit Region 2 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 3 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 4 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 5 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 6 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 7 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 8 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 9 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 10 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 11 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 12 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 13 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 14 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 15 Settings:

MPU Region	Disabled

2.4. CRC

mode: Activated

2.4.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D3

Basic Parameters:

Default Polynomial State	Enable
Default Init Value State	Enable

Advanced Parameters:

Input Data Inversion Mode	None
Output Data Inversion Mode	Disable

Input Data Format	Bytes

2.5. DEBUG

Debug: Trace Asynchronous Sw

2.5.1. Core(s) Settings:

Context(s):	Cortex-M7 Cortex-M4
Initialized Context:	Cortex-M7
Power Domain:	

2.6. DMA2D

mode: Activated

2.6.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Basic Parameters:

Transfer Mode	**Register to Memory ***
Color Mode	**RGB565 ***
Output Offset	0

2.7. FMC

SDRAM 2

Clock and chip enable: SDCKE1+SDNE1

Internal bank number: 4 banks

Address: 12 bits

Data: 16 bits

Byte enable: 16-bit byte enable

2.7.1. SDRAM 2:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

SDRAM control:

Bank	SDRAM bank 2
Number of column address bits	8 bits
Number of row address bits	12 bits
CAS latency	**2 memory clock cycles ***
Write protection	Disabled
SDRAM common clock	**2 HCLK clock cycles ***
SDRAM common burst read	**Enabled ***
SDRAM common read pipe delay	0 HCLK clock cycle

SDRAM timing in memory clock cycles:

Load mode register to active delay	**2 ***
Exit self-refresh delay	**6 ***
Self-refresh time	**4 ***
SDRAM common row cycle delay	**6 ***
Write recovery time	**2 ***
SDRAM common row precharge delay	**2 ***
Row to column delay	**2 ***

2.7.2. Bank Mapping:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Mapping parameters:

FMC bank mapping	Default mapping

2.8. LTDC

Display Type: RGB888 (24 bits)

2.8.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Synchronization for Width:

Horizontal Synchronization Width	8
Horizontal Back Porch	7
Active Width	640
Horizontal Front Porch	6
HSync Width	7
Accumulated Horizontal Back Porch Width	14
Accumulated Active Width	654
Total Width	660

Synchronization for Height:

Vertical Synchronization Height	4
Vertical Back Porch	2
Active Height	480
Vertical Front Porch	2
VSync Height	3
Accumulated Vertical Back Porch Height	5
Accumulated Active Height	485
Total Height	487

Signal Polarity:

Horizontal Synchronization Polarity	Active Low
Vertical Synchronization Polarity	Active Low
Data Enable Polarity	Active Low
Pixel Clock Polarity	Normal Input

Layer Default Color:

Red	0
Green	0
Blue	0

2.8.2. Layer Settings:

Core(s) Settings:

Context(s):	Cortex-M7

Initialized Context:	Cortex-M7
Power Domain:	D1

Layer Default Color:

Layer 0 - Alpha	0
Layer 0 - Blue	0
Layer 0 - Green	0
Layer 0 - Red	0
Layer 1 - Alpha	0
Layer 1 - Blue	0
Layer 1 - Green	0
Layer 1 - Red	0

Number of Layers:

Number of Layers	2 layers

Windows Position:

Layer 0 - Window Horizontal Start	0
Layer 0 - Window Horizontal Stop	0
Layer 0 - Window Vertical Start	0
Layer 0 - Window Vertical Stop	0
Layer 1 - Window Horizontal Start	0
Layer 1 - Window Horizontal Stop	0
Layer 1 - Window Vertical Start	0
Layer 1 - Window Vertical Stop	0

Pixel Parameters:

Layer 0 - Pixel Format	ARGB8888
Layer 1 - Pixel Format	ARGB8888

Blending:

Layer 0 - Alpha constant for blending	0
Layer 0 - Blending Factor1	Alpha constant
Layer 0 - Blending Factor2	Alpha constant
Layer 1 - Alpha constant for blending	0
Layer 1 - Blending Factor1	Alpha constant
Layer 1 - Blending Factor2	Alpha constant

Frame Buffer:

Layer 0 - Color Frame Buffer Start Adress	0
Layer 0 - Color Frame Buffer Line Length (Image Width)	0
Layer 0 - Color Frame Buffer Number of Lines (Image Height)	0
Layer 1 - Color Frame Buffer Start Adress	0
Layer 1 - Color Frame Buffer Line Length (Image Width)	0
Layer 1 - Color Frame Buffer Number of Lines (Image	0

Height)

2.9. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

2.9.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7 Cortex-M4
Initialized Context:	Cortex-M7
Power Domain:	D3

Power Parameters:

SupplySource	PWR_DIRECT_SMPS_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	**16 ***
HSI Calibration Value	**32 ***

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	2 WS (3 CPU cycle)
Product revision	rev.V

PLL range Parameters:

PLL1 clock Input range	Between 4 and 8 MHz
PLL2 input frequency range	Between 4 and 8 MHz
PLL3 input frequency range	Between 4 and 8 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	Wide VCO range
PLL3 clock Output range	Wide VCO range

2.10. SYS_M4

Timebase Source: SysTick

2.10.1. Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	

2.11. SYS

Timebase Source: TIM6

2.11.1. Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	

2.12. TIM3

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel4: PWM Generation No Output

2.12.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D2

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**750 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Update Event ***

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	**PWM mode 2 ***
Pulse (16 bits value)	**400 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	**PWM mode 2 ***
Pulse (16 bits value)	**400 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

2.13. TIM4

Slave Mode: External Clock Mode 1

Trigger Source: TI1_ED

2.13.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable
Slave Mode Controller	ETR mode 1

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Trigger:

Trigger Filter (4 bits value)	0

2.14. USART3

Mode: Asynchronous

2.14.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D2

Basic Parameters:

Baud Rate	**4000000 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

2.15. FREERTOS_M7

Interface: CMSIS_V2

2.15.1. Config parameters:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

API:

FreeRTOS API	CMSIS v2

Versions:

FreeRTOS version	10.3.1
CMSIS-RTOS version	2.00

MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	Disabled

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	56
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Enabled
USE_COUNTING_SEMAPHORES	Enabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Disabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	**32768 ***
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Enabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Enabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

CMSIS-RTOS V2 flags:

USE_OS2_THREAD_SUSPEND_RESUME	Enabled
USE_OS2_THREAD_ENUMERATE	Enabled
USE_OS2_EVENTFLAGS_FROM_ISR	Enabled
USE_OS2_THREAD_FLAGS	Enabled
USE_OS2_TIMER	Enabled
USE_OS2_MUTEX	Enabled

2.15.2. Include parameters:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Enabled
vTaskDelay	Enabled

xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Enabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Enabled
xTaskGetCurrentTaskHandle	Enabled
eTaskGetState	Enabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Enabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

2.15.3. Advanced settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT	**Enabled ***

Project settings (see parameter description first):

Use FW pack heap file	Enabled

2.16. STMicroelectronics.X-CUBE-TOUCHGFX.4.18.1_M7 mode: GraphicsJjApplication

2.16.1. TouchGFX Generator:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Display:

Interface	**Parallel RGB (LTDC) ***
Framebuffer Pixel Format (LTDC)	ARGB8888

Width (LTDC)	0
Height (LTDC)	0
Framebuffer Strategy	**Double Buffer ***
Buffer Location	**By Address ***
Start Address	**0xD0000000 ***
Start Address 2	**0xD0200000 ***

Driver:

Application Tick Source	**LTDC ***
Graphics Accelerator	**ChromART (DMA2D) ***
Real-Time Operating System	CMSIS_RTOS_V2

Video Decoding:

Type	Disabled

*** User modified value**

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
ADC1	PC0	ADC1_INP10	Analog mode	No pull-up and no pull-down	n/a	MEMS_AIN_1	Cortex-M4	D2
	PA0_C	ADC1_INP0	Analog mode	No pull-up and no pull-down	n/a	MEMS_AIN_3	Cortex-M4	D2
	PA1_C	ADC1_INP1	Analog mode	No pull-up and no pull-down	n/a	MEMS_AIN_4	Cortex-M4	D2
ADC3	PF8	ADC3_INP7	Analog mode	No pull-up and no pull-down	n/a	MEMS_AIN_2	Cortex-M4	D3
	PC2_C	ADC3_INP0	Analog mode	No pull-up and no pull-down	n/a	MEMS_AIN_5	Cortex-M4	D3
	PC3_C	ADC3_INP1	Analog mode	No pull-up and no pull-down	n/a	MEMS_AIN_6	Cortex-M4	D3
DEBUG	PA14 (JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a		Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PB3 (JTDO/TRACESWO	DEBUG_JTDO-SWO	n/a	n/a	n/a		Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PA13 (JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a		Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
FMC	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PG5	FMC_BA1	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PH5	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PH6	FMC_SDNE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PD9	FMC_D14	Alternate Function	No pull-up and no pull-	Very High		Cortex-M7	D1

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
			Push Pull	down				
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PH7	FMC_SDCKE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
LTDC	PK5	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D1
	PI1	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	**High ***		Cortex-M7	D1
	PI0	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull-down	**High ***		Cortex-M7	D1
	PK4	LTDC_B5	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D1
	PJ15	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_DISP	Cortex-M7	D1
	PK6	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull-down	**High ***		Cortex-M7	D1
	PK3	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull-down	**High ***		Cortex-M7	D1
	PK7	LTDC_DE	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D1
	PJ14	LTDC_B2	Alternate Function Push Pull	No pull-up and no pull-down	**High ***		Cortex-M7	D1
	PJ12	LTDC_B0	Alternate Function Push Pull	No pull-up and no pull-down	**High ***		Cortex-M7	D1
	PI9	LTDC_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D1
	PJ13	LTDC_B1	Alternate Function Push Pull	No pull-up and no pull-down	**High ***		Cortex-M7	D1
	PI12	LTDC_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	**High ***		Cortex-M7	D1
	PI14	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**High ***		Cortex-M7	D1
	PK2	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull-down	**High ***		Cortex-M7	D1
	PJ11	LTDC_G4	Alternate Function Push Pull	No pull-up and no pull-down	**High ***		Cortex-M7	D1
	PJ10	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down	**High ***		Cortex-M7	D1

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
	PJ9	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull-down	**High ***		Cortex-M7	D1
	PJ0	LTDC_R1	Alternate Function Push Pull	No pull-up and no pull-down	**High ***		Cortex-M7	D1
	PJ8	LTDC_G1	Alternate Function Push Pull	No pull-up and no pull-down	**High ***		Cortex-M7	D1
	PJ7	LTDC_G0	Alternate Function Push Pull	No pull-up and no pull-down	**High ***		Cortex-M7	D1
	PJ6	LTDC_R7	Alternate Function Push Pull	No pull-up and no pull-down	**High ***		Cortex-M7	D1
	PI15	LTDC_R0	Alternate Function Push Pull	No pull-up and no pull-down	**High ***		Cortex-M7	D1
	PJ1	LTDC_R2	Alternate Function Push Pull	No pull-up and no pull-down	**High ***		Cortex-M7	D1
	PJ5	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull-down	**High ***		Cortex-M7	D1
	PH9	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	**High ***		Cortex-M7	D1
	PJ3	LTDC_R4	Alternate Function Push Pull	No pull-up and no pull-down	**High ***		Cortex-M7	D1
	PJ4	LTDC_R5	Alternate Function Push Pull	No pull-up and no pull-down	**High ***		Cortex-M7	D1
RCC	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a		Cortex-M7* Cortex-M4	D3
	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a		Cortex-M7* Cortex-M4	D3
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	OSC_OUT	Cortex-M7* Cortex-M4	D3
	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	OSC_IN	Cortex-M7* Cortex-M4	D3
TIM3	PB4 (NJTRST)	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M4	D2
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D2
USART3	PB10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M4	D2
	PB11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M4	D2
Single Mapped Signals	PI6	SAI2_SD_A	Alternate Function Push Pull	No pull-up and no pull-down	Low			
	PI5	SAI2_SCK_A	Alternate Function	No pull-up and no pull-	Low			

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
			Push Pull	down				
	PI4	SAI2_MCLK_A	Alternate Function Push Pull	No pull-up and no pull-down	Low			
	PB5	FDCAN2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	FDCAN2_RX		
	PG10	SAI2_SD_B	Alternate Function Push Pull	No pull-up and no pull-down	Low			
	PG9	QUADSPI_BK2_IO2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***			
	PC10	SDMMC1_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SDIO1_D2		
	PI7	SAI2_FS_A	Alternate Function Push Pull	No pull-up and no pull-down	Low			
	PB6	QUADSPI_BK1_NCS	Alternate Function Push Pull	**Pull-up ***	**Very High ***			
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	Low	MII_TX_EN		
	PC11	SDMMC1_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SDIO1_D3		
	PH14	FDCAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	FDCAN2_RX		
	PE2	ETH_TXD3	Alternate Function Push Pull	No pull-up and no pull-down	Low	MII_TXD3		
	PG12	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low	MII_TXD1		
	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SDIO1_CK		
	PE5	SAI4_CK2	Alternate Function Push Pull	No pull-up and no pull-down	Low			
	PE4	SAI4_D2	Alternate Function Push Pull	No pull-up and no pull-down	Low			
	PB9	SDMMC1_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SDIO1_D5		
	PB8	SDMMC1_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SDIO1_D4		
	PG14	QUADSPI_BK2_IO3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***			
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low	MII_TXD0		
	PD2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SDIO1_CMD		
	PA9	USB_OTG_FS_VBUS	n/a	n/a	n/a	VBUS_FS2		

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
	PH13	FDCAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	FDCAN1_TX		
	PC8	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SDIO1_D0		
	PC9	SDMMC1_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SDIO1_D1		
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	Low	USB_OTG_FS2_P		
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	Low	USB_OTG_FS2_N		
	PI10	ETH_RX_ER	Alternate Function Push Pull	No pull-up and no pull-down	Low	MII_RX_ER		
	PC7	SDMMC1_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SDIO1_D7		
	PC6	SDMMC1_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SDIO1_D6		
	PF6	QUADSPI_BK1_IO3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***			
	PF7	QUADSPI_BK1_IO2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***			
	PF10	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***			
	PF9	QUADSPI_BK1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***			
	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	Low	MII_MDC		
	PC2	ETH_TXD2	Alternate Function Push Pull	No pull-up and no pull-down	Low	MII_TXD2		
	PC3	ETH_TX_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	MII_TX_CLK		
	PH2	ETH_CRS	Alternate Function Push Pull	No pull-up and no pull-down	Low	MII_CRS		
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	Low	MII_MDIO		
	PA1	ETH_RX_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	MII_RX_CLK		
	PH3	ETH_COL	Alternate Function Push Pull	No pull-up and no pull-down	Low	MII_COL		
	PA7	ETH_RX_DV	Alternate Function Push Pull	No pull-up and no pull-down	Low	MII_RX_DV		
	PD11	QUADSPI_BK1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***			
	PD13	TIM4_CH2	Alternate Function	No pull-up and no pull-	Low			

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
			Push Pull	down				
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low	ETH_RXD0		
	PB1	ETH_RXD3	Alternate Function Push Pull	No pull-up and no pull-down	Low	MII_RXD3		
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low	MII_RXD1		
	PB0	ETH_RXD2	Alternate Function Push Pull	No pull-up and no pull-down	Low	MII_RXD2		
	PB13	FDCAN2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	FDCAN2_TX		
GPIO	PD3	GPIO_Input	Input mode	**Pull-up ***	n/a	DEBUG_EN_IN	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PI2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DEBUG_GPIO_0	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PD7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LCD_DISP	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PI3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a		Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PA10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USB_OTG_FS2_ID	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	B1 [Blue PushButton]	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PI13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Green Led]	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PG3	GPIO_Input	Input mode	**Pull-up ***	n/a	D2_SWToggle	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PG2	GPIO_EXTI2	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	LCD_INT	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PK0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LCD_BL	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PK1	GPIO_Input	Input mode	**Pull-up ***	n/a	D4_MoButton	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PH11	GPIO_EXTI11	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	USB_OTG_FS2_OverCurrent	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PA6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D3_ImprGnD	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PJ2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD1 [Red Led]	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_RST	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4

* Initialized context

3.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Stream0	Peripheral To Memory	**High ***
ADC3	DMA1_Stream1	Peripheral To Memory	**High ***
USART3_TX	DMA1_Stream7	Memory To Peripheral	Low

ADC1: DMA1_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

ADC3: DMA1_Stream1 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

USART3_TX: DMA1_Stream7 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

3.3. BDMA configuration

nothing configured in DMA service

3.4. MDMA configuration

nothing configured in DMA service

3.5. NVIC configuration

3.5.1. NVIC1

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	true	15	0
DMA2D global interrupt	true	5	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line2 interrupt	unused		
TIM4 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
FMC global interrupt	unused		
CM4 send event interrupt for CM7	unused		
FPU global interrupt	unused		
LTDC global interrupt	unused		
LTDC global error interrupt	unused		
HSEM1 global interrupt	unused		
RAM ECC diagnostic global interrupt	unused		
Hold core interrupt	unused		

3.5.2. NVIC1 Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Pendable request for system service	false	false	false
System tick timer	false	false	true
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	false	true	true
DMA2D global interrupt	false	true	true

3.5.3. NVIC2

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
DMA1 stream0 global interrupt	true	0	0
DMA1 stream1 global interrupt	true	0	0
USART3 global interrupt	true	0	0
DMA1 stream7 global interrupt	true	0	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
EXTI line2 interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
TIM3 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
CM7 send event interrupt for CM4	unused		
FPU global interrupt	unused		
HSEM2 global interrupt	unused		
ADC3 global interrupt	unused		
RAM ECC diagnostic global interrupt	unused		
Hold core interrupt	unused		

3.5.4. NVIC2 Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false

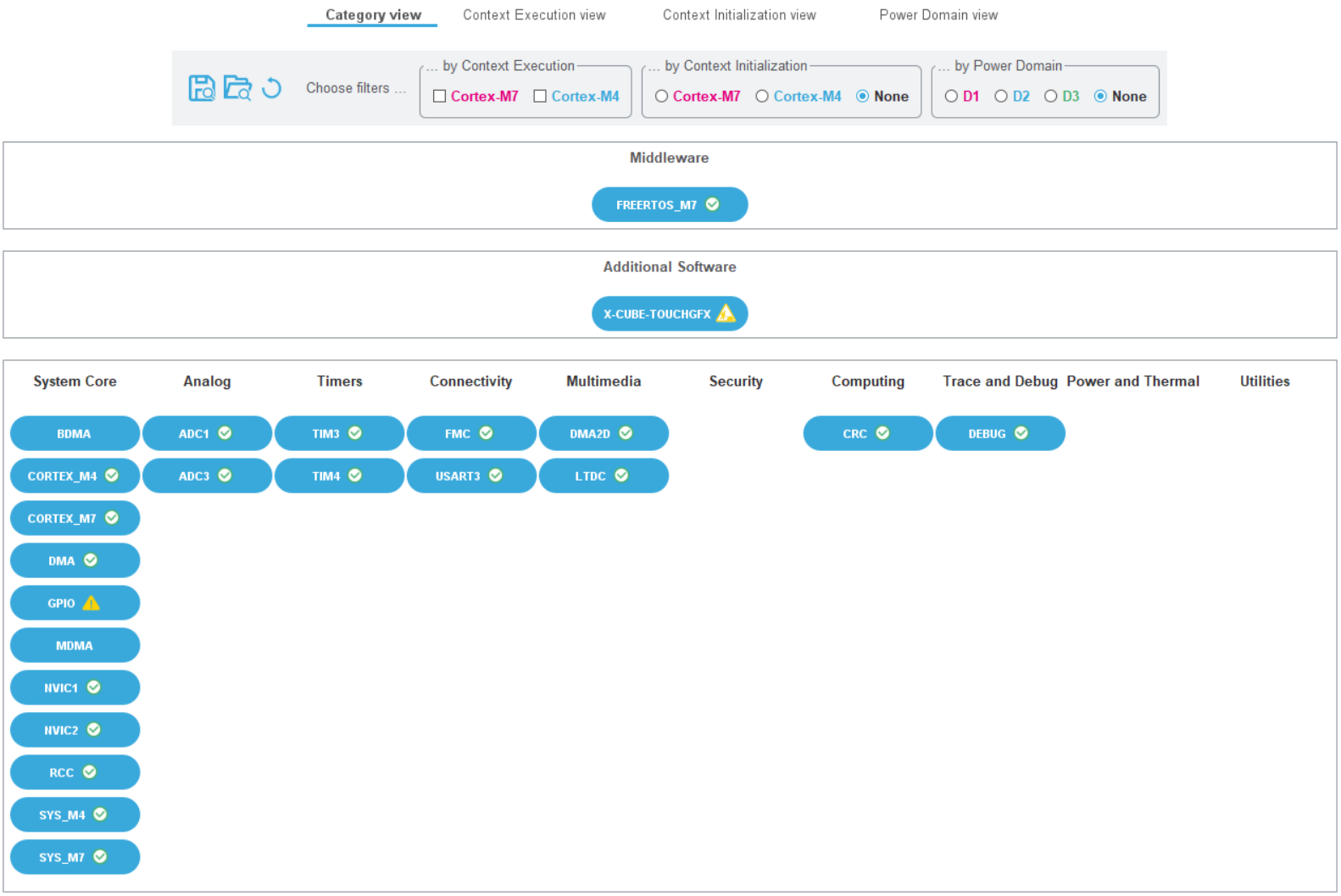
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 stream0 global interrupt	false	true	true
DMA1 stream1 global interrupt	false	true	true
USART3 global interrupt	false	true	true
DMA1 stream7 global interrupt	false	true	true

*** User modified value**

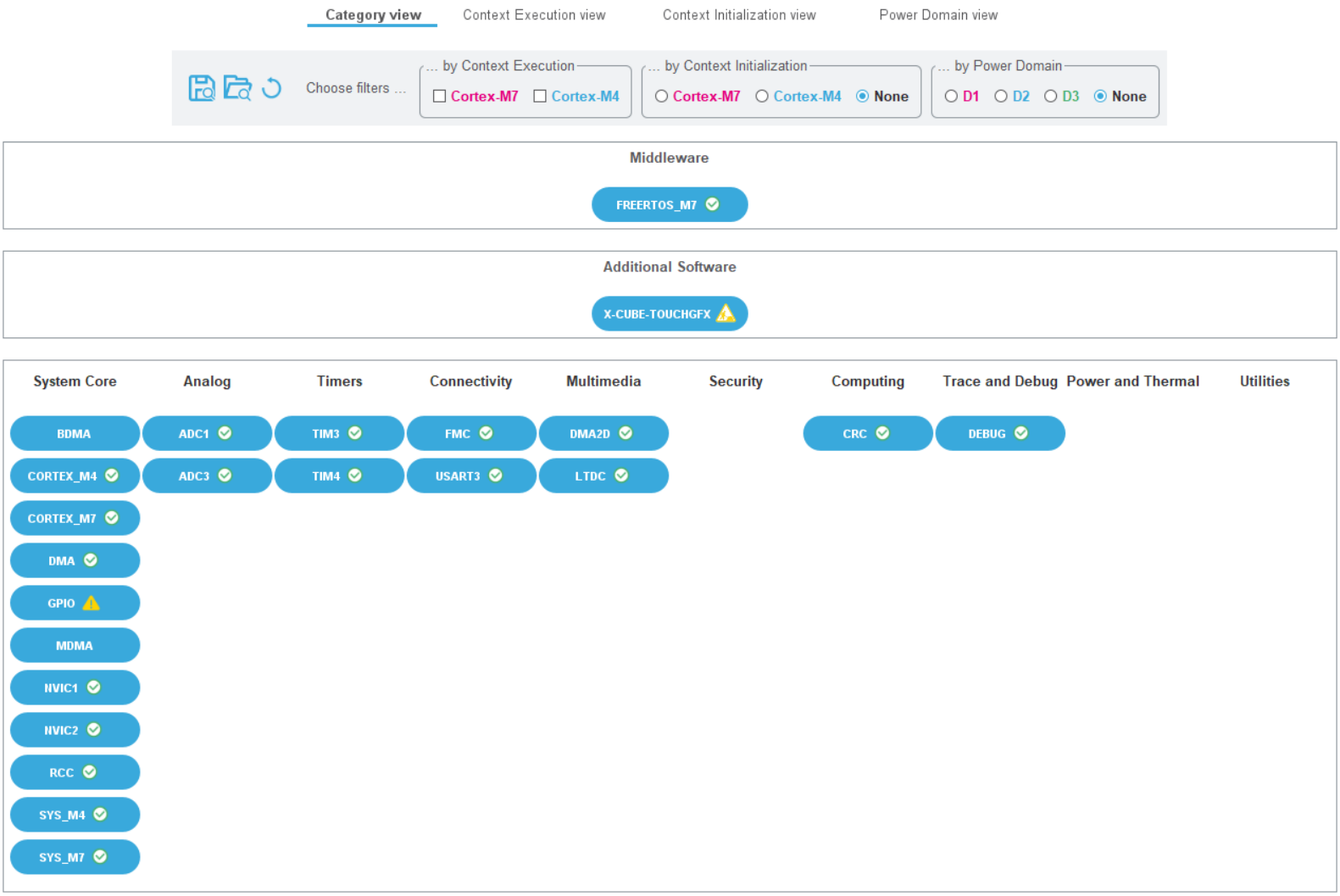
4. System Views

4.1. Category view

4.1.1. Current



4.1.2. Without filters



4.2. Context Execution view

4.3. Context Initialization view

4.4. Power Domain view

5. Software Pack Report

5.1. Software Pack selected

Vendor	Name	Version	Component
STMicroelectronics	X-CUBE-TOUCHGFX	4.18.1	Class : Graphics Group : Application Variant : TouchGFX Generator Version : 4.18.1

6. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32h7_bsdl.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32h7-svd.zip
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h7_series_product_overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf
Brochures	https://www.st.com/resource/en/brochure/brstm32h7.pdf
Brochures	https://www.st.com/resource/en/brochure/brstm32h7vl.pdf
Brochures	https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32nucleo.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32trust.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1181-electrostatic-discharge-sensitivity-measurement-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2606-stm32-microcontroller-system-memory-boot-mode-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2639-soldering-

	recommendations-and-package-information-for-leadfree-ecopack-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2867-oscillator-design-guide-for-stm8afals-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3126-audio-and-waveform-generation-using-the-dac-in-stm32-products-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3155-usart-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3156-usb-dfu-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4013-stm32-crossseries-timer-overview-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4221-i2c-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4229-how-to-implement-a-vocoder-solution-using-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4277-using-stm32-device-pwm-shutdown-features-for-motor-control-and-digital-power-conversion-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4286-spi-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4539-hrtim-cookbook-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4566-extending-the-dac-performance-of-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4635-minimization-of-power-consumption-using-lpuart-for-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4655-virtually-increasing-the-number-of-serial-communication-peripherals-in-stm32-applications-stmicroelectronics.pdf

Application Notes	https://www.st.com/resource/en/application_note/an4750-handling-of-soft-errors-in-stm32-applications-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4759-using-the-hardware-realtime-clock-rtc-and-the-tamper-management-unit-tamp-with-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4776-generalpurpose-timer-cookbook-for-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4803-highspeed-si-simulations-using-ibis-and-boardlevel-simulations-using-hyperlynx-si-on-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4839-level-1-cache-on-stm32f7-series-and-stm32h7-series-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4861-lcdtft-display-controller-ltdc-on-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4908-stm32-usart-automatic-baud-rate-detection-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4989-stm32-microcontroller-debug-toolbox-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4990-getting-started-with-sigmadelta-digital-interface-on-applicable-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4996-hardware-jpeg-codec-peripheral-in-stm32f7677xxx-and-stm32h743534555475750a3b3b0xx-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5020-digital-camera-interface-dcmi-on-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5027-interfacing-pdm-digital-microphones-using-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5033-stm32cube-mcu-package-examples-for-stm32h7-series-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5036-thermal-management-guidelines-for-stm32-applications-stmicroelectronics.pdf

Application Notes	https://www.st.com/resource/en/application_note/an5073-receiving-spdif-audio-stream-with-the-stm32f4f7h7-series-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5200-getting-started-with-stm32h7-series-sdmmc-host-controller-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5224-stm32-dmamux-the-dma-request-router-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5286-stm32h7x5x7-dualcore-microcontroller-debugging-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5337-stm32h7-series-lifetime-estimates-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5354-getting-started-with-the-stm32h7-series-mcu-16bit-adc-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5405-fdcan-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5543-enhanced-methods-to-handle-spi-communication-on-stm32-devices-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5557-stm32h745755-and-stm32h747757-lines-dualcore-architecture-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5617-stm32h745755-and-stm32h747757-lines-interprocessor-communications-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5690-vrefbuf-peripheral-applications-and-trimming-technique-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4899-stm32-microcontroller-gpio-hardware-settings-and-lowpower-consumption-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5507-cyclic-redundancy-check-in-stm32h7-series-flash-memory-interface-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5612-esd-protection-of-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5293-migration-guide-

	from-stm32f7-series-to-stmh74x75x-stm32h72x73x-and-stmh7a37bx-devices-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5156-introduction-to-stm32-microcontrollers-security-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4838-introduction-to-memory-protection-unit-management-on-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5348-introduction-to-fdcan-peripherals-for-stm32-product-classes-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4230-random-number-generation-validation-using-nist-statistical-test-suite-for-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5225-introduction-to-usb-typec-power-delivery-for-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5342--how-to-use-error-correction-code-ecc-management-for-internal-memories-protection-on-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2834-how-to-optimize-the-adc-accuracy-in-the-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4938-getting-started-with-stm32h74xig-and-stm32h75xig-mcu-hardware-development-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5816-how-to-build-stm32-lpbam-application-using-stm32cubemx-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5537-how-to-use-adc-oversampling-techniques-to-improve-signaltonoise-ratio-on-stm32-mcus-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an1202_freertos_guide-freertos-guide-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an1602_semihosting_in_truestudio-how-to-do-semihosting-in-truestudio-stmicroelectronics.pdf

Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an1801_stm32cubeprogrammer_in_truestudio-installing-stm32cubeprogrammer-in-truestudio-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/atollic_editing_keyboard_shortcuts-atollic-editing-keyboard-shortcuts-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/iar_to_atollic_truestudio_migration_guide-truestudio-for-arm-migration-guide-iar-embedded-workbench-to-truestudio-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/stm32cubemx_installation_in_truestudio-stm32cubemx-installation-in-truestudio-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an2606-stm32-microcontroller-system-memory-boot-mode-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an4323-getting-started-with-stemwin-library-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an4435-guidelines-for-obtaining-ulcsaiec-607301603351-class-b-certification-in-any-stm32-application-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an4635-minimization-of-power-consumption-using-lpuart-for-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an4657-stm32-inapplication-programming-iap-using-the-usart-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an4759-using-the-hardware-realtime-clock-rtc-and-the-tamper-management-unit-tamp-with-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an4841-digital-signal-processing-for-stm32-microcontrollers-using-cmsis-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4891-stm32h72x-

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