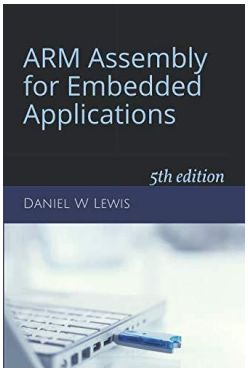
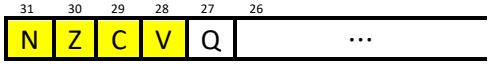


ARM Instructions Worksheet #9

Floating-Point Compares

And their effect on the NZCV Flags in the CPSR register:



Prerequisite Reading: Chapter 9
Revised: April 21, 2020

Objectives: *To use the web-based simulator ("CPUlator") to better understand …*

1. The use of VCMP and VMRS to perform floating-point comparisons.
2. The use of VSUB and VMOV to simplify some floating-point comparisons.
3. The use of floating-point equality comparisons.

To do offline: Answer the questions that follow the listing below. (Numbers at far left are memory addresses.)

```
                        .syntax      unified
                        .global      _start

            // *** EXECUTION STARTS HERE ***

00000000    _start:     MOVS         R0,0              // N flag = 0
00000004                VLDR         S0,posPt4         // S0 = +0.4
00000008                VLDR         S1,posPt5         // S1 = +0.5
0000000C                VCMP.F32     S0,S1             // 0.4 < 0.5 ?
00000010                VMRS         APSR_nzcv,FPSCR
00000014                LDR          R0,=1             // Assume MI
00000018                BMI          L1
0000001C                LDR          R0,=0             // Wasn't MI

00000020    L1:         VSUB.F32     S2,S0,S1          // S2 = 0.4 - 0.5
00000024                VMOV         R1,S2
00000028                LSR          R1,R1,31          // Same as R0?

0000002C                VLDR         S3,negPt1         // S3 = -0.1
00000030                VCMP.F32     S2,S3             // S2 == S3 ?
00000034                VMRS         APSR_nczv,FPSCR
00000038                LDR          R2,=1             // Assume EQ
0000003C                BEQ          done
00000040                LDR          R2,=0             // Wasn't EQ

00000044    done:       B            done              // Infinite loop

00000048    point5:     .float       +0.5
0000004C    point4:     .float       +0.4
00000050    point1:     .float       -0.1

                        .end
```

What is in the N flag (CPSR bit 31) after executing the VCMP at address $0000000C_{16}$?

N	C	Z	V
0	X	X	X

What is in the N flag (CPSR bit 31) after executing the VMRS at address 00000010_{16}?

N	C	Z	V
1	X	X	X

What is in register R0 ***before*** executing the VSUB instruction at address 00000020_{16}?

R0 (as decimal signed): 00000001

What is in register S2 after executing the VSUB instruction at address 00000020_{16}?

S2 (as decimal signed): bdcccccc

What is in register R1 after executing the VMOV instruction at address 00000024_{16}?

R1 (as hexadecimal): bdcccccc

What is in register R1 after executing the LSR instruction at address 00000028_{16}?

R1 (as decimal signed): 00000001

What is in register S3 after executing the VLDR instruction at address $0000002C_{16}$?

R2 (as decimal signed): bdccccd

What is in the Z flag (CPSR bit 29) after executing the VMRS at address 00000034_{16}?

N	C	Z	V
X	X	0	X

What is in register R2 ***before*** executing the B instruction at address 00000044_{16}?

R2 (as decimal signed): 00000000

Getting ready: Now use the simulator to collect the following information and compare to your earlier answers.

1. Click here to open a browser for the ARM instruction simulator with pre-loaded code.

Note: You can change the number format in the "Settings" window between hex, unsigned decimal and signed decimal as needed

Step 1: *Press F2 once per ARM instruction as needed to see what the simulator says for the following:*

What is in the N flag (CPSR bit 31) after executing the VCMP at address $0000000C_{16}$?

N	C	Z	V
0	X	X	X

What is in the N flag (CPSR bit 31) after executing the VMRS at address 00000010_{16}?

N	C	Z	V
1	X	X	X

What is in register R0 ***before*** executing the VSUB instruction at address 00000020_{16}?

R0 (as decimal signed): 00000001

What is in register S2 after executing the VSUB instruction at address 00000020_{16}?

S2 (as decimal signed): bdcccccc

What is in register R1 after executing the VMOV instruction at address 00000024_{16}?

R1 (as hexadecimal): bdcccccc

What is in register R1 after executing the LSR instruction at address 00000028_{16}?

R1 (as decimal signed): 00000001

What is in register S3 after executing the VLDR instruction at address $0000002C_{16}$?

R2 (as decimal signed): bdccccd

What is in the Z flag (CPSR bit 29) after executing the VMRS at address 00000034_{16}?

N	C	Z	V
X	X	0	X

What is in register R2 ***before*** executing the B instruction at address 00000044_{16}?

R2 (as decimal signed): 00000000