Group 54

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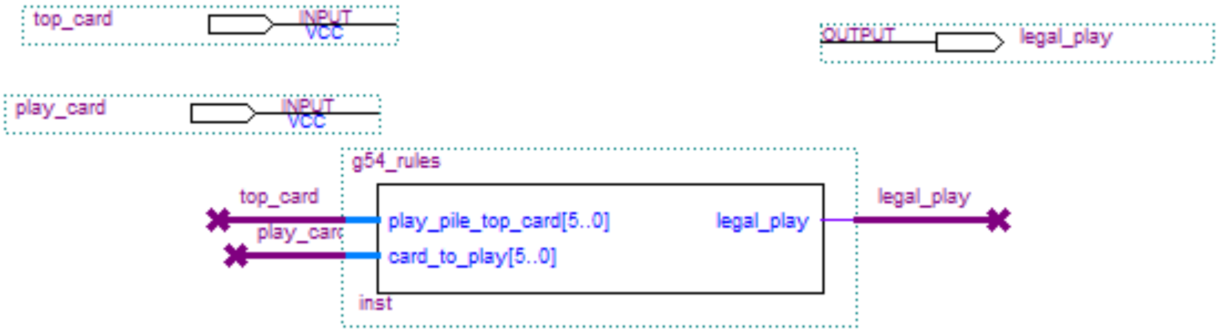
g54_Rules - Lab 4

Description

Input: 6 bit top_card, 6 bit play_card
Output: 1 bit legal_play

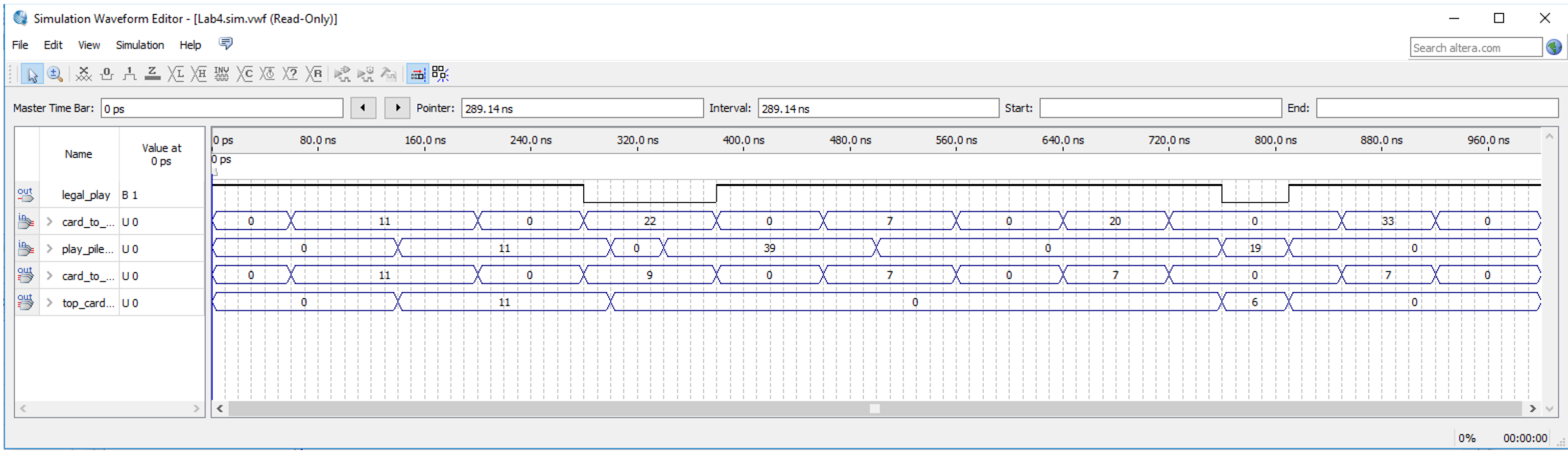


This circuit is designed to tell you whether a play is legal or not in the card game “Crazy Eights”. The circuit takes an input of the top card of the pile, encoded as (face value –1) + (suit * 13), and the card that the player wants to play and depending on the rules below tells you if you can play that card:

- A card with a face value of 8 (of any suit) can be played on any card.
- Any card can be played on a card with a face value of 8.
- Any card of a given suit can be played on a card with the same suit.
- Any card with a given face value can be played on a card with the same face value

Testing

To test our Rules circuit we simulated using Quartus wave Simulator. We created a wave form and then changed the values of the 2 input cards to see if the if the legal play output was displaying the correct value according to the crazy eights game. This is a picture of our simulation with added bottom 2 signals being face values of the card so it was easier to read. As you can see, when the suits or face value are matching, or when one of the cards is an eight (encoded as a face-value of 7) the legal play output is high and low when it is not.


Simulation Waveform Editor - [Lab4.sim.vwf (Read-Only)]

Master Time Bar: 0 ps
Pointer: 289.14 ns
Interval: 289.14 ns
Start:
End:

Name	Value at 0 ps
legal_play	B 1
card_to_...	U 0
play_pile...	U 0
card_to_...	U 0
top_card...	U 0

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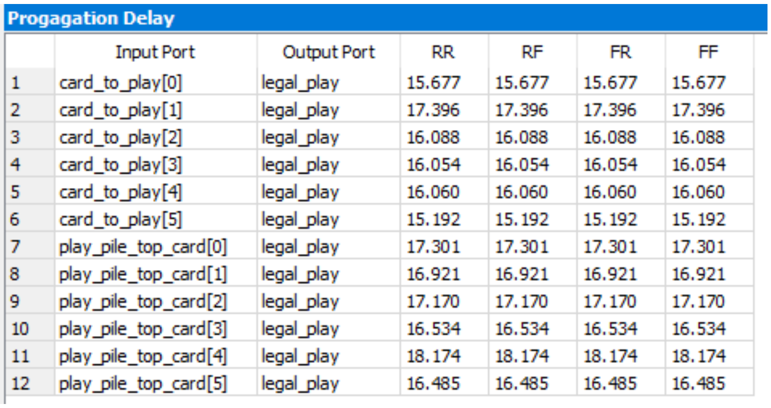
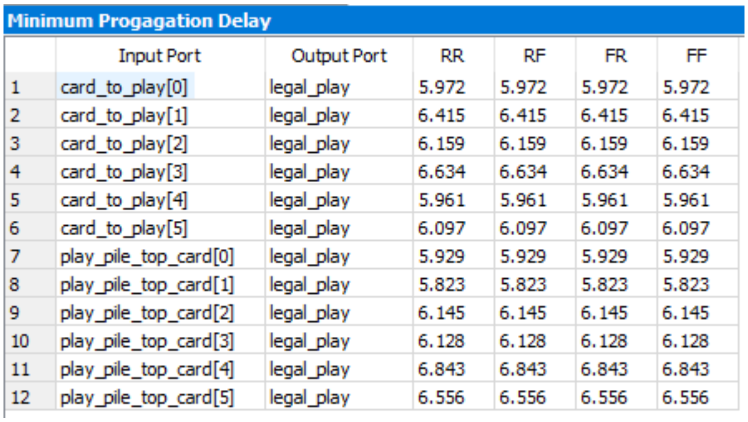
Timing Performance



Progagation Delay

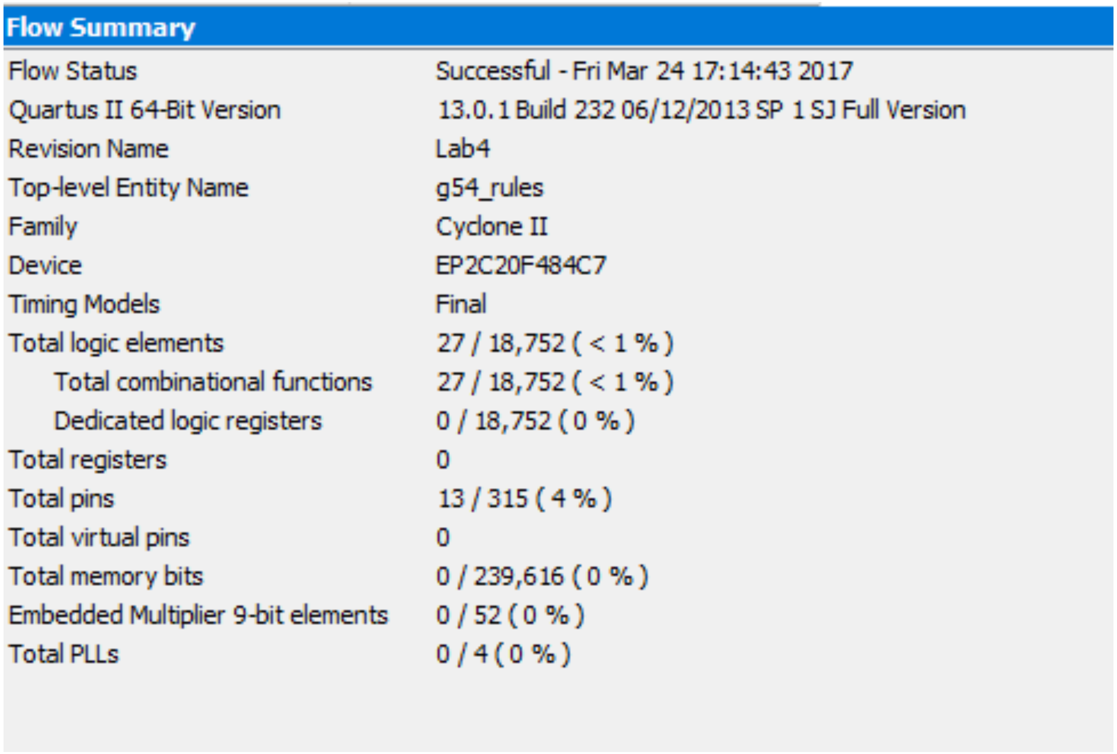
	Input Port	Output Port	RR	RF	FR	FF
1	card_to_play[0]	legal_play	15.677	15.677	15.677	15.677
2	card_to_play[1]	legal_play	17.396	17.396	17.396	17.396
3	card_to_play[2]	legal_play	16.088	16.088	16.088	16.088
4	card_to_play[3]	legal_play	16.054	16.054	16.054	16.054
5	card_to_play[4]	legal_play	16.060	16.060	16.060	16.060
6	card_to_play[5]	legal_play	15.192	15.192	15.192	15.192
7	play_pile_top_card[0]	legal_play	17.301	17.301	17.301	17.301
8	play_pile_top_card[1]	legal_play	16.921	16.921	16.921	16.921
9	play_pile_top_card[2]	legal_play	17.170	17.170	17.170	17.170
10	play_pile_top_card[3]	legal_play	16.534	16.534	16.534	16.534
11	play_pile_top_card[4]	legal_play	18.174	18.174	18.174	18.174
12	play_pile_top_card[5]	legal_play	16.485	16.485	16.485	16.485



Minimum Progagation Delay

	Input Port	Output Port	RR	RF	FR	FF
1	card_to_play[0]	legal_play	5.972	5.972	5.972	5.972
2	card_to_play[1]	legal_play	6.415	6.415	6.415	6.415
3	card_to_play[2]	legal_play	6.159	6.159	6.159	6.159
4	card_to_play[3]	legal_play	6.634	6.634	6.634	6.634
5	card_to_play[4]	legal_play	5.961	5.961	5.961	5.961
6	card_to_play[5]	legal_play	6.097	6.097	6.097	6.097
7	play_pile_top_card[0]	legal_play	5.929	5.929	5.929	5.929
8	play_pile_top_card[1]	legal_play	5.823	5.823	5.823	5.823
9	play_pile_top_card[2]	legal_play	6.145	6.145	6.145	6.145
10	play_pile_top_card[3]	legal_play	6.128	6.128	6.128	6.128
11	play_pile_top_card[4]	legal_play	6.843	6.843	6.843	6.843
12	play_pile_top_card[5]	legal_play	6.556	6.556	6.556	6.556

FPGA Resource Utilization



Flow Summary

Flow Status	Successful - Fri Mar 24 17:14:43 2017
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Full Version
Revision Name	Lab4
Top-level Entity Name	g54_rules
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Final
Total logic elements	27 / 18,752 (< 1 %)
Total combinational functions	27 / 18,752 (< 1 %)
Dedicated logic registers	0 / 18,752 (0 %)
Total registers	0
Total pins	13 / 315 (4 %)
Total virtual pins	0
Total memory bits	0 / 239,616 (0 %)
Embedded Multiplier 9-bit elements	0 / 52 (0 %)
Total PLLs	0 / 4 (0 %)

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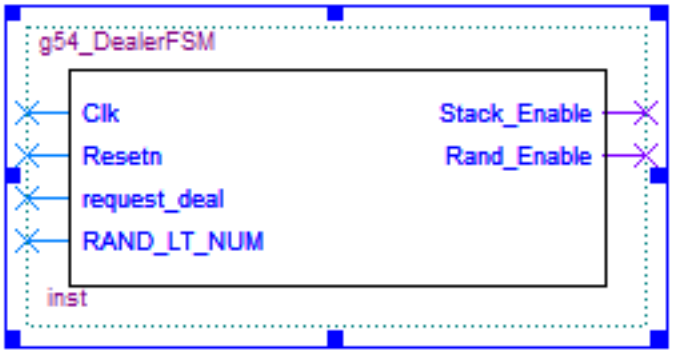
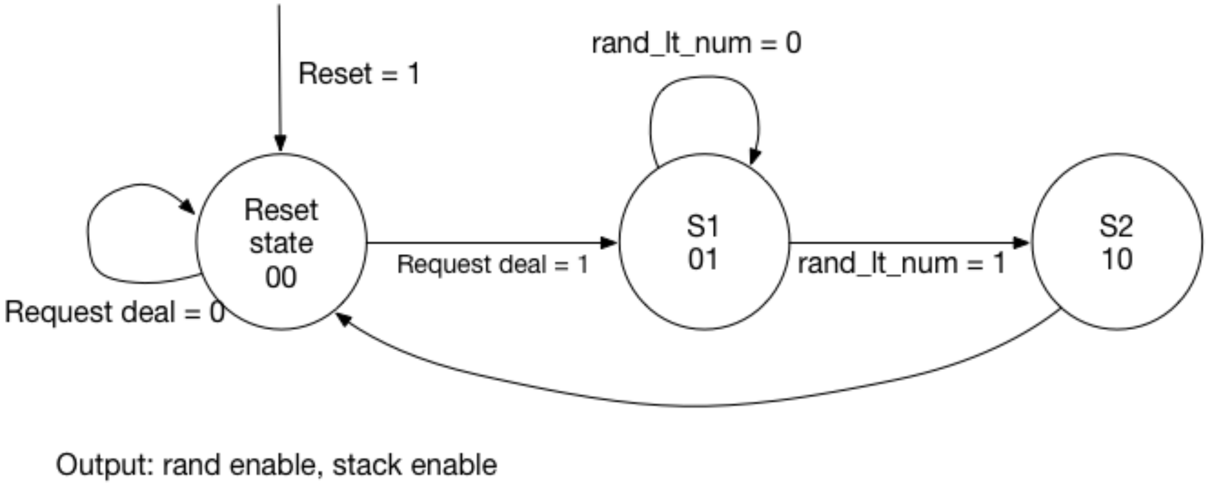
g54_DealerFSM - Lab 4

Description

Input: 1 bit clk, 1 bit Restn, 1 bit request deal, 1 bit rand_lt_num
Output: 1 bit stack enable, 1 bit rand enable



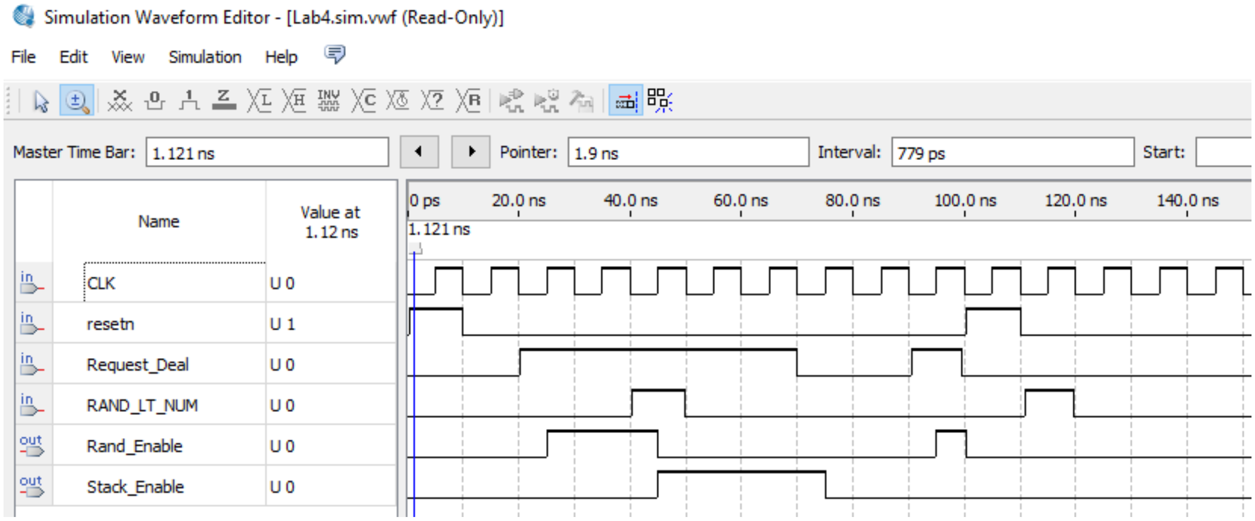
This circuit represents a card dealer. The finite state machine is pictured below.



When input request deal is high, the rand enable output is asserted which causes a new random number to be loaded into a register. Compare the random number to the value of NUM If RAND_LT_NUM is high (i.e. the output of RANDU is less than NUM) then assert the Stack_Enable output (which enables a POP operation on the stack), and repeat.

Testing

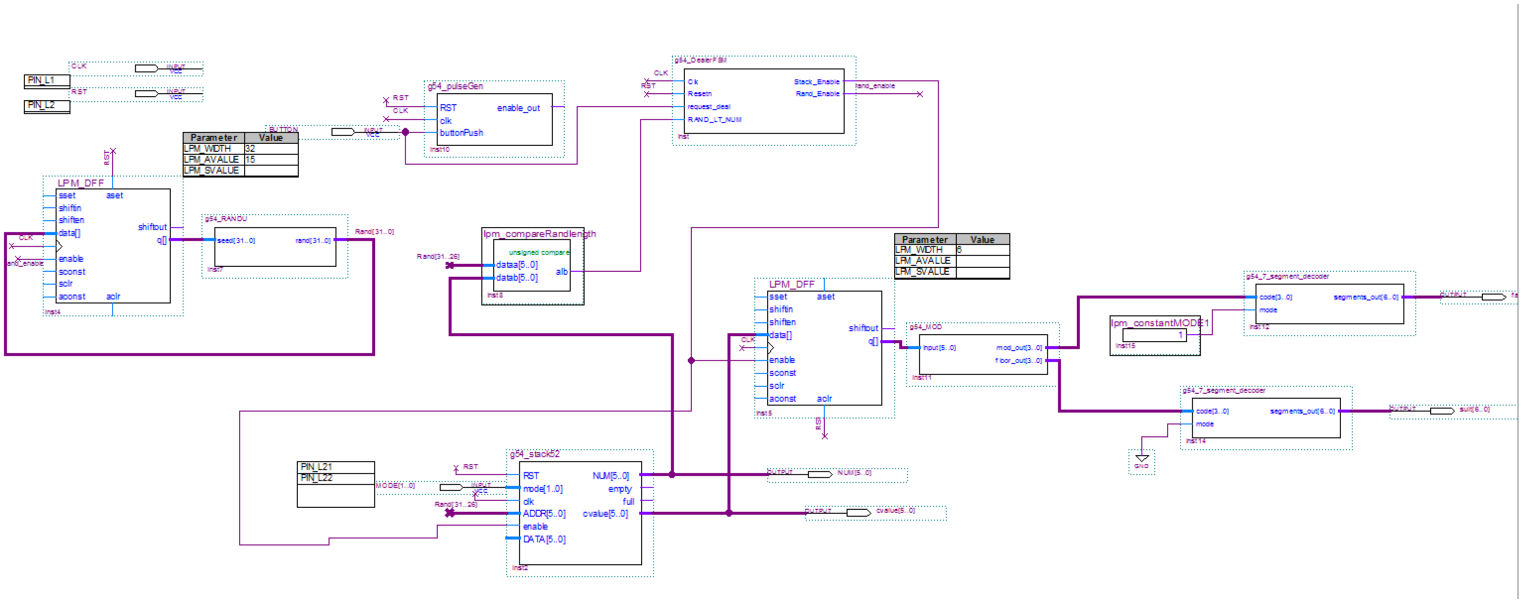
To first test that the dealer FSM works we ran a Quartus wave simulation (figure below). As you can see, once the request deal is enabled, the rand enable is asserted and if the RAND_LT_NUM is high the stack enable output is asserted.



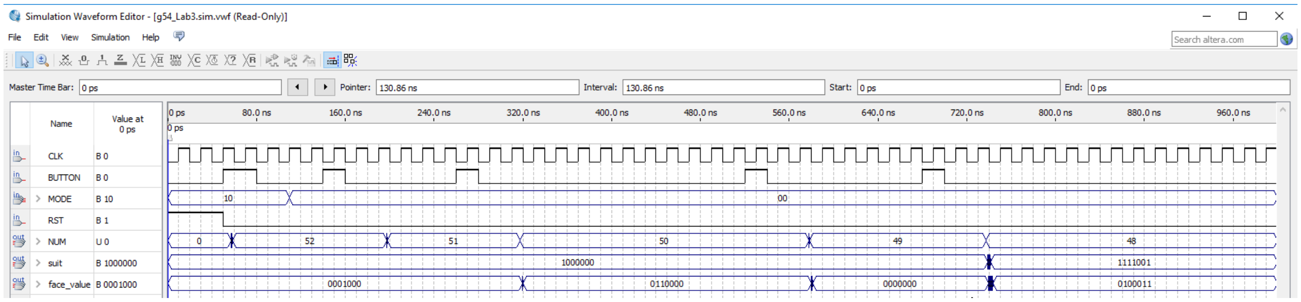
Master Time Bar: 1.121 ns   Pointer: 1.9 ns   Interval: 779 ps   Start:

	Name	Value at 1.12 ns
in	CLK	U 0
in	resetn	U 1
in	Request_Deal	U 0
in	RAND_LT_NUM	U 0
out	Rand_Enable	U 0
out	Stack_Enable	U 0

We then created a testbed for the dealer to present inputs to the dealer and displays outputs of to let us evaluate the performance of the dealer. This is shown below:



We then simulated the testbed on the Quartus wave simulator, to make sure it was functioning as expected:

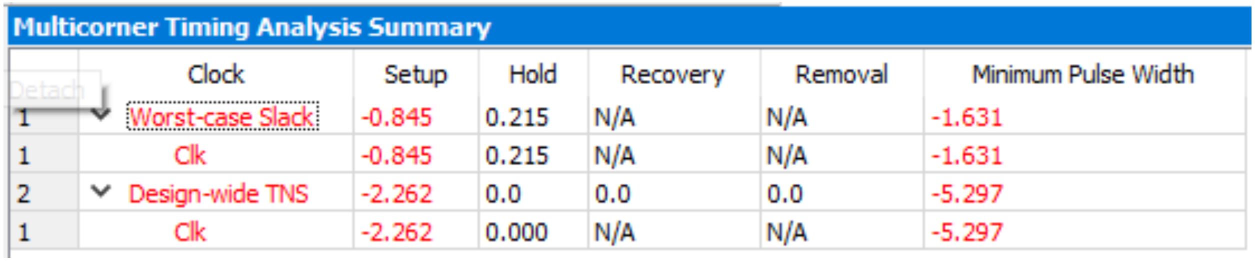


Master Time Bar: 0 ps   Pointer: 130.86 ns   Interval: 130.86 ns   Start: 0 ps   End: 0 ps

	Name	Value at 0 ps
in	CLK	B 0
in	BUTTON	B 0
in	MODE	B 10
in	RST	B 1
out	NUM	U 0
out	suit	B 1000000
out	face_value	B 0001000

We also uploaded the testbed to the Altera board to test it. We connected the 7 segment decoders to the LED displays to see if the values were as expected, and tested the dealer.

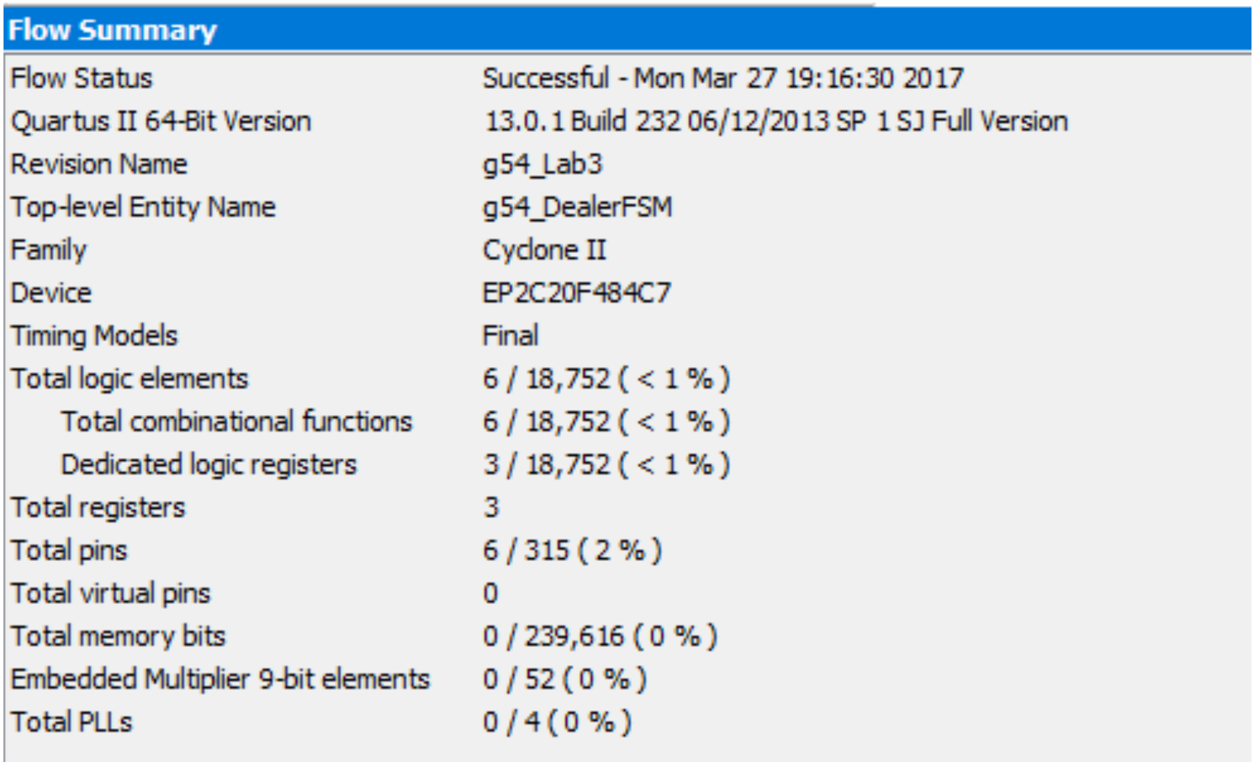
Timing Performance



Multicorner Timing Analysis Summary

	Clock	Setup	Hold	Recovery	Removal	Minimum Pulse Width
1	Worst-case Slack	-0.845	0.215	N/A	N/A	-1.631
1	Clk	-0.845	0.215	N/A	N/A	-1.631
2	Design-wide TNS	-2.262	0.0	0.0	0.0	-5.297
1	Clk	-2.262	0.000	N/A	N/A	-5.297

FPGA Resource Utilization



Flow Summary

Flow Status	Successful - Mon Mar 27 19:16:30 2017
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Full Version
Revision Name	g54_Lab3
Top-level Entity Name	g54_DealerFSM
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Final
Total logic elements	6 / 18,752 (< 1 %)
Total combinational functions	6 / 18,752 (< 1 %)
Dedicated logic registers	3 / 18,752 (< 1 %)
Total registers	3
Total pins	6 / 315 (2 %)
Total virtual pins	0
Total memory bits	0 / 239,616 (0 %)
Embedded Multiplier 9-bit elements	0 / 52 (0 %)
Total PLLs	0 / 4 (0 %)