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PUBLISHABLE SUMMARY

This report provides the initial guidelines on the technical transfer of neuromorphic perception from iCub to humanoid robots. First, there is an overview of the event-drive sensors in the iCub neuromorphic robot developed by IIT Genoa. The sensorimotor architecture of the robot is designed to detect and respond to events. New perception architectures are proposed so that the same sensors will be transferred to a standard iCub robot in Manchester and to a new robot being developed on the Kangaroo platform by PAL Robotics. The new architectures are designed to be flexible so it can be installed on other types of humanoid robots as well.

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1. EXECUTIVE SUMMARY

This document collects information about event driven sensors installed on iCub neuromorphic robot (IIT Genoa) and that will be ported to a standard iCub hosted in Manchester and on a new robot under development based on the Kangaroo platform by PAL Robotics. The architecture has been conceived to be adapted and installed on other humanoid robots.

2. INTRODUCTION

2.1. Perception architecture proposals

The computational core will be offered by the SpiNNaker2[1] board which will host also a SoC-FPGA[2] based module capable of managing the event flow and to offer availability for hardware calculation to speed-up algorithms by pre-processing or faster processing.SpiNNaker2 board will expose at least 3 Ethernet ports for net connection as well as a few Aurora links[3] for direct high-speed board-to-board connections.

2.1.1. iCub Genoa

Event based sensor are connected to a board named UZCB that hosts a SoC-FPGA based daughter board that manages the event flow coming from sensor boards. It applies a time stamp to each event, then injects data in YARP[4] and send events to SpiNNaker2 board via Aurora links as well. The FPGA fabric is also available for implementing hardware computation for pre-processing. UZCB manages the Event Cameras, the Event Based Skin and the frame-based cameras. The UZCB would be connected to SpiNNaker2 board by two direct Aurora lanes, one dedicated to the daughter board, the other to SpiNNaker2 array. The rest of the robot's items (standard sensors, control PC, motor controllers and feedback, etc.) are connected together through a Gigabit Ethernet net.

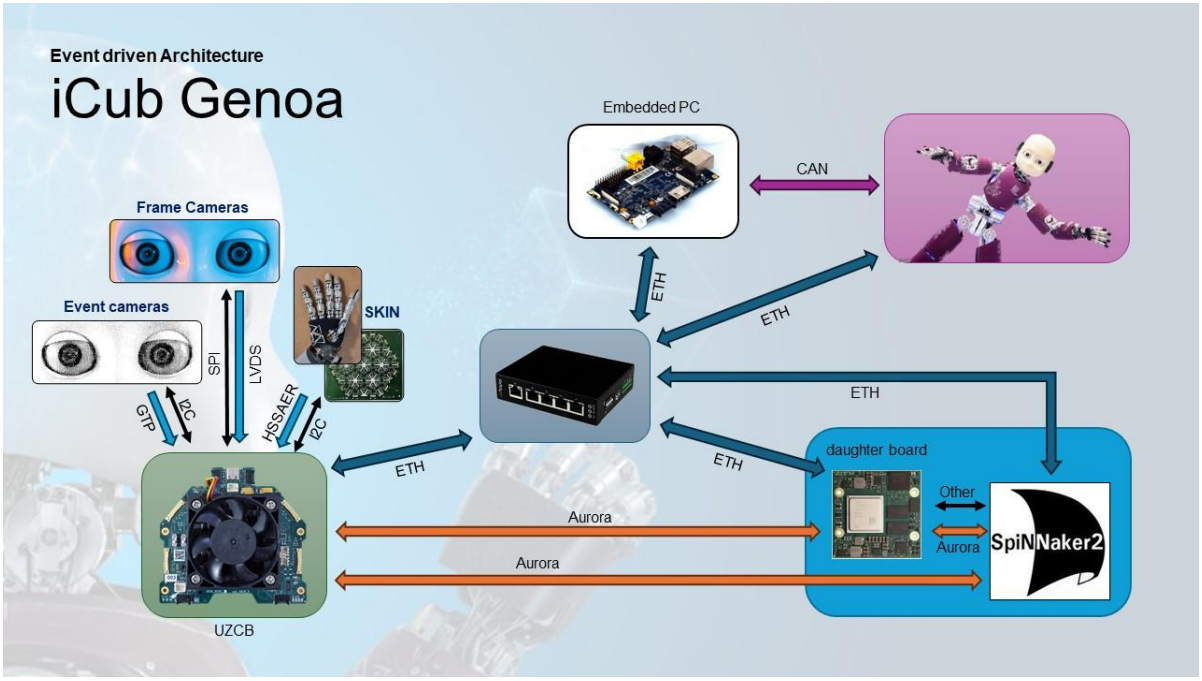


Figure 2.1.1 – iCub "Genoa" architecture

[1] **SpiNNaker** (Spiking Neural Network Architecture) is a many-core computer architecture based on spiking neural networks, useful in simulating the human brain. It was designed at the Dept. of Computer Science, Univ. of Manchester.

[2] **System on Chip**, composed by one or more Microprocessor core and a FPGA fabric (Field Programmable Gate Array) in a single package

[3] A link layer communications protocol for use on point-to-point serial links. It was developed by Xilinx

[4] **Yet Another Robot Platform**, a middleware capable to sustain the dataflow through the robot

2.1.2. iCub Manchester

Event based sensors (skin and USB3 event-based cameras) are managed directly by the SoC-FPGA based daughter board, that injects data in YARP and sends events to SpiNNaker2 board via Aurora links. Frame Cameras are connected to the system through the Embedded PC

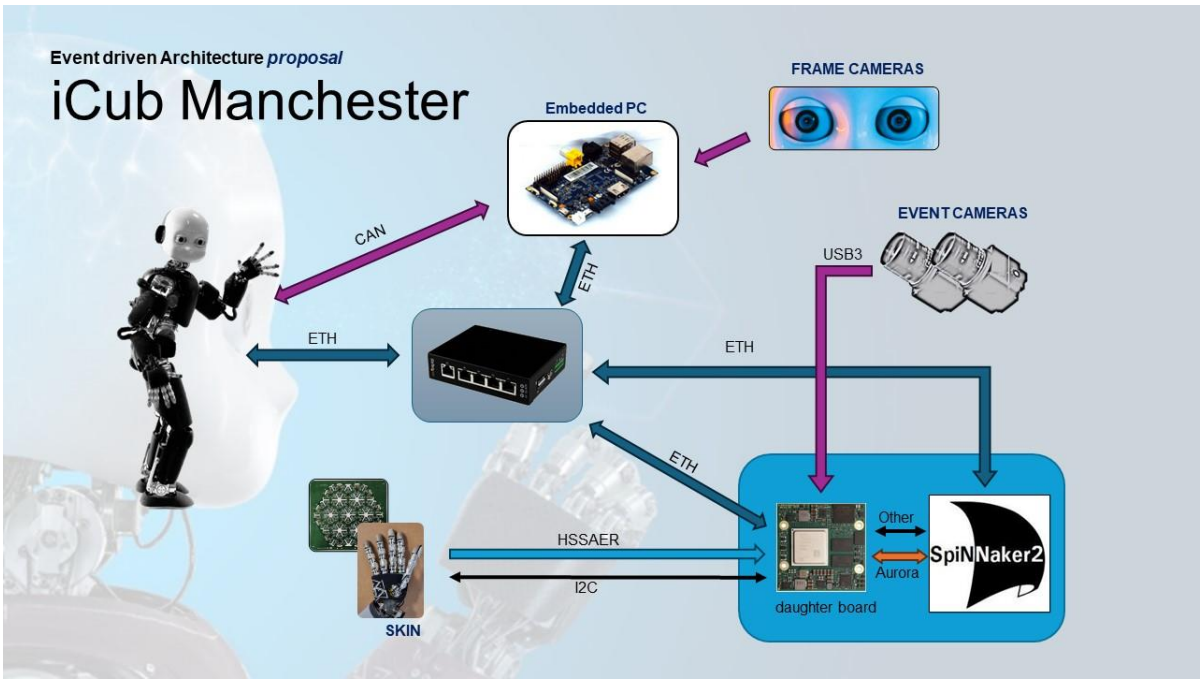


Figure 2.1.2 – iCub "Manchester" perception architecture

2.1.3. Kangaroo

The architecture is similar to iCub Manchester, but the hand would be provided by Seed Robotics (TBC) and their tactile sensors would be connected to the Multimedia PC. Kangaroo robot is controlled over EtherCAT by the Control PC. The motors of the hand are controlled with RS485 by the Control PC

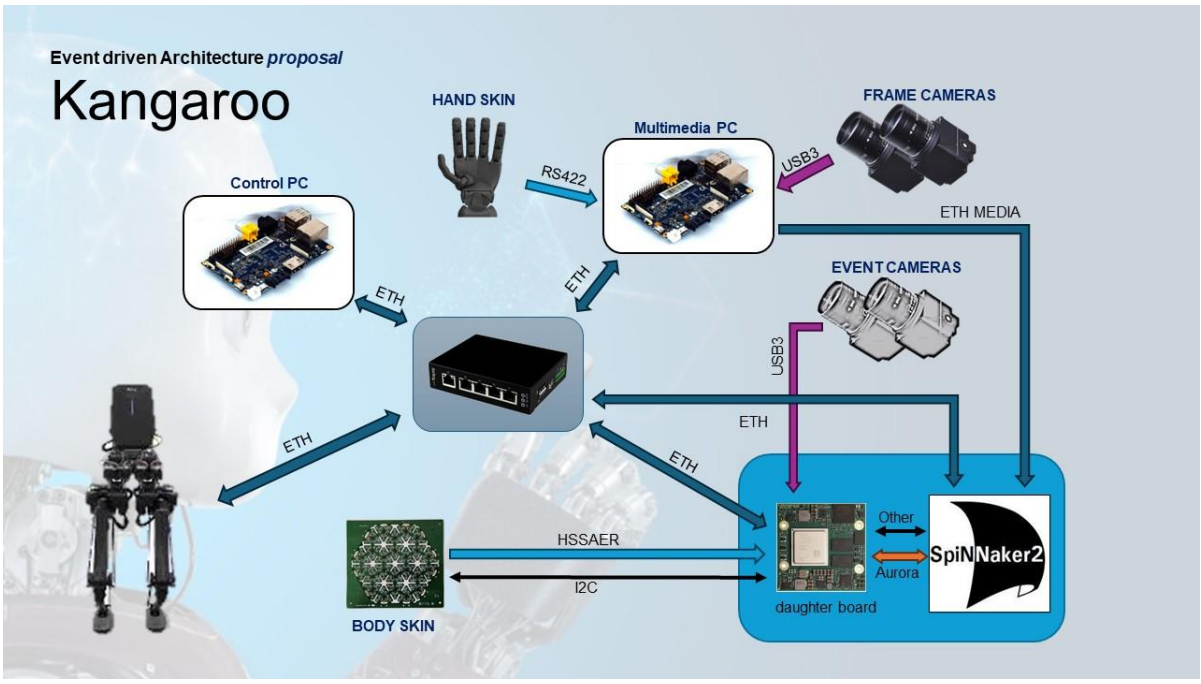


Figure 2.1.3 – Kangaroo architetture

3. ED-SKIN (EVENT DRIVEN SKIN)

3.1. Introduction

Ed-Skin stands for Event Driven Skin, an implementation of event-driven based tactile sensing. The current version of implementation is referred to **ED-MTB** Assembly Rev 1.0 that is a prototype derived from CCAM3-IIT_GEN3[5] assembly, from which the "PROC" board (based on XILINX Artix XC7A50T-CPG236-1) was taken (Synoptic Processing Board) and applied to a customized carrier board (ED-MTB), with the **ed-skin** FPGA firmware loaded.

ED-MTB Assembly Rev 1.0 is composed by:

- Synoptic Processing Board - Rev B – 19/02/2016
- ED-MTB – Rev A – 16/12/2016
- the **ed-skin** FPGA release 0.1 – 17/01/2024

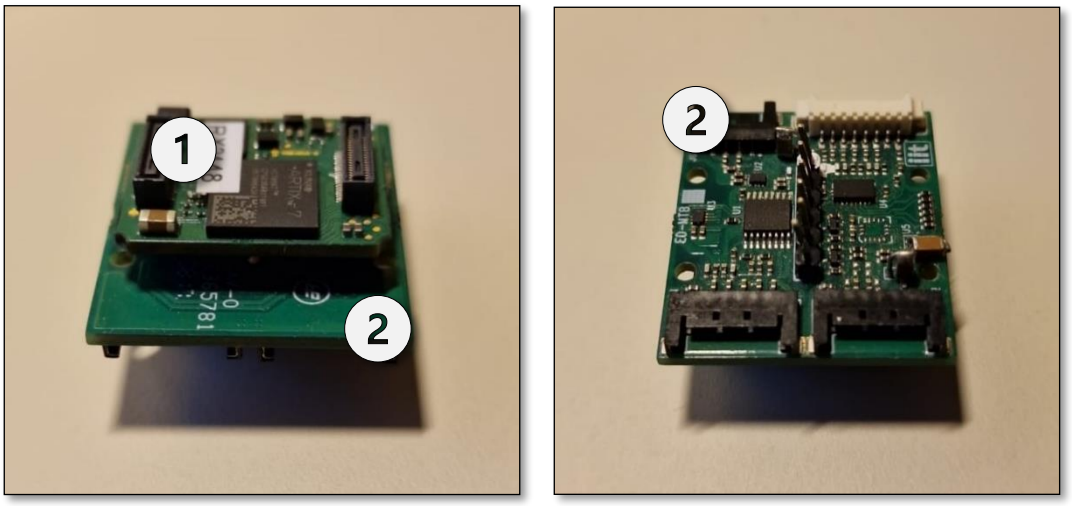


Figure 3.1.1 – ED-MTB assembly, derived from PROC board (1) of CCAM-IIT_GEN3 and a custom carrier board (2)

3.2. ED-MTB Connections

ED-MTB is provided with:

1) power/data connector towards master board (e.g. UZCB) or mirror board (for implementing a tree architecture via HSSAER[6] (1))
2) power connector (for standalone operation)
3) data connector towards other slave boards (for implementing a tree architecture via HSSAER)
4) connector towards sensor boards
5) JTAG for FPGA programming and debugging

[5] **CCAM3-IIT_GEN3** is the event-based vision system installed on Neuromorphic iCub, IIT Genoa. See paragraph 4

[6] **HSSAER** (High Speed Serial Address Event Representation) is a serial protocol developed by IIT to serially transmit an AER (Address Event Representation) data

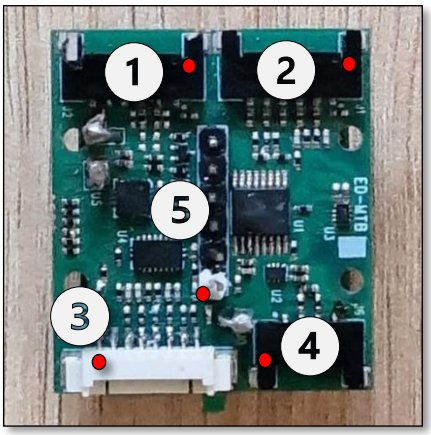


Figure 3.2.1 – ED-MTB connectors (red dots indicate pins 1)

#	ID	PIN	SIG. NAME	DESCRIPTION	DIR
1	J2	1	GND	Ground	-
		2	SCL_in	**SCL – I2C clock from master** / LVDS Input Auxiliary lane n side	I
		3	SDA_in	**SDA – I2C data from/to master** / LVDS Input Auxiliary lane p side	I/O
		4	LVDS_out_p	LVDS_p – HSSAER output side p	O
		5	LVDS_out_n	LVDS_n – HSSAER output side n	O
		6	5V	+5V power supply (output if the board is powered)	I/O
2	J1	1	GND	Ground	
		2	SDA_out	**SDA_in turned out** / signal from FPGA / LVDS Output Auxiliary lane p side	I/O
		3	SCL_out	**SCL_in turned out** / signal from FPGA / LVDS Output Auxiliary lane n side	I/O
		4	LVDS_in_p	LVDS_p – HSSAER input side p	I
		5	LVDS_in_n	LVDS_n – HSSAER input side n	I
		6	5V	+5V power supply (output if the board is powered)	I/O
3	J0	1	GND	Ground	-
		2	AN0	Not connected	-
		3	SD4_sensor	SDA Lane 4	I/O
		4	SD3_sensor	SDA Lane 3	I/O
		5	SD2_sensor	SDA Lane 2	I/O
		6	SD1_sensor	SDA Lane 1	I/O
		7	SCL_sensor	SCL (common)	O
		8	3.3V	Sensor Power supply output	O
4	J6	1	5V	ED-MTB Power Supply	I
		2	5V	ED-MTB Power Supply	I
		3	GND	Ground	-
		6	GND	Ground	-
5	J5	1	1.8V	JTAG Power Supply	O
		2	GND	Ground	-
		3	Ext_fpga_TCK	JTAG TCK	I
		4	Ext_fpga_TDO	JTAG TDO	O
		5	Ext_fpga_TMS	JTSG TMS	I
		6	Ext_fpga_TDI	JTAG TDI	I

Table 3.2.1 – ED-MTB connectors

3.3. The Skin

The touch is detected by CDC (Capacitance to Digital Converter) devices that sense an amount of capacitance (generically named "taxels") deployed along the surface of some body districts, hand palms and fingertips (generically called "skin"). There are three different patches for "skin" that are different for taxel displacement and physical characteristics that arise in different CDC configuration needs. They are here named as "standard", "palm" and "fingertip".

Note: the CDC device here used is the Analog Devices AD7147 (2) .

3.3.1. Standard Skin

The atomic standard skin patch is a triangular and flexible PCB with a CDC onboard on the top side and 13 capacitance pads (10 used as touch sensors, 3 available for thermal compensation) on the bottom side. The sensitive side of the PCB is the bottom side.

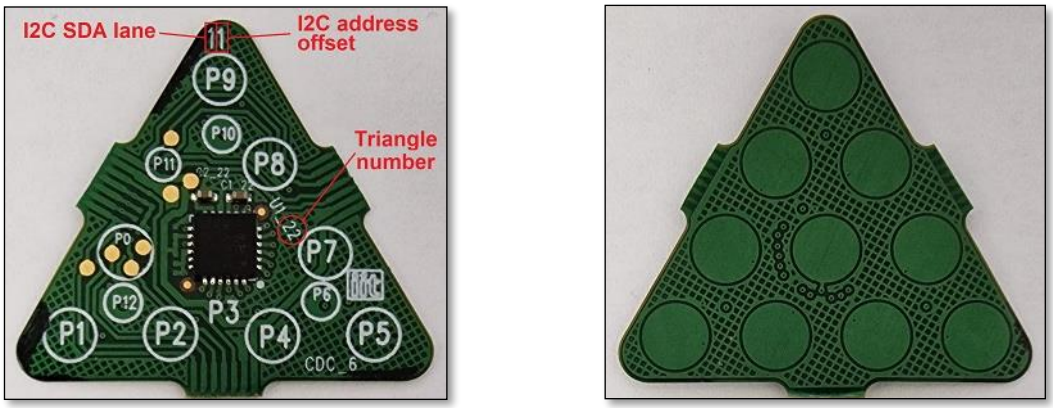


Figure 3.3.1 – Standard skin atomic patch. Top view, *component side* (left), Bottom view, *taxels side* (right)

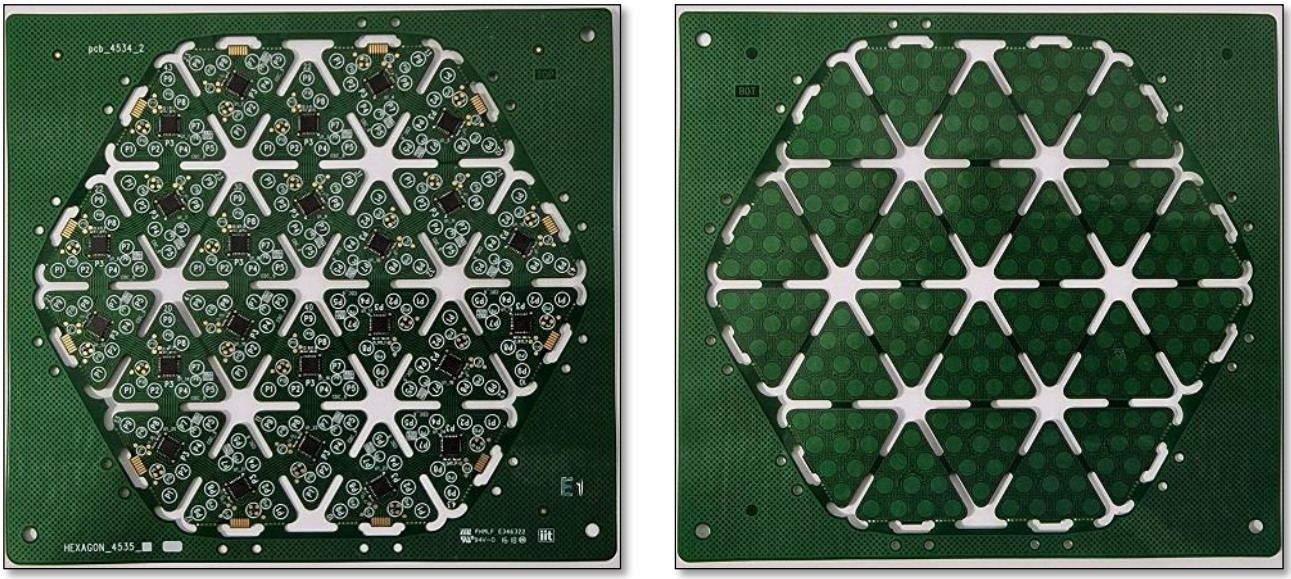


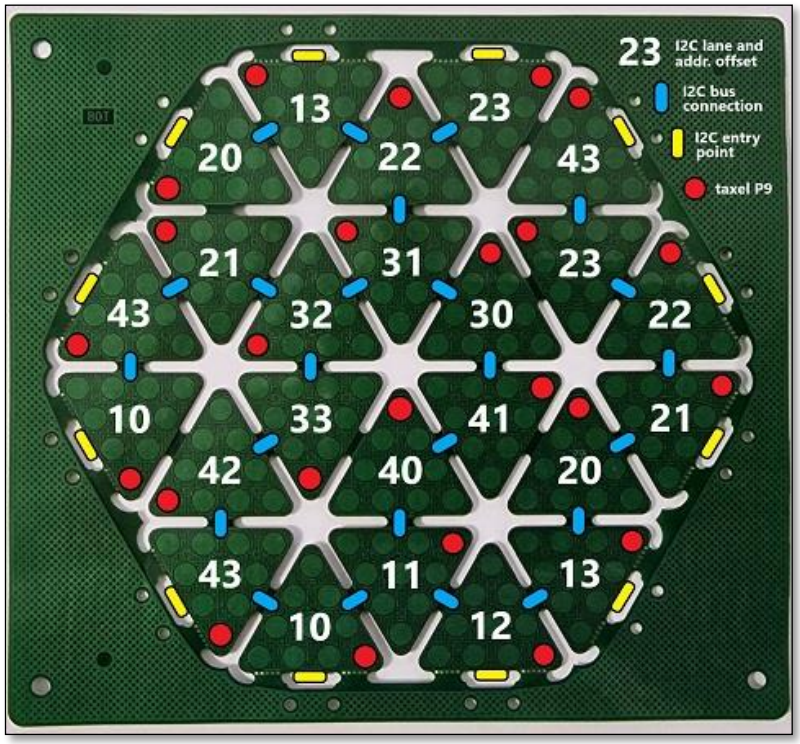
Figure 3.3.2 – "Hexagon". Top view, *component side* (left), Bottom view, *taxels side* (right)

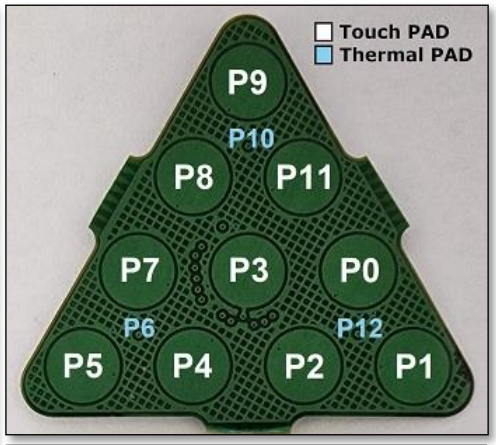
The CDC mounted on the PCB communicates via I2C bus; the five most significant bits of device address are "01011", but the two less significant bits are settable by tying two dedicated pins to Vcc or GND. It means that I2C address of device has a base of 0x2C and a hardware selectable offset from 0 to 3; that means, it is possible to connect up to 4 CDC on the same I2C bus.

ED-Skin is capable to master up to 4 different lanes (meaning 4 different SDA[7] lines with the same SCL[8] line), so it can handle 16 different triangles. Triangles are provided grouped in a bigger flexible PCB called *Hexagon* that comprehend 24 triangles conveniently connected each to others in a sort of hexagonal shape. Hexagon has 1 SCL clock line and 4 SDA data lines (lanes) conveniently distributed and connected through triangles. The number printed on the top corner of each triangle declares the I2C lane that CDC is connected to (left digit) and the offset of I2C address.

For example, the CDC of triangle shown in Figure 3.3.1 is connected to lane 1 with address 0x2D. The "triangle number" is just a decimal tag that identifies the triangle in the "Hexagon".

User can crop appropriately the Hexagon to create shapes best fitting the body area he has to cover





ED-Skin can handle up to 16 triangles, and user can crop the *hexagon* to create different shapes considering that each triangle must be reached by I2C bus by bus connection (blue marks) and they must have

Figure 3.3.3 – Labels of triangle in Hexagon and labels of taxels in triangle. Bottom view

TAXEL	CDC input
P0	CIN0
P1	CIN1
P2	CIN2
P3	CIN3
P4	CIN4
P5	CIN5
P6	CIN6
P7	CIN7
P8	CIN8
P9	CIN9
P10	CIN10
P11	CIN11
P12	CIN12

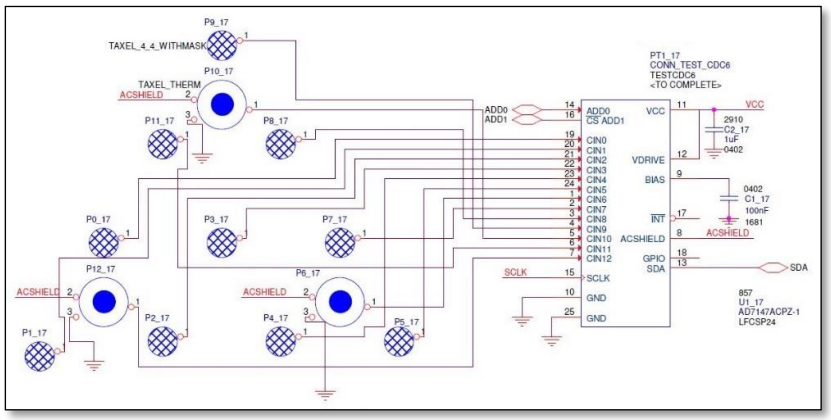


Table 3.3.1 and **Figure 3.3.4** – Connection between Taxel pads of standard skin and CIN input of CDC

[7] **SDA** Serial Data for I2C communication Protocol

[8] **SCL** Serial Clock for I2C communication Protocol

The following data are relative to the flexible PCB that composes the standard skin; measures (sides of triangles and their thickness) are important to understand how triangles may fit to destination

PRINTED CIRCUIT BOARD (PCB) SPECIFICATIONS	
	All measurements in mm
PCB IIT code	4534
PCB revision	2
Layer number	PCB FLEX 4 (see build-up)
Total PCB thickness	0.24+/-10%
Base Copper thick ext/int	(see build-up)
Minimum trace width ext/int	0,3/0,3
Minimum clearance ext/int	0,125/0,125
Minimum hole	0,2 th - 0,1 laser (1-n)
Single PCB max dimesions	145x132
Surface finish	ENIG (Rohs)
Silkscreen	Yes, top only (white)
Solder mask	Yes, top and bottom (green)

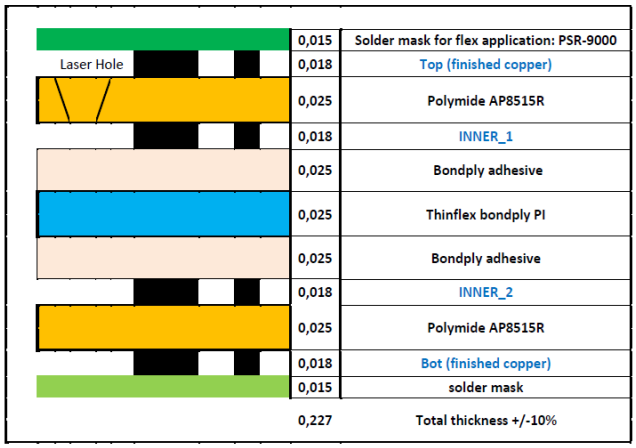


Figure 3.3.5 – Specification of Hexagon PCB

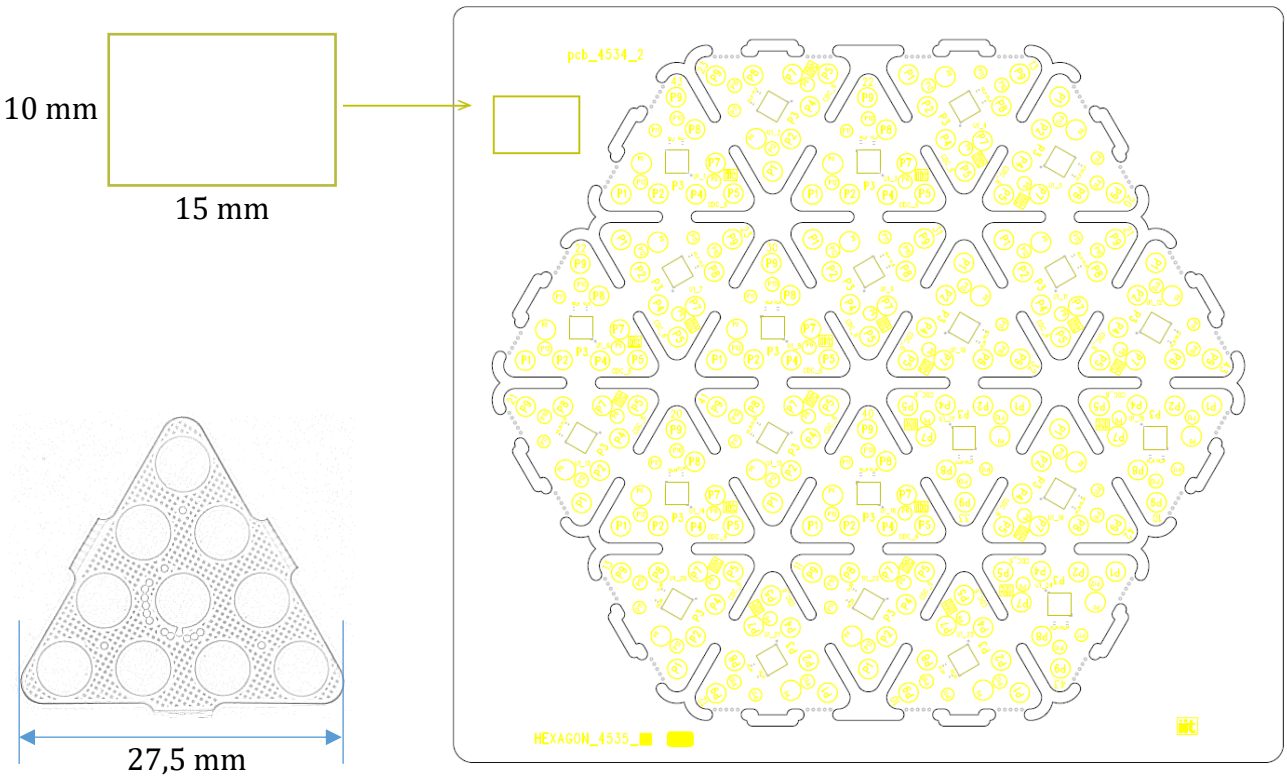


Figure 3.3.6 – Measures of Hexagon

3.3.2. Palm Skin

Palm skin (flexible PCB) is composed by four districts managed by 4 different CDC. As mentioned above, up to 4 CDC can share the same I2C bus so the palm has got only one I2C lane. At current date, the palm is connected to SDA3 lane.

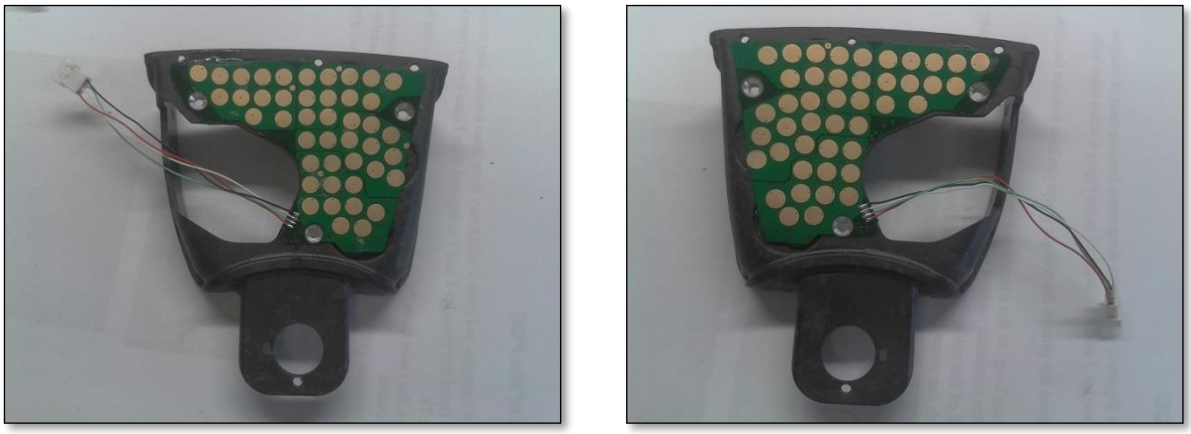


Figure 3.3.7 – Palm skin, bottom view. Left hand (left) and right hand (right)

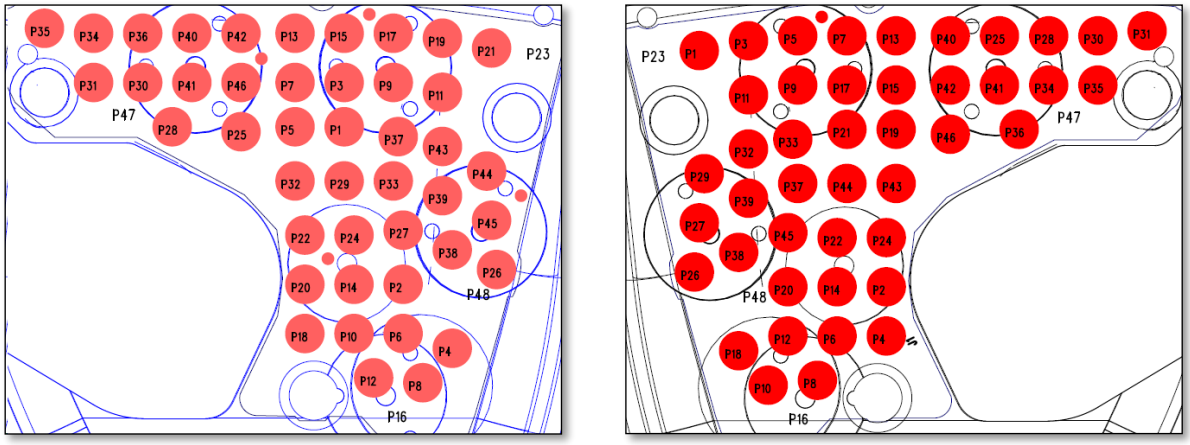


Figure 3.3.8 – Displacement of the taxels in palms. Left hand (left) and right hand (right). P23, P47, P48 and P16 are available for thermal compensation. Please note the displacement is not symmetrical

0x2C device		0x2D device		0x2E device		0x2F device	
TAXEL	**CDC input**	**TAXEL**	**CDC input**	**TAXEL**	**CDC input**	**TAXEL**	**CDC input**
P1	CIN0	P26	CIN0	P25	CIN0	P2	CIN0
P3	CIN1	P27	CIN1	P28	CIN1	P4	CIN1
P5	CIN2	P29	CIN2	P30	CIN2	P6	CIN2
P7	CIN3	P32	CIN3	P31	CIN3	P8	CIN3
P9	CIN4	P33	CIN4	P34	CIN4	P10	CIN4
P11	CIN5	P37	CIN5	P35	CIN5	P12	CIN5
P13	CIN6	P38	CIN6	P36	CIN6	P14	CIN6
P15	CIN7	P39	CIN7	P40	CIN7	P16 (thermal)	CIN7
P17	CIN8	P43	CIN8	P41	CIN8	P18	CIN8
P19	CIN9	P44	CIN9	P42	CIN9	P20	CIN9
P21	CIN10	P45	CIN10	P46	CIN10	P22	CIN10
P23 (thermal)	CIN11	P48 (thermal)	CIN11	P47 (thermal)	CIN11	P24	CIN11
N.C.	CIN12	N.C.	CIN12	N.C.	CIN12	N.C.	CIN12

Table 3.3.2 – Connection between *Taxel* pads of palm skin and CIN input of CDCs (valid for both palms)

PRINTED CIRCUIT BOARD (PCB) SPECIFICATIONS	
	All measurements in mm
PCB IIT code	4700
PCB revision	0
Material	Kapton
Total PCB thickness	0.25 mm
Base Copper thick	17 um
Surface finish	Gold (Rohs)
Silkscreen	Yes, top
Single PCB max dimesions	70x50 mm
Layers	4

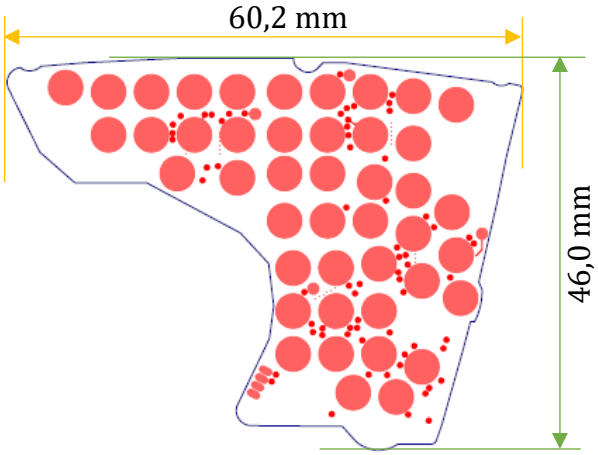
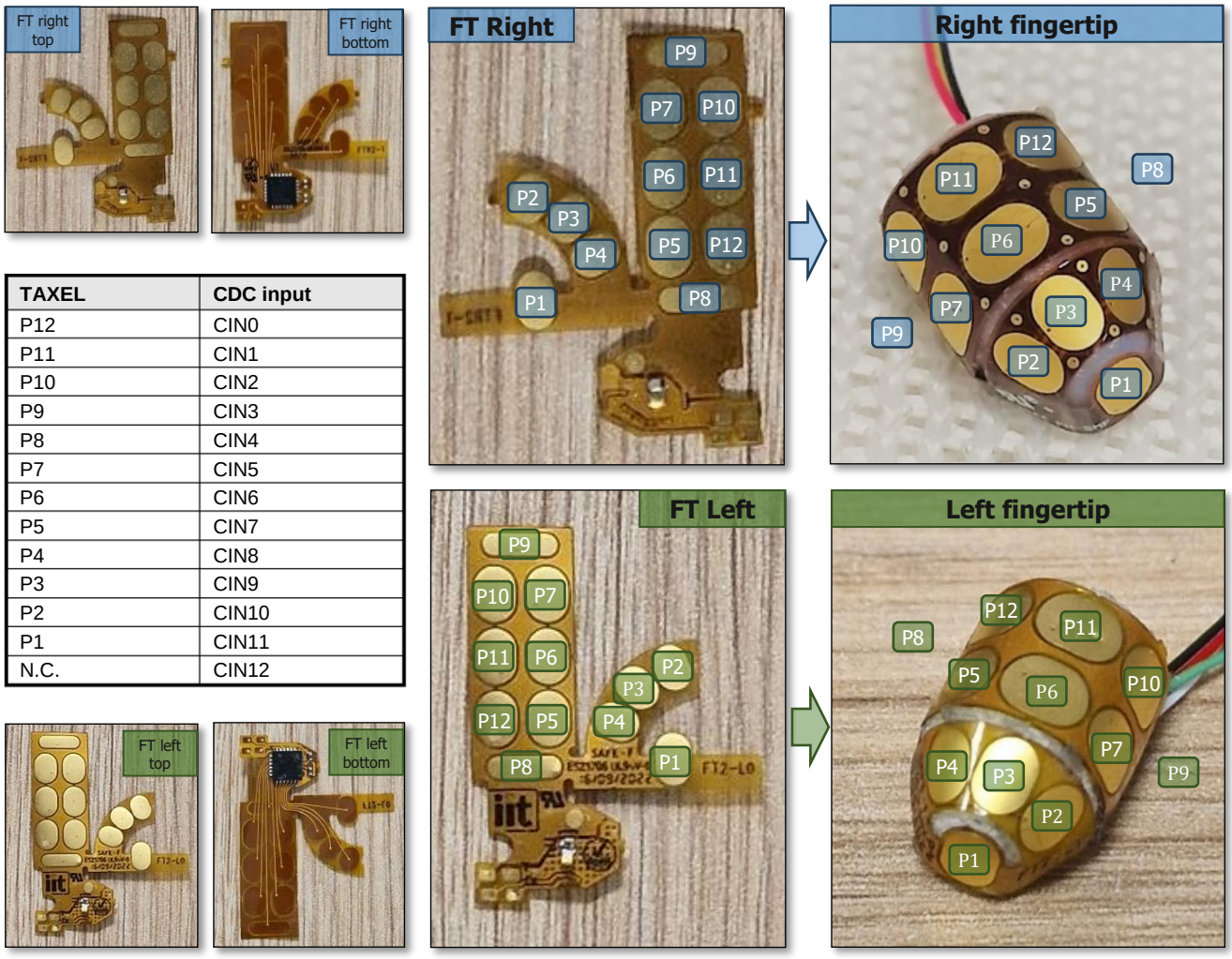


Figure 3.3.9 – Palm skin, technical information

3.3.3. Fingertip Skin

Fingertip skin version 2 (FT2) is composed by a flexible PCB with a particular outline suitable for a 3D fitting over a cylindrical and truncated cone shape. PCBs for left-hand fingertips and right-hand fingertips are symmetric and are the same for all the five fingers. At current date, the thumb is connected to SDA2 lane and the other fingers to SDA1 lane.



TAXEL	CDC input
P12	CIN0
P11	CIN1
P10	CIN2
P9	CIN3
P8	CIN4
P7	CIN5
P6	CIN6
P5	CIN7
P4	CIN8
P3	CIN9
P2	CIN10
P1	CIN11
N.C.	CIN12

Figure 3.3.10 and Table 3.3.3 – Displacement of the taxels in fingertips and their connection to CIN inputs of CDC

4. CCAM3 (EVENT BASED VISION)

4.1. Introduction

The FPGA based system, an assembly named CCAM3-IIT_GEN3, is used to manage the ATIS GEN3 camera and generate its AER Events over the AER backbone, sent via Gigabit Transceivers. It's composed by three boards:

1. ATIS board:
   This is the board hosting the ATIS GEN3 sensor.
2. CCAM3-Processing
   This board is based upon the usage of Artix XC7A50T-CPG236-1. It contains also the SPI flash memory used to store the bitstream for the FPGA,
3. CCAM-CTR
   This board is used as bridge to proper connectors (LVDS lines for HSSAER, Gigabit Transceivers lanes, I2C lines, eventually through buffers/drivers; it also hosts the JTAG connector for programming the flash memory and debugging the FPGA).

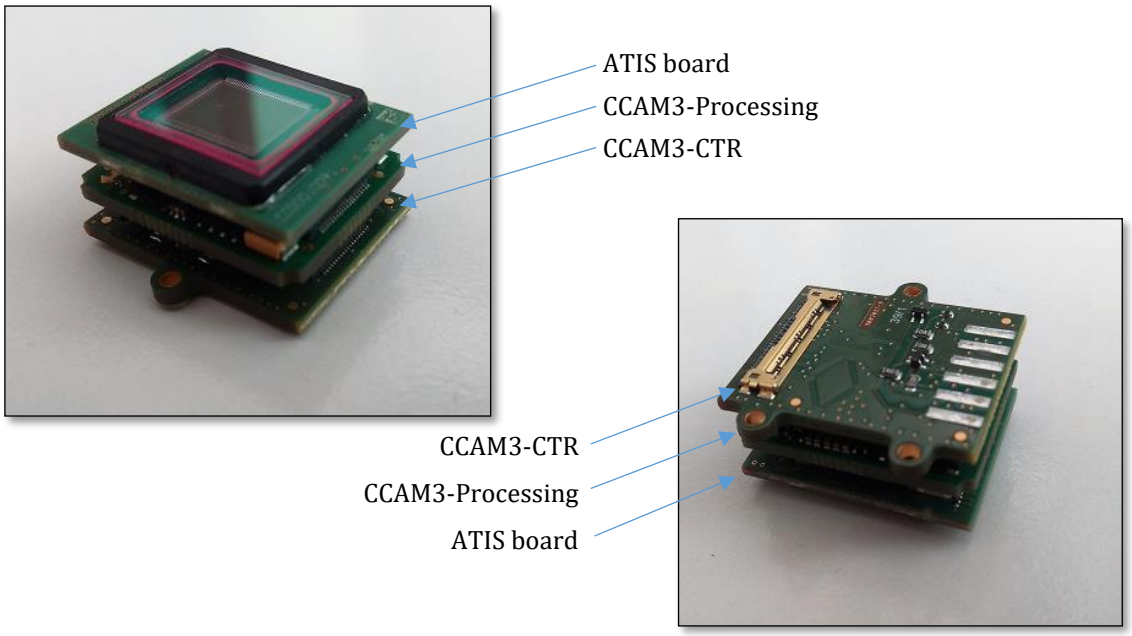


Figure 4.1.1 - The CCAM3-Processing/CCAM3-CTR/ATIS boards

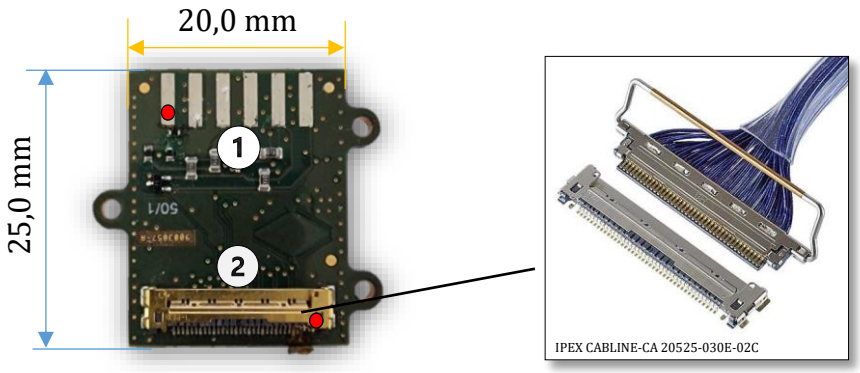


Figure 4.1.2 - The CCAM3-CTR board dimension and connectors

#	ID	PIN	SIG. NAME	DESCRIPTION	DIR
				JTAG	
1	J1	1	+5V	+5V power supply	
		2	GND	Ground	
		3	TCK	JTAG - Test Clock	I
		4	TDO	JTAG - Test Data Out	O
		5	TMS	JTAG - Test Mode Select	I
		6	TDI	JTAG - Test Data In	I
				MAIN CAMERA CONNECTOR	
2	J2	1	+5V	+5V power supply	
		2	+5V	+5V power supply	
		3	+5V	+5V power supply	
		4	GND	Ground	
		5	lvds4_n	Generic differential line, n side (originally used as HSSAER Lane 3)	O
		6	lvds4_p	Generic differential line, p side (originally used as HSSAER Lane 3)	O
		7	GND	Ground	
		8	lvds3_n	Generic differential line, n side (originally used as HSSAER Lane 2)	O
		9	lvds3_p	Generic differential line, p side (originally used as HSSAER Lane 2)	O
		10	GND	Ground	
		11	lvds2_n	Generic differential line, n side (originally used as HSSAER Lane 1)	O
		12	lvds2_p	Generic differential line, p side (originally used as HSSAER Lane 1)	O
		13	GND	Ground	
		14	lvds1_n	Generic differential line, n side (originally used as HSSAER Lane 0)	O
		15	lvds1_p	Generic differential line, p side (originally used as HSSAER Lane 0)	O
		16	GND	Ground	
		17	fpga_Slave_CSn	Used as I2C SDA signal (data)	I/O
		18	fpga_Slave_MISO	Spare	
		19	fpga_Slave_MOSI	Spare	
		20	fpga_Slave_SCK	Used as I2C SCK signal (clock)	I/O
		21	GND	Ground	
		22	mgtrefCLK0p	Reference clock for Gigabit Transceiver, p side	I
		23	mgtrefCLK0n	Reference clock for Gigabit Transceiver, n side	I
		24	GND	Ground	
		25	mgtpTXp1	Gigabit Transceiver TX lane 1, p side	O
		26	mgtpTXn1	Gigabit Transceiver TX lane 1, n side	O
		27	GND	Ground	
		28	mgtpTXp0	Gigabit Transceiver TX lane 0, p side	O
		29	mgtpTXn0	Gigabit Transceiver TX lane 0, n side	O
		30	GND	Ground	

Table 4.1.1 – CCAM3 connectors

4.2. ATIS GEN3 Event Based sensor

The adopted ATIS GEN3 camera (part Number CCVS1STMU0300A) is a VGA event-based vision sensor developed around 15-um x 15-um contrast detection pixels. This vision sensor technology features low power consumption, always-on full awareness, high dynamic range and compressed data output. The pixel array contains 640 x 480 event-driven pixels.

GEN3 produces output data as “AER events” on a synchronous **21-bit bus** (DY + DX + DPOL for coordinates and polarity) with **valid** (DV) and **ready** (RD) signals, plus a **type** (DTYP) for TD (contrast Detection) or EM (Exposure Measurement) data signal.

Please note that EM data are available only with CCVS1SAMU0170A device (not adopted)

The maximum rate is 30 Mevents/sec.

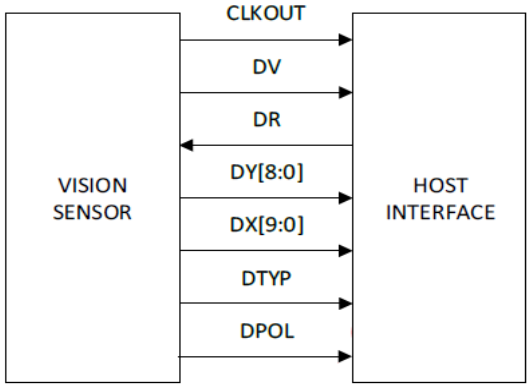


Figure 4.2.1 – GEN3 data connections

5. USB EVENT BASED CAMERAS

5.1. Introduction

For iCub Manchester and Kangaroo, two (optionally one) external USB3 Event Based Cameras would be used.

Two suitable candidates could be:

1. Metavision® EVK4 – HD
   With IMX636 (1280x720) realized in collaboration between Sony and PROPHESEE.
   Details can be found at https://www.prophesee.ai/

2. SilkyEvCam VGA
   Equipped with PROPHESEE event-based vision sensor (640x480)
   Details can be found at https://centuryarks.com/en/silkyevcam-vga/

6. PEYE - PYTHON CAMERAS (FRAME BASED)

6.1. Introduction

For completeness, here are mentioned also the Frame Based camera adopted on iCub – Genoa; they are interfaced with YARP and sends data coming from the same field of view of event based camera (a beam splitter placed into the eyes of iCub permits both cameras in the same eye to receive the same real image). The adopted device is a Python 1.3 MegaPixel Global Shutter CMOS image sensor (1280 x 1024 Active Pixels, 1/2" Optical Format), Bayer Color, with 4 LVDS Data Channels data output, 10 bit, 210/165 frames per second (depending on operational mode). Part number Onsemi NOIP1SN1300A-QDI (3)

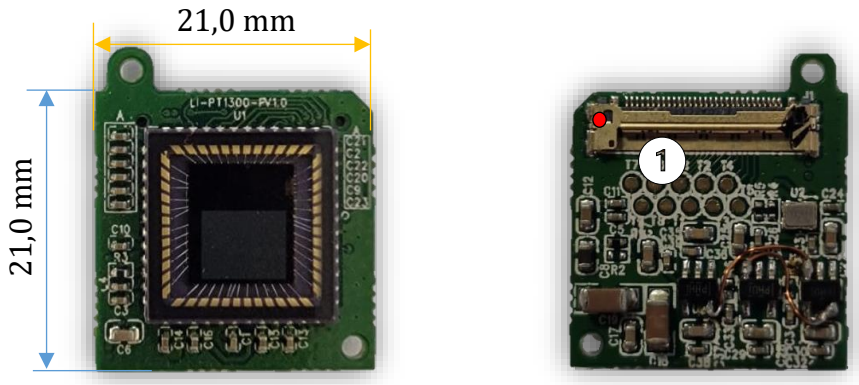


Figure 6.1.1 – Python camera modules

6.2. Connections

#	ID	PIN	SIG. NAME	DESCRIPTION	DIR
MAIN CAMERA CONNECTOR					
1	J1	1	SCK	SPI Clock	
		2	MISO	SPI Master In – Slave Out	
		3	MOSI	SPI Master Out – Slave In	
		4	NSEL	SPI Slave Select (Active Low)	

		5	RSTN	Sensor Reset (Active Low)	O
		6	GND	Ground	O
		7	CLK_OUTN	LVDS Clock Output (Negative)	
		8	CLK_OUTP	LVDS Clock Output (Positive)	O
		9	DOUTN0	LVDS Data Output Channel #0 (Negative)	O
		10	DOUTP0	LVDS Data Output Channel #0 (Positive)	
		11	DOUTN1	LVDS Data Output Channel #1 (Negative)	O
		12	DOUTP1	LVDS Data Output Channel #1 (Positive)	O
		13	MON1	Monitor Output #1	
		14	MON0	Monitor Output #0	O
		15	TRIGGER1	Trigger Input #1	O
		16	TRIGGER0	Trigger Input #0	
		17	CLK_PLL	Reference Clock Input for PLL	I/O
		18	GND	Ground	
		19	DOUTN2	LVDS Data Output Channel #2 (Negative)	
		20	DOUTP2	LVDS Data Output Channel #2 (Positive)	I/O
		21	DOUTN3	LVDS Data Output Channel #3 (Negative)	
		22	DOUTP3	LVDS Data Output Channel #3 (Positive)	I
		23	LVDS_CLKINN	LVDS Clock Input (Negative)	I
		24	LVDS_CLKINP	LVDS Clock Input (Positive)	
		25	SYNCN	LVDS Sync Channel Output (Negative)	O
		26	SYNCP	LVDS Sync Channel Output (Positive)	O
		27	GND	Ground	
		28	+5V	+5V power supply	O
		29	+5V	+5V power supply	O
		30	+5V	+5V power supply	

Table 6.2.1 – Python module connectors

7. UZCB

7.1. Introduction

UZCB stands for **Ultrascale Zynq Carrier Board** and acts as bridge between sensors and YARP; it hosts a commercial daughter board based on a XILINX Ultrascale+ SoC device that, basically, has in charge to merge, arbitrate and manage events coming from sensor boards; it also tags them with a Timestamp permitting to have also a temporal representation of events.

Figure 7.1.1 – UZCB with the SoC module (and cooling fan)

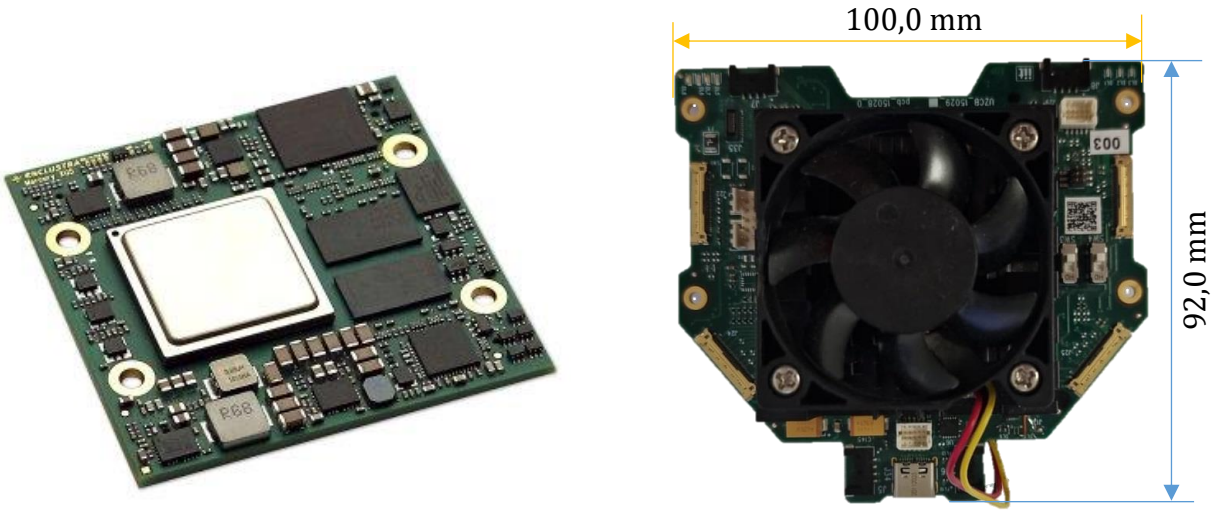
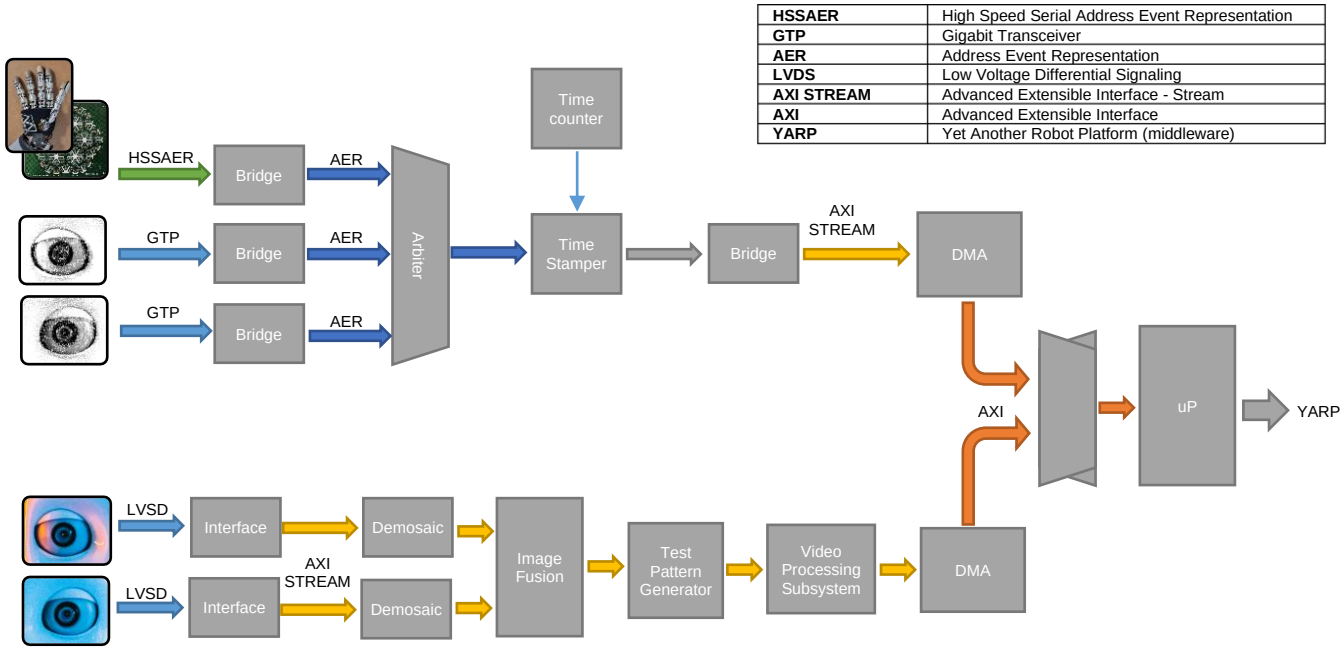


Figure 7.1.2 - The SoC module and size of UZCB

The used Ultrascale+ Soc Module is a Mercury XU5 provided by Enclustra (4)
The part adopted is the ME-XU5-5EV-2I-D12E, equipped with an AMD-Xilinx Ultrascale+ (5) XCZU5EV-2SFVC784I (industrial range), 4GB DDR for PS side[9] and 1 GB DDR for PL side[10].

7.2. Block Diagram



HSSAER	High Speed Serial Address Event Representation
GTP	Gigabit Transceiver
AER	Address Event Representation
LVDS	Low Voltage Differential Signaling
AXI STREAM	Advanced Extensible Interface - Stream
AXI	Advanced Extensible Interface
YARP	Yet Another Robot Platform (middleware)

Figure 7.2.1 – UCZCB block Diagram

[9] **Processor** side is the computational part of the SoC, powered by ARM processors

[10] **Programmable Logic** side is the FPGA fabric part of the SoC

7.3. Connectors

Here are described connectors to sensors relevant to the scope of this document.

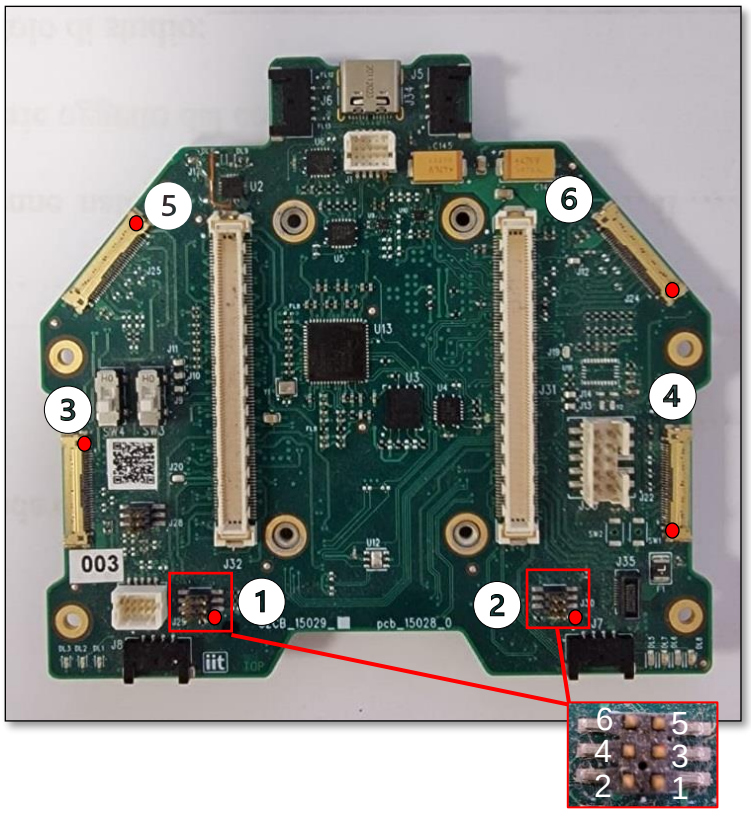


Figure 7.3.1 – UZCB top

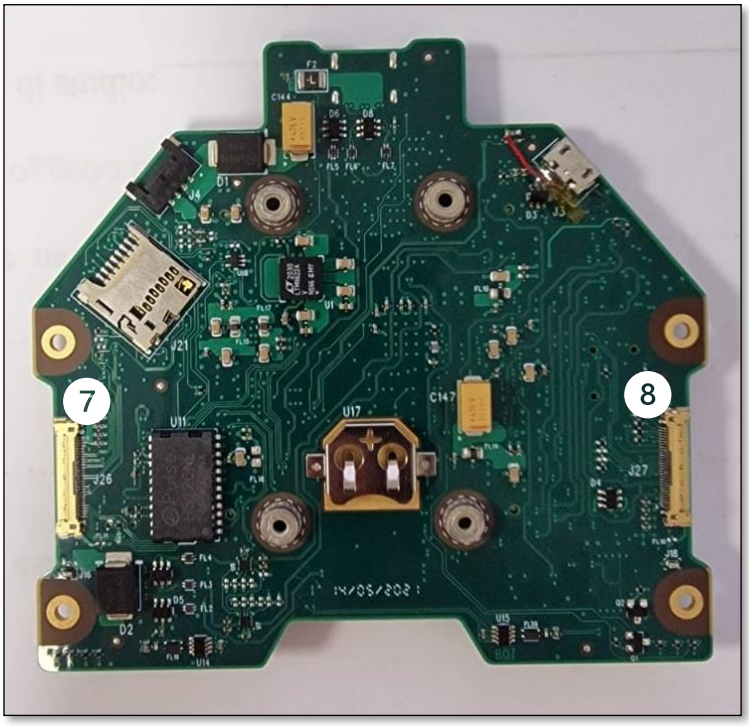


Figure 7.3.2 – UZCB bottom

#	ID	PIN	SIG. NAME	DESCRIPTION	DIR
SKIN – Left Side					
1	J29	1	+5V	+5V power supply (+3,3V hardware selectable)	
		2	GND	Ground	
		3	I2C_SKx_SCL	I2C clock (shared with right side connector #2 – J30)	I/O
		4	I2C_SKL_SDA	I2C data – left skin	I/O
		5	SKL_HSSAER_p	HSSAER input side p (LVDS)	I
		6	SKL_HSSAER_n	HSSAER input side n (LVDS)	I
SKIN – Right Side					
2	J30	1	+5V	+5V power supply (+3,3V hardware selectable)	
		2	GND	Ground	
		3	I2C_SKx_SCL	I2C clock (shared with left side connector #1 – J29)	I/O
		4	I2C_SKL_SDA	I2C data – right skin	I/O
		5	SKL_HSSAER_p	HSSAER input side p (LVDS)	I
		6	SKL_HSSAER_n	HSSAER input side n (LVDS)	I
EVENT BASED CAMERA CONNECTOR - Left					
3	J23	1	GND	Ground	
		2	EDL_MGT_RX_n	Gigabit Transceiver RX lane 1, n side – left camera	I
		3	EDL_MGT_RX_p	Gigabit Transceiver RX lane 1, p side – left camera	I
		4	GND	Ground	
		5	EDL_MGT_TX_n	Gigabit Transceiver TX lane 1, n side – Spare for other applications	O
		6	EDL_MGT_TX_p	Gigabit Transceiver TX lane 1, p side – Spare for other applications	O
		7	GND	Ground	
		8	EDL_MGT_CK_n	Reference clock for Gigabit Transceiver, n side – left camera	O
		9	EDL_MGT_CK_p	Reference clock for Gigabit Transceiver, p side – left camera	O
		10	GND	Ground	
		11	I2C_EDx_SPx_SCL	I2C SCK signal (clock) – shared with connectors 4, 5 and 6	I/O
		12	EDL_SPARE_p	Spare signal	
		13	EDL_SPARE_n	Spare signal	
		14	I2C_EDL_SPA_SDA	I2C SDA signal (data) – left camera - shared with connector 5	I/O
		15	GND	Ground	
		16	EDL_HSSAER_0_n	Spare differential line, n side	
		17	EDL_HSSAER_0_p	Spare differential line, p side	
		18	GPIO_L_0		
		19	EDL_HSSAER_1_p	Spare differential line, n side	
		20	EDL_HSSAER_1_n	Spare differential line, p side	
		21	GND	Ground	
		22	EDL_HSSAER_2_n	Spare differential line, n side	
		23	EDL_HSSAER_2_p	Spare differential line, p side	
		24	GND	Ground	
		25	EDL_HSSAER_3_p	Spare differential line, n side / hardware selectable as +5V or +3,3V	
		26	EDL_HSSAER_3_n	Spare differential line, p side / hardware selectable as +5V or +3,3V	
		27	GND	Ground	
		28	+5V	+5V power supply	
		29	+5V	+5V power supply	
		30	+5V	+5V power supply	
EVENT BASED CAMERA CONNECTOR - Right					
4	J22	1	GND	Ground	
		2	EDR_MGT_RX_n	Gigabit Transceiver RX lane 1, n side – right camera	I
		3	EDR_MGT_RX_p	Gigabit Transceiver RX lane 1, p side – right camera	I
		4	GND	Ground	
		5	EDR_MGT_TX_n	Gigabit Transceiver TX lane 1, n side – Spare for other applications	O
		6	EDR_MGT_TX_p	Gigabit Transceiver TX lane 1, p side – Spare for other applications	O
		7	GND	Ground	
		8	EDR_MGT_CK_n	Reference clock for Gigabit Transceiver, n side – right camera	O
		9	EDR_MGT_CK_p	Reference clock for Gigabit Transceiver, p side – right camera	O
		10	GND	Ground	
		11	I2C_EDx_SPx_SCL	I2C SCK signal (clock) – shared with connectors 3, 5 and 6	I/O
		12	EDR_SPARE_p	Spare signal	
		13	EDR_SPARE_n	Spare signal	
		14	I2C_EDR_SPA_SDA	I2C SDA signal (data) – right camera	I/O

#	ID	PIN	SIG. NAME	DESCRIPTION	DIR
		15	GND	Ground	
		16	EDR_HSSAER_0_n	Spare differential line, n side	
		17	EDR_HSSAER_0_p	Spare differential line, p side	
		18	GPIO_L_0		
		19	EDR_HSSAER_1_p	Spare differential line, n side	
		20	EDR_HSSAER_1_n	Spare differential line, p side	
		21	GND	Ground	
		22	EDR_HSSAER_2_n	Spare differential line, n side	
		23	EDR_HSSAER_2_p	Spare differential line, p side	
		24	GND	Ground	
		25	EDR_HSSAER_3_p	Spare differential line, n side / hardware selectable as +5V or +3,3V	
		26	EDR_HSSAER_3_n	Spare differential line, p side / hardware selectable as +5V or +3,3V	
		27	GND	Ground	
		28	+5V	+5V power supply	
		29	+5V	+5V power supply	
		30	+5V	+5V power supply	
SPARE CONNECTOR A					
		1	GND	Ground	
		2	SPA_MGT_RX_n	Gigabit Transceiver RX lane 1, n side	I
		3	SPA_MGT_RX_p	Gigabit Transceiver RX lane 1, p side	I
		4	GND	Ground	
		5	SPA_MGT_TX_n	Gigabit Transceiver TX lane 1, n side	O
		6	SPA_MGT_TX_p	Gigabit Transceiver TX lane 1, p side	O
		7	GND	Ground	
		8	SPA_MGT_CK_n	Reference clock for Gigabit Transceiver, n side	O
		9	SPA_MGT_CK_p	Reference clock for Gigabit Transceiver, p side	O
		10	GND/SPA_SPARE_p	Ground / Hardware selectable as a signal named SPA_SPARE_p	
		11	I2C_EDx_SPx_SCL	I2C SCK signal (clock) – shared with connectors 3, 4 and 6	I/O
		12	SPA_DIFF4_MIPI4_p	Spare signal (suitable for MIPI)	
		13	SPA_DIFF4_MIPI4_n	Spare signal (suitable for MIPI)	
		14	I2C_EDL_SPA_SDA	I2C SDA signal (data) – shared with connector 3	I/O
		15	GND/SPA_SPARE_n	Ground / Hardware selectable as a signal named SPA_SPARE_n	
5	J25	16	SPA_DIFF0_MIPICLK_n	Spare signal (suitable for MIPI)	
		17	SPA_DIFF0_MIPICLK_p	Spare signal (suitable for MIPI)	
		18	GND		
		19	SPA_DIFF1_MIPI1_p	Spare signal (suitable for MIPI)	
		20	SPA_DIFF1_MIPI1_n	Spare signal (suitable for MIPI)	
		21	GND	Ground	
		22	SPA_DIFF2_MIPI2_p	Spare signal (suitable for MIPI)	
		23	SPA_DIFF2_MIPI2_n	Spare signal (suitable for MIPI)	
		24	GND	Ground	
		25	SPA_DIFF3_MIPI3_p	Spare signal (suitable for MIPI)/ hardware selectable as +5V or +3,3V	
		26	SPA_DIFF3_MIPI3_n	Spare signal (suitable for MIPI)/ hardware selectable as +5V or +3,3V	
		27	GND	Ground	
		28	+5V	+5V power supply	
		29	+5V	+5V power supply	
		30	+5V	+5V power supply	
SPARE CONNECTOR B					
		1	GND	Ground	
		2	SPB_MGT_RX_n	Gigabit Transceiver RX lane 1, n side	I
		3	SPB_MGT_RX_p	Gigabit Transceiver RX lane 1, p side	I
		4	GND	Ground	
		5	SPB_MGT_TX_n	Gigabit Transceiver TX lane 1, n side	O
		6	SPB_MGT_TX_p	Gigabit Transceiver TX lane 1, p side	O
		7	GND	Ground	
6	J24	8	SPB_MGT_CK_n	Reference clock for Gigabit Transceiver, n side	O
		9	SPB_MGT_CK_p	Reference clock for Gigabit Transceiver, p side	O
		10	GND/SPB_SPARE_p	Ground / Hardware selectable as a signal named SPA_SPARE_p	
		11	I2C_EDx_SPx_SCL	I2C SCK signal (clock) – shared with connectors 3, 4 and 5	I/O
		12	SPB_DIFF4_MIPI4_p	Spare signal (suitable for MIPI)	
		13	SPB_DIFF4_MIPI4_n	Spare signal (suitable for MIPI)	
		14	I2C_EDL_SPB_SDA	I2C SDA signal (data) – shared with connector 3	I/O
		15	GND/SPB_SPARE_n	Ground / Hardware selectable as a signal named SPA_SPARE_n	

#	ID	PIN	SIG. NAME	DESCRIPTION	DIR
		16	SPB_DIFF0_MIPICLK_n	Spare signal (suitable for MIPI)	
		17	SPB_DIFF0_MIPICLK_p	Spare signal (suitable for MIPI)	
		18	GND		
		19	SPB_DIFF1_MIPI1_p	Spare signal (suitable for MIPI)	
		20	SPB_DIFF1_MIPI1_n	Spare signal (suitable for MIPI)	
		21	GND	Ground	
		22	SPB_DIFF2_MIPI2_p	Spare signal (suitable for MIPI)	
		23	SPB_DIFF2_MIPI2_n	Spare signal (suitable for MIPI)	
		24	GND	Ground	
		25	SPA_DIFF3_MIPI3_p	Spare signal (suitable for MIPI)/ hardware selectable as +5V or +3,3V	
		26	SPA_DIFF3_MIPI3_n	Spare signal (suitable for MIPI)/ hardware selectable as +5V or +3,3V	
		27	GND	Ground	
		28	+5V	+5V power supply	
		29	+5V	+5V power supply	
		30	+5V	+5V power supply	
FRAME BASED CAMERA CONNECTOR - Left					
		1	+5V	+5V power supply	
		2	+5V	+5V power supply	
		3	+5V	+5V power supply	
		4	GND	Ground	
		5	FRL_SYNC_p	LVDS Sync Channel Input (Positive)	
		6	FRL_SYNC_n	LVDS Sync Channel Input (Negative)	
		7	FRL_HSCLK_p	LVDS Clock Output (Positive)	
		8	FRL_HSCLK_n	LVDS Clock Output (Negative)	
		9	FRL_DATA3_p	LVDS Data Input Channel #3 (Positive)	
		10	FRL_DATA3_n	LVDS Data Input Channel #3 (Negative)	
		11	FRL_DATA2_p	LVDS Data Input Channel #2 (Positive)	
		12	FRL_DATA2_n	LVDS Data Input Channel #2 (Negative)	
		13	GND	Ground	
		14	FRL_CLK_PLL	Reference Clock Output for PLL	
7	J27	15	FRL_TRIGGER_0_HW2	Trigger Output #0	
		16	FRL_TRIGGER_1_HW3	Trigger Output #1	
		17	FRL_MONITOR_0	Monitor Input #0	
		18	FRL_MONITOR_1	Monitor Input #1	
		19	FRL_DATA1_p	LVDS Data Input Channel #1 (Positive)	
		20	FRL_DATA1_n	LVDS Data Input Channel #1 (Negative)	
		21	FRL_DATA0_p	LVDS Data Input Channel #0 (Positive)	
		22	FRL_DATA0_n	LVDS Data Input Channel #0 (Negative)	
		23	FRL_DATACLK_p	LVDS Clock Input (Positive)	
		24	FRL_DATACLK_n	LVDS Clock Input (Negative)	
		25	GND	Ground	
		26	FRx_RSTn	Sensor Reset (Active Low) – shared with connector 8	
		27	SPI_SSn_FRL	SPI Slave Select (Active Low)	
		28	SPI_MOSI	SPI Master Out − Slave In – shared with connector 8	
		29	SPI_MISO	SPI Master In − Slave Out – shared with connector 8	
		30	SPI_SCK	SPI Clock – shared with connector 8	
FRAME BASED CAMERA CONNECTOR - Right					
		1	+5V	+5V power supply	
		2	+5V	+5V power supply	
		3	+5V	+5V power supply	
		4	GND	Ground	
		5	FRR_SYNC_p	LVDS Sync Channel Input (Positive)	
		6	FRR_SYNC_n	LVDS Sync Channel Input (Negative)	
		7	FRR_HSCLK_p	LVDS Clock Output (Positive)	
		8	FRR_HSCLK_n	LVDS Clock Output (Negative)	
8	J26	9	FRR_DATA3_p	LVDS Data Input Channel #3 (Positive)	
		10	FRR_DATA3_n	LVDS Data Input Channel #3 (Negative)	
		11	FRR_DATA2_p	LVDS Data Input Channel #2 (Positive)	
		12	FRR_DATA2_n	LVDS Data Input Channel #2 (Negative)	
		13	GND	Ground	
		14	FRR_CLK_PLL	Reference Clock Output for PLL	
		15	FRR_TRIGGER_0_HW2	Trigger Output #0	
		16	FRR_TRIGGER_1_HW3	Trigger Output #1	
		17	FRR_MONITOR_0	Monitor Input #0	
		18	FRR_MONITOR_1	Monitor Input #1	

#	ID	PIN	SIG. NAME	DESCRIPTION	DIR
		19	FRR_DATA1_p	LVDS Data Input Channel #1 (Positive)	
		20	FRR_DATA1_n	LVDS Data Input Channel #1 (Negative)	
		21	FRR_DATA0_p	LVDS Data Input Channel #0 (Positive)	
		22	FRR_DATA0_n	LVDS Data Input Channel #0 (Negative)	
		23	FRR_DATACLK_p	LVDS Clock Input (Positive)	
		24	FRR_DATACLK_n	LVDS Clock Input (Negative)	
		25	GND	Ground	
		26	FRx_RSTn	Sensor Reset (Active Low) – shared with connector 7	
		27	SPI_SSn_FRL	SPI Slave Select (Active Low)	
		28	SPI_MOSI	SPI Master Out − Slave In – shared with connector 7	
		29	SPI_MISO	SPI Master In − Slave Out – shared with connector 7	
		30	SPI_SCK	SPI Clock – shared with connector 7	

Table 7.3.1 –UZCB connectors

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