# Lab 4

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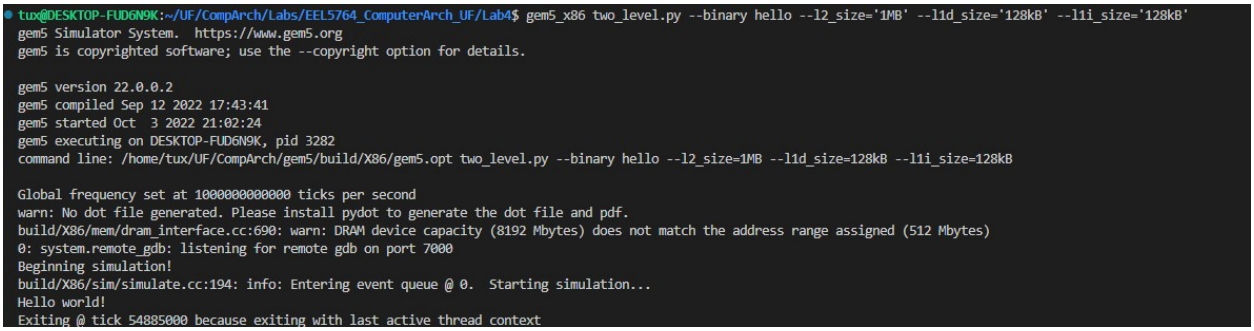
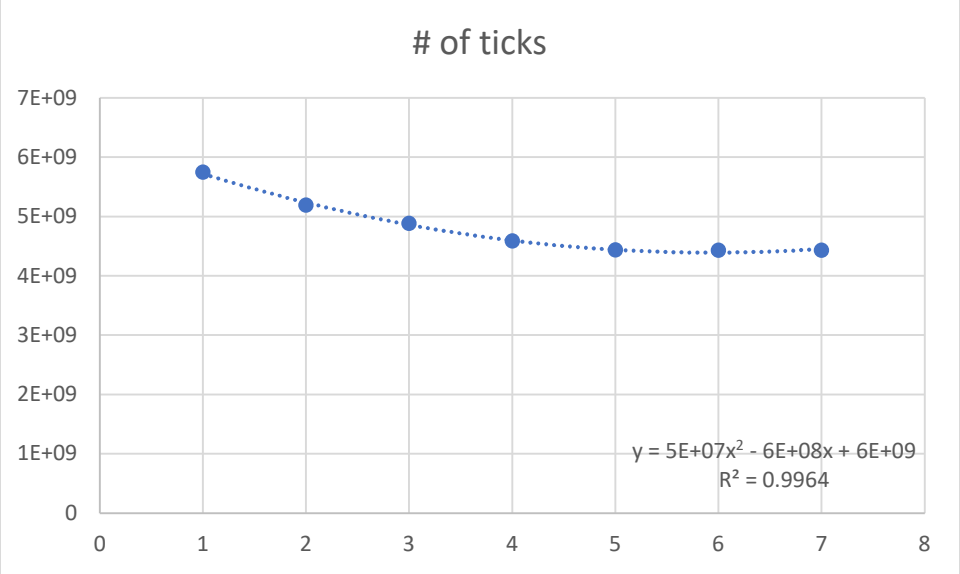


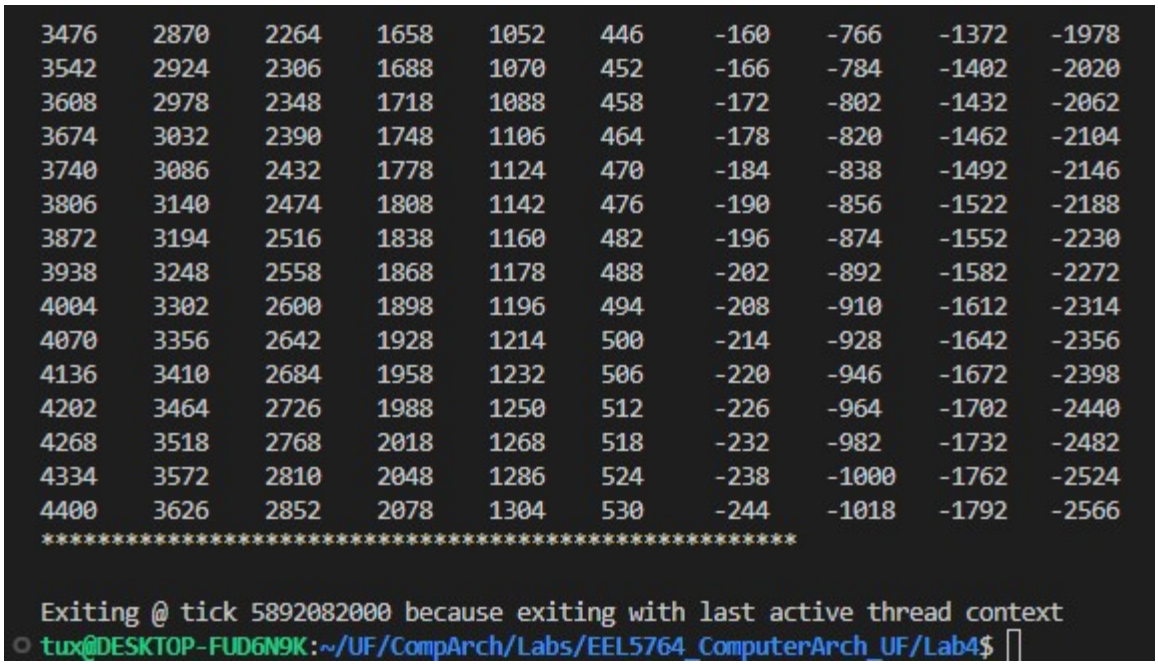

**Part A: Screenshot of added capabilities**

| L1ICache.size | # of ticks |
|---|---|
| 1kB | 5747481000 |
| 2kB | 5191374000 |
| 4kB | 4883423000 |
| 8kB | 4586946000 |
| 16kB | 4439466000 |
| 32kB | 4433041000 |
| 64kB | 4433041000 |

**Part B Table: L1Cache Size vs # of Ticks**




**Part B Graph: L1Cache Size vs # of Ticks**




**Part C: Screenshot**

| Row # | l1i_assoc = | 1 | 2 | 4 | 8 |
|---|---|---|---|---|---|
| 1 | **Exit tick #** (from last screen) | 4592817000 | 4433041000 | 4345860000 | 4334274000 |
| 2 | # number of overall hits (Count) | 1631678 | 1638313 | 1641937 | 1642429 |
| 3 | # number of overall misses (Count) | 11321 | 4686 | 1062 | 570 |
| 4 | # number of overall miss ticks (Tick) | 337063000 | 164119000 | 69607000 | 57013000 |
| 5 | # average overall miss latency ((Tick/Count)) | 29773.2532 | 35023.2608 | 65543.3145 | 100022.807 |
| 6 | # number of overall (read+write) accesses (Count) | 1642999 | 1642999 | 1642999 | 1642999 |
| 7 | # miss rate for overall accesses (Ratio) | 0.00689 | 0.002852 | 0.000646 | 0.000347 |
| 8 | # number of replacements (Count) | 11091 | 4437 | 808 | 314 |

**Part D: Experimental Findings**

**Question**

**Q1:** Overall the performance increased each time the associativity was raised. The rate of increase in performance decreased as the associativity was increased.

**Q2:** Direct mapped cache

**Q3:** Row 5 **=** Row 4 / Row 3

**Q4:** Row 7 = Row 3 / Row 6

**Q5:** Rows 1, 2, 3, 4, 7, 8