

python3 `which scons` build/X86/gem5.opt -j7

```
[ SHCC] X86/ext/libelf/gelf_cap.c -> .os
[ SHCC] X86/ext/libelf/gelf_fsize.c -> .os
[ SHCC] X86/ext/libelf/elf_end.c -> .os
[ SHCC] X86/ext/libelf/libelf_ehdr.c -> .os
[ SHCC] X86/ext/libelf/elf_phnum.c -> .os
[ SHCC] X86/ext/libelf/gelf_ehdr.c -> .os
[ SHCC] X86/ext/libelf/elf.c -> .os
[ SHCC] X86/ext/libelf/libelf_checksum.c -> .os
[ SHCC] X86/ext/libelf/gelf_shdr.c -> .os
[ SHCC] X86/ext/libelf/elf_getarsym.c -> .os
[ SHCC] X86/ext/libelf/gelf_syminfo.c -> .os
[ SHCC] X86/ext/libelf/elf_hash.c -> .os
[ SHCC] X86/ext/libelf/elf_rawfile.c -> .os
[ SHCC] X86/ext/libelf/libelf_allocate.c -> .os
[ SHCC] X86/ext/libelf/elf_version.c -> .os
[ SHCC] X86/ext/libelf/libelf_open.c -> .os
[ SHCC] X86/ext/libelf/elf_data.c -> .os
[ SHCC] X86/ext/libelf/elf_open.c -> .os
[ SHCC] X86/ext/libelf/libelf_xlate.c -> .os
[ SHCC] X86/ext/libelf/gelf_phdr.c -> .os
[ AR] -> X86/ext/libfdt/libfdt.a
[ M4] X86/ext/libelf/elf_types.m4, libelf_fsize.m4 -> libelf_fsize.c
[ RANLIB] -> X86/ext/libfdt/libfdt.a
[ M4] X86/ext/libelf/elf_types.m4, libelf_msize.m4 -> libelf_msize.c
[ SHCXX] X86/ext/iostream3/zfstream.cc -> .os
[ SHCC] X86/ext/libelf/libelf_msize.c -> .os
[ SHCC] X86/ext/libelf/libelf_fsize.c -> .os
[ SHCC] X86/ext/fputils/fp64.c -> .os
[ SHCC] X86/ext/fputils/fp80.c -> .os
[ SHCXX] X86/ext/drampower/src/CommandAnalysis.cc -> .os
[ SHCXX] X86/ext/drampower/src/MemArchitectureSpec.cc -> .os
[ SHCXX] X86/ext/drampower/src/MemCommand.cc -> .os
[ SHCXX] X86/ext/drampower/src/MemPowerSpec.cc -> .os
[ SHCXX] X86/ext/drampower/src/MemTimingSpec.cc -> .os
[ SHCXX] X86/ext/drampower/src/MemoryPowerModel.cc -> .os
[ SHCXX] X86/ext/drampower/src/MemorySpecification.cc -> .os
[ AR] -> X86/ext/fputils/libfputils.a
[ AR] -> X86/ext/libelf/libelf.a
[ RANLIB] -> X86/ext/fputils/libfputils.a
[ SHCXX] X86/ext/drampower/src/Parameter.cc -> .os
[ SHCXX] X86/ext/drampower/src/Parametrisable.cc -> .os
[ RANLIB] -> X86/ext/libelf/libelf.a
[ SHCXX] X86/ext/drampower/src/libdrampower/LibDRAMPower.cc -> .os
[ SHCXX] X86/ext/drampower/src/CAHelpers.cc -> .os
[ SHCXX] X86/ext/drampower/src/CmdHandlers.cc -> .os
[ AR] -> X86/ext/iostream3/libiostream3.a
[ RANLIB] -> X86/ext/iostream3/libiostream3.a
[ SHCXX] X86/ext/drampower/src/MemBankWiseParams.cc -> .os
[ AR] -> X86/ext/drampower/libdrampower.a
[ RANLIB] -> X86/ext/drampower/libdrampower.a
[ CXX] X86/base/date.cc -> .o
[ LINK] -> X86/gem5.opt
scons: done building targets.
*** Summary of Warnings ***
Warning: Deprecated namespaces are not supported by this compiler.
Please make sure to check the mailing list for deprecation
announcements.
```

python3 `which scons` build/ARM/gem5.opt -j7

```
[ SHCC] ARM/ext/libelf/elf_errno.c -> .os
[ SHCC] ARM/ext/libelf/gelf_getclass.c -> .os
[ SHCC] ARM/ext/libelf/elf_flag.c -> .os
[ SHCC] ARM/ext/libelf/elf_getident.c -> .os
[ SHCC] ARM/ext/libelf/elf_version.c -> .os
[ SHCC] ARM/ext/libelf/gelf_cap.c -> .os
[ SHCC] ARM/ext/libelf/libelf_xlate.c -> .os
[ SHCC] ARM/ext/libelf/libelf_open.c -> .os
[ SHCC] ARM/ext/libelf/elf_shstrndx.c -> .os
[ SHCC] ARM/ext/libelf/gelf_rela.c -> .os
[ SHCC] ARM/ext/libelf/elf_next.c -> .os
[ SHCC] ARM/ext/libelf/elf_fill.c -> .os
[ SHCC] ARM/ext/libelf/elf.c -> .os
[ SHCC] ARM/ext/libelf/elf_getbase.c -> .os
[ SHCC] ARM/ext/libelf/libelf.c -> .os
[ SHCC] ARM/ext/libelf/elf_strptr.c -> .os
[ SHCC] ARM/ext/libelf/elf_errmsg.c -> .os
[ SHCC] ARM/ext/libelf/libelf_align.c -> .os
[ SHCC] ARM/ext/libelf/libelf_memory.c -> .os
[ SHCC] ARM/ext/libelf/gelf_symshndx.c -> .os
[ SHCC] ARM/ext/libelf/gelf_rel.c -> .os
[ SHCC] ARM/ext/libelf/elf_memory.c -> .os
[ AR] -> ARM/ext/libfdt/libfdt.a
[ M4] ARM/ext/libelf/elf_types.m4, libelf_msize.m4 -> libelf_msize.c
[ RANLIB] -> ARM/ext/libfdt/libfdt.a
[ SHCXX] ARM/ext/iostream3/zfstream.cc -> .os
[ SHCC] ARM/ext/fputils/fp64.c -> .os
[ SHCC] ARM/ext/libelf/libelf_msize.c -> .os
[ SHCC] ARM/ext/fputils/fp80.c -> .os
[ SHCXX] ARM/ext/drampower/src/CommandAnalysis.cc -> .os
[ SHCXX] ARM/ext/drampower/src/MemArchitectureSpec.cc -> .os
[ SHCXX] ARM/ext/drampower/src/MemCommand.cc -> .os
[ SHCXX] ARM/ext/drampower/src/MemPowerSpec.cc -> .os
[ AR] -> ARM/ext/libelf/libelf.a
[ SHCXX] ARM/ext/drampower/src/MemTimingSpec.cc -> .os
[ AR] -> ARM/ext/fputils/libfputils.a
[ RANLIB] -> ARM/ext/libelf/libelf.a
[ RANLIB] -> ARM/ext/fputils/libfputils.a
[ SHCXX] ARM/ext/drampower/src/MemoryPowerModel.cc -> .os
[ SHCXX] ARM/ext/drampower/src/MemorySpecification.cc -> .os
[ SHCXX] ARM/ext/drampower/src/Parameter.cc -> .os
[ AR] -> ARM/ext/iostream3/libiostream3.a
[ RANLIB] -> ARM/ext/iostream3/libiostream3.a
[ SHCXX] ARM/ext/drampower/src/Parametrisable.cc -> .os
[ SHCXX] ARM/ext/drampower/src/libdrampower/LibDRAMPower.cc -> .os
[ SHCXX] ARM/ext/drampower/src/CAHelpers.cc -> .os
[ SHCXX] ARM/ext/drampower/src/CmdHandlers.cc -> .os
[ SHCXX] ARM/ext/drampower/src/MemBankWiseParams.cc -> .os
[ AR] -> ARM/ext/drampower/libdrampower.a
[ RANLIB] -> ARM/ext/drampower/libdrampower.a
[ CXX] ARM/base/date.cc -> .o
[ LINK] -> ARM/gem5.opt
scons: done building targets.
*** Summary of Warnings ***
Warning: Deprecated namespaces are not supported by this compiler.
Please make sure to check the mailing list for deprecation
announcements.
```


ls -l ~/gem5/build/X86

```
server@t320:/mnt/tmp/gem5/build/X86$ ls -l
total 584276
drwxrwxr-x 11 server server    300 Aug 30 20:22 arch
drwxrwxr-x  7 server server   2440 Aug 30 20:26 base
drwxrwxr-x  2 server server    280 Aug 30 20:22 config
drwxrwxr-x 10 server server   2120 Aug 30 20:22 cpu
drwxrwxr-x  2 server server  15400 Aug 30 20:24 debug
drwxrwxr-x 18 server server   1480 Aug 30 20:17 dev
drwxrwxr-x  2 server server   1900 Aug 30 20:24 enums
drwxrwxr-x 13 server server    260 Aug 30 20:05 ext
drwxrwxr-x  3 server server    120 Aug 30 20:28 gem5.build
-rwxrwxr-x  1 server server 594970344 Aug 30 20:28 gem5.opt
-rwxrwxr-x  1 server server   595832 Aug 30 20:05 gem5py
-rwxrwxr-x  1 server server 2726088 Aug 30 20:08 gem5py_m5
drwxrwxr-x  2 server server    480 Aug 30 20:14 gpu-compute
drwxrwxr-x  4 server server    220 Aug 30 20:17 kern
drwxrwxr-x  3 server server     60 Aug 30 20:05 learning_gem5
drwxrwxr-x  7 server server   4400 Aug 30 20:23 mem
drwxrwxr-x  2 server server   8060 Aug 30 20:23 params
drwxrwxr-x  2 server server    400 Aug 30 20:12 proto
drwxrwxr-x  6 server server    500 Aug 30 20:12 python
lrwxrwxrwx  1 server server     28 Aug 30 20:12 SConscript -> /mnt/tmp/gem5/src/SConscript
drwxrwxr-x  5 server server   4760 Aug 30 20:23 sim
drwxrwxr-x  2 server server    260 Aug 30 20:12 sst
drwxrwxr-x 12 server server    360 Aug 30 20:12 systemc
```

ls -l ~/gem5/build/ARM

```
server@t320:/mnt/tmp/gem5/build/ARM$ ls -l
total 685372
drwxrwxr-x 11 server server    300 Aug 30 20:46 arch
drwxrwxr-x  7 server server   2480 Aug 30 20:53 base
drwxrwxr-x  2 server server    300 Aug 30 20:46 config
drwxrwxr-x 10 server server   2120 Aug 30 20:46 cpu
drwxrwxr-x  2 server server  15760 Aug 30 20:47 debug
drwxrwxr-x 18 server server   1480 Aug 30 20:39 dev
drwxrwxr-x  2 server server   1900 Aug 30 20:47 enums
drwxrwxr-x 13 server server    260 Aug 30 20:30 ext
drwxrwxr-x  3 server server    120 Aug 30 20:55 gem5.build
-rwxrwxr-x  1 server server 698453600 Aug 30 20:55 gem5.opt
-rwxrwxr-x  1 server server  595832 Aug 30 20:30 gem5py
-rwxrwxr-x  1 server server 2768376 Aug 30 20:31 gem5py_m5
drwxrwxr-x  2 server server    480 Aug 30 20:36 gpu-compute
drwxrwxr-x  4 server server    220 Aug 30 20:39 kern
drwxrwxr-x  3 server server     60 Aug 30 20:30 learning_gem5
drwxrwxr-x  7 server server   4380 Aug 30 20:35 mem
drwxrwxr-x  2 server server   8480 Aug 30 20:47 params
drwxrwxr-x  2 server server    400 Aug 30 20:34 proto
drwxrwxr-x  6 server server    500 Aug 30 20:34 python
lrwxrwxrwx  1 server server     28 Aug 30 20:30 SConscript -> /mnt/tmp/gem5/src/SConscript
drwxrwxr-x  5 server server   4760 Aug 30 20:47 sim
drwxrwxr-x  2 server server    260 Aug 30 20:32 sst
drwxrwxr-x 12 server server    360 Aug 30 20:30 systemc
```

Does gem5 support the RISC-V CPU?

Yes gem5 does support the RISC-V cpu. Referencing the build guide on the gem5 website [[gem5: Building gem5](#)] it can be seen that the following ISA's are supported. RISC-V can be found in the list of supported ISA's. Also based on the documentation the required cli to compile the model would be **"scons build/RISCV/gem5.opt -j7"**.

The valid ISAs are:

- ARM
- NULL
- MIPS
- POWER
- RISCV
- SPARC
- X86