Lab 3

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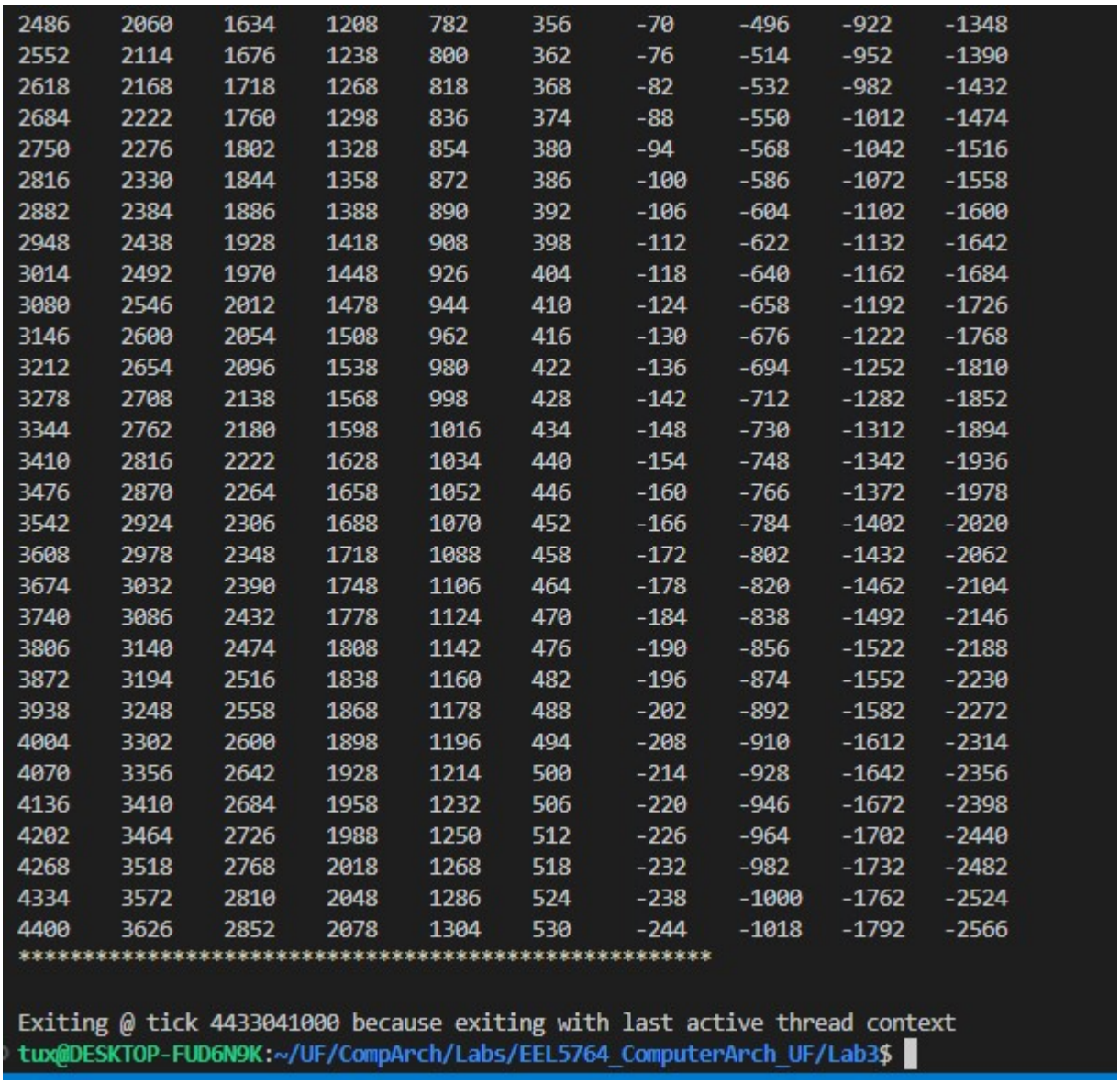
```
tux@DESKTOP-FUD6N9K:~/UF/CompArch/Labs/EEL5764_ComputerArch_UF/Lab3$ gem5_x86 two_level.py
gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 22.0.0.2
gem5 compiled Sep 12 2022 17:43:41
gem5 started Sep 17 2022 12:55:34
gem5 executing on DESKTOP-FUD6N9K, pid 4102
command line: /home/tux/UF/CompArch/gem5/build/X86/gem5.opt two_level.py

Global frequency set at 1000000000000 ticks per second
warn: No dot file generated. Please install pydot to generate the dot file and pdf.
build/X86/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
0: system.remote_gdb: listening for remote gdb on port 7000
Beginning simulation!
build/X86/sim/simulate.cc:194: info: Entering event queue @ 0.  Starting simulation...
Hello world!
Exiting @ tick 55068000 because exiting with last active thread context
```

Part A


2486 2060 1634 1208 782 356 -70 -496 -922 -1348
2552 2114 1676 1238 800 362 -76 -514 -952 -1390
2618 2168 1718 1268 818 368 -82 -532 -982 -1432
2684 2222 1760 1298 836 374 -88 -550 -1012 -1474
2750 2276 1802 1328 854 380 -94 -568 -1042 -1516
2816 2330 1844 1358 872 386 -100 -586 -1072 -1558
2882 2384 1886 1388 890 392 -106 -604 -1102 -1600
2948 2438 1928 1418 908 398 -112 -622 -1132 -1642
3014 2492 1970 1448 926 404 -118 -640 -1162 -1684
3080 2546 2012 1478 944 410 -124 -658 -1192 -1726
3146 2600 2054 1508 962 416 -130 -676 -1222 -1768
3212 2654 2096 1538 980 422 -136 -694 -1252 -1810
3278 2708 2138 1568 998 428 -142 -712 -1282 -1852
3344 2762 2180 1598 1016 434 -148 -730 -1312 -1894
3410 2816 2222 1628 1034 440 -154 -748 -1342 -1936
3476 2870 2264 1658 1052 446 -160 -766 -1372 -1978
3542 2924 2306 1688 1070 452 -166 -784 -1402 -2020
3608 2978 2348 1718 1088 458 -172 -802 -1432 -2062
3674 3032 2390 1748 1106 464 -178 -820 -1462 -2104
3740 3086 2432 1778 1124 470 -184 -838 -1492 -2146
3806 3140 2474 1808 1142 476 -190 -856 -1522 -2188
3872 3194 2516 1838 1160 482 -196 -874 -1552 -2230
3938 3248 2558 1868 1178 488 -202 -892 -1582 -2272
4004 3302 2600 1898 1196 494 -208 -910 -1612 -2314
4070 3356 2642 1928 1214 500 -214 -928 -1642 -2356
4136 3410 2684 1958 1232 506 -220 -946 -1672 -2398
4202 3464 2726 1988 1250 512 -226 -964 -1702 -2440
4268 3518 2768 2018 1268 518 -232 -982 -1732 -2482
4334 3572 2810 2048 1286 524 -238 -1000 -1762 -2524
4400 3626 2852 2078 1304 530 -244 -1018 -1792 -2566
****
Exiting @ tick 4433041000 because exiting with last active thread context
tux@DESKTOP-FUD6N9K:~/UF/CompArch/Labs/EEL5764_ComputerArch_UF/Lab3$

Part B1

```
2486    2060    1634    1208    782     356     -70     -496    -922    -1348
2552    2114    1676    1238    800     362     -76     -514    -952    -1390
2618    2168    1718    1268    818     368     -82     -532    -982    -1432
2684    2222    1760    1298    836     374     -88     -550    -1012   -1474
2750    2276    1802    1328    854     380     -94     -568    -1042   -1516
2816    2330    1844    1358    872     386     -100    -586    -1072   -1558
2882    2384    1886    1388    890     392     -106    -604    -1102   -1600
2948    2438    1928    1418    908     398     -112    -622    -1132   -1642
3014    2492    1970    1448    926     404     -118    -640    -1162   -1684
3080    2546    2012    1478    944     410     -124    -658    -1192   -1726
3146    2600    2054    1508    962     416     -130    -676    -1222   -1768
3212    2654    2096    1538    980     422     -136    -694    -1252   -1810
3278    2708    2138    1568    998     428     -142    -712    -1282   -1852
3344    2762    2180    1598    1016    434     -148    -730    -1312   -1894
3410    2816    2222    1628    1034    440     -154    -748    -1342   -1936
3476    2870    2264    1658    1052    446     -160    -766    -1372   -1978
3542    2924    2306    1688    1070    452     -166    -784    -1402   -2020
3608    2978    2348    1718    1088    458     -172    -802    -1432   -2062
3674    3032    2390    1748    1106    464     -178    -820    -1462   -2104
3740    3086    2432    1778    1124    470     -184    -838    -1492   -2146
3806    3140    2474    1808    1142    476     -190    -856    -1522   -2188
3872    3194    2516    1838    1160    482     -196    -874    -1552   -2230
3938    3248    2558    1868    1178    488     -202    -892    -1582   -2272
4004    3302    2600    1898    1196    494     -208    -910    -1612   -2314
4070    3356    2642    1928    1214    500     -214    -928    -1642   -2356
4136    3410    2684    1958    1232    506     -220    -946    -1672   -2398
4202    3464    2726    1988    1250    512     -226    -964    -1702   -2440
4268    3518    2768    2018    1268    518     -232    -982    -1732   -2482
4334    3572    2810    2048    1286    524     -238    -1000   -1762   -2524
4400    3626    2852    2078    1304    530     -244    -1018   -1792   -2566
**********

Exiting @ tick 104103870000 because exiting with last active thread context
tux@DESKTOP-FUD6N9K:~/UF/CompArch/Labs/EEL5764_ComputerArch_UF/Lab3$
```

Part B2

The caching makes a huge difference in performance for this C file, providing over 2 magnitudes in reduction of ticks to completion.

Note: 104103870000 vs 4433041000 ticks

```
Exiting @ tick 4433041000 because exiting with last active thread context
```

Part B3: Value = 1

```
Exiting @ tick 4433041000 because exiting with last active thread context
```

Part B3: Value = 2

```
Exiting @ tick 8311533000 because exiting with last active thread context
```

Part B3: Value = 4

```
Exiting @ tick 16068397000 because exiting with last active thread context
```

Part B3: Value = 8

Changing the data latency of the L1 cache seemed to have a significant impact on tick count. The default value of the latency, 2 has over double the performance figures of 4 and four times that of 8. This shows that the data latency has a linear effect on the speed of the L1 cache. One oddity that should be noted is that there was no increase in speed between a data rate of 1 and 2 for the L1 cache. This lack of a difference has not been investigated in detail but could demonstrate that the data rate of the CPU is bottlenecked by a system or component other than the L1 cache. This could explain why there was no increase in the performance.

```
[system.cpu.dcache.replacement_policy]
type=LRURP
eventq_index=0

[system.cpu.icache.replacement_policy]
type=LRURP
eventq_index=0

[system.l2cache.replacement_policy]
type=LRURP
eventq_index=0
```

replacement_policy

```
[system.cpu.dcache.tags]
type=BaseSetAssoc
children=indexing_policy power_state
assoc=2
block_size=64
clk_domain=system.clk_domain
entry_size=64
eventq_index=0
indexing_policy=system.cpu.dcache.tags.indexing_policy
power_model=
power_state=system.cpu.dcache.tags.power_state
replacement_policy=system.cpu.dcache.replacement_policy
sequential_access=false
size=65536
system=system
tag_latency=2
warmup_percentage=0

[system.cpu.icache.tags]
type=BaseSetAssoc
children=indexing_policy power_state
assoc=2
block_size=64
clk_domain=system.clk_domain
entry_size=64
eventq_index=0
indexing_policy=system.cpu.icache.tags.indexing_policy
```

```
power_model=
power_state=system.cpu.icache.tags.power_state
replacement_policy=system.cpu.icache.replacement_policy
sequential_access=false
size=16384
system=system
tag_latency=2
warmup_percentage=0

[system.l2cache.tags]
type=BaseSetAssoc
children=indexing_policy power_state
assoc=8
block_size=64
clk_domain=system.clk_domain
entry_size=64
eventq_index=0
indexing_policy=system.l2cache.tags.indexing_policy
power_model=
power_state=system.l2cache.tags.power_state
replacement_policy=system.l2cache.replacement_policy
sequential_access=false
size=262144
system=system
tag_latency=20
warmup_percentage=0
```

tags

```
[system.cpu.dcache.tags.indexing_policy]
type=SetAssociative
assoc=2
entry_size=64
eventq_index=0
size=65536

[system.cpu.icache.tags.indexing_policy]
type=SetAssociative
assoc=2
entry_size=64
eventq_index=0
size=16384

[system.l2cache.tags.indexing_policy]
type=SetAssociative
```

```
assoc=8
entry_size=64
eventq_index=0
size=262144
```

tags.indexing_policy