

Lab 4

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```
tux@DESKTOP-FUD6N9K:~/UF/CompArch/Labs/EEL5764_ComputerArch_UF/Lab4$ gem5_x86 two_level.py --binary hello --l2_size='1MB' --l1d_size='128kB' --l1i_size='128kB'
gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

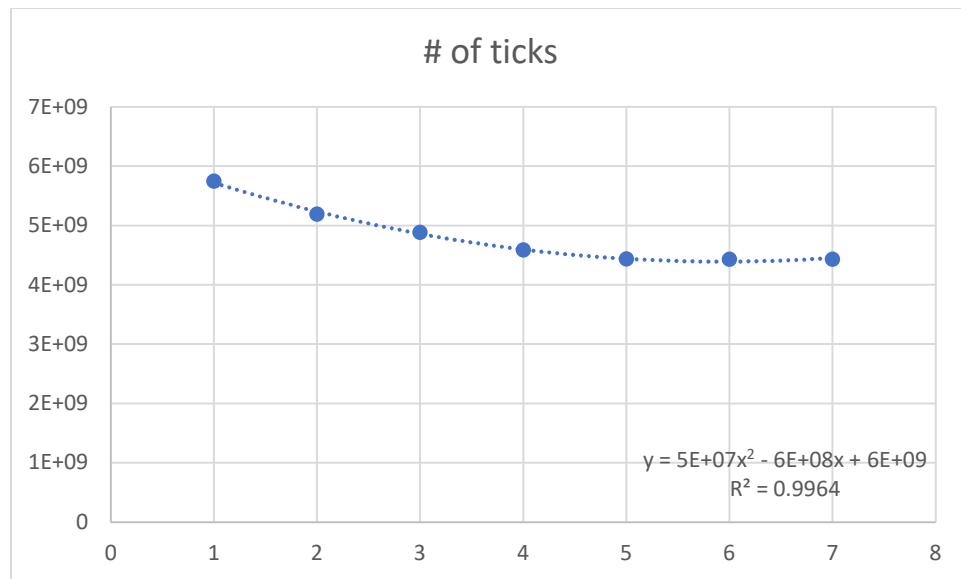
gem5 version 22.0.0.2
gem5 compiled Sep 12 2022 17:43:41
gem5 started Oct  3 2022 21:02:24
gem5 executing on DESKTOP-FUD6N9K, pid 3282
command line: /home/tux/UF/CompArch/gem5/build/X86/gem5.opt two_level.py --binary hello --l2_size=1MB --l1d_size=128kB --l1i_size=128kB

Global frequency set at 100000000000 ticks per second
warn: No dot file generated. Please install pydot to generate the dot file and pdf.
build/X86/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
0: system.remote_gdb: listening for remote gdb on port 7000
Beginning simulation!
build/X86/sim/simulate.cc:194: info: Entering event queue @ 0.  Starting simulation...
Hello world!
Exiting @ tick 54885000 because exiting with last active thread context
```

Part A: Screenshot of added capabilities

L1Cache.size	# of ticks
1kB	5747481000
2kB	5191374000
4kB	4883423000
8kB	4586946000
16kB	4439466000
32kB	4433041000
64kB	4433041000

Part B Table: L1Cache Size vs # of Ticks



Part B Graph: L1Cache Size vs # of Ticks

```
3476    2870    2264    1658    1052    446     -160    -766    -1372   -1978
3542    2924    2306    1688    1070    452     -166    -784    -1402   -2020
3608    2978    2348    1718    1088    458     -172    -802    -1432   -2062
3674    3032    2390    1748    1106    464     -178    -820    -1462   -2104
3740    3086    2432    1778    1124    470     -184    -838    -1492   -2146
3806    3140    2474    1808    1142    476     -190    -856    -1522   -2188
3872    3194    2516    1838    1160    482     -196    -874    -1552   -2230
3938    3248    2558    1868    1178    488     -202    -892    -1582   -2272
4004    3302    2600    1898    1196    494     -208    -910    -1612   -2314
4070    3356    2642    1928    1214    500     -214    -928    -1642   -2356
4136    3410    2684    1958    1232    506     -220    -946    -1672   -2398
4202    3464    2726    1988    1250    512     -226    -964    -1702   -2440
4268    3518    2768    2018    1268    518     -232    -982    -1732   -2482
4334    3572    2810    2048    1286    524     -238    -1000   -1762   -2524
4400    3626    2852    2078    1304    530     -244    -1018   -1792   -2566
*****

Exiting @ tick 5892082000 because exiting with last active thread context
tux@DESKTOP-FUD6N9K:~/UF/CompArch/Labs/EEL5764 ComputerArch UF/Lab4$
```

Part C: Screenshot

Row #	l1i_assoc =	1	2	4	8
1	Exit tick # (from last screen)	4592817000	4433041000	4345860000	4334274000
2	# number of overall hits (Count)	1631678	1638313	1641937	1642429
3	# number of overall misses (Count)	11321	4686	1062	570
4	# number of overall miss ticks (Tick)	337063000	164119000	69607000	57013000
5	# average overall miss latency ((Tick/Count))	29773.2532	35023.2608	65543.3145	100022.807
6	# number of overall (read+write) accesses (Count)	1642999	1642999	1642999	1642999
7	# miss rate for overall accesses (Ratio)	0.00689	0.002852	0.000646	0.000347
8	# number of replacements (Count)	11091	4437	808	314

Part D: Experimental Findings

Question

Q1: Overall the performance increased each time the associativity was raised. The rate of increase in performance decreased as the associativity was increased.

Q2: Direct mapped cache

Q3: Row 5 = Row 4 / Row 3

Q4: Row 7 = Row 3 / Row 6

Q5: Rows 1, 2, 3, 4, 7, 8