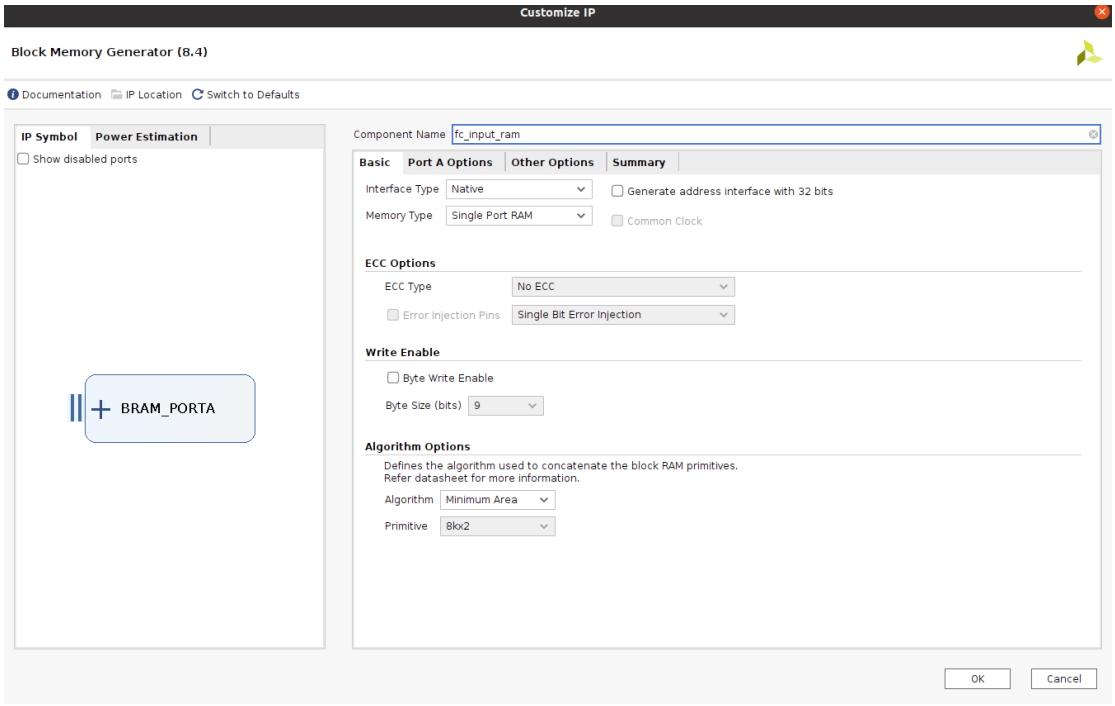
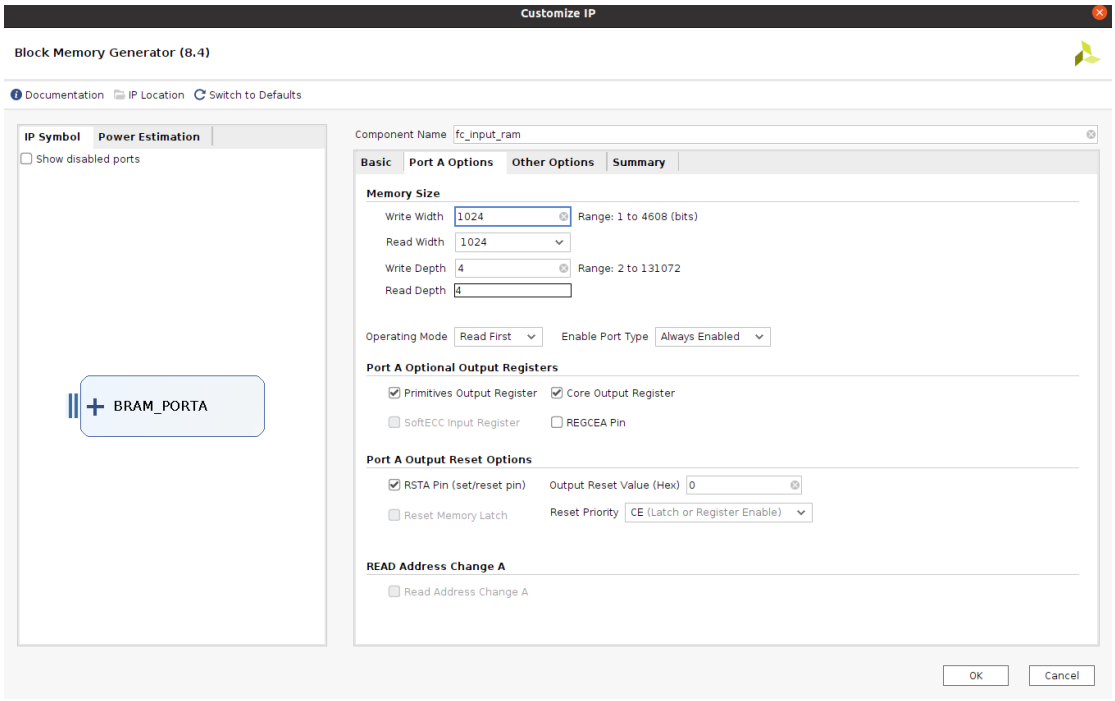
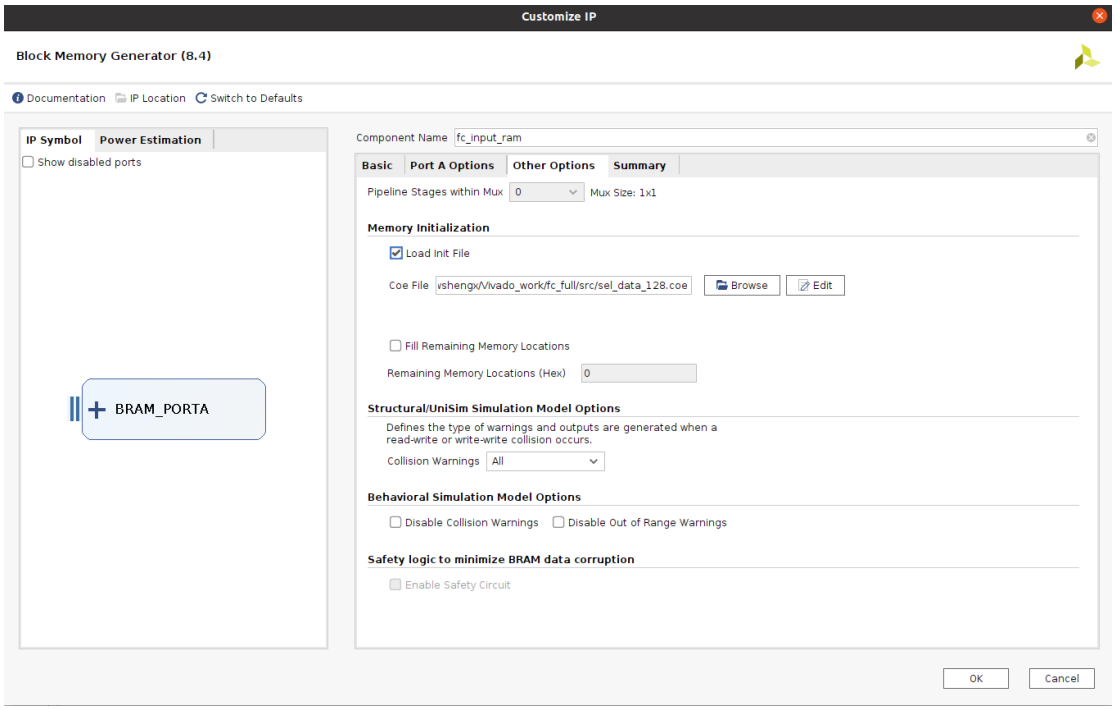
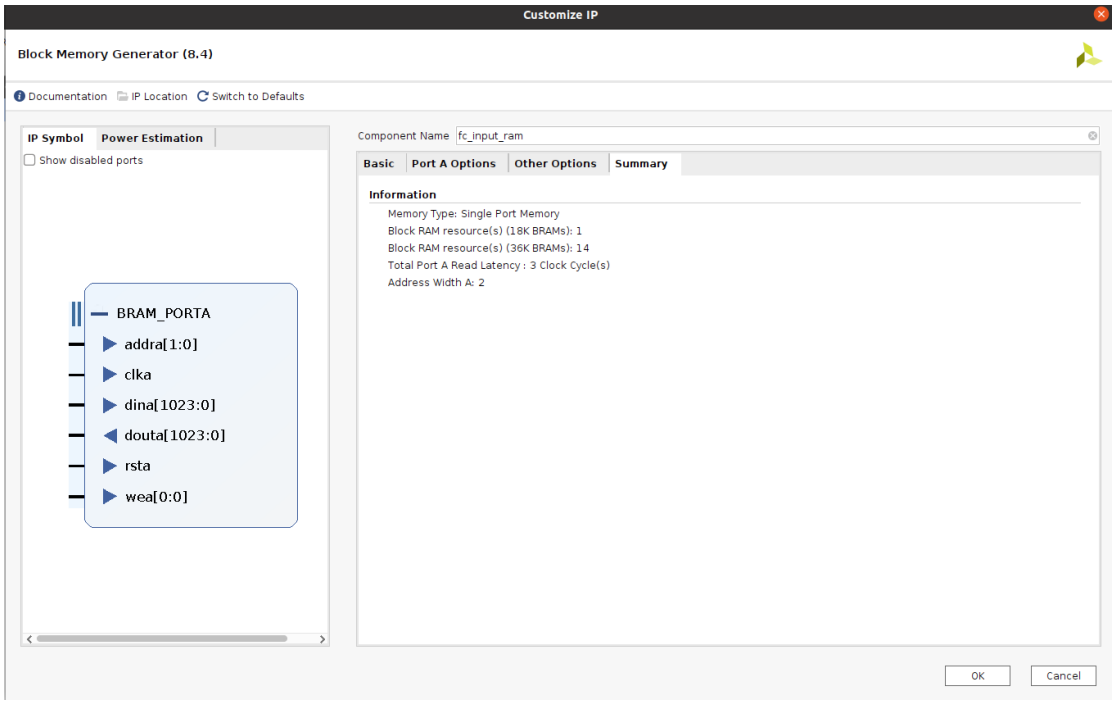
BRAM 设置指南（示例）

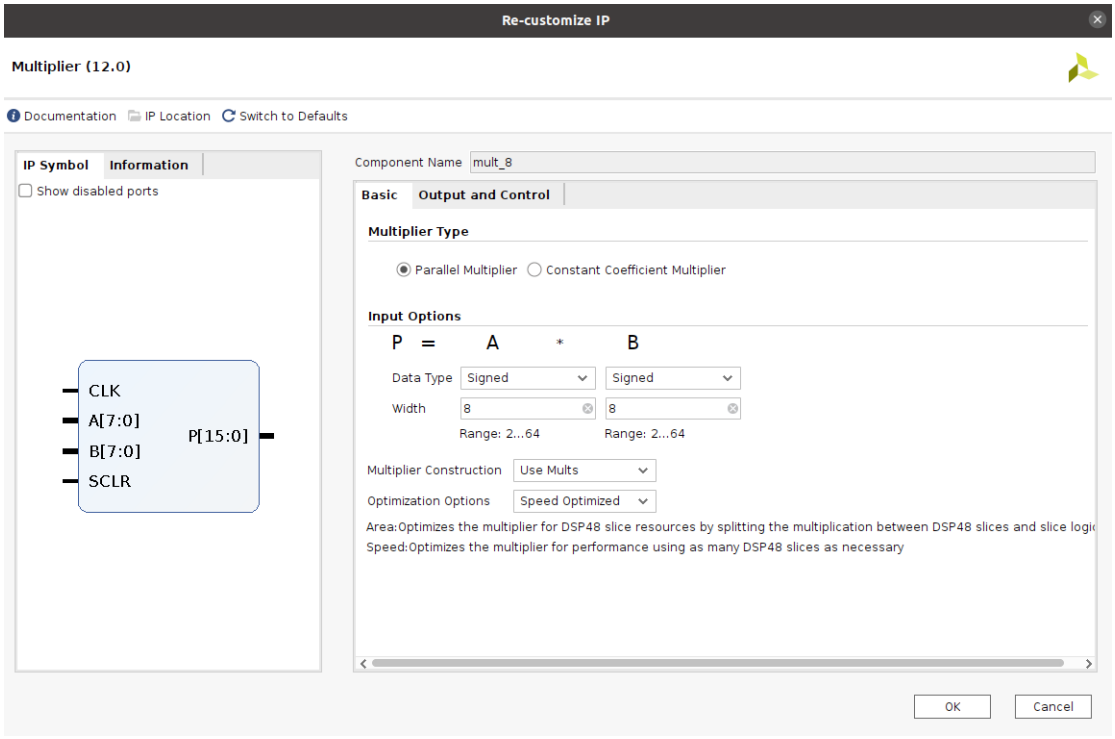

Customize IP
Block Memory Generator (8.4)
Documentation
IP Location
Switch to Defaults
IP Symbol
Power Estimation
Show disabled ports
BRAM_PORTA
Component Name
fc_input_ram
Basic
Port A Options
Other Options
Summary
Interface Type
Native
Generate address interface with 32 bits
Memory Type
Single Port RAM
Common Clock
ECC Options
ECC Type
No ECC
Error Injection Pins
Single Bit Error Injection
Write Enable
Byte Write Enable
Byte Size (bits)
9
Algorithm Options
Defines the algorithm used to concatenate the block RAM primitives.
Refer datasheet for more information.
Algorithm
Minimum Area
Primitive
8kx2
OK
Cancel

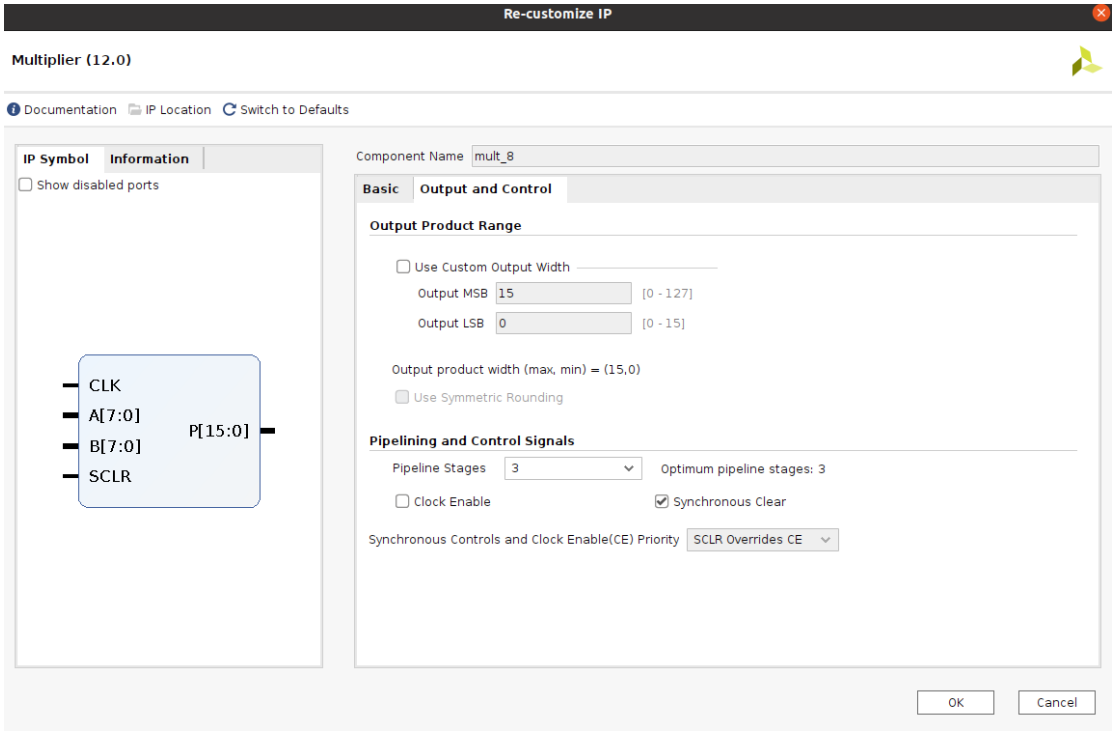

Customize IP
Block Memory Generator (8.4)
Documentation
IP Location
Switch to Defaults
IP Symbol
Power Estimation
Show disabled ports
BRAM_PORTA
Component Name
fc_input_ram
Basic
Port A Options
Other Options
Summary
Memory Size
Write Width
1024
Range: 1 to 4608 (bits)
Read Width
1024
Write Depth
4
Range: 2 to 131072
Read Depth
4
Operating Mode
Read First
Enable Port Type
Always Enabled
Port A Optional Output Registers
Primitives Output Register
Core Output Register
SoftECC Input Register
REGCEA Pin
Port A Output Reset Options
RSTA Pin (set/reset pin)
Output Reset Value (Hex)
0
Reset Memory Latch
Reset Priority
CE (Latch or Register Enable)
READ Address Change A
Read Address Change A
OK
Cancel


Customize IP
Block Memory Generator (8.4)
Documentation
IP Location
Switch to Defaults
IP Symbol
Power Estimation
Show disabled ports
BRAM_PORTA
Component Name
fc_input_ram
Basic
Port A Options
Other Options
Summary
Pipeline Stages within Mux
0
Mux Size: 1x1
Memory Initialization
Load Init File
Coe File
vshengx/Vivado_work/fc_full/src/sel_data_128.coe
Browse
Edit
Fill Remaining Memory Locations
Remaining Memory Locations (Hex)
0
Structural/UniSim Simulation Model Options
Defines the type of warnings and outputs are generated when a read-write or write-write collision occurs.
Collision Warnings
All
Behavioral Simulation Model Options
Disable Collision Warnings
Disable Out of Range Warnings
Safety logic to minimize BRAM data corruption
Enable Safety Circuit
OK
Cancel


Customize IP
Block Memory Generator (8.4)
Documentation
IP Location
Switch to Defaults
IP Symbol
Power Estimation
Show disabled ports
BRAM_PORTA
addra[1:0]
clka
dina[1023:0]
douta[1023:0]
rsta
wea[0:0]
Component Name
fc_input_ram
Basic
Port A Options
Other Options
Summary
Information
Memory Type: Single Port Memory
Block RAM resource(s) (18K BRAMs): 1
Block RAM resource(s) (36K BRAMs): 14
Total Port A Read Latency : 3 Clock Cycle(s)
Address Width A: 2
OK
Cancel

乘法器设置指南


Re-customize IP
Multiplier (12.0)
Documentation
IP Location
Switch to Defaults
IP Symbol
Information
Show disabled ports
CLK
A[7:0]
B[7:0]
SCLR
P[15:0]
Component Name
mult_8
Basic
Output and Control
Multiplier Type
Parallel Multiplier
Constant Coefficient Multiplier
Input Options
P = A * B
Data Type
Signed
Signed
Width
8
8
Range: 2...64
Range: 2...64
Multiplier Construction
Use Mults
Optimization Options
Speed Optimized
Area:Optimizes the multiplier for DSP48 slice resources by splitting the multiplication between DSP48 slices and slice logi
Speed:Optimizes the multiplier for performance using as many DSP48 slices as necessary
OK
Cancel


Re-customize IP
Multiplier (12.0)
Documentation
IP Location
Switch to Defaults
IP Symbol
Information
Show disabled ports
CLK
A[7:0]
B[7:0]
SCLR
P[15:0]
Component Name
mult_8
Basic
Output and Control
Output Product Range
Use Custom Output Width
Output MSB
15
[0 - 127]
Output LSB
0
[0 - 15]
Output product width (max, min) = (15,0)
Use Symmetric Rounding
Pipelining and Control Signals
Pipeline Stages
3
Optimum pipeline stages: 3
Clock Enable
Synchronous Clear
Synchronous Controls and Clock Enable(CE) Priority
SCLR Overrides CE
OK
Cancel