

Real-Time Quality Index Estimation for Redundant Sampled Values Streams in Digital Substations

Everton Matheus Oriente

**Dissertation submitted in partial fulfilment of the requirements for the
Master's degree in Critical Computing Systems Engineering**

Supervisor: António Barros

Porto, September 26, 2024

Statement of Integrity

I hereby declare having conducted this academic work with integrity. I have not plagiarised or applied any form of undue use of information or falsification of results along the process leading to its elaboration.

I declare that the work presented in this document is original and my own, and has not previously been used for any other purpose.

I further declare that I have fully followed the Code of Good Practices and Conduct of the Polytechnic Institute of Porto.

ISEP, Porto, September 26, 2024

Abstract

Protection devices are essential elements in the electric power grid, as they safeguard equipment and ensure the stability and reliability of the network by detecting faults and preventing damage through timely isolation of affected areas. With technological advancements, electromechanical protection relays have evolved into Intelligent Electronic Devices (IEDs), essentially protection relays with built-in communication capabilities. These modern relays not only protect equipment but also exchange critical information with other devices.

However, the variety of events and data exchanged between power grid components is substantial. In this respect, communication protocols present both advantages and challenges. On one hand, they enable the signalling of diverse events and the transmission of multiple pieces of information over a single medium. On the other hand, a protocol is only effective if all components within the system comply with it.

The introduction of the IEC-61850 standard has established a unified communication across the energy sector, promotes interoperability between manufacturers, offering significant advantages over other standards. Real-time data exchange is facilitated by specific protocols within the IEC 61850 framework, which specifically address the communication requirements of IEDs, ensuring enhanced data quality and availability.

As IEDs play a crucial role in substations, with many of their functions being both critical and time-sensitive, any developments incorporated into these devices can significantly impact the entire system. An IED analyses the stream of Sampled Values (SVs) sent by a Merging Unit to detect faults and implement protective measures. The Merging Unit sends SVs over two independent channels: the primary and the secondary (redundant) channels. When the primary channel fails, the secondary channel takes over, ensuring the information that the primary channel could not transmit is conveyed. As such, the current decision-making process for switching channels is based solely on the occurrence of a total channel failure.

This thesis aims to enhance IED functionality by adding intelligence to this channel selection method. It proposes ways to evaluate, quantify, and qualify the received information to determine the most reliable signal source, whether from Channel 1 (primary) or Channel 2 (secondary). This approach ensures that protection relays receive better information, enabling protection algorithms to act correctly and promptly within their operating parameters.

Keywords: IEC61850-9-2 Sampled Values, Intelligent Electronic Devices (IED) and Protection Relays

Resumo

Relés de proteção são elementos essenciais na rede elétrica, pois protegem os equipamentos e garantem a estabilidade e confiabilidade da rede, detectando falhas e prevenindo danos através da isolação oportuna das áreas afetadas.

Com os avanços tecnológicos, os relés de proteção eletromecânicos evoluíram para Dispositivos Eletrônicos Inteligentes (IEDs), essencialmente relés de proteção com capacidades de comunicação integradas. Esses relés modernos não apenas protegem os equipamentos, mas também trocam informações críticas com outros dispositivos.

No entanto, a variedade de eventos e dados trocados entre os componentes da rede elétrica é substancial. Nesse aspecto, os protocolos de comunicação apresentam tanto vantagens quanto desafios. Por um lado, eles permitem a sinalização de diversos eventos e a transmissão de múltiplas informações através de um único meio. Por outro lado, um protocolo só é eficaz se todos os componentes do sistema o seguirem.

A introdução da norma IEC-61850 estabeleceu uma comunicação unificada no setor de energia, promovendo a interoperabilidade entre fabricantes e oferecendo vantagens significativas em relação a outros padrões. A troca de dados em tempo real é facilitada por protocolos específicos dentro da estrutura da IEC 61850, que abordam especificamente os requisitos de comunicação dos IEDs, garantindo melhor qualidade e disponibilidade dos dados.

Como os IEDs desempenham um papel crucial nas subestações, com muitas de suas funções sendo críticas e sensíveis ao tempo, qualquer desenvolvimento incorporado a esses dispositivos pode impactar significativamente todo o sistema. Um IED analisa o fluxo de Valores Amostrados (SVs) enviados por uma Unidade de Mesclagem para detectar falhas e implementar medidas de proteção. A Unidade de Mesclagem envia SVs por dois canais independentes: o canal primário e o canal secundário (redundante). Quando o canal primário falha, o canal secundário assume, garantindo que a informação que o canal primário não pôde transmitir seja transmitida.

Assim, o processo de tomada de decisão atual para a troca de canais baseia-se unicamente na ocorrência de uma falha total do canal.

Esta tese tem como objetivo aprimorar a funcionalidade dos IEDs, adicionando inteligência a esse método de seleção de canal. Propõe maneiras de avaliar, quantificar e qualificar a informação recebida para determinar a fonte de sinal mais confiável, seja do Canal 1 (primário) ou do Canal 2 (secundário). Essa abordagem garante que os relés de proteção recebam informações de melhor qualidade, permitindo que os algoritmos de proteção atuem de forma correta e rápida dentro dos seus parâmetros de operação.

Acknowledgement

I would like to express my deepest gratitude to my wife, Graziela Preisegalavicius, for her unwavering support and encouragement throughout this journey. Your patience, love, and understanding have been my greatest source of strength.

To my son, Theo Preisegalavicius Oriente, thank you for bringing endless joy into my life and giving me the motivation to push forward. Your smiles and laughter have been my driving force.

I am also profoundly grateful to my parents, Irani Matheus Oriente and Hamilton Angelo Oriente, for their lifelong support and guidance. Your belief in me has been the foundation upon which I have built my achievements.

Finally, I would like to extend my sincere thanks to my supervisor, Antonio Barros, for his insightful guidance and encouragement throughout the development of this thesis.

Contents

List of Figures	xv
List of Source Code	xvii
List of Abbreviations	xix
1 Introduction	1
1.1 Overview	1
1.2 Digital Substation	2
1.3 Research Motivation and Context	4
1.4 Research Objectives	5
1.5 Research Contributions	5
1.6 Thesis Structure	5
2 State of the Art	7
2.1 Introduction to Substation Automation System	7
2.2 Backyard System	8
2.2.1 Circuit Breakers	8
2.2.2 Switches	9
2.2.3 Voltage Transformers	9
2.2.4 Current Transformers	9
2.3 Intelligent Electronic Devices	9
2.3.1 Protection Algorithm System	10
2.3.2 Control System	10
2.3.3 Measurement	10
2.3.4 Monitoring	11
2.3.5 Communication Protocols	11
2.4 Overview of IEC 61850	12
2.4.1 IEC 61850-1 - Introduction and Overview	12
2.4.2 IEC 61850-2 - Glossary	13
2.4.3 IEC 61850-3 - General Requirement	13
2.4.4 IEC 61850-4 - System and Project Management	13
2.4.5 IEC 61850-5 - Communication Requirements for Functions and Device Models	13
2.4.6 IEC 61850-6 - Configuration Language for Communication in Elec- trical Substations	13
2.4.7 IEC 61850-7 - Basic Communication Structure	13
2.4.8 IEC 61850-8 - Specific Communication Service Mapping	13
2.4.9 IEC 61850-9 - Specific Communication Service Mapping	14
2.4.10 IEC 61850-10 - Conformance Testing	14
2.5 IEC 61850-9-2 Sampled Values (SV)	14

2.5.1	IEC 60044-8/2002	14
2.5.2	IEC 61850-9-1/2003	15
2.5.3	IEC 61850-9-2(Ed1)/2004	15
2.5.4	IEC 61850-9-2 Ed2/2011	16
2.5.5	IEC 61869-9/2016	17
2.5.6	IEC 61850-9-2 Ed2.1/2020	17
3	Insights	19
3.1	Identification of the research gap	19
3.1.1	Existing Literature and Related Research	19
3.1.2	Identification of the Gap	19
3.1.3	Importance of Addressing the Gap	20
3.1.4	Conclusion of the research gap	20
3.2	Architecture of the Algorithm	20
4	Architecture	23
4.1	Overview	23
4.2	Setup of the Algorithm	23
4.2.1	Hardware	24
4.2.2	Software	25
4.2.3	Cargo	26
4.2.4	Crates	27
4.2.5	Tokio Crate	28
4.2.6	Serde Crate	29
4.2.7	Crc32Fast Crate	29
4.2.8	Pnet Crate	30
4.2.9	Log Crate	30
4.2.10	Env_Logger Crate	31
4.2.11	Chrono	31
4.3	Algorithm for Selecting the Best Sampled Values	31
4.3.1	Results	34
5	Implementation	37
5.1	Structure of Sampled Values	37
5.2	Development of a Publisher of IEC 61850-9-2-SV	38
5.2.1	Structuring the Data: Defining Rust Structs	39
5.2.2	Implementing the Core Functions	40
5.2.3	Simulating an Electrical Grid Signal	40
5.2.4	Introducing Invalid Samples for Testing	41
5.2.5	Finalizing the Publisher	41
5.3	Development of a Subscriber of IEC 61850-9-2-SV	42
5.3.1	Structs Reused in the Subscriber	42
5.3.2	Implementation of Data Reception and Logging	42
5.3.3	Error Handling and Invalid Data Processing	42
5.3.4	Finalizing the Subscriber	43
5.4	Development of the Algorithm	43
6	Tests and Evaluation	47
6.1	Test of Publisher of IEC 61850-9-2-SV	47
6.2	Test of Subscriber of IEC 61850-9-2-SV	50

6.3	Test of the Algorithm	52
7	Conclusion	105
7.1	Limitations	105
7.2	Conclusions and Final Considerations	105
7.3	Future Work	106
7.3.1	Add an ADC to acquire values of Voltage Transformer and Current Transformer	106
7.3.2	Add a PTP server regarding the IEC61850-9-3-PTP	107
7.3.3	Implement a more secure Sampled Value (SV) packet in modern substations	108
	Bibliography	111

List of Figures

1.1	Electricity Generation, Transmission, and Distribution Pathway (Image credits: U.S. Energy Information Administration)	2
2.1	Design of Substation Automation Systems(Image credits: KTH, "Lecture 5: Substation Automation Systems")	8
2.2	Concept of the Merging Unit.	15
2.3	Frequency regarding Sampled Values.	17
2.4	Evolution of IEC 61850-9-2	18
3.1	Simple Single Line Diagram (SLD) of Electrical Substation with SV's. (Credits: Efacec Energia, Máquinas e Equipamentos Eléctricos, S.A.)	21
4.1	How the implementation was designed to work.	32
4.2	How is constructed a Sampled Values Packet following the standard IEC 61850-9-2 (Image credits: Typhoon HIL)	33
5.1	Sampled Value packets fields. (Image credits: MDPI)	38
5.2	Sampled Value packets fields. (Image credits: UCA International)	38
5.3	State Machine of Decision Make.	44
5.4	How is connected the two simulators of SV's to exchange the information.	45
6.1	Wireshark view of the SV packets.	48
6.2	SV packet with sample counter with value 0.	48
6.3	SV packet with sample counter with value 1.	49
6.4	SV packet with sample counter with value 2.	49
6.5	SV packet with bad quality sample counter with value 114.	50
6.6	SV packet with bad quality sample counter with value 115.	50
6.7	SV packet at subscriber side	51
6.8	Information provided by Log of publisher and subscriber, the same packet in both equipment	52

List of Source Code

5.1	Structs added	39
5.2	How to implement an impl for the struct	40
5.3	How to calculate the value of the SV's	41
5.4	How to calculate the value of the SV's	41
5.5	EthernetFrame struct.	42
5.6	State Machine struct.	44

List of Abbreviations

ACSI	A bstract C ommunication S ervice I nterface
ASCII	A merican S tandard C ode for I nformation I nterchange
CB	C ircuit B reaker
CT	C urrent T ransformer
GOOSE	G eneric O bject O riented S ubstation E vents
IEC	I nternational E lectrotechnical C ommission
IED	I ntelligent E lectronic D evelopments
IEEE	I nstitute of E lectrical and E lectronic E ngineers
IRIG-B	I nter- R ange I nstrumentation G roup
IP	I nternet P rotocol
LAN	L ocal A rea N etwork
LD	L ogical D evice
LN	L ogical N ode
MMS	M anufacturing M essage S pecification
OS	O perating S ystem
PTP	P recision T ime P rotocol
RTOS	R ead-Time O perating S ystem
SAS	S ubstation A utomation S ystems
SCADA	S upervisory C ontrol and D ata A cquisition
SCL	S ubstation C onfiguration description L anguage
SCSM	S pecific C ommunication S ervice M apping
SW	D isconnector
SV	S ampled- V alues
TCP	T ransmission C ontrol P rotocol
UDP	U ser D atagram P rotocol
VT	V oltage T ransformer

Chapter 1

Introduction

1.1 Overview

Since the discovery of electricity, humanity has harnessed electrical energy for a multitude of purposes. As the demand for electricity grew, encompassing applications like heating, ventilation, and lighting, the need to generate more electrical power became paramount to accommodate the evolving array of functionalities that emerged over time.

Consequently, diverse power plants were established to meet the increasing demand. These included thermal power plants, hydroelectric plants, nuclear facilities, geothermal installations, combined-cycle plants, and others. In contemporary times, we have witnessed the advent of novel energy sources, such as wind, solar, tidal, biomass, and green hydrogen. Classified as renewable energies, these sources, along with hydroelectric power, offer a pathway towards planetary decarbonization, as they eschew reliance on fossil fuels.

However, these power-generating facilities often found themselves situated at a considerable distance from major consumers, specifically large urban centers. This spatial disparity necessitated the development of a means to efficiently transport the energy generated by these plants to the significant consumer hubs. This necessity gave rise to electrical substations, pivotal in facilitating the transmission of energy from power plants to end consumers, thereby playing a fundamental role in the entire energy cycle.

However, the introduction of electrical substations takes place, and while various types exist, here spotlight four specific substation categories here:

- **Step-up substations:** Positioned in close proximity to power plants, these substations serve the crucial function of elevating the energy voltage. This strategic placement aims to minimize losses attributable to phenomena such as Foucault currents and parasitic currents, ensuring the delivery of generated power with utmost efficiency. Given the substantial distances involved in transmission, the decision to increase voltage at this stage becomes imperative to effectively mitigate the mentioned challenges.
- **Distribution Substation:** Following the transmission of energy from remote areas at higher voltages to minimize losses, it becomes essential to lower the voltage before reaching consumers at safer levels. This leads to distribution substations, where the voltage is reduced, allowing for a more seamless distribution of energy within urban centers.

- **Step-Down Substation:** The step-down substation is the one located very close to the end consumer, operating at a lower voltage than in distribution, thereby reducing the risks to the individuals who utilize it.
- **Switching Substation:** This facility is designed to interconnect supply circuits operating at the same voltage level. It allows for the segmentation of circuits, facilitating the power on of shorter sections, and enabling a more flexible and efficient distribution of electrical power.

Figure 1.1 is a diagram illustrating the path from the power plant where the energy is generated, going through high power transformer to elevate the voltage to have minimum losses, the transmission line to transmit all the power, a high power transformer to step down the voltage and send the energy to the end consumer,¹.

Electricity generation, transmission, and distribution

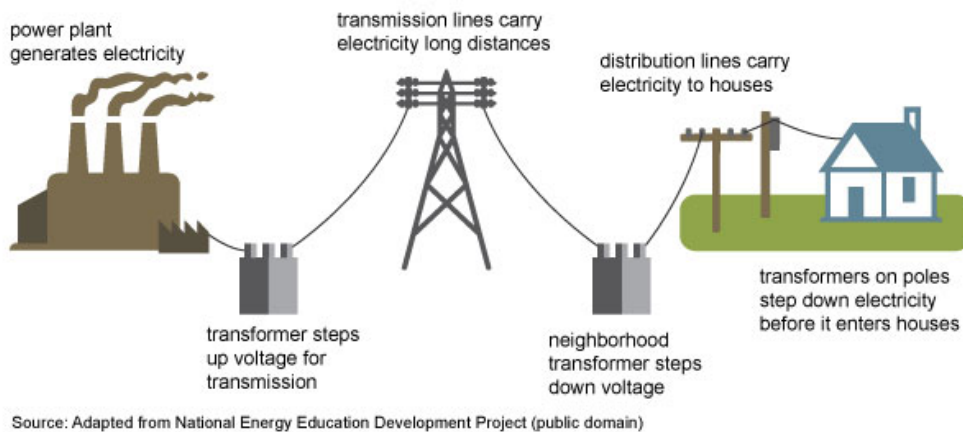


FIGURE 1.1: Electricity Generation, Transmission, and Distribution Pathway (Image credits: U.S. Energy Information Administration)

1.2 Digital Substation

Electric power substations play a fundamental role in the entire cycle of electric energy and its transformations. Simultaneously, as we witness several generating sources converting energy, such as hydroelectric (water turbines), thermal (steam turbines), combined cycle (gas turbines and steam turbines), wind (wind energy), solar farms (solar energy), among others into electric energy, numerous consumers draw upon this produced energy. The absence of an energy storage location underscores the substantial importance of substations. Without them, meeting the extensive demand and need for electric energy would be impracticable, hindering economic growth and the development of industries, businesses, and even entire countries. Today, every facet of operation, from mega-factories to simple light bulbs, relies on electric energy.

Substations facilitate the extended reach of energy to diverse locations, enabling a direct connection from the generating source to consumers. Serving as the link between

¹<https://www.eia.gov/energyexplained/electricity/delivery-to-consumers.php>

generation and consumption, substations categorize the electric energy chain into four major divisions: electric energy generation, electric energy transmission, electric energy distribution, and electric energy consumption. These processes start with High Voltage (Generation), increases to Very High Voltage (Transmission), goes to Medium Voltage (Distribution) and when finally reaches the consumer is Low Voltage (Consumers).

The evolution of electric substations has embraced new technologies, as preventive maintenance, predictability of problem occurrences, fault alerts, backyard equipment switching, and visualization of currents and voltages. Follow these advancements are electromechanical protection relays, monitoring and safeguarding against electrical faults in backyard equipment. Backyard equipment, including high-voltage circuit breakers, switches, capacitor banks, reactors, transformers, and transmission lines, retains the basic concept from the 1990s but now has features enhanced performance and added functionalities due to technological advances.

Electric power systems within a substation can be categorized into four levels:

- Level 0 - Backyard Equipment: Encompassing all devices responsible for transmitting energy from the power generation station to customers, factories, public lighting, residences, hospitals, data centers, etc. These devices are responsible for the entire energy system.
- Level 1 - Protection Relays: Formerly known as Intelligent Electronic Devices (IED), these devices have replaced the need for multiple protection relays, executing a lot of protection functions, such as overcurrent, overvoltage and transformer differential, within a single device and add the communications possibilities, exchange information between devices.
- Level 2 - Supervisory Control and Data Acquisition (SCADA): SCADA systems communicate with IEDs to acquire data, including readings of currents and voltages, facilitating the supervision of the entire substation and remote operation of backyard equipment.
- Level 3 - Control Center: This centralizes information from multiple substations, commanding them in a manner conducive to the grid and handling functions inherent to Level 2. Typically used by those overseeing the distribution of electrical energy system throughout a country, it ensures a balanced load throughout varying consumption periods.

Over the years, substations have evolved to the concept of a digital substation. Even today, it is a very current topic, we moved from having less 'smart' equipment to having every device becoming more 'smart'.

The concept of a digital substation involves seamless communication between devices across all levels, minimizing the need for electrical wires and favoring optical fiber as the primary means of information exchange. Devices communicate with each other, enabling actions such as a trip originating from an IED communicating with a circuit breaker via the network to address a fault identified by the IED. This is achieved through a message called Generic Object-Oriented Substation Event (GOOSE), and the circuit breaker itself triggers the operation through the GOOSE protocol, exemplifying the digital substation concept. While the world still faces limitations in fully embracing the digital substation concept, notable progress has been made at Level 0, particularly with the introduction

of Merging Units (MU). These units perform analog acquisition of current and voltage sensor data and inform other devices digitally on the network.

This marks another step towards the digital substation concept, where only this equipment is connected to the sensors, and a single optical fiber connects to a switch to publish information from the respective sensors. Today, there is no longer a need to connect wires to the electrical protection panel, connect the IEDs to the same network as the Merging Unit provides the necessary information to execute electrical protection algorithms.

1.3 Research Motivation and Context

With the advent of the IEC 61850 standard in the energy sector, emerging as the definitive standard for the entire industry, facilitating essential interoperability among diverse equipment from various manufacturers, ensuring reliability, real-time responsiveness, and resilience over time. Fueled by a deep passion for the field of electrical energy.

Presently, It is actively contributed to the improve of IEDs, developing a solution wherein the device possesses decision-making capabilities. This involves choosing, through the IEC 61850-9-2 Samples Values protocol, which sample provided by the Merging Units to employ in the algorithms of the protection device.

This endeavor allows me to amalgamate my extensive experience in commissioning electrical substations, particularly in conducting primary and secondary tests with a focused emphasis on secondary evaluations.

The insights gained from my pursuit of a Master's degree in Critical Computing Systems are seamlessly integrated into this tangible development. The aim is to enhance a critical functionality of IEDs, positioning these devices as the cornerstone with the most critical actuation power within an electrical substation. This commitment ensures optimal response times while steadfastly adhering to the foundational principles of electrical protections and the four pillars of electrical protection:

- **Reliability:** The likelihood of a component, equipment, or system meeting its intended function under specified circumstances, while avoiding unnecessary operations during routine system operation or in the presence of faults outside its protection zone.
- **Sensitivity:** The capacity of the protection system to respond to abnormalities in the designated operating conditions, selectively isolating only the portion of the system experiencing a fault, while allowing the rest to operate normally.
- **Selectivity:** The ability to completely isolate the faulty element and disconnect the smallest possible portion of the system by operating associated breakers.
- **Speed:** The commitment to minimizing the impact of faults and the risk of instability, quantified by the time between fault occurrence and the opening command of the circuit breaker issued by the relay or IED.

1.4 Research Objectives

The ongoing digital transformation of electrical substations has led to the development of a crucial component known as the Merging Unit. This advanced equipment plays a significant role in modernizing substations by enabling the acquisition of data from current and voltage transformers. Its main function is to read and process these values and then transmit them via the IEC 61850-9-2 Sampled Values (SV) protocol.

A scenario may occur in which two Merging Units simultaneously read data from the same current or voltage transformer. Both units independently send Sampled Values over the Ethernet network, creating a need for a decision-making mechanism within the IED. The IED, which is a key element in protection systems, must possess the capability to identify and select the optimal sample for use in its protection algorithms.

This research focuses on developing the intelligence required for the IED to autonomously evaluate and choose between the multiple samples provided by the Merging Units. By improving the decision-making abilities of the IED, the research aims to optimize the performance and reliability of protection systems in digital substations, ultimately enhancing the overall efficiency and resilience of the power grid.

1.5 Research Contributions

This thesis introduces a significant contribution through the proposition of an algorithm designed to optimize the selection of samples from each current transformer and voltage transformer for individual electrical protection relays. These algorithms are instrumental in ensuring that electrical protection systems adhere to the four key principles of protection philosophy. Recognizing that the same Merging Unit may not yield optimal results for all protection relays, the effectiveness of the algorithm is contingent on various factors, including communication routes, the distance information travels, and potential network issues such as information overload, given the abundance of sampled values in the network. As such, the primary contribution of this thesis lies in the development of an algorithm capable of discerning the most suitable sample for consumption by the IED in the network.

1.6 Thesis Structure

The current thesis is organized into seven sections: Introduction, State of the Art, Research Topic, Implementation, Development of the Algorithm, Tests and Evaluation, and Conclusions. Together, these chapters comprehensively cover all aspects of the topic, ensuring a thorough exploration and analysis within the scope of this master's thesis.

In Chapter 2 - State of Art: This chapter reviews the existing literature and technologies related to substation automation systems, with a focus on digital substations. It provides a detailed analysis of various components such as circuit breakers, switches, and transformers, as well as the role of Intelligent Electronic Devices (IEDs) in protection, control, measurement, and monitoring. The chapter also delves into the IEC 61850 standard, explaining its different parts and their significance in modern substation communication protocols.

In Chapter 3 - Research Topic: This chapter explores the specific research problem addressed in the thesis. It identifies the research gap by analyzing existing literature and related studies, discussing why addressing this gap is important. The chapter outlines the architecture of the algorithm developed to solve the identified problem, setting the groundwork for the implementation and testing described in subsequent chapters.

In Chapter 4 - Implementation: This chapter details the practical aspects of developing the proposed algorithm. It covers the hardware and software components used, including specific technologies and tools such as Rust crates. The chapter explains how the algorithm was developed, including the selection of sampled values and the overall architecture. It also discusses the challenges faced during implementation and how they were overcome.

In Chapter 5 - Development of Algorithm: This chapter focuses on the detailed development process of the algorithm for IEC 61850-9-2-SV. It explains the structure of sampled values, the creation of a publisher and subscriber for SVs, and the core functions of the algorithm. The chapter also discusses the simulation of electrical grid signals and the introduction of invalid samples for testing purposes. The finalization of both the publisher and subscriber is covered, along with the overall development of the algorithm.

In Chapter 6 - Tests and Evaluation: This chapter presents the testing and evaluation of the developed algorithm. It includes detailed tests of the publisher and subscriber for IEC 61850-9-2-SV, as well as the overall algorithm's performance. The chapter discusses the results of these tests, evaluating the algorithm's effectiveness in meeting the research objectives and its potential for real-world application.

In Chapter 7 - Conclusion: The final chapter summarizes the thesis, discussing the limitations of the research and the conclusions drawn from the study. It also offers suggestions for future work, including potential improvements to the algorithm, the addition of new features, and the exploration of further research opportunities in digital substations and related technologies.

Chapter 2

State of the Art

2.1 Introduction to Substation Automation System

In the past, electrical grids faced serious limitations in terms of the employed technologies. However, in today's world, there is a notable increase and significant growth in digital communication technologies in terms of performance and reliability. To adapt to this evolution, Substation Automation Systems (SAS) are based on dedicated software embedded in hardware components. Additionally, SAS provides a straightforward way to control and monitor all equipment in the substation, both locally and remotely. SCADA systems offer users a Human-Machine Interface (HMI) used to control, monitor, and protect devices. Moreover, SAS perform this control and monitoring in real-time, contributing to maximizing availability, efficiency, safety, and data integration, resulting in a significant cost reduction.

Furthermore, the IEC 61850 standard and its associated communication protocols are introduced, to be employed within individual substations and between substations. Consequently, the implementation of the Manufacturing Message Specification (MMS), GOOSE, and SV protocols allows for efficient control and monitoring, ensuring that the system is made more robust and future-proof.

Figure 2.1 is a diagram illustrating how is inside a SAS system, this figure represents the minimum equipment it is needed to have a substation, as IED, Global Positioning System (GPS), switches, routers, personal computer and all the electrical equipment to manage the grid.¹

¹<https://docplayer.net/40767859-Lecture-5-substation-automation-systems-course-map.html>

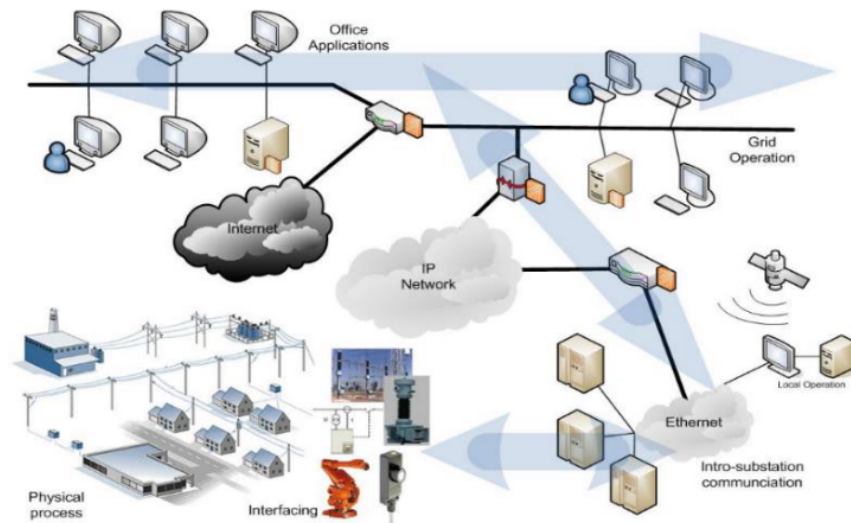


FIGURE 2.1: Design of Substation Automation Systems(Image credits: KTH, "Lecture 5: Substation Automation Systems")

2.2 Backyard System

The backyard system serves as the hub for all high-power apparatus, responsible for channeling energy from the power plant and facilitating its delivery to homes. It encompasses a range of critical devices, such as high-voltage circuit breakers, switches, voltage transformers for protection and measurement, current transformers for protection and measurement, high-voltage power transformers, capacitor banks, reactors, and synchronous compensators, devices that have gained increasing prominence in recent times. However, let's delve into the components found in any substation, as they will be detailed in the subsequent subsections.

2.2.1 Circuit Breakers

High-voltage circuit breakers play a crucial role in the operation and protection of electrical networks at very high, high, and medium voltages. They are electromechanical devices designed to interrupt the flow of electric current under abnormal conditions in the electrical network, such as short circuits and overloads. In the event of a network fault, the circuit breaker receives a signal from the electrical protection system detecting abnormalities. With this signal, the circuit breaker contacts quickly open to interrupt the electric current and extinguish the electrical arc generated when the contacts open, preventing damage to the network equipment.

Circuit breakers ensure the reliability of electrical power supply, with a focus on making electricity available to the entire network. High-voltage and very high-voltage circuit breakers are responsible for isolating detected faults in the system, preventing the spread of the defect to other parts of the network and thus avoiding widespread blackouts.

2.2.2 Switches

High-voltage switches play a pivotal role in the seamless operation of electrical networks at very high, high, and medium voltages. These electromechanical devices are intricately designed to isolate a section of the electrical system during normal operating conditions. When conducting maintenance on the electrical network, the switch opens a specific circuit segment, necessary for the safe and efficient execution of maintenance tasks. This ensures the well-being of maintenance personnel while simultaneously preserving the continuous operation of the electrical network.

In essence, very high, high, and medium voltage switches serve as integral components in power substations, offering a secure and dependable method for isolating designated sections of the electrical system. This isolation is essential for the maintenance of power system equipment, including transformers, circuit breakers, and capacitor banks. Importantly, this isolation process does not compromise the overall functionality of the substation (Starck, Wimmer, and Majer 2013).

2.2.3 Voltage Transformers

Voltage transformers play a critical role in electrical systems by providing precise voltage measurements for each phase of the circuit. Their primary function is to convert very high voltages into more manageable, general-purpose voltages like 110V. The utilization of lower voltages facilitates easier handling, both in terms of magnitude and the insulation required for compatibility with IEDs.

Ensuring optimal signal quality is a key responsibility of voltage transformers. Their primary objective is to accurately replicate the high voltage in a lower voltage format, creating a precise replica with reduced values. This replication process is essential for utilizing the information in electrical protection, enabling the analysis of network disturbances, and facilitating timely action in the event of a fault.

2.2.4 Current Transformers

Current transformers play a crucial role in electrical systems, offering precise current measurements for each phase of the circuit. Their primary function is to convert very high currents into more manageable, general-purpose currents, typically around 1A. This reduction in current values enhances ease of handling, both in terms of magnitude and the insulation required for compatibility with IEDs.

Ensuring optimal signal quality is a paramount responsibility of current transformers. Their principal objective is to accurately replicate the high current in a lower current format, creating a precise duplicate with reduced values. This replication process is vital for utilizing information in electrical protection, enabling the analysis of network disturbances, and facilitating prompt action in the event of a fault.

2.3 Intelligent Electronic Devices

The IED formed by the set of units for data acquisition, processing, and transmission, located in substations, is generically referred to as a Remote Terminal Unit (RTU). At a

given moment, it represented a significant evolution within a sector known for its conservatism in adopting new technologies, allowing remote control of substations by a central-level system, initiating the evolution of data transmission capacity through advances in telecommunications and the application of computers on a large scale. This enabled the expansion of the potential use of digital technology as a reality in substation environments (Ribeiro 2010).

With consolidated digital electronics technology, the first proposals for Integrated Protection and Control Systems emerged, using protection relays and control units based on microprocessors and memories, with intelligence at the equipment level for logic execution and automation, introducing the concept of IED. These devices enable the use of computer networks for communication via fiber optics between terminals and relays within the same substation. In addition, personal computers are used at the control and monitoring level of the substation (Ribeiro 2010).

2.3.1 Protection Algorithm System

Protection stands as one of the paramount functions within a substation or any power system. Its primary goal is to ensure the safeguarding of equipment and personnel, while also minimizing damage in the event of electrical faults, short circuits, or overloads. This critical function is inherently local, designed to operate independently if necessary, irrespective of the substation's automation system. Even though it seamlessly integrates into the automation system under normal conditions, the integrity and effectiveness of protection functions should never be compromised or restricted within any power system automation (Ribeiro 2010).

2.3.2 Control System

Local control involves autonomous control actions that a device can independently perform, such as interlocks, switching sequences, synchronism verification, and others. In this context, human intervention is limited, and the risks of errors are minimized. Similar to protection, local control should continue to operate even if the automation system is compromised.

Remote control functions are related to substation control executed by SCADA software. Commands can be directly issued to devices managed remotely, such as opening or closing a circuit breaker. Relay settings can be adjusted either through the device itself or a computer equipped with manufacturer-specific software. Additionally, desired information can be collected from protection relays using the IEC 61850 protocol via the MMS protocol. This eliminates the need for human actions within the substation to perform switching operations, making these actions faster. Furthermore, the SCADA terminal provides an overview of the entire plant, offering insights into ongoing activities and status (Ribeiro 2010).

2.3.3 Measurement

A range of information from a substation is collected and analyzed in real-time by the automation system for its proper functioning. The measurement system consists of:

- Electrical Measurements - voltages, currents, power, power factor, harmonics, etc;

- Monitoring Measurements of Equipment - such as transformer and motor temperatures;
- Disturbance Recorder - Recordings of disturbances for fault analysis.

This vast amount of information can assist in studies such as load flow analysis and planning for disturbances, in addition to being essential for protection and control functions (Ribeiro 2010).

2.3.4 Monitoring

It is a sequence of events or part of the automation system with information that allows monitoring the state of the substation, such as equipment status, maintenance alerts, relay configurations, etc. This improves the overall system efficiency, enhancing the effectiveness of protection and control. These pieces of information are useful in fault analysis, determining what happened, when, where, and how it happened (location, time, and sequence)(Ribeiro 2010).

2.3.5 Communication Protocols

The significant progress in substation automation has led to substantial investments by major IED manufacturers aiming to provide differentiation in protection and control equipment for substations. This competition has also given rise to a large number of proprietary communication protocols, which, to some extent, generated undesirable results in terms of interoperability. Substations with a large number of IEDs are highly likely to have undergone growth, with the current topology not being the original one. In such cases, equipment from different manufacturers is often present, and when connected to a single network, they do not communicate as expected in the vast majority of cases.

Faced with the communication challenges between devices, standardized protocols have emerged with the goal of achieving the desired interoperability. In other words, these protocols aim to enable communication between devices from different manufacturers on the same network. Figure ?? displays some of the most commonly used protocols in substation networks (Ribeiro 2010).

Protocol	Originally used by	Speed	Access Principle	OSI Layers
MODBUS	Gould-Modicon	19.2 kbps	Cyclic scanning	1, 2, 7
SPABUS	ABB (exclusive)	19.2 kbps	Cyclic scanning	1, 2, 7
DNP3.0	GE-Harris	19.2 kbps	Cyclic scanning ²	1, 2, 7 ³
IEC 60870-5	All manufacturers	19.2 kbps	Cyclic scanning	1, 2, 7
MODBUS+	Gould-Modicon	Token	Cyclic scanning	1, 2, 7
PROFIBUS	Siemens	12 Mbps	Token	1, 2, 7
MVB	ABB	1.5 Mbps	TDM	1, 2, 7 ⁴
FIP	Merlin-Gerin	2.5 Mbps	TDM	1, 2, 7
Ethernet + TCP/IP	All manufacturers	10 Mbps	CSMA/CD	1-7
LON	ABB (exclusive)	1.25 Mbps	PCMSA/CD	1-7
UCA 2.0	GE	10 Mbps	CSMA/CD	1-7

TABLE 2.1: Communication Protocols used by energy company.

2.4 Overview of IEC 61850

IEC 61850 is an international standard for communication in substations and power utility automation. It defines a set of protocols and data models to enable the interoperability of devices within a substation, facilitating efficient and standardized communication for protection, control, monitoring, and automation purposes. Key features of IEC 61850 include:

- **Data Modeling:** The standard introduces a standardized way of modeling substation data, using a hierarchical structure known as the Common Information Model (CIM). This allows for consistent representation of information across different devices.
- **Communication Protocols:** IEC 61850 specifies communication protocols for substation automation, with an emphasis on Ethernet-based communication. It defines how devices such as protection relays, controllers, and meters exchange information using protocols like MMS and GOOSE.
- **Sampled Values:** Part 9 of the standard, IEC 61850-9, introduces Sampled Values, enabling the transmission of digitized analog values, such as voltages and currents, in a standardized manner. This is crucial for real-time protection applications.
- **Configuration Language:** IEC 61850 includes SCL (Substation Configuration Language), a standardized language for describing the configuration of devices and systems within a substation. SCL allows for the exchange of configuration information between different devices.
- **GOOSE Messaging:** GOOSE messaging is a key feature that allows devices to exchange critical information in a peer-to-peer manner, enabling faster and more deterministic communication for protection and control functions.
- **Interoperability:** The standard aims to improve interoperability between devices from different manufacturers, promoting vendor-neutral solutions and reducing integration efforts in substations.
- **Engineering Process:** IEC 61850 defines an engineering process that standardizes the design, configuration, and testing of substation automation systems. This helps ensure consistency and reliability in the deployment of automation solutions.

IEC 61850 plays a vital role in modern and optimal power systems by provide a standardized framework for communication and automation in substations. It enhances reliability, flexibility, and interoperability in the evolving field of power utility automation.

2.4.1 IEC 61850-1 - Introduction and Overview

This initial segment provides a comprehensive introduction to the entire IEC 61850 series, offering a foundational framework for communication within substations. It sets the stage for subsequent standards, establishing a cohesive context for the standardization of communication in substation automation systems (R.E. Mackiewicz 2006).

2.4.2 IEC 61850-2 - Glossary

Part 2 of the standard IEC61850, meticulously defines the glossary of terms used throughout the IEC 61850 series. By ensuring a uniform understanding of terminology, this section fosters clear communication and interpretation of the standards among diverse stakeholders in the energy sector (R.E. Mackiewicz 2006).

2.4.3 IEC 61850-3 - General Requirement

This section outlines overarching requirements for communication networks and systems in substations. Covering aspects such as performance, testing procedures, and documentation standards, it provides a robust set of guidelines for the effective implementation of IEC 61850 (R.E. Mackiewicz 2006).

2.4.4 IEC 61850-4 - System and Project Management

Centered on system and project management, this section provides valuable guidance for the seamless orchestration of IEC 61850 within substation communication systems. It encompasses essential aspects of planning, execution, and documentation, contributing to the successful deployment of the standard (R.E. Mackiewicz 2006).

2.4.5 IEC 61850-5 - Communication Requirements for Functions and Device Models

Part 5 plays a pivotal role by defining communication profiles for specific functions and device models in substations. This ensures seamless interoperability between devices from different manufacturers, facilitating their integration within substation automation systems (R.E. Mackiewicz 2006).

2.4.6 IEC 61850-6 - Configuration Language for Communication in Electrical Substations

This segment specifies a standardized language for articulating the configuration of communication in electrical substations, particularly in relation to IEDs. It streamlines the configuration process, enhancing consistency across diverse implementations(R.E. Mackiewicz 2006).

2.4.7 IEC 61850-7 - Basic Communication Structure

Establishing the fundamental communication structure for substation and feeder equipment, Part 7 provides a foundational framework. It defines essential elements necessary for communication within substations, fostering a standardized structure for various devices (R.E. Mackiewicz 2006).

2.4.8 IEC 61850-8 - Specific Communication Service Mapping

Part 8 concentrates on Specific Communication Service Mappings (SCSM), offering guidance for mapping diverse protocols used in substation communication. This ensures

compatibility and smooth interaction between devices employing different communication protocols (R.E. Mackiewicz 2006).

2.4.9 IEC 61850-9 - Specific Communication Service Mapping

Part 9 specifically deals with defining SCSM tailored for diverse protocols used in substation communication. It establishes a standardized framework to ensure compatibility and seamless interaction among different devices within substation automation systems. IEC 61850-9 is crucial for promoting interoperability and facilitating efficient communication among IEDs in substations by addressing the intricacies of various network layers (R.E. Mackiewicz 2006).

2.4.10 IEC 61850-10 - Conformance Testing

Focusing on conformance testing, Part 10 establishes rigorous procedures and requirements to verify that devices and systems adhere to the IEC 61850 standard. This contributes to the reliability and compatibility of implementations by ensuring strict compliance through thorough testing processes (R.E. Mackiewicz 2006).

2.5 IEC 61850-9-2 Sampled Values (SV)

This section discusses the evolution of the IEC 61850-9-2 protocols, tracing its development from its precursor in 2002, IEC 60044, to its current version, IEC 61850-9-2 Ed2, finalized in 2020.

2.5.1 IEC 60044-8/2002

Many in the industry are familiar with the IEC 60044 standard, a predecessor to the current IEC 61869 standard for instrument transformers. Part 8 of IEC 60044, dealing with electronic instrument transformers, introduced the concept of a "merging unit." This unit acts as a bridge between analog and digital signals, facilitating the conversion of analog network signals for use in digital IEDs. Additionally, the standard introduced the idea of a data set, later utilized in IEC 61850 for network communication.

Figure 2.2 The concept of the MU represents the integration of various sensor data, such as current and voltage measurements, into a single digital output, streamlining communication between equipment and control systems. This concept laid the foundation for the development of the MUs available in the market today. The initial integration and design of MUs introduced a unified approach to handling data, which has since evolved into a critical component for ensuring efficient, reliable, and accurate data transmission in substations. ²

²<https://www.linkedin.com/pulse/history-iec-61850-sampled-values-tibor-congo/>

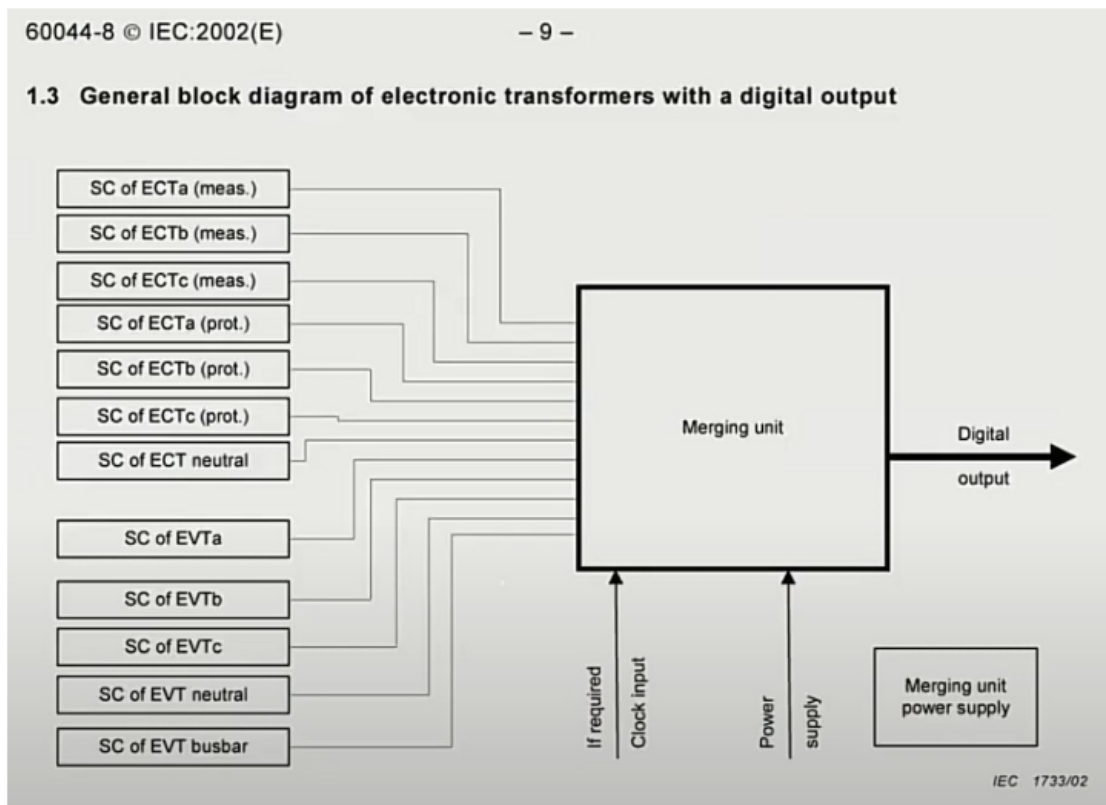


FIGURE 2.2: Concept of the Merging Unit.

2.5.2 IEC 61850-9-1/2003

This marks the beginning of the protocol known today. However, it initially leaned towards a point-to-point communication model, resembling its predecessor IEC 60044. This approach lacked considerations for network applications, crucial for the interoperability that the protocol now provides. The concept of the Process Bus network, prevalent today, was not present during this period, causing delays in releasing the next version (Tibor 2022).

2.5.3 IEC 61850-9-2(Ed1)/2004

At this stage, the abstraction of the IEC 61850 standard is being carefully applied once more. Initially introduced in the IEC 61850-7-2 standard, this service specification has since developed into a well-defined standard within IEC 61850-9-2, where it is clearly outlined within the context of Ethernet communication.

The data structure is characterized by its generic definition, and the communication process operates entirely independently. This implies that, in the future, we could seamlessly transition to another standard beyond Ethernet, tailored to the system's evolving needs. This flexibility is a testament to the power that abstraction brings. However, it's important to note that, thus far, the Ethernet protocol has been utilized and has consistently met the expected performance requirements.

In this revised standard, the noteworthy inclusion is the implementation of the process bus for Sampled Values, signaling a departure from the initial point-to-point communication approach. Here, to propagate Ethernet packets across the network, it leverages the existing multicast definition of the Ethernet protocol.

A widely embraced guideline employed by manufacturers in the development of Sampled Values is the UCA Implementation Guideline for IEC 61850-9-2.. It's crucial to recognize that this is a guideline, not a standard(Tibor 2022).

2.5.4 IEC 61850-9-2 Ed2/2011

In this new edition, there were not many changes, mainly due to the fact that the energy industry was not significantly progressing in the adoption of this technology, even with lighter versions like IEC 61850-9-2-LE. The reasons for this lack of progress are attributed to the skeptical nature of many protection engineers. They tend to be more conservative when it comes to supplying electrical power, sometimes justified by negative experiences in the field(Tibor 2022).

There were also some technical issues with SVs due to time synchronization. At that time, the most used protocol was SNTP, which allowed only millisecond precision. For SVs, higher precision in samples was needed. Additionally, there was immaturity in redundancy solutions in the network. Consequently, these two significant problems were only resolved later with the implementation of the following technologies:

- Time Synchronization - Precision Time Protocol (PTP): This protocol enables time synchronization via Ethernet with a timing error of less than 1 microsecond. Synchronization could now be achieved through the Ethernet network connection, eliminating the need for a separate network for time synchronization of merging units in the field.
- Redundancy - Parallel Redundancy Protocol (PRP): PRP operates with effectively two duplicated networks, resembling the approach adopted by service providers in the transmission of electrical energy networks. These providers often maintain redundant protection/control systems. The loss of service in one of these networks does not compromise functionality, as the parallel network continues to perform its communication functions without affecting the protection/control systems.
- High Availability Continuous Redundancy (HSR): HSR provides redundancy through a ring architecture. This is essentially the same ring architecture, where communication service continuity is maintained through the open ring, in case of service loss in any part of the closed ring. In both cases, specific hardware (and software) requirements must be met to consider the implementation of the solution. This is a fundamental element in the design of the Digital Substation.

For time synchronization, the adopted solution was the Precision Time Protocol (PTP). With a resolution below 1 microsecond, this was sufficient for SVs to be synchronized, making it possible to reconstruct the digital waveform into analog again and check for faults or network issues by IEDs. In terms of redundancy, two solutions were implemented: PRP and HSR, with PRP being the more widely used due to lower associated implementation costs and the assurance of redundancy(Tibor 2022).

2.5.5 IEC 61869-9/2016

The IEC 61869-9 standard is familiar to everyone using instrument transformers for other applications in the industry. This standard provided recommendations for measuring instruments, ranging from light versions to more demanding ones. The Figure 2.3 below summarizes this information.³

Sampling Frequency	Samples per Packet	Packet Frequency	
4000Hz (80SPC @ 50Hz)	1	4000Hz	9-2LE
4800Hz (80SPC @ 60Hz)	1	4800Hz	
12800Hz (256SPC @ 50Hz)	8	1600Hz	
15360Hz (256SPC @ 60Hz)	8	1920Hz	
4800Hz	2	2400Hz	New preferred
14400Hz	6	2400Hz	
5760Hz	1	5760Hz	96SPC @ 60Hz

FIGURE 2.3: Frequency regarding Sampled Values.

The information derived from the table indicates that protection functions use a sampling rate of 4800Hz at 60Hz and 4000Hz at 50Hz according to the IEC 61850-9-2-LE version. When we talk about preferred streams, the sampling rates remain the same regardless of their use, such as protection, measurement, or power quality. This balance is achieved by adjusting the necessary samples per Application Specific Data Unit (ASDUs) per packet.

The IEC61869-9 standard mentions the use of configurable datasets. The IEC 61850-9-2-LE version simplified this by publishing 4 currents + 4 voltages for all datasets. While this approach was efficient, it lacked flexibility. Therefore, IEC61869-9 introduces flexibility in this regard, optimizing the implementation. However, this increased flexibility also brings greater complexity to data processing(Tibor 2022).

2.5.6 IEC 61850-9-2 Ed2.1/2020

In this latest update, there was a small reinforcement of what was mentioned in the previous version. Here, a new field called SynchSrcID was introduced, which is used to specify the synchronization source of the merging unit. This new feature is one of the optional fields. In the IEC 61850-9-2-LE version, there was only one field, but breaking free from the limitations of this version, now there are more fields to configure. Again, a note on what was mentioned above, it is essential to analyze configuration issues and implementation costs, as it will be more complex(Tibor 2022).

The evolution from IEC 60044-8 to IEC 61850-9-2 ED2.1 marks the shift from analog to digital in substation communication. Starting with the digitization of transformer outputs,

³<https://www.linkedin.com/pulse/history-iec-61850-sampled-values-tibor-congo/>

it progressed through increasingly sophisticated standards (IEC 61850-9-1, 9-2 ED1, and 9-2 LE), refining the transmission of sampled values over Ethernet. The development culminated in IEC 61869-9 and IEC 61850-9-2 ED2.1, which ensure interoperability and advanced digital communication in modern substations, in Figure 2.4 ⁴ has shown the progress through years.

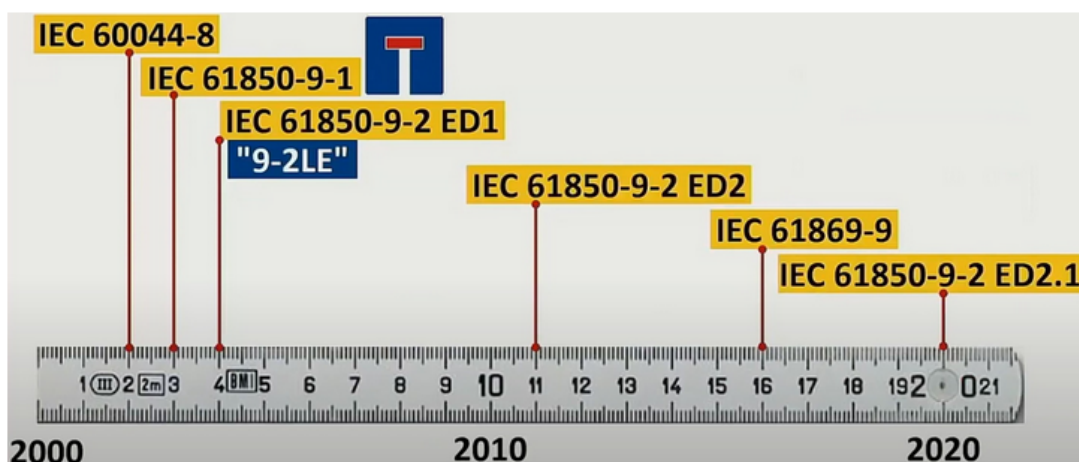


FIGURE 2.4: Evolution of IEC 61850-9-2

⁴<https://www.linkedin.com/pulse/history-iec-61850-sampled-values-tibor-congo/>

Chapter 3

Insights

3.1 Identification of the research gap

The advent of the IEC 61850 standard has significantly revolutionized the substation automation systems by facilitating interoperability and enhancing communication efficiency. Particularly, IEC 61850-9-2, which specifies the transmission of SV from MU to protection and control devices, has been pivotal in this transformation. Despite the substantial body of literature focusing on the implementation and benefits of IEC 61850-9-2, there remains a notable gap concerning the development of algorithms designed to optimize the selection of SVs in real-time protection scenarios involving multiple merging units.

3.1.1 Existing Literature and Related Research

A comprehensive literature review was conducted using databases such as IEEE Xplore, ScienceDirect, and Google Scholar. Keywords included "IEC 61850-9-2", "sampled values", "merging units", "protection relay", and "algorithm optimization". The search encompassed studies published from 2000 to 2023. The review revealed numerous studies addressing various aspects of IEC 61850-9-2, such as its implementation challenges, communication performance, and impact on substation automation.

For example, (Leupp and Ryttoft 2010) explores the general benefits of IEC 61850-9-2 in improving the accuracy and speed of data transmission in substations. Similarly, (Baumgartner, Riesch, and Schenk n.d.) investigates the synchronization issues in SV transmission and proposes methods to mitigate these challenges. Additionally, (Chen 2016) examines the integration of IEC 61850-9-2 with other substation protocols to enhance system reliability.

3.1.2 Identification of the Gap

Despite these valuable contributions, none of the reviewed studies specifically address the development of an algorithm to select the optimal SV from multiple MUs for protection relays. This gap is critical, given the increasing complexity of modern substations where multiple MUs may collect data from the same current transformers (CTs), leading to potential conflicts and inefficiencies in data selection for protection purposes.

For instance, while (Skendzic, Ender, Zweigle, et al. 2007) discusses the general principles of SV selection, it does not propose a concrete algorithmic approach to dynamically choose the best SV in real-time. Moreover, (Galkin et al. 2023) focuses on the latency

and performance of SV transmission but does not consider the scenario of multiple MUs and the subsequent need for optimal SV selection.

3.1.3 Importance of Addressing the Gap

Addressing this gap is essential for several reasons. First, the ability to dynamically select the best SV from multiple MUs can significantly enhance the reliability and speed of protection relays, thereby improving overall substation safety and performance. Second, developing such an algorithm can provide a blueprint for future research and practical implementations, fostering further advancements in substation automation.

By focusing on the development of an algorithm that selects the optimal SV arriving before the protection relay, this research aims to fill a crucial void in the existing literature. This study will not only propose a novel solution to the identified problem but also provide empirical validation through simulations and real-world testing, thereby contributing valuable insights and practical tools to the field of substation automation and protection.

3.1.4 Conclusion of the research gap

In summary, while the IEC 61850-9-2 standard has been extensively studied, there remains a significant gap concerning the development of real-time algorithms for optimal SV selection from multiple MUs. This research aims to address this gap, providing a much-needed solution that enhances protection relay performance and overall substation reliability.

3.2 Architecture of the Algorithm

The algorithm involves receiving two measurements from the same measuring sensor (Current Transformers or Voltage Transformers), providing redundancy in the data acquisition required by the IED to process electrical protection algorithms. From a critical acquisition perspective, this approach is beneficial to address the scenario where one Merging Unit fails; the other Merging Unit can still send the data from that sensor. However, from the perspective of the IED, it needs to determine which of the two samples to use for running the protection algorithm to detect faults that may or may not occur based on the measurements received by the Merging Unit.

To address this issue, the proposed solution involves developing an algorithm that first monitors the SVs, classifying them, and then delivering only the sample that is most well-qualified to run the protection algorithms. The architecture of this solution is akin to a switch, where two or more SVs from the same current or voltage transformer arrive, and the switch allows only the path of the best-qualified sample, discarding the others. Consequently, two SVs may arrive, but the protection system will only consider one SVs with the best metric, Figure 3.1¹, shown has a simple connection.

¹https://www.efacec.pt/en/wp-content/uploads/2022/08/CS491I2207A1_MCU-500.pdf

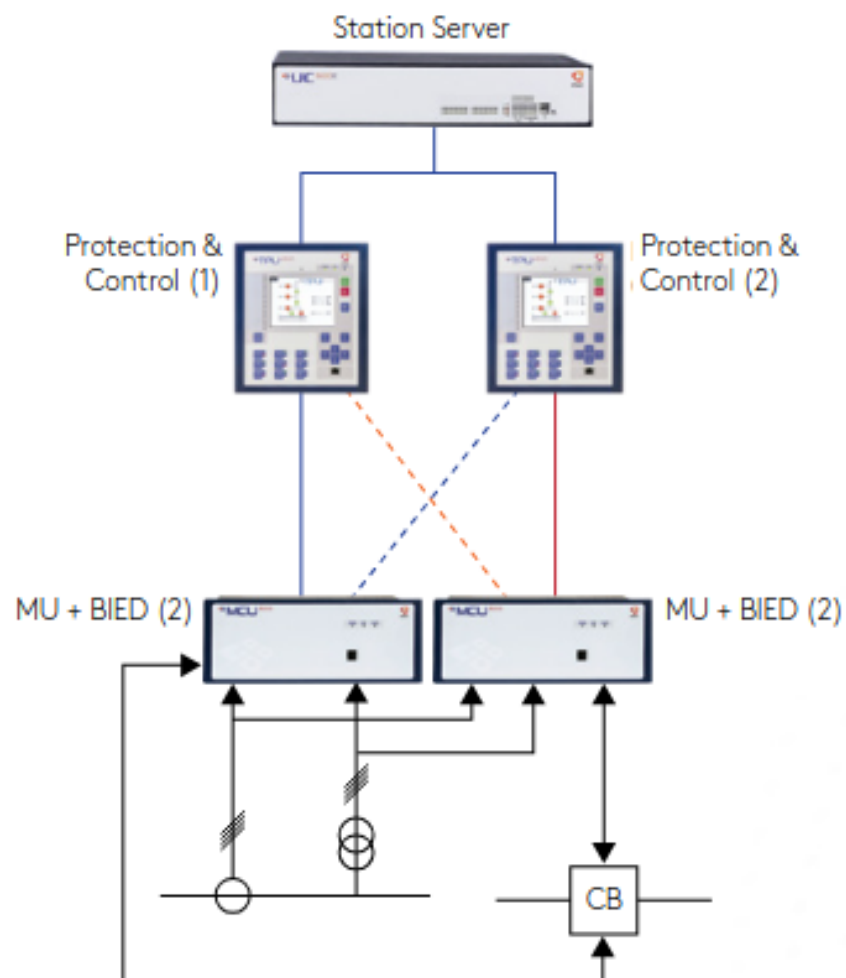


FIGURE 3.1: Simple Single Line Diagram (SLD) of Electrical Substation with SV's. (Credits: Efacec Energia, Máquinas e Equipamentos Eléctricos, S.A.)

Chapter 4

Architecture

This chapter details on the practical implementation of the proposed algorithm. It begins with an overview in Section 4.1, which outlines the key methods and tools used throughout the development process. Section 4.2 dives into the detailed steps taken to develop the algorithm, including both hardware and software components, as well as the various tools and libraries (crates) employed. Section 4.3 then describes the algorithm designed to select the best SVs and presents the results of this selection process. This chapter provides a comprehensive view of how the theoretical concepts were translated into a working solution.

4.1 Overview

The demand for an algorithm that selects the optimal analog signal has grown alongside the increasing adoption of merging units in substations. As substations transition to digitalization, merging units become indispensable for ensuring efficient performance. These units play a critical role by making various other substation components dependent on their technology. Previously, the only critical protocol was GOOSE, used for transmitting trip signals and equipment interlocks. Now, with the adoption of merging units, the communication network itself becomes critical. It ensures the accurate reception of analog signals from CTs and VTs, allowing protection algorithms to promptly identify network faults.

Consequently, formerly non-critical equipment like switches must now meet stringent performance criteria to prevent delays. This necessitates the implementation of PTP across all critical network devices, establishing PTP as the master clock for the entire substation network.

Merging units are ushering substations into the digital age, yet they also introduce new challenges. In older substations, concerns about analog signals were limited to issues like broken wires and induction. Today, with numerous interconnected devices requiring precise timing and high performance, ensuring proper system operation becomes crucial.

4.2 Setup of the Algorithm

The development was carried out using two hardware platforms to deploy the programs for running the algorithm. One of these platforms is a Jetson Nano, and the other is a personal computer. The Jetson Nano was selected due to its ease of use, as it allows for

straightforward setup of all the necessary tools to deploy the program. Additionally, an extra Ethernet card can be added using a USB-to-Ethernet adapter, which is truly plug-and-play. This feature is essential for the setup, as it requires two Ethernet interfaces.

4.2.1 Hardware

For the development and execution of this project, a Dell Inspiron personal computer has been utilized. This machine is equipped with robust specifications to support the complex computational and networking requirements of the research. The key features of this computer are as follows:

- **Processor:** Intel Core i5 10th Generation, offering a balanced blend of performance and efficiency for handling various computational tasks required during the development and testing phases.
- **Memory:** 8 GB of RAM, providing sufficient memory capacity to run multiple applications and perform intensive data processing operations seamlessly.
- **Networking:** The system includes two Ethernet cards to facilitate network connectivity: Integrated Ethernet Card: The built-in Ethernet card that comes with the computer. Gigabit USB to Ethernet Adapter: An additional gigabit Ethernet adapter connected via USB, enhancing the computer's networking capabilities. Network Speed Limitation: Despite the presence of a gigabit Ethernet adapter, the overall system network speed is limited to 100 Mbits/s. This is due to the maximum speed supported by the Jetson Nano, which is being used in conjunction with the Dell Inspiron for this project.

The Jetson Nano stands out for its versatility and compact design, making it an ideal choice for deploying sophisticated algorithms in research projects. Key features include:

- **Processing Power:** Equipped with a 1.43 GHz quad-core ARM Cortex-A57 processor and a 128-core NVIDIA Maxwell GPU, offering robust computational capabilities necessary for real-time data processing and algorithm execution.
- **Memory:** Includes 4 GB of LPDDR4 RAM, ensuring efficient storage and retrieval of data crucial for running complex algorithms and maintaining system responsiveness.
- **Connectivity:** Integrated with Gigabit Ethernet, enabling high-speed wired communication essential for modern substation automation applications, and also an ethernet adapter using USB3.0 with gigabit connection.
- **GPIO Pins:** Equipped with a 40-pin GPIO header, allowing direct interfacing with external sensors, actuators, and other peripherals, which is indispensable for hardware integration in substation environments.

The specifications of the Dell Inspiron ensure it can manage the comprehensive demands of the research, ranging from the development and testing of algorithms to interfacing with the Jetson Nano for real-time data processing and network simulations. Equipped with an Intel Core i5 10th Generation processor and 8 GB of RAM, this personal computer provides the necessary performance and memory capacity for running complex applications and intensive data operations. The inclusion of dual Ethernet

cards—one integrated and one gigabit USB to Ethernet adapter—enables flexible and reliable network configurations, essential for accurately emulating substation environments and conducting thorough testing.

The Jetson Nano is equally well-suited for executing the algorithm designed to optimize SV selection in substation automation systems. Its powerful ARM processor and NVIDIA GPU offer robust computational capabilities and efficient data handling. The integrated Gigabit Ethernet facilitates high-speed wired communication, while the 40-pin GPIO header allows for direct interfacing with external sensors and actuators. Despite the network speed being limited to 100 Mbps/s due to the maximum capacity of certain interfaces, these features collectively ensure reliable performance and effective integration into research and development efforts.

By harnessing the strengths of both the Dell Inspiron and the Jetson Nano, this research project benefits from a synergistic blend of hardware capabilities. The Dell Inspiron serves as a robust foundation for development, testing, and executing the algorithm, leveraging its computational power and memory capacity. Meanwhile, the Jetson Nano operates as both a merging unit and a protection relay, demonstrating its adaptability and connectivity. This dual functionality makes the Jetson Nano an optimal platform for handling real-time data processing and network simulations. Together, these platforms play a pivotal role in advancing substation automation, improving operational efficiency, and bolstering the reliability of substation systems.

4.2.2 Software

The software development process began with selecting the programming language for developing the algorithm. Today, we have many languages that meet performance needs and are widely used in the market, such as C and C++. These languages prioritize performance, which is why they are predominantly used in embedded systems. However, we also have languages that are easier to develop and write, although not as performant, such as Python/MicroPython.

After thoroughly analyzing the scenario in which my development needed to be inserted, I came across the Rust language. Rust offers performance comparable to C and C++ but without the memory management issues inherent to these languages. Given that this development is related to critical systems, I opted to use a safer language. Thus, the development was carried out in Rust.

The decision to use Rust was also influenced by its modern design principles and strong community support. Rust's ownership model ensures memory safety and eliminates common bugs such as null pointer dereferencing and buffer overflows. This is particularly important in critical systems where reliability and safety are essential.

Furthermore, Rust's rich type system and pattern matching capabilities facilitate the development of robust and maintainable code. The language's concurrency model is designed to prevent data races, making it a suitable choice for applications requiring high performance and safety.

By choosing Rust, the development process benefits from both high efficiency and enhanced safety, ensuring that the algorithm operates reliably within the substation automation system. This strategic choice underscores the commitment to using cutting-edge

technologies to achieve optimal performance and reliability in critical system applications.

4.2.3 Cargo

Cargo is Rust's official package manager and build system, integral to managing Rust projects. It simplifies the process of managing dependencies, compiling code, running tests, and creating documentation. Here's an overview of Cargo's key features:

- **Dependency Management**
 - **Crates:** Cargo allows developers to easily include third-party libraries (known as crates) into their projects. These crates are listed in a Cargo.toml file, where you can specify the version of each dependency.
 - **Automatic Resolution:** Cargo automatically fetches and compiles these dependencies, ensuring that the correct versions are used, and resolving any conflicts between different versions of the same crate.
- **Build and Compilation**
 - **Automatic Resolution:** Cargo automatically fetches and compiles these dependencies, ensuring that the correct versions are used, and resolving any conflicts between different versions of the same crate.
 - **Cross-Compilation:** Cargo supports cross-compilation, allowing developers to build their Rust projects for different target platforms, which is particularly useful for embedded systems.
- **Project Management**
 - **Project Initialization:** Starting a new Rust project is simple with Cargo. By running `cargo new 'project name'`, Cargo automatically creates a new directory with a basic Rust project structure, including the necessary Cargo.toml file and a default source directory.
 - **Workspaces:** Cargo supports workspaces, enabling the management of multiple related packages within a single repository. This is particularly useful for large projects with multiple components that need to be developed and managed together.
- **Community and Ecosystem**
 - **Crates.io:** Cargo is tightly integrated with Crates.io, the Rust community's official crate registry. This allows developers to publish their libraries and applications, making them available to others in the community.
 - **Cargo.lock:** Cargo manages a Cargo.lock file that records the exact versions of all dependencies used in a project, ensuring consistency across different builds and environments.

Cargo's function in the Rust ecosystem is fundamental, as it provides a unified way to manage the entire lifecycle of a Rust project—from development and dependency management to testing, documentation, and deployment. Its user-friendly interface and

powerful features make it an essential tool for Rust developers, facilitating a smooth and efficient development process.

4.2.4 Crates

Crates in Rust are the building blocks of Rust projects and packages. A "crate" refers to a compilation unit in Rust and can be a library or a binary.

- Types of Crates
 - Binary Crates: These are executable applications. When you create a binary crate, it generates a single executable file.
 - Example: If you write a Rust program with a `main.rs` file, it's a binary crate because it compiles to an executable.
 - Library Crates: These contain reusable code that other projects can depend on. Instead of producing an executable, a library crate compiles to a `.rlib` file that other projects can link against.
 - Example: A collection of utility functions or algorithms that you can share across multiple projects.
- Crates.io
 - Crates.io is the official Rust package registry where developers can publish and share their library crates. It's similar to npm for Node.js or PyPI for Python.
 - Developers can search for and download crates published by others, integrating them into their projects with ease.
- Dependency Management with Crates
 - In Rust, projects can depend on other crates. You specify these dependencies in the `Cargo.toml` file, which lists all the crates your project needs, along with their versions.
 - Cargo, Rust's package manager, handles fetching these dependencies from Crates.io, ensuring compatibility and managing versions.
- Benefits of using Crates
 - Modularity: Crates encourage modular design, making it easy to split a project into smaller, reusable components. Each crate can be developed, tested, and compiled independently.
 - Reusability: By using crates, you can leverage existing solutions for common problems. Whether it's handling dates, parsing JSON, or working with databases, there's likely a crate for it.
 - Dependency Management: Cargo automatically manages dependencies, ensuring that you're using the correct versions of the crates your project depends on, thus avoiding compatibility issues.
- Community and Ecosystem

- The Rust community actively contributes to the ecosystem by publishing high-quality crates on Crates.io. This makes it easier for developers to find reliable, well-maintained packages for their projects.

In this project, I am exclusively using library crates, which are essential to the development process. These libraries significantly streamline the development work and provide crucial functionality. Additionally, by managing these libraries with Cargo, I can easily track and control the versions I'm using, ensuring consistency throughout the project.

Crates are central to the Rust ecosystem, promoting code reuse, modularity, and collaboration. Whether you're building a small utility or a large-scale application, crates help structure your project and tap into the wealth of libraries and tools available in the Rust community. Below, I'll describe the most important libraries that have been integral to this development.

4.2.5 Tokio Crate

Tokio¹ is one of the most popular and robust asynchronous runtimes in the Rust ecosystem, offering essential components for building high-performance, reliable, and scalable network applications. Leveraging Rust's concurrency model, Tokio provides an event-driven, non-blocking I/O system that allows developers to handle thousands of concurrent connections with minimal overhead. This is particularly beneficial for applications that perform extensive I/O operations, such as reading from or writing to sockets, without needing to wait for these operations to complete before continuing with other tasks.

In addition to its asynchronous runtime, Tokio includes a comprehensive set of utilities such as timers, channels, and synchronization primitives, which are invaluable in managing complex concurrent systems. Its seamless integration with Rust's `async/await` syntax significantly simplifies the development of asynchronous code, making it more readable and maintainable.

A key feature of Tokio is its advanced multithreaded, work-stealing task scheduler, which is critical for optimizing the performance of asynchronous applications in Rust. This scheduler distributes tasks efficiently across multiple threads, ensuring full utilization of available CPU cores. By using a work-stealing approach, Tokio ensures that no single thread becomes a performance bottleneck. If one thread finishes its tasks while others are still occupied, it can "steal" tasks from the busy threads, leading to a more balanced and efficient distribution of workload.

This design is particularly beneficial in scenarios where an application must manage a large number of concurrent operations, such as handling network connections or processing real-time data streams. The scheduler minimizes idle time and maximizes throughput, which is essential for maintaining high-performance levels in demanding applications. Additionally, by automatically balancing the load, the scheduler reduces the need for manual optimization, allowing developers to concentrate on the core logic of their applications rather than focusing on performance tuning across threads. This makes Tokio an ideal choice for building scalable and responsive systems in Rust.

Tokio has to offer essential tools for managing concurrency and parallelism efficiently like:

¹<https://crates.io/crates/tokio>

- **Concurrency and Parallelism:** Tokio enables the handling of numerous tasks concurrently, facilitating the development of highly efficient and responsive applications. By utilizing asynchronous programming, Tokio helps manage multiple operations simultaneously without blocking the execution of other tasks.
- **Asynchronous I/O:** Tokio excels in non-blocking I/O operations, making it ideal for applications that need to handle multiple network connections concurrently. This is particularly relevant for the merging unit and protection relay functions in this project.
- **Scalability:** With Tokio, systems can scale efficiently, handling increased loads without a significant decline in performance. This is especially important for real-time data processing and network simulations required in substation automation systems.

By incorporating Rust and leveraging the Tokio crate, the development process benefits from high efficiency and enhanced safety, ensuring that the algorithm functions reliably within the substation automation system. This strategic choice highlights the commitment to using cutting-edge technologies to deliver optimal performance and reliability in critical system applications.

4.2.6 Serde Crate

Serde² is the standard crate for serialization and deserialization in Rust, offering a flexible and highly efficient framework for converting complex data structures to and from various formats, such as JSON, TOML, YAML, and more. Serialization is the process of converting a data structure into a format that can be stored or transmitted, while deserialization is the reverse operation. Serde's performance is one of its standout features; it's designed to minimize overhead and maximize speed, making it suitable for high-performance applications where data exchange is frequent and data structures are large or complex.

Serde ecosystem is extensive, with support for a wide range of data formats and seamless integration with other Rust crates. The framework is highly extensible, allowing developers to define custom serialization and deserialization logic for their data types. This flexibility ensures that Serde can handle nearly any data representation need, whether it's a simple JSON API or a complex, nested configuration file. Furthermore, Serde derive macros (`#[derive(Serialize, Deserialize)]`) make it incredibly easy to implement serialization and deserialization for Rust structs and enums, saving developers from writing boilerplate code.

4.2.7 Crc32Fast Crate

Crc32Fast³ is a high-performance crate designed to compute CRC-32 checksums efficiently. CRC-32 (Cyclic Redundancy Check) is a widely used algorithm for detecting errors in data transmission or storage. It's a lightweight but powerful tool that can quickly determine if data has been corrupted, making it indispensable in contexts like file integrity checks, network communications, and data archival. The `crc32fast` crate is optimized for

²<https://crates.io/crates/serde>

³<https://crates.io/crates/crc32fast>

speed, using techniques like loop unrolling and SIMD (Single Instruction, Multiple Data) instructions to process data in parallel, significantly speeding up checksum computations.

This crate is particularly useful in applications where performance is critical, such as systems that handle large volumes of data or require real-time error detection. For example, in networking, CRC-32 checksums are often used to ensure that packets are received without errors. By integrating `crc32fast` into such a system, developers can maintain high throughput while ensuring data integrity. Additionally, its simplicity and efficiency make it a go-to choice for Rust developers needing a reliable method for error-checking large datasets or streams.

4.2.8 Pnet Crate

`Pnet`⁴ (Packet Network) is a low-level networking crate in Rust that provides extensive capabilities for crafting, sending, and receiving raw network packets. It offers granular control over network communications, making it an essential tool for developers working on networking protocols, network security applications, or custom network infrastructure. `Pnet` allows you to build and dissect packets for various network layers (Ethernet, IP, TCP/UDP, etc.), giving you the ability to create highly customized network interactions that go beyond what standard networking libraries offer.

One of `Pnet`'s key strengths is its flexibility. It supports a wide range of protocols and can be used for tasks like network monitoring, building packet sniffers, creating custom firewall rules, or even developing your own network protocol. Additionally, `Pnet` is well-integrated with Rust's safety guarantees, meaning you can perform low-level network programming with fewer risks of common bugs, such as buffer overflows or memory leaks. This makes `Pnet` an excellent choice for developers who need both the power of low-level networking and the safety of Rust.

4.2.9 Log Crate

`Log`⁵ is a logging facade for Rust that provides a simple and flexible way to capture log messages in your applications. It's designed to be lightweight and minimal, focusing on defining a standard logging API that libraries and applications can use without committing to a specific logging implementation. This approach allows you to write code that logs messages at various levels (error, warn, info, debug, trace) and later decide how those logs are handled, whether they're printed to the console, written to a file, or sent to a logging service.

The log crate's primary advantage is its decoupling of log producers from log consumers. You can use the log macros (`log!`, `info!`, `error!`, etc.) throughout your codebase, and then choose or implement a logging backend (like `env_logger` or `slog`) that suits your application's needs. This flexibility makes `log` an ideal choice for libraries, as it allows the library to emit logs without enforcing a specific logging behavior on the end user. As a result, the log crate has become a standard in the Rust ecosystem, used by many libraries and applications to ensure consistent and configurable logging.

⁴<https://crates.io/crates/pnet>

⁵<https://crates.io/crates/log>

4.2.10 Env_Logger Crate

Env Logger⁶ is a simple but powerful logging backend for the log crate, designed to configure logging via environment variables. This crate is particularly useful in situations where you need to adjust the verbosity of logging without modifying the code itself, such as in different deployment environments (development, testing, production). By setting environment variables, you can control which log levels are enabled and where the log output is directed, making env_logger extremely flexible and easy to use.

For example, in a production environment, you might want to only log warnings and errors, while in a development environment, you might enable debug and trace logs to troubleshoot issues. Env_logger supports these scenarios by allowing you to configure log levels on a per-module basis, providing granular control over the logging output. This makes it an invaluable tool for developers who need to maintain visibility into their applications' behavior across different environments without cluttering the codebase with log configuration details.

4.2.11 Chrono

Chrono⁷ is a comprehensive and robust date and time library for Rust, offering a rich set of features for working with dates, times, and time zones. It's designed to be easy to use yet powerful enough to handle complex date and time manipulations. Chrono allows you to parse and format date/time strings, perform arithmetic operations on dates and times (e.g., adding or subtracting time durations), and work with time zones, including conversions between UTC and local times.

One of Chrono's most significant advantages is its flexibility and precision, making it suitable for a wide range of applications. Whether you need to manage timestamps in a database, schedule tasks, log events, or handle time-sensitive operations in a global application, Chrono provides the tools you need. It also supports custom date and time formats, allowing you to work with both standard and non-standard representations of time. Chrono is widely adopted in the Rust ecosystem for any application that requires accurate and reliable date/time handling.

4.3 Algorithm for Selecting the Best Sampled Values

This thesis proposes a method for selecting the best analog/digital signal sent by multiple Merging Units. The signal is initially analog because it is acquired in that form from VT and CT, but the Merging Unit converts it into a digital signal following the IEC-61850-9-2 protocol. The device proposed in this work receives the digital signal, compares it with another one that's come from another Merging Unit. After this comparison, an algorithm implemented using a state machine selects which signal will be forwarded to the protection systems subscribing to these SV.

To achieve this, it was necessary to develop and implement the IEC 61850-9-2 protocol from the ground up. Since there is no available library for the RUST programming language, one had to be created. As a result, a publisher, a subscriber, and the core algorithm which is the main focus of this thesis were developed. This algorithm must

⁶https://crates.io/crates/env_logger

⁷<https://crates.io/crates/chrono>

receive information from two Merging Units and, after processing it, send the selected data to the protection system.

Figure 4.1 The components of the thesis are interconnected as follows: Two MUs send data to the algorithm. The algorithm then evaluates the information from both MUs, selects the most optimal data, and transmits it to the Protection Relay. This selection process ensures that the Protection Relay receives the best possible data based on the criteria defined by the algorithm.

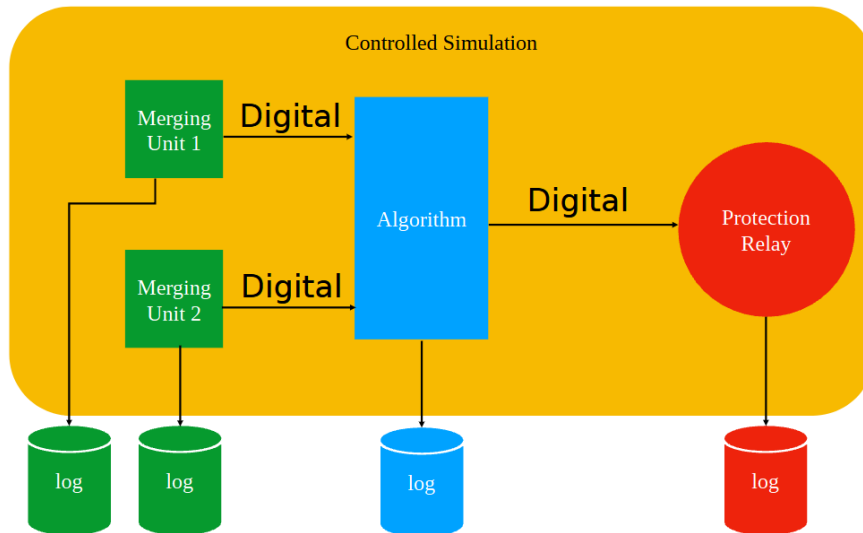


FIGURE 4.1: How the implementation was designed to work.

The development process began with the creation of the publisher, a software that emulates the operation of a Merging Unit. This software was built in accordance with the standard IEC 61850-9-2 for SV packets. Figure 4.2 how is constructed a Sampled Value Packet ⁸.

⁸https://www.typhoon-hil.com/documentation/typhoon-hil-software-manual/References/iec_61850_sampled_values_protocol.html

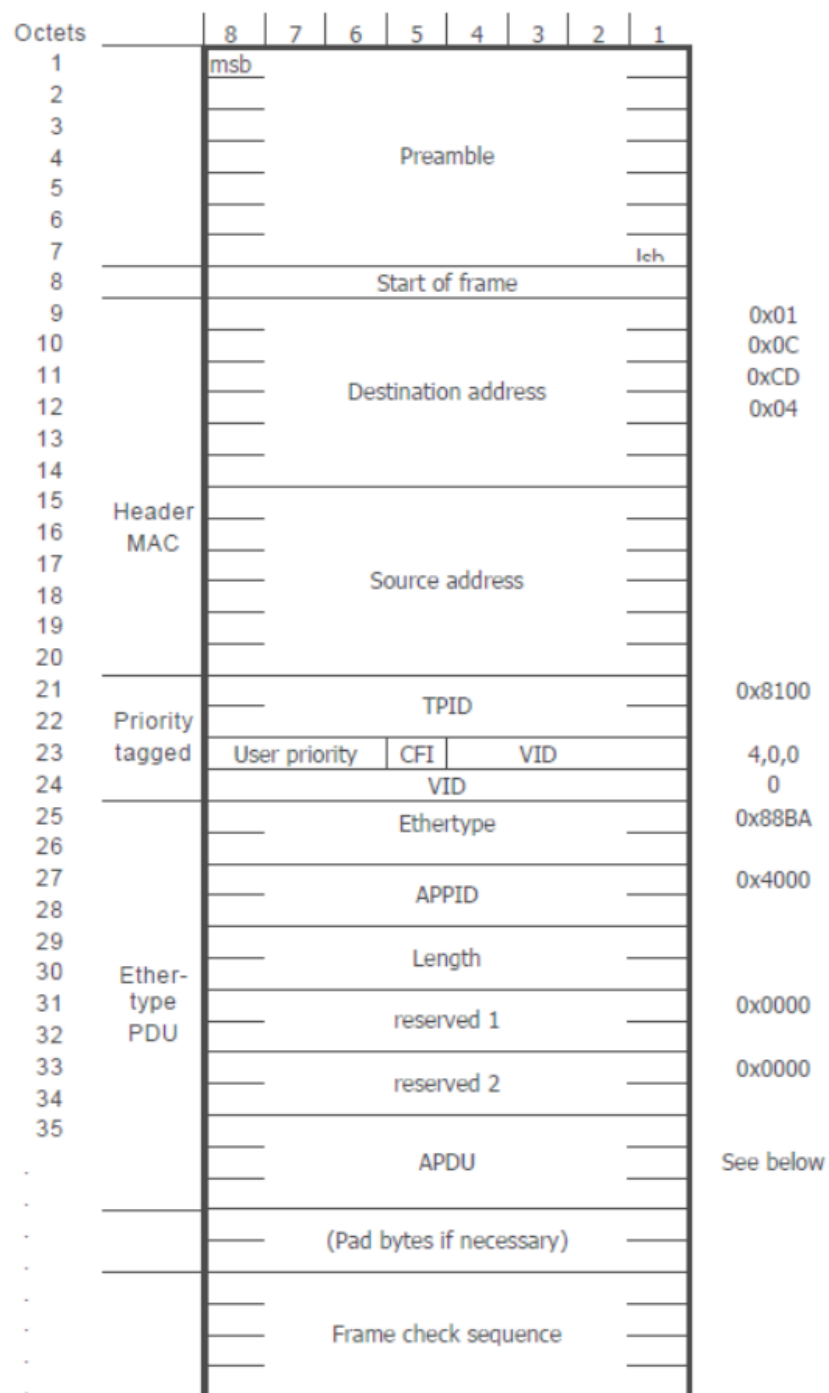


FIGURE 4.2: How is constructed a Sampled Values Packet following the standard IEC 61850-9-2 (Image credits: Typhoon HIL)

Once the packet structure was defined, a function was created to calculate the values to be sent along with the SVs. This function uses the current execution time to generate similar values between the two Merging Units.

We also implemented verification and validation of the packets using Cyclic Redundancy Check (CRC). The CRC is added to the SV packet during its creation, and on the subscriber side, it is verified to ensure the packet's validity.

The second phase of development focused on the subscriber. Upon receiving the packet over the Ethernet network, and in compliance with the IEC 61850-9-2 protocol standards, the packet is reconstructed, its integrity validated using CRC, and the relevant information extracted and logged. The subscriber device we developed acts as a protection relay, where the received information is converted back to an analog signal and applied to the relay's protection algorithms.

The third phase centered on developing the algorithm for selecting the best SV. This selection process involves analyzing the values received in the SV packets. To achieve this, we implemented an SV subscriber capable of retrieving data transmitted via this protocol, utilizing components from the earlier development stages. After receiving the data via Ethernet, the information is extracted, evaluated, and the best signal is chosen between the packets sent by Merging Unit 1 and Merging Unit 2. Once the best signal is identified, it is sent using the SV publisher, thus completing the development process aligned with the thesis's objectives.

The algorithm utilizes the Tokio crate, which provides a work-stealing task scheduler, allowing for concurrent and parallel processing. This enables the immediate retransmission of packets from the Merging Unit with the better signal, with the algorithm switching only when another Merging Unit provides a superior analog signal. This approach ensures real-time performance, essential for the required application.

This thesis specifically addresses scenarios involving two Merging Units. Although the case of more than two Merging Units was not considered, the algorithm can be adapted to handle such situations.

4.3.1 Results

Leading the development and implementation of a communication protocol like IEC 61850-9-2 presented a completely different challenge. It required me to ensure that any other equipment connected to the network could understand exactly what was being sent. This involved understanding how operating systems handle network packets, the various headers that are added to ensure the information is properly routed and delivered to the correct destination, and how to assemble SV packets. The packets had to be sent in a way that the receiving application could correctly reassemble and interpret the data after it had been converted into bytes. This process required not only receiving and converting the bytes back into usable information within the IEC 61850-9-2 protocol but also ensuring that the destination equipment could understand the payload. Furthermore, it was critical to verify that the packet was intact and suitable for content analysis, while also maintaining synchronization between the two applications. This was particularly important given that the information needs to be transmitted every 250 microseconds, making network latency a critical factor.

The results obtained after all phases of development were satisfactory, considering the existing conditions. We used the Network Time Protocol (NTP) as the master clock, which provides a precision of 1 millisecond. However, achieving 100% accuracy in timing was challenging because the protocol itself has a precision that exceeds the 250-microsecond interval at which we were transmitting the SV packets. Despite this limitation, the tests yielded values that were close to what was expected, demonstrating the feasibility of the models used. The ability to achieve such precision, even within these constraints, underscored the robustness and potential of the developed solution.

This experience not only deepened my technical understanding but also highlighted the complexities involved in real-time data transmission. It provided valuable insights into the challenges of ensuring data integrity, synchronization, and performance in real-time critical systems, where even the slightest delay or error can have significant consequences. content...

Chapter 5

Implementation

This chapter focuses on the development of the merging unit (publisher), the protection relay (subscriber), and algorithm essential to this project. It begins with Section 5.1, which explains the structure of SVs, laying the foundation for the algorithm's operation. Section 5.2 details the development of a publisher for IEC 61850-9-2-SV, covering data structuring, core function implementation, and testing through simulated signals. Section 5.3 addresses the development of a subscriber, highlighting the reuse of structures, data reception, error handling, and final implementation. The chapter also provides detailed insights into key portions of the code and the structures involved, particularly focusing on the state machine implemented to select the best sample of the analog signal. Finally, Section 5.4 discusses the overall development of the algorithm, integrating the components into a cohesive system and identifying the essential steps needed to advance the project. Initially, the path forward wasn't always clear, but as development progressed, the necessary methods and solutions were uncovered to ensure the successful completion of the project.

5.1 Structure of Sampled Values

The IEC 61850-9-2 Sampled Values protocol operates based on the Ethernet standard, meaning the packet structure must follow that of Ethernet packets. As such, we have the preamble, destination MAC address, source MAC address, Ethertype, data, and FCS. However, since it's a SV packet, there is an additional field that isn't always present in all Ethernet standard packets: the Priority Tagging VLAN ID. This field must be included in the SV packet.

These elements are divided into the header, payload, and checksum. The header includes the Destination MAC address, Source MAC address, Priority Tagging VLAN ID, and Ethertype. The payload contains the Sampled Value Protocol Data Unit (SVPDU), which itself consists of the APPID, length, Reserved 1, Reserved 2, and the APDU. The APDU is made up of the savPDU, noASDU, SeqASDU, and ASDU, and within the ASDU, we have fields such as svID, smpCnt, confRev, smpSynch, SeqData, and the data. Finally, we have the FCS (Frame Check Sequence), which in this case uses CRC (Cyclic Redundancy Check). This ensures the frame is validated and the information is accurate.

Figure 5.1 Below in the figure has how it is compound the sampled values packets. ¹.

¹<https://www.mdpi.com/1996-1073/12/19/3731>

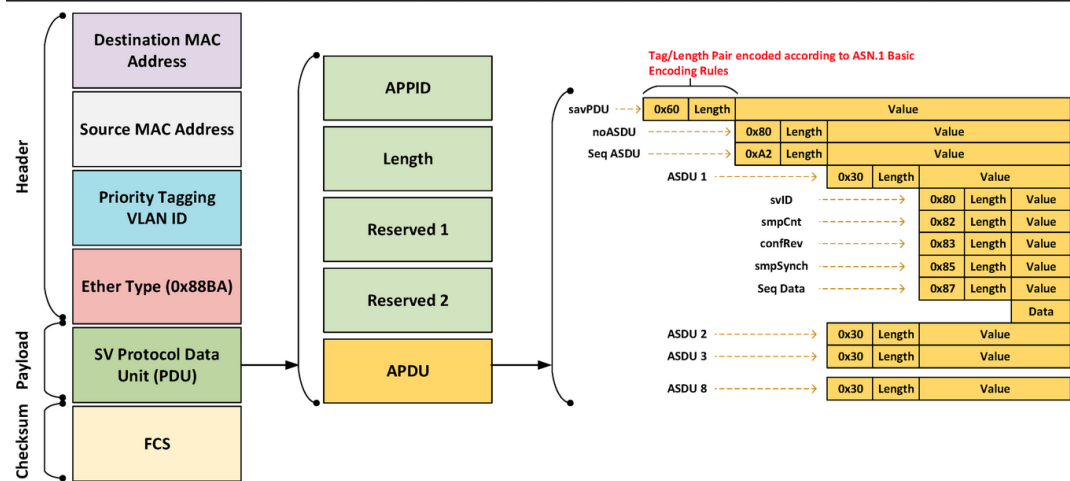


FIGURE 5.1: Sampled Value packets fields. (Image credits: MDPI)

Following the recommendations of UCA International Users Group 2024, the description is well documented in Zhao (2012, Subsection 4.2), which explains this in detail.

Figure 5.2 Here has a representation of all the field until the values, and all the layers of the packet. UCA International Users Group 2024

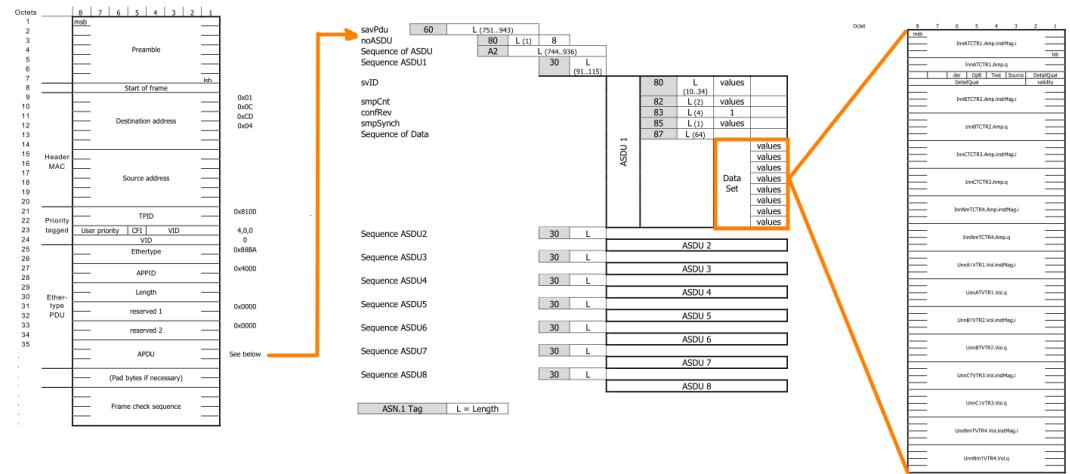


FIGURE 5.2: Sampled Value packets fields. (Image credits: UCA International)

5.2 Development of a Publisher of IEC 61850-9-2-SV

The development of the publisher is a critical component in the implementation of the IEC 61850-9-2 Sampled Values communication standard. This section outlines the structured approach taken to build the publisher, focusing on the creation of key data structures (structs) and the implementation of essential functions that enable the generation and transmission of SV packets.

5.2.1 Structuring the Data: Defining Rust Structs

The process begins with defining the necessary structs. Rust, known for its strong emphasis on safety and concurrency, offers a well-organized way to build and manage complex data structures. This allows for clear and readable code, where each step of the data flow is defined in a sequence that is easy to understand and maintain.

The primary structs used in this project are designed to mirror the components of an Ethernet frame, as required by the IEC 61850-9-2 standard. These structs are nested to represent the hierarchy of the data, from the Ethernet frame down to the individual data points in the SV payload.

```

1  pub struct EthernetFrame
2  {
3      pub destination:    [u8; 6],
4      pub source:         [u8; 6],
5      pub tpid:           u16,
6      pub tci:            u16,
7      pub ethertype:      u16,
8      pub payload:        SvPDU,
9      pub fcs:            [u8; 4],
10 }
11
12 pub struct SvPDU
13 {
14     pub appid:           [u8; 2],
15     pub length:          [u8; 2],
16     pub reserved1:       [u8; 2],
17     pub reserved2:       [u8; 2],
18     pub apdu: SmvData,
19 }
20
21 pub struct SmvData
22 {
23     pub sav_pdu_asn:     [u8; 2],
24     pub no_asdu_asn:     [u8; 2],
25     pub no_asdu:         u8,
26     pub seq_asdu_asn:    [u8; 2],
27     pub asdu_asn:        [u8; 2],
28     pub sv_id_asn:       [u8; 2],
29     pub sv_id:           [u32; 1],
30     pub smp_cnt_asn:     [u8; 2],
31     pub smp_cnt:         [u16; 1],
32     pub conf_rev_asn:    [u8; 2],
33     pub conf_rev:        [u32; 1],
34     pub smp_synch_asn:   [u8; 2],
35     pub smp_synch:       u8,
36     pub seq_data:        [u8; 2],
37     pub logical_node: LogicalNode,
38 }
39
40 pub struct LogicalNode
41 {
42     pub i_a:             [i32; 1],
43     pub q_ia:            [u32; 1],
44     pub i_b:             [i32; 1],
45     pub q_ib:            [u32; 1],
46     pub i_c:             [i32; 1],
47     pub q_ic:            [u32; 1],

```

```

48     pub i_n:      [i32; 1],
49     pub q_in:     [u32; 1],
50     pub v_a:      [i32; 1],
51     pub q_va:     [u32; 1],
52     pub v_b:      [i32; 1],
53     pub q_vb:     [u32; 1],
54     pub v_c:      [i32; 1],
55     pub q_vc:     [u32; 1],
56     pub v_n:      [i32; 1],
57     pub q_vn:     [u32; 1],
58 }

```

LISTING 5.1: Structs added

These structs allow for a comprehensive representation of the Ethernet frame and the SV data contained within, ensuring that each element of the SV packet is accurately captured and can be easily manipulated during transmission.

5.2.2 Implementing the Core Functions

Once the data structures are in place, the next step is to implement the functions that will operate on these structs. Rust uses the 'impl' keyword to define methods for structs, allowing for the creation of constructors, data manipulation functions, and other essential operations.

For example, the implementation of a constructor for the 'EthernetFrame' struct might look like this:

```

1  / Implementation of functions regarding EthernetFrame struct
2  impl EthernetFrame {
3      pub fn new(destination: [u8; 6], source: [u8; 6], tpid: u16, tci: u16,
4          ethertype: u16, payload: SvPDU, fcs: [u8; 4]) -> Self {
5          Self {
6              destination,
7              source,
8              tpid,
9              tci,
10             ethertype,
11             payload,
12             fcs,
13         }
14     }

```

LISTING 5.2: How to implement an impl for the struct

This function allows for the creation of a new EthernetFrame instance, ensuring that all necessary fields are initialized correctly.

5.2.3 Simulating an Electrical Grid Signal

A key functionality of the publisher is to simulate the sinusoidal signal of an electrical grid. This simulation is essential for generating realistic SV packets that can be used to test and validate the SV communication system.

To achieve this, the current time is used as an input to calculate the voltage and current values, with predefined amplitudes representing the electrical parameters. This simulation is implemented in the following function:

```

1  pub fn cal_current_phase_b ()-> [i32;1]
2  {
3      let now = Local::now();
4      let t: f32 = now.timestamp_subsec_nanos() as f32 / 1_000_000_000.0;
5      let phase_degrees: f32 = 120.0; // Example phase in degrees
6      let phase_radians: f32 = phase_degrees * PI / 180.0; // Convert
7      // phase to radians
8      let omega: f32 = 2.0 * PI * FREQUENCY;
9      let amplitude: f32 = AMPLITUDE_CURRENT * ((omega * t + phase_radians
10     ).sin());
11     [amplitude as i32;1]

```

LISTING 5.3: How to calculate the value of the SV's

This function calculates the current value for phase B at a given moment, using the system's local time to simulate the progression of the sinusoidal wave. The result is an array containing the current value, which can then be included in the SV packet.

5.2.4 Introducing Invalid Samples for Testing

To fully test the algorithm's ability to handle real-world scenarios, it was necessary to introduce invalid samples. This was accomplished by altering the quality of certain samples within the SV packets, making them invalid. The publisher was enhanced with a feature that allows these quality changes, enabling the testing of how well the algorithm can identify and respond to invalid data.

```

1  if increment > 50 \&\& increment < 100
2  {
3      // Implement Bad Quality to the samples
4      // The value of 0 is good quality
5      // The value of 1 and 2 is invalid
6      //The value of 3 it is questionable
7      sv_packet.payload.apdu.logical_node.q_ia[0] = sv_packet.payload.apdu
8      .logical_node.q_ia[0].wrapping_add(1);
9  }

```

LISTING 5.4: How to calculate the value of the SV's

This method directly modifies the 'sv_packet.payload.apdu.logical_node.q_ia' field, effectively marking the sample as invalid. This invalid data can then be used to test the robustness of the SV communication and processing algorithm.

5.2.5 Finalizing the Publisher

With the basic structure, implementation, and testing features in place, the development of the publisher was completed. The final publisher is capable of generating and transmitting SV packets, simulating electrical grid signals, and introducing invalid data for testing purposes. These features are critical to the overall success of the thesis, as they enable comprehensive testing and validation of the IEC 61850-9-2 SV standard.

5.3 Development of a Subscriber of IEC 61850-9-2-SV

The development process for the subscriber followed a similar structured approach as that of the publisher. Having already established the necessary structs during the publisher's development, the focus for the subscriber shifted towards receiving and processing the data transmitted by the publisher over the network.

In this context, the subscriber was designed to handle incoming Sampled Values (SV) packets, log the received data, and print the relevant information to the log. This approach not only facilitated real-time monitoring of the transmitted SV data but also provided a foundation for verifying the integrity and accuracy of the data exchange between the publisher and subscriber.

5.3.1 Structs Reused in the Subscriber

Given that the subscriber's primary role is to interpret the data sent by the publisher, the same set of structs, including 'EthernetFrame', 'SvPDU', 'SmvData', and 'LogicalNode', were reused. These structs allowed the subscriber to decode the incoming Ethernet frames and extract the necessary information from the SV packets.

```
1  pub struct EthernetFrame {  
2      pub destination: [u8; 6],  
3      pub source: [u8; 6],  
4      pub tpid: u16,  
5      pub tci: u16,  
6      pub ethertype: u16,  
7      pub payload: SvPDU,  
8      pub fcs: [u8; 4],  
9  }  
10  
11  // Other structs reused as shown in the publisher's code...  
12
```

LISTING 5.5: EthernetFrame struct.

5.3.2 Implementation of Data Reception and Logging

The implementation phase involved creating functions to capture the network packets, parse them into the appropriate struct fields, and log the data for analysis. The impl blocks provided a seamless way to define these methods, ensuring that the subscriber could efficiently process the data.

5.3.3 Error Handling and Invalid Data Processing

An essential part of the subscriber's functionality involved handling errors and invalid data. Similar to the publisher, where invalid samples were introduced to test the algorithm, the subscriber needed to identify and appropriately respond to these invalid samples. This was achieved by checking the quality of the received data and ensuring that any invalid samples were flagged and processed correctly.

5.3.4 Finalizing the Subscriber

By incorporating robust data reception, validation, and logging mechanisms, the subscriber was completed with the essential features required to support the overall thesis objectives. The subscriber was now fully equipped to interact with the publisher, process the received SV packets, and handle any errors or invalid data that might arise during transmission. This setup provided a solid foundation for testing and verifying the performance of the implemented communication protocol.

5.4 Development of the Algorithm

The development of the algorithm hinges on a deep understanding of both the publisher and subscriber functions. The aim is to create an algorithm capable of selecting the optimal samples from two independent devices that measure the same electrical quantity. This involves transmitting these measurements via a protocol, decompressing the data, extracting the necessary values, evaluating them, and ultimately selecting the best sample. All of this must be accomplished within a timeframe that ensures the SVs reach the protection devices without delay each SV being transmitted every 250 microseconds.

The algorithm is triggered upon the reception of an SV from one of the merging units. Once received, the SV is processed and evaluated to determine whether it is valid, invalid, or questionable. If the sample is valid, its values are extracted for comparison with those from the other merging unit. In the case of an invalid or questionable sample, it is excluded from the value acquisition process. However, the algorithm keeps track of the number of invalid samples, which is one of the criteria used to decide whether to switch the SVs being sent to the protection relays.

For valid samples, a comparison is made on a sample-by-sample basis to ensure the best result. If the error does not exceed 25%, the current SV is maintained; however, if the error surpasses 25%, the SV being sent to the protection relays is switched. A state machine was implemented to make the decision on which SV to send to the protection devices. Although the system receives values from two merging units, only one of the two received SVs is transmitted.

The state machine processes all incoming SV frames according to the logic outlined below.

Figure 5.3 Here has a representation of the state machines it was implemented to make a decision which SV's is going to send.

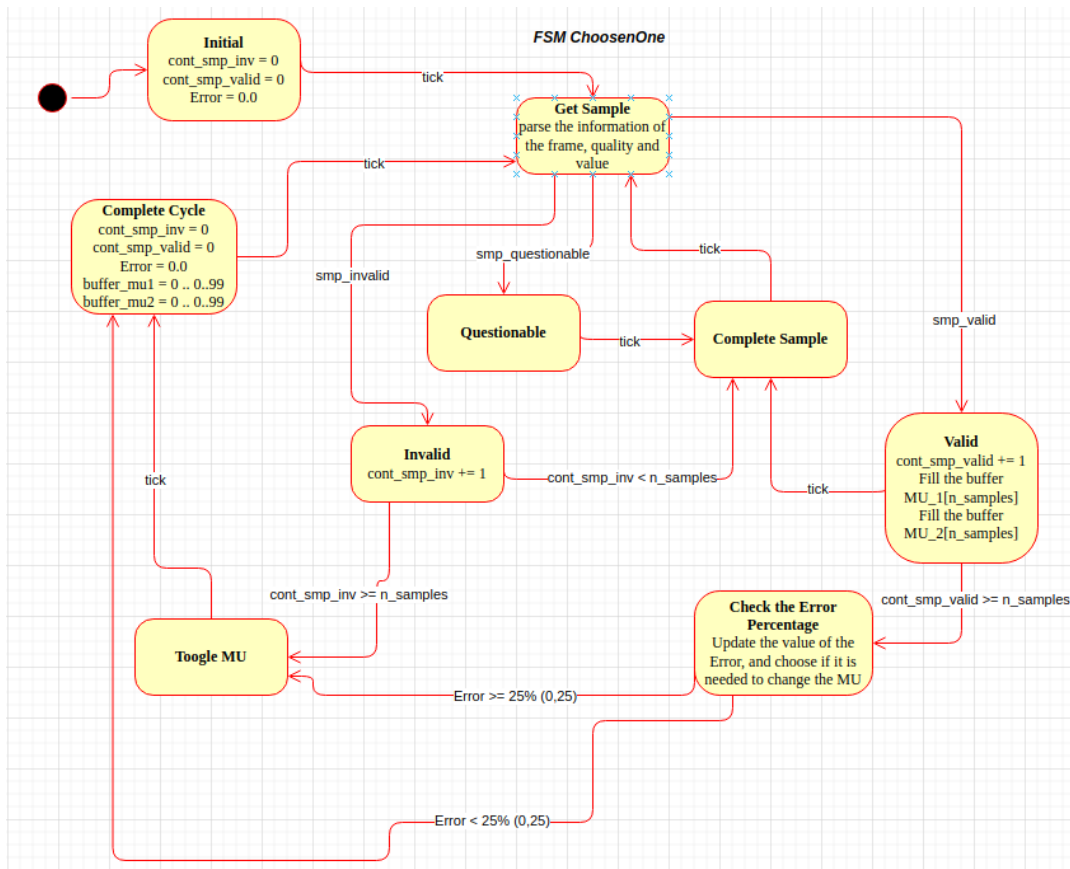


FIGURE 5.3: State Machine of Decision Make.

The state machine was implemented in Rust, utilizing two mechanisms for state transitions: events and ticks. Events are specific actions that must occur to progress through the state machine, while ticks represent units of time. When the stipulated time elapses and the state requires only a tick to advance, the state machine proceeds to the next state, just as it does in response to events.

```

1  // Define the state machine
2  struct FrameProcessor {
3      state: State,
4      cont_smp_inv: u32,
5      cont_smp_valid_sv_id_1: u32,
6      cont_smp_valid_sv_id_2: u32,
7      error_percentage: f32,
8      buffer_mu1: [[i32; N_SAMPLES as usize]; 8], // buffer MU 1 current A
9      buffer_mu2: [[i32; N_SAMPLES as usize]; 8], // buffer MU 2 current A
10     toggle_mu: bool,
11 }
12 impl FrameProcessor {
13     fn new() -> Self {
14         Self {
15             state: State::Initial,
16             cont_smp_inv: 0, // Initialize cont_invalid
17             cont_smp_valid_sv_id_1: 0,
18             cont_smp_valid_sv_id_2: 0,
19             error_percentage: 0.0,

```



```

20     buffer_mu1: [[0 ; N_SAMPLES as usize]; 8],
21     buffer_mu2: [[0 ; N_SAMPLES as usize]; 8],
22     toggle_mu: false,
23
24 }
25 }
26

```

LISTING 5.6: State Machine struct.

Figure 5.4 This diagram represents the connection between the two Merging Units (MUs) and the algorithm. After the algorithm selects the optimal sample, it transmits the selected data to the IED.

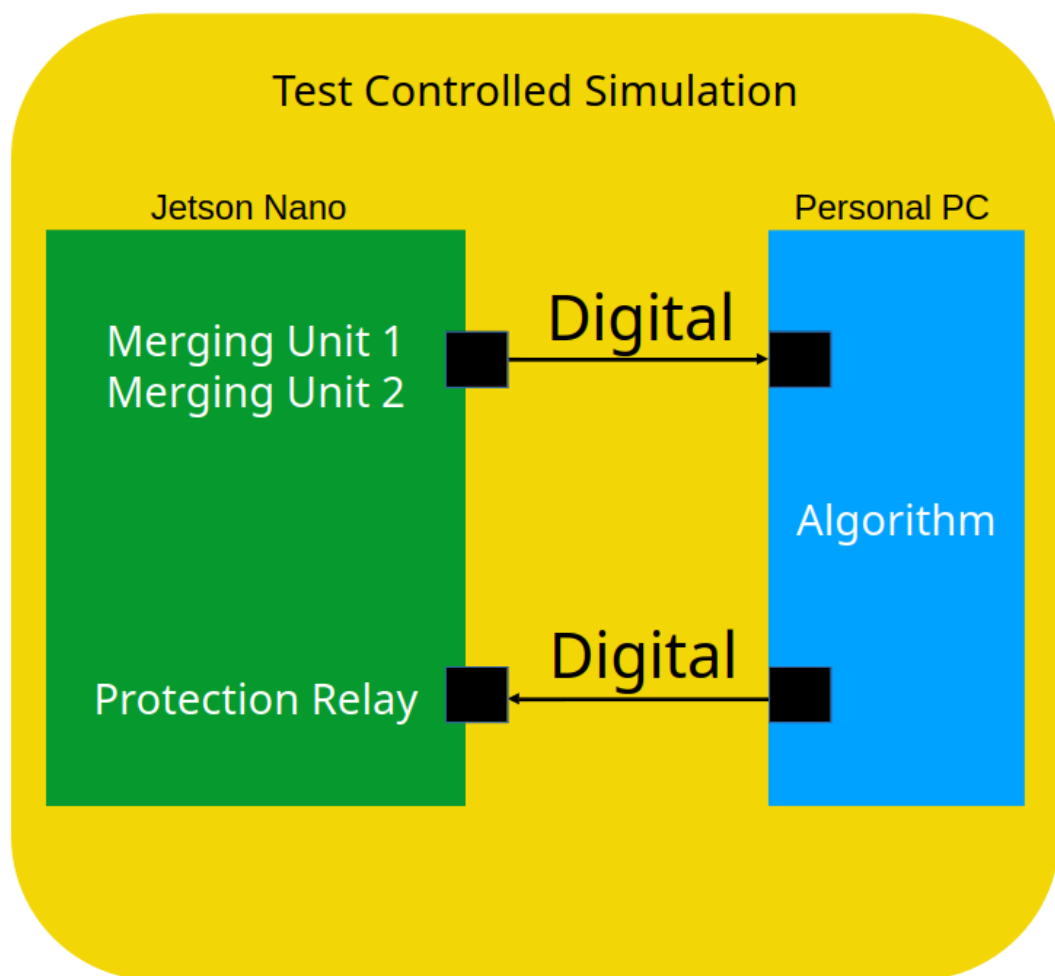


FIGURE 5.4: How is connected the two simulators of SV's to exchange the information.

All information regarding the development is available on GitHub, along with additional resources in the following location: https://github.com/evertton-oriente/IEC61850_9_2_SV/tree/main

These platforms collectively provide comprehensive access to the project's documentation, code, and related materials.

Chapter 6

Tests and Evaluation

This chapter outlines the testing and evaluation processes crucial to achieving the project's objectives. It begins with Section 6.1, which focuses on the tests conducted on the merging unit (publisher of IEC 61850-9-2-SV, ensuring it performs accurately under various conditions. Section 6.2 details the testing of the subscriber, examining its ability to receive and process the data correctly. Finally, Section 6.3 evaluates the algorithm, particularly the state machine implemented to select the best sample of the analog signal. Throughout this chapter, rigorous testing approaches are emphasized, highlighting the steps taken to validate the algorithm's performance and secure the project's overall success. Initially, the testing path wasn't entirely clear, but as it progressed, the necessary methods and solutions were identified to ensure the algorithm's successful validation.

6.1 Test of Publisher of IEC 61850-9-2-SV

The testing phase for the publisher was critical to ensure its proper functionality, confirm that the data structures were correctly constructed, and verify that the checksum maintained packet integrity, all in strict compliance with the IEC 61850 standard.

Initial tests focused on validating that the publisher was generating Sampled Value (SV) packets accurately, with values consistent with the configured parameters. It was equally important to verify that the subscriber was correctly receiving and processing these transmitted packets. Wireshark software was extensively employed to capture and analyze the packets, ensuring that all content was transmitted as expected. Throughout development, several issues emerged, but each was methodically resolved to ensure the publisher's reliable performance and seamless communication.

Figure 6.1 Below is a Wireshark capture that illustrates the integrity of the acquired packets and their identification as SV packets.

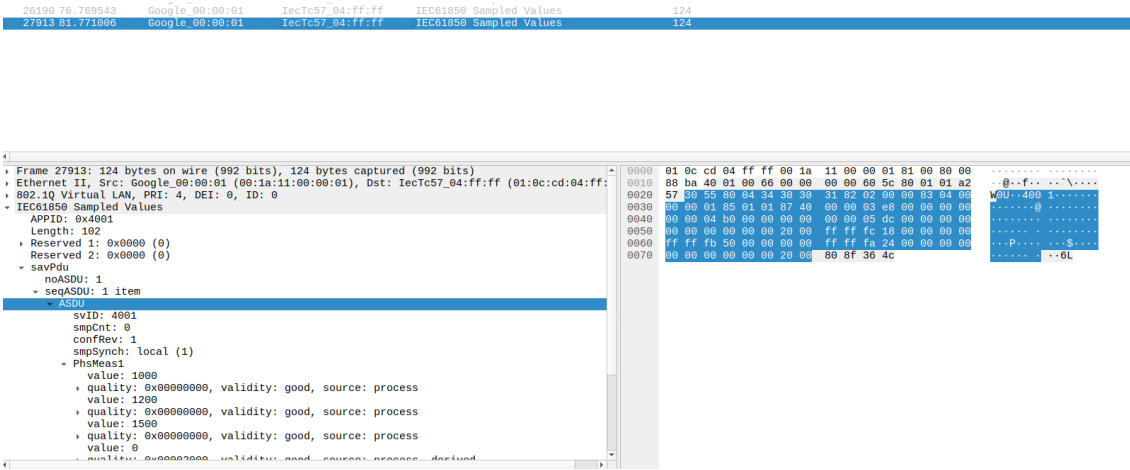


FIGURE 6.1: Wireshark view of the SV packets.

Figure 6.2 The packets are sequentially numbered, ensuring proper identification. The following image demonstrates that the frames are correctly ordered, the field to check it is sample counter as smpcnt.

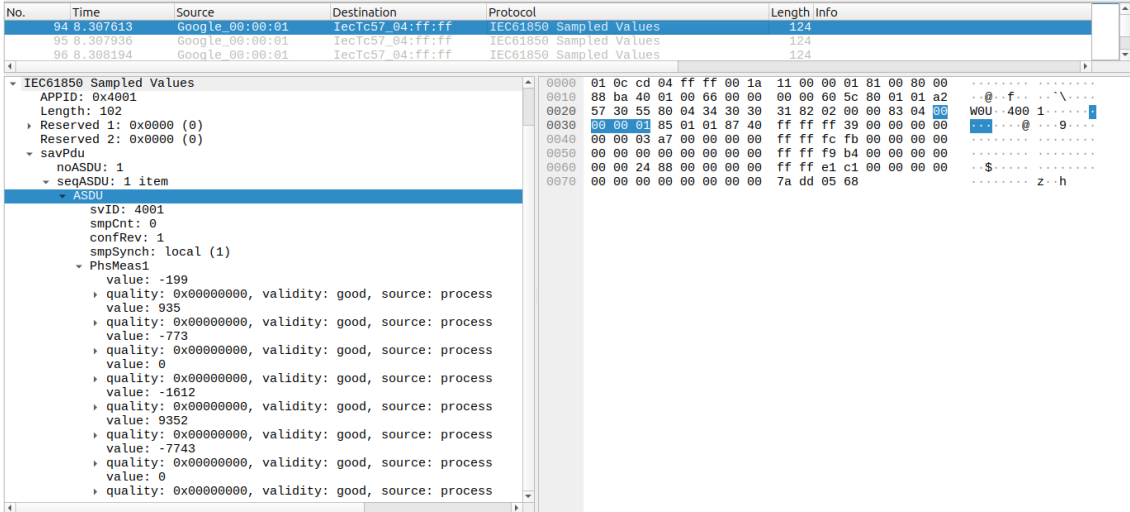


FIGURE 6.2: SV packet with sample counter with value 0.

No.	Time	Source	Destination	Protocol	Length	Info
94	8.307613	Google-00:00:01	IecIc57_04:ff:ff	IEC61850 Sampled Values	124	
95	8.307936	Google-00:00:01	IecIc57_04:ff:ff	IEC61850 Sampled Values	124	
96	8.308194	Google-00:00:01	IecIc57_04:ff:ff	IEC61850 Sampled Values	124	

<div>IEC61850 Sampled Values</div> <div>APPID: 0x4001</div> <div>Length: 102</div> <div>Reserved 1: 0x0000 (0)</div> <div>Reserved 2: 0x0000 (0)</div> <div>savPdu <div>noASDU: 1</div> <div>seqASDU: 1 item <div>ASDU <div>svID: 4001</div> <div>smpCnt: 1</div> <div>confRev: 1</div> <div>smpSynch: local (1)</div> <div>PhsMeas1 <div>value: -56</div> <div>quality: 0x00000000, validity: good, source: process</div> <div>value: 892</div> <div>quality: 0x00000000, validity: good, source: process</div> <div>value: -837</div> <div>quality: 0x00000000, validity: good, source: process</div> <div>value: 0</div> <div>quality: 0x00000000, validity: good, source: process</div> <div>value: -550</div> <div>quality: 0x00000000, validity: good, source: process</div> <div>value: 8921</div> <div>quality: 0x00000000, validity: good, source: process</div> <div>value: -8373</div> <div>quality: 0x00000000, validity: good, source: process</div> <div>value: 0</div> <div>quality: 0x00000000, validity: good, source: process</div> </div> </div> </div> </div>	<div>0000 01 0c cd 04 ff ff 00 1a 11 00 00 01 81 00 80 00</div> <div>0010 88 ba 40 01 00 66 00 00 00 00 00 5c 80 01 01 a2</div> <div>0020 57 30 55 80 04 34 30 30 31 82 02 00 01 83 04 00</div> <div>0030 90 00 01 85 01 01 87 40 ff ff ff c8 00 00 00 00</div> <div>0040 90 00 03 7c 00 00 00 00 ff ff fc bb 00 00 00 00</div> <div>0050 90 00 00 00 00 00 00 ff ff fd da 00 00 00 00</div> <div>0060 90 00 22 49 00 00 00 00 ff ff df 4b 00 00 00 00</div> <div>0070 00 00 00 00 00 00 00 00 77 e8 e7 11</div>	<div>.....@..f..\\.....</div> <div>W0U..400 1.....</div> <div>.....@.....</div> <div>.....T.....</div> <div>.....K.....</div> <div>.....W.....</div>
---	--	--

FIGURE 6.3: SV packet with sample counter with value 1.

No.	Time	Source	Destination	Protocol	Length	Info
94	8.307613	Google-00:00:01	IecIc57_04:ff:ff	IEC61850 Sampled Values	124	
95	8.307936	Google-00:00:01	IecIc57_04:ff:ff	IEC61850 Sampled Values	124	
96	8.308194	Google-00:00:01	IecIc57_04:ff:ff	IEC61850 Sampled Values	124	

<div>IEC61850 Sampled Values</div> <div>APPID: 0x4001</div> <div>Length: 102</div> <div>Reserved 1: 0x0000 (0)</div> <div>Reserved 2: 0x0000 (0)</div> <div>savPdu <div>noASDU: 1</div> <div>seqASDU: 1 item <div>ASDU <div>svID: 4001</div> <div>smpCnt: 2</div> <div>confRev: 1</div> <div>smpSynch: local (1)</div> <div>PhsMeas1 <div>value: 26</div> <div>quality: 0x00000000, validity: good, source: process</div> <div>value: 852</div> <div>quality: 0x00000000, validity: good, source: process</div> <div>value: -879</div> <div>quality: 0x00000000, validity: good, source: process</div> <div>value: 0</div> <div>quality: 0x00000000, validity: good, source: process</div> <div>value: 275</div> <div>quality: 0x00000000, validity: good, source: process</div> <div>value: 8518</div> <div>quality: 0x00000000, validity: good, source: process</div> <div>value: -8795</div> <div>quality: 0x00000000, validity: good, source: process</div> <div>value: 0</div> <div>quality: 0x00000000, validity: good, source: process</div> </div> </div> </div> </div>	<div>0000 01 0c cd 04 ff ff 00 1a 11 00 00 01 81 00 80 00</div> <div>0010 88 ba 40 01 00 66 00 00 00 00 00 5c 80 01 01 a2</div> <div>0020 57 30 55 80 04 34 30 30 31 82 02 00 02 83 04 00</div> <div>0030 90 00 01 85 01 01 87 40 90 00 00 1a 00 00 00 00</div> <div>0040 90 00 03 7c 00 00 00 00 ff ff fc 31 00 00 00 00</div> <div>0050 90 00 00 00 00 00 00 00 90 00 01 13 00 00 00 00</div> <div>0060 90 00 21 46 00 00 00 00 ff ff dd a5 00 00 00 00</div> <div>0070 00 00 00 00 00 00 00 00 b6 a1 80 63</div>	<div>.....@..f..\\.....</div> <div>W0U..400 1.....</div> <div>.....@.....</div> <div>.....T.....</div> <div>.....!F.....</div> <div>.....C.....</div>
---	---	---

FIGURE 6.4: SV packet with sample counter with value 2.

Figure 6.5 Here, we showcase samples marked with bad quality, which were used to test the handling of invalid samples and trigger a switch to alternate samples received from another merging unit. The following images provide examples of the transmitted packets.

No.	Time	Source	Destination	Protocol	Length	Info
1	0.000000	Google_00:00:01	IecTc57_04:ff:ff	IEC61850 Sampled Values	124	
2	1.001654	Google_00:00:01	IecTc57_04:ff:ff	IEC61850 Sampled Values	124	
7	2.002132	Google_00:00:01	IecTc57_04:ff:ff	IEC61850 Sampled Values	124	
12	3.003635	Google_00:00:01	IecTc57_04:ff:ff	IEC61850 Sampled Values	124	

<p>Frame 1: 124 bytes on wire (992 bits), 124 bytes captured (992 bits)</p> <p>Ethernet II, Src: Google_00:00:01 (00:1a:11:00:00:01), Dst: IecTc57_04:ff:ff (01:0c:cd:04:ff:ff)</p> <p>802.1Q Virtual LAN, PRI: 4, DEI: 0, ID: 0</p> <p>IEC61850 Sampled Values</p> <p>APPID: 0x4001</p> <p>Length: 102</p> <p>Reserved 1: 0x0000 (0)</p> <p>Reserved 2: 0x0000 (0)</p> <p>savPdu</p> <p>noASDU: 1</p> <p>seqASDU: 1 item</p> <p>ASDU</p> <p>svID: 4001</p> <p>smcCnt: 114</p> <p>confRev: 1</p> <p>smcSynch: local (1)</p> <p>PhsMeas1</p> <p>value: 712</p> <p>quality: 0x00000001, validity: invalid (backwards compatible), source: process</p> <p>value: 245</p> <p>quality: 0x00000000, validity: good, source: process</p> <p>value: -962</p> <p>quality: 0x00000000, validity: good, source: process</p> <p>value: 0</p> <p>quality: 0x00002000, validity: good, source: process, derived</p> <p>value: 7170</p> <p>quality: 0x00000000, validity: good, source: process</p> <p>value: 2449</p> <p>quality: 0x00000000, validity: good, source: process</p> <p>value: -9620</p>	<p>0000 01 0c cd 04 ff ff 00 1a 11 00 00 01 81 00 80 00</p> <p>0010 88 ba 40 01 00 00 00 00 00 00 00 5c 80 01 01 02</p> <p>0020 57 30 55 80 04 34 30 30 31 82 02 00 72 83 04 00</p> <p>0030 00 00 01 85 01 01 87 40 00 00 02 c8 00 00 00 01</p> <p>0040 00 00 00 f5 00 00 00 00 ff ff fc 3e 00 00 00 00</p> <p>0050 00 00 00 00 00 20 00 00 00 1c 02 00 00 00 00</p> <p>0060 00 00 00 91 00 00 00 00 ff ff da 6c 00 00 00 00</p> <p>0070 00 00 00 00 00 20 00 37 c6 ab 7e</p>
---	---

FIGURE 6.5: SV packet with bad quality sample counter with value 114.

No.	Time	Source	Destination	Protocol	Length	Info
1	0.000000	Google_00:00:01	IecTc57_04:ff:ff	IEC61850 Sampled Values	124	
2	1.001654	Google_00:00:01	IecTc57_04:ff:ff	IEC61850 Sampled Values	124	
7	2.002132	Google_00:00:01	IecTc57_04:ff:ff	IEC61850 Sampled Values	124	
12	3.003635	Google_00:00:01	IecTc57_04:ff:ff	IEC61850 Sampled Values	124	

<p>Frame 2: 124 bytes on wire (992 bits), 124 bytes captured (992 bits)</p> <p>Ethernet II, Src: Google_00:00:01 (00:1a:11:00:00:01), Dst: IecTc57_04:ff:ff (01:0c:cd:04:ff:ff)</p> <p>802.1Q Virtual LAN, PRI: 4, DEI: 0, ID: 0</p> <p>IEC61850 Sampled Values</p> <p>APPID: 0x4001</p> <p>Length: 102</p> <p>Reserved 1: 0x0000 (0)</p> <p>Reserved 2: 0x0000 (0)</p> <p>savPdu</p> <p>noASDU: 1</p> <p>seqASDU: 1 item</p> <p>ASDU</p> <p>svID: 4001</p> <p>smcCnt: 115</p> <p>confRev: 1</p> <p>smcSynch: local (1)</p> <p>PhsMeas1</p> <p>value: 966</p> <p>quality: 0x00000001, validity: invalid (backwards compatible), source: process</p> <p>value: -268</p> <p>quality: 0x00000000, validity: good, source: process</p> <p>value: -699</p> <p>quality: 0x00000000, validity: good, source: process</p> <p>value: 0</p> <p>quality: 0x00002000, validity: good, source: process, derived</p> <p>value: 9685</p> <p>quality: 0x00000000, validity: good, source: process</p> <p>value: -2687</p> <p>quality: 0x00000000, validity: good, source: process</p> <p>value: -6997</p>	<p>0000 01 0c cd 04 ff ff 00 1a 11 00 00 01 81 00 80 00</p> <p>0010 88 ba 40 01 00 00 00 00 00 00 00 5c 80 01 01 02</p> <p>0020 57 30 55 80 04 34 30 30 31 82 02 00 73 83 04 00</p> <p>0030 00 00 01 85 01 01 87 40 00 00 03 c6 00 00 00 01</p> <p>0040 ff ff fe f4 00 00 00 00 ff ff fd 45 00 00 00 00</p> <p>0050 00 00 00 00 00 20 00 00 00 25 d5 00 00 00 00</p> <p>0060 ff ff f5 81 00 00 00 00 ff ff e4 ab 00 00 00 00</p> <p>0070 00 00 00 00 00 20 00 2d 43 ac 62</p>
---	---

FIGURE 6.6: SV packet with bad quality sample counter with value 115.

These comprehensive tests confirm the publisher's correct functionality, ensuring reliable and accurate information exchange between different devices. The three pictures above show a invalid in the field of quality of the samples, this means I have tested also the way through bad quality samples and ensure the algorithm change which Merging Unit is sending the SV packets, it is also possible to verify the sample counter to realize it is also in order the packets.

6.2 Test of Subscriber of IEC 61850-9-2-SV

The testing phase for the subscriber was essential to ensure it functioned correctly, accurately processed SV packets, and adhered to the IEC 61850 standard.

Initial tests focused on verifying that the subscriber could correctly receive and decode SV packets generated by the publisher. It was crucial to confirm that the subscriber subscribed to the data stream and processed the information as expected. Wireshark was

extensively used to monitor and analyze the packet flow, and despite several challenges, each issue was promptly addressed to ensure reliable performance and seamless integration with the publisher.

Throughout testing, both Wireshark and application logs were used to carefully analyze every byte sent and received. This thorough inspection allowed for quick detection of inconsistencies and corrections. Initially, testing on the same machine concealed a problem that became evident only when packets were transmitted across a network: the VLAN information in SV packets was stripped by the operating system when sent to another device. This behavior is normal, as the VLAN data is only necessary for routing but doesn't reach the application level. Understanding this behavior was crucial for addressing the issue and implementing a solution.

Once the core issues were resolved, testing confirmed the accurate exchange of data, ensuring each byte was correctly serialized and deserialized. This was vital since the state machine relies on precise data to make decisions. Any discrepancies would have caused failures or erratic behavior in the sample selection algorithm. The thorough testing guaranteed that the system operated as intended, free of errors.

Figure 6.7 Here, we have the wireshark sniffing the information at the subscriber side, and also one packet of the publisher and the subscriber side.

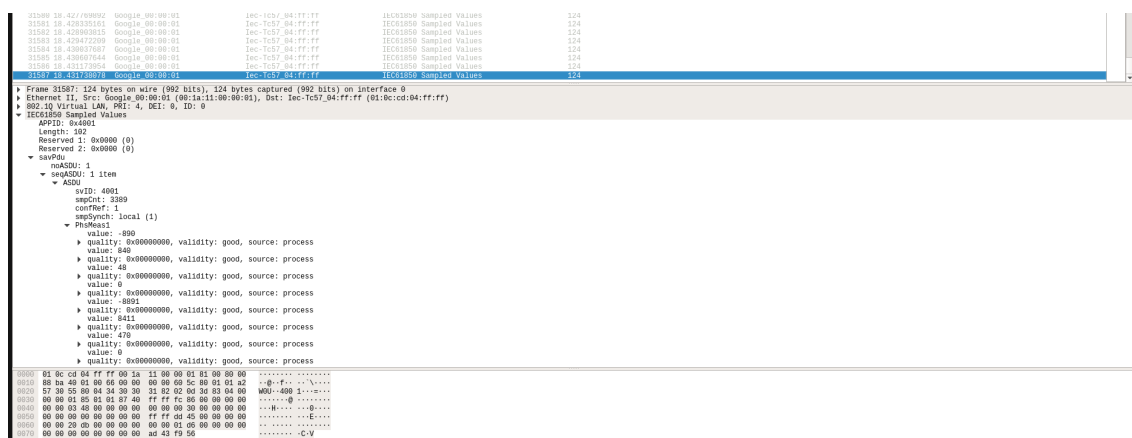


FIGURE 6.7: SV packet at subscriber side

Publisher

[2024-09-05T22:31:42Z INFO pub_je] The frame has been sended at time: 2024-09-05T23:31:42.583814787+01:00

[2024-09-05T22:31:42Z INFO pub_je] Message publish: [1, 12, 205, 4, 255, 255, 0, 26, 17, 0, 0, 1, 129, 0, 128, 0, 136, 186, 64, 1, 0, 102, 0, 0, 0, 0, 96, 92, 128, 1, 1, 162, 87, 48, 85, 128, 4, 52, 48, 48, 49, 130, 2, 5, 60, 131, 4, 0, 0, 0, 1, 133, 1, 1, 135, 64, 0, 0, 3, 128, 0, 0, 0, 0, 255, 255, 255, 191, 0, 0, 0, 0, 255, 255, 252, 194, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 35, 16, 0, 0, 0, 0, 255, 255, 253, 90, 0, 0, 0, 0, 255, 255, 223, 151, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 53, 61, 149, 73]

Subscriber

[2024-09-05T22:31:42Z INFO sub_je] The frame has been received at time: 2024-09-05T23:31:42.604614344+01:00

[2024-09-05T22:31:42Z INFO sub_je] Received Ethernet Frame: EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26, 17, 0, 0, 1], ethertype: 35002, payload: SyPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2: [0, 0], apdu: SrvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1], no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn: [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [1340], conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1], smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a: [896], q_ia: [0], i_b: [-65], q_ib: [0], i_c: [-830], q_ic: [0], i_n: [0], q_in: [0], v_a: [8976], q_ya: [0], v_b: [-678], q_vb: [0], v_c: [-8297], q_yc: [0], v_n: [0], q_yn: [0] } }, fcs: [53, 61, 149, 73] }

FIGURE 6.8: Information provided by Log of publisher and subscriber, the same packet in both equipment

Upon completing the tests, it was confirmed that the data sent by the publisher was correctly received and properly serialized by the subscriber, from the destination fields to the Frame Check Sequence (FCS).

However, an issue was identified during tests conducted on the same machine, where additional VLAN packets were processed by the subscriber. This occurred because, when running on the same system, the operating system does not discard VLAN data, as the packets don't actually leave the machine. As a result, the data serialization became incorrect when the system was moved to a real-world test environment involving two separate devices communicating through network switches. In this scenario, the operating system on each device appropriately "consumes" the VLAN data, which is not needed beyond the network transmission phase.

After thorough investigation, it was determined that the VLAN packets should indeed be consumed by the operating system, as they are part of the lower layers in the OSI model. Recognizing this, we made the necessary adjustments to ensure proper data serialization when transferring packets across different devices in a networked environment, resolving the issue and ensuring reliable communication between publisher and subscriber.

6.3 Test of the Algorithm

This chapter outlines the testing of the code used by the algorithm and the evaluation process for achieving the project's objectives. It provides a detailed description of the testing approach, with an emphasis on the steps taken to rigorously validate the algorithm's performance. Throughout the process, the necessary methods and solutions were identified to ensure the successful validation of the algorithm and the overall project.

With the development and testing of both the publisher and subscriber complete, the testing of the algorithm could begin, knowing that both components were functioning as expected. The initial tests focused on correctly serializing data and acquiring the necessary information for the state machine to progress and make decisions. The publisher was configured to generate valid, invalid, and questionable samples, ensuring that all states of the state machine could be tested. This comprehensive testing approach allowed for the verification and validation of transitions through all states, ensuring proper functionality.

The first trials followed the normal flow of the algorithm, as represented in Figure 5.3. The state machine is initialized and waits to receive a sample, which can be one of three types: Valid, Invalid, or Questionable. Initially, tests were conducted with Valid samples.

Once a valid sample is acquired, the state transitions to the Valid state. Within this state, both the tick transition and the condition `cont_smp_valid >= n_samples` were tested. The state machine successfully transitioned to either the Complete Sample state or the Check the Error Percentage state. As the Complete Sample state processes all samples and returns to the Get Sample state, this scenario was tested multiple times and functioned correctly in all cases. This allowed us to move forward with testing the transitions related to the Check the Error Percentage state.

In the Check the Error Percentage state, the values in the buffer are evaluated. All values are summed, and a percentage is calculated. If this percentage exceeds 25%, the state transitions to Toggle MU; otherwise, it proceeds to Complete Cycle. Multiple tests with values above and below this threshold were performed, and the state machine behaved correctly in all cases. The buffer values and percentages were analyzed to confirm the application's calculations, and the decision-making process was verified through implemented logs, ensuring that all transitions were accurate.

In the Toggle MU state, the SV packets sent to the protection devices are switched. If packets from Merging Unit 1 were being sent, the system switches to Merging Unit 2, and vice versa.

In the Complete Cycle state, all values are reset to their initial states, preparing the system for the next evaluation, where it determines whether or not to switch Merging Units.

The Initial state is responsible for initializing all necessary variables to zero, ensuring the process starts correctly.

When dealing with Invalid samples, the process begins in the Get Sample state, similar to Valid samples. After the analysis confirms the sample is invalid, the state transitions to Invalid. If the number of invalid samples exceeds `n_samples`, the system moves to the Toggle MU state; otherwise, it transitions to Complete Sample.

Finally, for Questionable samples, the state machine simply waits for the tick and then transitions to Complete Sample. No additional handling is applied for questionable samples.

The following debug output captures the comprehensive testing of the state machine. This output provides a clear record of the testing process, illustrating how each message corresponds to various scenarios within the state machine. By tracing these messages,

one can see the meticulous examination of every possible state and transition, ensuring that all functionalities were thoroughly validated. Additionally, the debug information offers insights into the algorithm's performance, demonstrating its ability to respond accurately to different conditions. This rigorous testing process was essential for confirming the reliability and effectiveness of both the state machine and the algorithm. Look at the debug below.

```

1 debug git:(main) sudo RUST_LOG=info ./sub_with_fsm_iec wlp0s20f3
2 [2024-07-14T18:22:49Z INFO sub_with_fsm_iec] Listening on interface
  wlp0s20f3
3 [2024-07-14T18:22:49Z INFO sub_with_fsm_iec] Mu0 before evaluation
4 [2024-07-14T18:22:49Z INFO sub_with_fsm_iec] Mu0 after evaluation
5 [2024-07-14T18:22:49Z INFO sub_with_fsm_iec] Time of work of thread is:
  112.979418ms
6 [2024-07-14T18:22:49Z INFO sub_with_fsm_iec] Mu0 before evaluation
7 [2024-07-14T18:22:49Z INFO sub_with_fsm_iec] Mu0 after evaluation
8 [2024-07-14T18:22:49Z INFO sub_with_fsm_iec] Time of work of thread is:
  18.965microseconds
9 [2024-07-14T18:22:49Z INFO sub_with_fsm_iec] Mu0 before evaluation
10 [2024-07-14T18:22:49Z INFO sub_with_fsm_iec] Mu0 after evaluation
11 [2024-07-14T18:22:49Z INFO sub_with_fsm_iec] Time of work of thread is:
  20.073microseconds
12 [2024-07-14T18:22:49Z INFO sub_with_fsm_iec] Mu0 before evaluation
13 [2024-07-14T18:22:49Z INFO sub_with_fsm_iec] Mu0 after evaluation
14 [2024-07-14T18:22:49Z INFO sub_with_fsm_iec] Time of work of thread is:
  9.477microseconds
15 [2024-07-14T18:22:49Z INFO sub_with_fsm_iec] Mu0 before evaluation
16 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Received Ethernet Frame:
  EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
      [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
      no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
      [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2118],
      conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
      smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
      [558], q_ia: [0], i_b: [-997], q_ib: [0], i_c: [443], q_ic: [0], i_n:
      [0], q_in: [0], v_a: [5540], q_va: [0], v_b: [-9980], q_vb: [0], v_c:
      [4446], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [255, 99, 229, 192]
    }
17 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] frame inside FSM
  EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
      [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
      no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
      [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2118],
      conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
      smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
      [558], q_ia: [0], i_b: [-997], q_ib: [0], i_c: [443], q_ic: [0], i_n:
      [0], q_in: [0], v_a: [5540], q_va: [0], v_b: [-9980], q_vb: [0], v_c:
      [4446], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [255, 99, 229, 192]
    }
18 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] System ticked
19 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] State: Initial
20 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] System ticked
21 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] State: Get Sample
22 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Verify Quality of the Sample
23 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Logical Node : 0

```

```

24 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Get Sample -> Valid
25 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] System ticked
26 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] State: Valid
27 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 0
    value: 558
28 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 1
    value: -997
29 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 2
    value: 443
30 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 3
    value: 0
31 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 4
    value: 5540
32 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 5
    value: -9980
33 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 6
    value: 4446
34 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 7
    value: 0
35 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU1: 1
36 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Valid -> CompleteSample
37 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] System ticked
38 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] State: CompleteSample
39 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
40 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Mu0 after evaluation
41 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Time of work of thread is:
    287.475447ms
42 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Mu0 before evaluation
43 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2122],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [-642], q_ia: [0], i_b: [-338], q_ib: [0], i_c: [984], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [-6458], q_va: [0], v_b: [-3380], q_vb: [0], v_c:
    [9840], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [110, 147, 65, 36] }
44 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2122],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [-642], q_ia: [0], i_b: [-338], q_ib: [0], i_c: [984], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [-6458], q_va: [0], v_b: [-3380], q_vb: [0], v_c:
    [9840], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [110, 147, 65, 36] }
45 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] System ticked
46 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] State: Get Sample
47 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Verify Quality of the Sample
48 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Logical Node : 0
49 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Get Sample -> Valid
50 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] System ticked

```

```

51 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] State: Valid
52 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 0
    value: -642
53 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 1
    value: -338
54 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 2
    value: 984
55 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 3
    value: 0
56 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 4
    value: -6458
57 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 5
    value: -3380
58 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 6
    value: 9840
59 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 7
    value: 0
60 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU2: 1
61 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Valid -> CompleteSample
62 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] System ticked
63 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] State: CompleteSample
64 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
65 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Mu0 after evaluation
66 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Time of work of thread is:
    82.047737ms
67 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Mu0 before evaluation
68 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2119],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [-75], q_ia: [0], i_b: [-822], q_ib: [0], i_c: [904], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [-821], q_va: [0], v_b: [-8219], q_vb: [0], v_c:
    [9043], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [116, 110, 236, 40]
    }
69 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2119],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [-75], q_ia: [0], i_b: [-822], q_ib: [0], i_c: [904], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [-821], q_va: [0], v_b: [-8219], q_vb: [0], v_c:
    [9043], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [116, 110, 236, 40]
    }
70 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] System ticked
71 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] State: Get Sample
72 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Verify Quality of the Sample
73 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Logical Node : 0
74 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Get Sample -> Valid
75 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] System ticked

```

```

76 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] State: Valid
77 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 0
    value: -75
78 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 1
    value: -822
79 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 2
    value: 904
80 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 3
    value: 0
81 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 4
    value: -821
82 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 5
    value: -8219
83 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 6
    value: 9043
84 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 7
    value: 0
85 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU1: 2
86 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Valid -> CompleteSample
87 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] System ticked
88 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] State: CompleteSample
89 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
90 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Mu0 after evaluation
91 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Time of work of thread is:
    416.734426ms
92 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Mu0 before evaluation
93 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2123],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [-949], q_ia: [0], i_b: [209], q_ib: [0], i_c: [741], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [-9517], q_va: [0], v_b: [2101], q_vb: [0], v_c:
    [7392], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [244, 142, 174, 38]
    }
94 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2123],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [-949], q_ia: [0], i_b: [209], q_ib: [0], i_c: [741], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [-9517], q_va: [0], v_b: [2101], q_vb: [0], v_c:
    [7392], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [244, 142, 174, 38]
    }
95 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] System ticked
96 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] State: Get Sample
97 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Verify Quality of the Sample
98 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Logical Node : 0
99 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Get Sample -> Valid
100 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] System ticked

```

```

101 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] State: Valid
102 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 0
    value: -949
103 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 1
    value: 209
104 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 2
    value: 741
105 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 3
    value: 0
106 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 4
    value: -9517
107 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 5
    value: 2101
108 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 6
    value: 7392
109 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 7
    value: 0
110 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU2: 2
111 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Valid -> CompleteSample
112 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] System ticked
113 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] State: CompleteSample
114 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
115 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Mu0 after evaluation
116 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Time of work of thread is:
    81.506315ms
117 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Mu0 before evaluation
118 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Mu0 after evaluation
119 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Time of work of thread is:
    125.978514ms
120 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Mu0 before evaluation
121 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Mu0 after evaluation
122 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Time of work of thread is:
    11.278microseconds
123 [2024-07-14T18:22:50Z INFO sub_with_fsm_iec] Mu0 before evaluation
124 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2120],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [-619], q_ia: [0], i_b: [-368], q_ib: [0], i_c: [989], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [-6214], q_va: [0], v_b: [-3675], q_vb: [0], v_c:
    [9891], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [98, 174, 168, 174]
    }

```

```

125 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
      17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
      SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
        [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
        no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
        [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2120],
        conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
        smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
        [-619], q_ia: [0], i_b: [-368], q_ib: [0], i_c: [989], q_ic: [0], i_n:
        [0], q_in: [0], v_a: [-6214], q_va: [0], v_b: [-3675], q_vb: [0], v_c:
        [9891], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [98, 174, 168, 174]
    }
126 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] System ticked
127 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] State: Get Sample
128 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Verify Quality of the Sample
129 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Logical Node : 0
130 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Get Sample -> Valid
131 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] System ticked
132 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] State: Valid
133 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 0
    value: -619
134 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 1
    value: -368
135 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 2
    value: 989
136 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 3
    value: 0
137 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 4
    value: -6214
138 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 5
    value: -3675
139 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 6
    value: 9891
140 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 7
    value: 0
141 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU1: 3
142 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Valid -> CompleteSample
143 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] System ticked
144 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] State: CompleteSample
145 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
146 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Mu0 after evaluation
147 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Time of work of thread is:
    288.166014ms
148 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Mu0 before evaluation
149 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
      17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
      SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
        [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
        no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
        [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2124],
        conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
        smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
        [-964], q_ia: [0], i_b: [712], q_ib: [0], i_c: [251], q_ic: [0], i_n:
        [0], q_in: [0], v_a: [-9640], q_va: [0], v_b: [7123], q_vb: [0], v_c:
        [2514], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [174, 92, 174, 178]
    }

```

```

150 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
      17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
      SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
        [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
        no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
        [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2124],
        conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
        smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
        [-964], q_ia: [0], i_b: [712], q_ib: [0], i_c: [251], q_ic: [0], i_n:
        [0], q_in: [0], v_a: [-9640], q_va: [0], v_b: [7123], q_vb: [0], v_c:
        [2514], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [174, 92, 174, 178]
    }
151 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] System ticked
152 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] State: Get Sample
153 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Verify Quality of the Sample
154 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Logical Node : 0
155 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Get Sample -> Valid
156 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] System ticked
157 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] State: Valid
158 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 0
    value: -964
159 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 1
    value: 712
160 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 2
    value: 251
161 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 3
    value: 0
162 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 4
    value: -9640
163 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 5
    value: 7123
164 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 6
    value: 2514
165 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 7
    value: 0
166 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU2: 3
167 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Valid -> CompleteSample
168 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] System ticked
169 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] State: CompleteSample
170 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
171 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Mu0 after evaluation
172 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Time of work of thread is:
    83.727664ms
173 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Mu0 before evaluation
174 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
      17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
      SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
        [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
        no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
        [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2121],
        conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
        smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
        [-949], q_ia: [0], i_b: [210], q_ib: [0], i_c: [741], q_ic: [0], i_n:
        [0], q_in: [0], v_a: [-9519], q_va: [0], v_b: [2109], q_vb: [0], v_c:
        [7409], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [38, 88, 70, 172] }

```



```

175 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
      17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
      SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
        [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
        no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
        [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2121],
        conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
        smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
        [-949], q_ia: [0], i_b: [210], q_ib: [0], i_c: [741], q_ic: [0], i_n:
        [0], q_in: [0], v_a: [-9519], q_va: [0], v_b: [2109], q_vb: [0], v_c:
        [7409], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [38, 88, 70, 172] }
176 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] System ticked
177 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] State: Get Sample
178 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Verify Quality of the Sample
179 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Logical Node : 0
180 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Get Sample -> Valid
181 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] System ticked
182 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] State: Valid
183 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 0
    value: -949
184 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 1
    value: 210
185 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 2
    value: 741
186 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 3
    value: 0
187 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 4
    value: -9519
188 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 5
    value: 2109
189 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 6
    value: 7409
190 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 7
    value: 0
191 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU1: 4
192 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Valid -> CompleteSample
193 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] System ticked
194 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] State: CompleteSample
195 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
196 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Mu0 after evaluation
197 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Time of work of thread is:
    417.070147ms
198 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Mu0 before evaluation
199 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
      17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
      SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
        [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
        no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
        [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2125],
        conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
        smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
        [-762], q_ia: [0], i_b: [943], q_ib: [0], i_c: [-185], q_ic: [0], i_n:
        [0], q_in: [0], v_a: [-7584], q_va: [0], v_b: [9436], q_vb: [0], v_c:
        [-1855], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [247, 235, 252, 55]
    }

```

```

200 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
      17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
      SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
        [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
        no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
        [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2125],
        conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
        smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
        [-762], q_ia: [0], i_b: [943], q_ib: [0], i_c: [-185], q_ic: [0], i_n:
        [0], q_in: [0], v_a: [-7584], q_va: [0], v_b: [9436], q_vb: [0], v_c:
        [-1855], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [247, 235, 252, 55]
    }
201 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] System ticked
202 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] State: Get Sample
203 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Verify Quality of the Sample
204 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Logical Node : 0
205 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Get Sample -> Valid
206 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] System ticked
207 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] State: Valid
208 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 0
    value: -762
209 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 1
    value: 943
210 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 2
    value: -185
211 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 3
    value: 0
212 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 4
    value: -7584
213 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 5
    value: 9436
214 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 6
    value: -1855
215 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 7
    value: 0
216 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU2: 4
217 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Valid -> CompleteSample
218 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] System ticked
219 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] State: CompleteSample
220 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
221 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Mu0 after evaluation
222 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Time of work of thread is:
    82.023732ms
223 [2024-07-14T18:22:51Z INFO sub_with_fsm_iec] Mu0 before evaluation
224 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
      17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
      SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
        [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
        no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
        [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2122],
        conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
        smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
        [-964], q_ia: [0], i_b: [711], q_ib: [0], i_c: [252], q_ic: [0], i_n:
        [0], q_in: [0], v_a: [-9640], q_va: [0], v_b: [7122], q_vb: [0], v_c:
        [2516], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [33, 116, 140, 136]
    }

```

```

225 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
      17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
      SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
        [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
        no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
        [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2122],
        conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
        smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
        [-964], q_ia: [0], i_b: [711], q_ib: [0], i_c: [252], q_ic: [0], i_n:
        [0], q_in: [0], v_a: [-9640], q_va: [0], v_b: [7122], q_vb: [0], v_c:
        [2516], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [33, 116, 140, 136]
    }
226 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] System ticked
227 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] State: Get Sample
228 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Verify Quality of the Sample
229 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Logical Node : 0
230 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Get Sample -> Valid
231 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] System ticked
232 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] State: Valid
233 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 0
    value: -964
234 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 1
    value: 711
235 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 2
    value: 252
236 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 3
    value: 0
237 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 4
    value: -9640
238 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 5
    value: 7122
239 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 6
    value: 2516
240 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 7
    value: 0
241 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU1: 5
242 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Valid -> CompleteSample
243 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] System ticked
244 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] State: CompleteSample
245 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
246 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Mu0 after evaluation
247 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Time of work of thread is:
    417.45059ms
248 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Mu0 before evaluation
249 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Mu0 after evaluation
250 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Time of work of thread is:
    25.455468ms
251 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Mu0 before evaluation

```

```

252 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
      17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
      SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
        [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
        no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
        [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2126],
        conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
        smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
        [-549], q_ia: [0], i_b: [998], q_ib: [0], i_c: [-450], q_ic: [0], i_n:
        [0], q_in: [0], v_a: [-5474], q_va: [0], v_b: [9984], q_vb: [0], v_c:
        [-4512], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [7, 196, 45, 5] }
253 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
      17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
      SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
        [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
        no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
        [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2126],
        conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
        smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
        [-549], q_ia: [0], i_b: [998], q_ib: [0], i_c: [-450], q_ic: [0], i_n:
        [0], q_in: [0], v_a: [-5474], q_va: [0], v_b: [9984], q_vb: [0], v_c:
        [-4512], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [7, 196, 45, 5] }
254 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] System ticked
255 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] State: Get Sample
256 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Verify Quality of the Sample
257 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Logical Node : 0
258 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Get Sample -> Valid
259 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] System ticked
260 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] State: Valid
261 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 0
    value: -549
262 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 1
    value: 998
263 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 2
    value: -450
264 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 3
    value: 0
265 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 4
    value: -5474
266 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 5
    value: 9984
267 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 6
    value: -4512
268 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 7
    value: 0
269 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU2: 5
270 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Valid ->
    CheckErrorPercentage
271 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] System ticked
272 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] State: CheckErrorPercentage
273 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] buffer_mul: [[558, -75,
    -619, -949, -964], [-997, -822, -368, 210, 711], [443, 904, 989, 741,
    252], [0, 0, 0, 0, 0], [5540, -821, -6214, -9519, -9640], [-9980,
    -8219, -3675, 2109, 7122], [4446, 9043, 9891, 7409, 2516], [0, 0, 0, 0,
    0]]

```

```

274 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] buffer_mu2: [[-642, -949,
    -964, -762, -549], [-338, 209, 712, 943, 998], [984, 741, 251, -185,
    -450], [0, 0, 0, 0, 0], [-6458, -9517, -9640, -7584, -5474], [-3380,
    2101, 7123, 9436, 9984], [9840, 7392, 2514, -1855, -4512], [0, 0, 0, 0,
    0]]
275 [2024-07-14T18:22:52Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
276 [2024-07-14T18:22:52Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
277 [2024-07-14T18:22:52Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
278 [2024-07-14T18:22:52Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
279 [2024-07-14T18:22:52Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
280 [2024-07-14T18:22:52Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
281 [2024-07-14T18:22:52Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
282 [2024-07-14T18:22:52Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
283 [2024-07-14T18:22:52Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
284 [2024-07-14T18:22:52Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
285 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of the sum of MU1:
    8.340152
286 [2024-07-14T18:22:52Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
287 [2024-07-14T18:22:52Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
288 [2024-07-14T18:22:52Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
289 [2024-07-14T18:22:52Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
290 [2024-07-14T18:22:52Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
291 [2024-07-14T18:22:52Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
292 [2024-07-14T18:22:52Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
293 [2024-07-14T18:22:52Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
294 [2024-07-14T18:22:52Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
295 [2024-07-14T18:22:52Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
296 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of the sum of MU2:
    -23.258024
297 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of error of MU1:
    0.2085038
298 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of error of MU2:
    0.5814506
299 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of the error:
    0.5814506
300 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Actual State: CompleteCycle
301 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] System ticked
302 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] State: CompleteCycle
303 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] CompleteCycle -> GetSample

```

```

304 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Mu0 after evaluation
305 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Time of work of thread is:
    55.535516ms
306 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Mu0 before evaluation
307 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Mu0 after evaluation
308 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Time of work of thread is:
    9.849874ms
309 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Mu0 before evaluation
310 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Mu0 after evaluation
311 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Time of work of thread is:
    239.521815ms
312 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Mu0 before evaluation
313 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2123],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [-841], q_ia: [0], i_b: [893], q_ib: [0], i_c: [-57], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [-8355], q_va: [0], v_b: [8937], q_vb: [0], v_c:
    [-589], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [61, 52, 11, 70] }
314 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2123],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [-841], q_ia: [0], i_b: [893], q_ib: [0], i_c: [-57], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [-8355], q_va: [0], v_b: [8937], q_vb: [0], v_c:
    [-589], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [61, 52, 11, 70] }
315 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] System ticked
316 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] State: Get Sample
317 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Verify Quality of the Sample
318 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Logical Node : 0
319 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Get Sample -> Valid
320 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] System ticked
321 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] State: Valid
322 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 0
    value: -841
323 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 1
    value: 893
324 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 2
    value: -57
325 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 3
    value: 0
326 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 4
    value: -8355
327 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 5
    value: 8937
328 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 6
    value: -589
329 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 7
    value: 0

```

```

330 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU1: 1
331 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Valid -> CompleteSample
332 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] System ticked
333 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] State: CompleteSample
334 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
335 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Mu0 after evaluation
336 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Time of work of thread is:
    164.721695ms
337 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Mu0 before evaluation
338 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2127],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [-13], q_ia: [0], i_b: [869], q_ib: [0], i_c: [-862], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [-76], q_va: [0], v_b: [8697], q_vb: [0], v_c:
    [-8623], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [9, 235, 140, 58] }
339 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2127],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [-13], q_ia: [0], i_b: [869], q_ib: [0], i_c: [-862], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [-76], q_va: [0], v_b: [8697], q_vb: [0], v_c:
    [-8623], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [9, 235, 140, 58] }
340 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] System ticked
341 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] State: Get Sample
342 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Verify Quality of the Sample
343 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Logical Node : 0
344 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Get Sample -> Valid
345 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] System ticked
346 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] State: Valid
347 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 0
    value: -13
348 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 1
    value: 869
349 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 2
    value: -862
350 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 3
    value: 0
351 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 4
    value: -76
352 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 5
    value: 8697
353 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 6
    value: -8623
354 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 7
    value: 0
355 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU2: 1

```

```

356 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Valid -> CompleteSample
357 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] System ticked
358 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] State: CompleteSample
359 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
360 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Mu0 after evaluation
361 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Time of work of thread is:
    82.201612ms
362 [2024-07-14T18:22:52Z INFO sub_with_fsm_iec] Mu0 before evaluation
363 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2124],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [-393], q_ia: [0], i_b: [992], q_ib: [0], i_c: [-601], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [-3904], q_va: [0], v_b: [9924], q_vb: [0], v_c:
    [-6023], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [161, 27, 175, 68]
    }
364 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2124],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [-393], q_ia: [0], i_b: [992], q_ib: [0], i_c: [-601], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [-3904], q_va: [0], v_b: [9924], q_vb: [0], v_c:
    [-6023], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [161, 27, 175, 68]
    }
365 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] System ticked
366 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] State: Get Sample
367 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Verify Quality of the Sample
368 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Logical Node : 0
369 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Get Sample -> Valid
370 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] System ticked
371 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] State: Valid
372 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 0
    value: -393
373 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 1
    value: 992
374 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 2
    value: -601
375 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 3
    value: 0
376 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 4
    value: -3904
377 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 5
    value: 9924
378 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 6
    value: -6023
379 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 7
    value: 0
380 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU1: 2

```



```

381 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Valid -> CompleteSample
382 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] System ticked
383 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] State: CompleteSample
384 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
385 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Mu0 after evaluation
386 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Time of work of thread is:
    417.770846ms
387 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Mu0 before evaluation
388 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2128],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [561], q_ia: [0], i_b: [431], q_ib: [0], i_c: [-997], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [5657], q_va: [0], v_b: [4308], q_vb: [0], v_c:
    [-9969], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [85, 92, 201, 255]
    }
389 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2128],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [561], q_ia: [0], i_b: [431], q_ib: [0], i_c: [-997], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [5657], q_va: [0], v_b: [4308], q_vb: [0], v_c:
    [-9969], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [85, 92, 201, 255]
    }
390 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] System ticked
391 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] State: Get Sample
392 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Verify Quality of the Sample
393 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Logical Node : 0
394 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Get Sample -> Valid
395 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] System ticked
396 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] State: Valid
397 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 0
    value: 561
398 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 1
    value: 431
399 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 2
    value: -997
400 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 3
    value: 0
401 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 4
    value: 5657
402 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 5
    value: 4308
403 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 6
    value: -9969
404 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 7
    value: 0
405 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU2: 2

```

```

406 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Valid -> CompleteSample
407 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] System ticked
408 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] State: CompleteSample
409 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
410 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Mu0 after evaluation
411 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Time of work of thread is:
    81.426253ms
412 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Mu0 before evaluation
413 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
      17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
      SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
        [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
        no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
        [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2125],
        conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
        smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
        [-97], q_ia: [0], i_b: [907], q_ib: [0], i_c: [-817], q_ic: [0], i_n:
        [0], q_in: [0], v_a: [-906], q_va: [0], v_b: [9077], q_vb: [0], v_c:
        [-8172], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [127, 133, 164, 9]
    }
414 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
      17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
      SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
        [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
        no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
        [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2125],
        conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
        smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
        [-97], q_ia: [0], i_b: [907], q_ib: [0], i_c: [-817], q_ic: [0], i_n:
        [0], q_in: [0], v_a: [-906], q_va: [0], v_b: [9077], q_vb: [0], v_c:
        [-8172], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [127, 133, 164, 9]
    }
415 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] System ticked
416 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] State: Get Sample
417 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Verify Quality of the Sample
418 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Logical Node : 0
419 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Get Sample -> Valid
420 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] System ticked
421 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] State: Valid
422 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 0
    value: -97
423 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 1
    value: 907
424 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 2
    value: -817
425 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 3
    value: 0
426 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 4
    value: -906
427 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 5
    value: 9077
428 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 6
    value: -8172
429 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 7
    value: 0
430 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU1: 3

```

```

431 [2024-07-14T18:22:53Z INFO    sub_with_fsm_iec] Valid -> CompleteSample
432 [2024-07-14T18:22:53Z INFO    sub_with_fsm_iec] System ticked
433 [2024-07-14T18:22:53Z INFO    sub_with_fsm_iec] State: CompleteSample
434 [2024-07-14T18:22:53Z INFO    sub_with_fsm_iec] CompleteSample -> GetSample
435 [2024-07-14T18:22:53Z INFO    sub_with_fsm_iec] Mu0 after evaluation
436 [2024-07-14T18:22:53Z INFO    sub_with_fsm_iec] Time of work of thread is:
    417.023148ms
437 [2024-07-14T18:22:53Z INFO    sub_with_fsm_iec] Mu0 before evaluation
438 [2024-07-14T18:22:53Z INFO    sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2129],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [818], q_ia: [0], i_b: [81], q_ib: [0], i_c: [-903], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [8226], q_va: [0], v_b: [808], q_vb: [0], v_c:
    [-9035], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [118, 74, 12, 209]
    }
439 [2024-07-14T18:22:53Z INFO    sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2129],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [818], q_ia: [0], i_b: [81], q_ib: [0], i_c: [-903], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [8226], q_va: [0], v_b: [808], q_vb: [0], v_c:
    [-9035], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [118, 74, 12, 209]
    }
440 [2024-07-14T18:22:53Z INFO    sub_with_fsm_iec] System ticked
441 [2024-07-14T18:22:53Z INFO    sub_with_fsm_iec] State: Get Sample
442 [2024-07-14T18:22:53Z INFO    sub_with_fsm_iec] Verify Quality of the Sample
443 [2024-07-14T18:22:53Z INFO    sub_with_fsm_iec] Logical Node : 0
444 [2024-07-14T18:22:53Z INFO    sub_with_fsm_iec] Get Sample -> Valid
445 [2024-07-14T18:22:53Z INFO    sub_with_fsm_iec] System ticked
446 [2024-07-14T18:22:53Z INFO    sub_with_fsm_iec] State: Valid
447 [2024-07-14T18:22:53Z INFO    sub_with_fsm_iec] Value of Buffer MU 2 fase: 0
    value: 818
448 [2024-07-14T18:22:53Z INFO    sub_with_fsm_iec] Value of Buffer MU 2 fase: 1
    value: 81
449 [2024-07-14T18:22:53Z INFO    sub_with_fsm_iec] Value of Buffer MU 2 fase: 2
    value: -903
450 [2024-07-14T18:22:53Z INFO    sub_with_fsm_iec] Value of Buffer MU 2 fase: 3
    value: 0
451 [2024-07-14T18:22:53Z INFO    sub_with_fsm_iec] Value of Buffer MU 2 fase: 4
    value: 8226
452 [2024-07-14T18:22:53Z INFO    sub_with_fsm_iec] Value of Buffer MU 2 fase: 5
    value: 808
453 [2024-07-14T18:22:53Z INFO    sub_with_fsm_iec] Value of Buffer MU 2 fase: 6
    value: -9035
454 [2024-07-14T18:22:53Z INFO    sub_with_fsm_iec] Value of Buffer MU 2 fase: 7
    value: 0
455 [2024-07-14T18:22:53Z INFO    sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU2: 3

```

```

456 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Valid -> CompleteSample
457 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] System ticked
458 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] State: CompleteSample
459 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
460 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Mu0 after evaluation
461 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Time of work of thread is:
    82.271011ms
462 [2024-07-14T18:22:53Z INFO sub_with_fsm_iec] Mu0 before evaluation
463 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2126],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [69], q_ia: [0], i_b: [827], q_ib: [0], i_c: [-899], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [720], q_va: [0], v_b: [8276], q_vb: [0], v_c:
    [-8999], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [24, 207, 158, 218]
    }
464 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2126],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [69], q_ia: [0], i_b: [827], q_ib: [0], i_c: [-899], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [720], q_va: [0], v_b: [8276], q_vb: [0], v_c:
    [-8999], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [24, 207, 158, 218]
    }
465 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] System ticked
466 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] State: Get Sample
467 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Verify Quality of the Sample
468 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Logical Node : 0
469 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Get Sample -> Valid
470 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] System ticked
471 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] State: Valid
472 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 0
    value: 69
473 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 1
    value: 827
474 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 2
    value: -899
475 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 3
    value: 0
476 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 4
    value: 720
477 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 5
    value: 8276
478 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 6
    value: -8999
479 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 7
    value: 0
480 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU1: 4

```

```

481 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Valid -> CompleteSample
482 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] System ticked
483 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] State: CompleteSample
484 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
485 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Mu0 after evaluation
486 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Time of work of thread is:
    416.146999ms
487 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Mu0 before evaluation
488 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
      17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
      SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
        [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
        no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
        [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2130],
        conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
        smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
        [999], q_ia: [0], i_b: [-477], q_ib: [0], i_c: [-521], q_ic: [0], i_n:
        [0], q_in: [0], v_a: [9996], q_va: [0], v_b: [-4781], q_vb: [0], v_c:
        [-5214], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [132, 82, 185, 175]
    }
489 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
      17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
      SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
        [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
        no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
        [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2130],
        conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
        smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
        [999], q_ia: [0], i_b: [-477], q_ib: [0], i_c: [-521], q_ic: [0], i_n:
        [0], q_in: [0], v_a: [9996], q_va: [0], v_b: [-4781], q_vb: [0], v_c:
        [-5214], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [132, 82, 185, 175]
    }
490 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] System ticked
491 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] State: Get Sample
492 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Verify Quality of the Sample
493 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Logical Node : 0
494 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Get Sample -> Valid
495 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] System ticked
496 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] State: Valid
497 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 0
    value: 999
498 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 1
    value: -477
499 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 2
    value: -521
500 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 3
    value: 0
501 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 4
    value: 9996
502 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 5
    value: -4781
503 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 6
    value: -5214
504 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 7
    value: 0
505 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU2: 4

```

```

506 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Valid -> CompleteSample
507 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] System ticked
508 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] State: CompleteSample
509 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
510 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Mu0 after evaluation
511 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Time of work of thread is:
    83.508245ms
512 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Mu0 before evaluation
513 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Mu0 after evaluation
514 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Time of work of thread is:
    189.679953ms
515 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Mu0 before evaluation
516 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Mu0 after evaluation
517 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Time of work of thread is:
    11.025microseconds
518 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Mu0 before evaluation
519 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
      17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
      SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
        [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
        no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
        [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2127],
        conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
        smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
        [627], q_ia: [0], i_b: [350], q_ib: [0], i_c: [-986], q_ic: [0], i_n:
        [0], q_in: [0], v_a: [6363], q_va: [0], v_b: [3495], q_vb: [0], v_c:
        [-9860], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [67, 100, 160, 202]
    }
520 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
      17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
      SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
        [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
        no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
        [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2127],
        conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
        smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
        [627], q_ia: [0], i_b: [350], q_ib: [0], i_c: [-986], q_ic: [0], i_n:
        [0], q_in: [0], v_a: [6363], q_va: [0], v_b: [3495], q_vb: [0], v_c:
        [-9860], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [67, 100, 160, 202]
    }
521 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] System ticked
522 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] State: Get Sample
523 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Verify Quality of the Sample
524 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Logical Node : 0
525 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Get Sample -> Valid
526 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] System ticked
527 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] State: Valid
528 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 0
    value: 627
529 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 1
    value: 350
530 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 2
    value: -986
531 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 3
    value: 0
532 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 4
    value: 6363

```

```

533 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 5
    value: 3495
534 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 6
    value: -9860
535 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 7
    value: 0
536 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU1: 5
537 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Valid -> CompleteSample
538 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] System ticked
539 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] State: CompleteSample
540 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
541 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Mu0 after evaluation
542 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Time of work of thread is:
    225.200327ms
543 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Mu0 before evaluation
544 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2131],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [848], q_ia: [0], i_b: [-888], q_ib: [0], i_c: [48], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [8405], q_va: [0], v_b: [-8895], q_vb: [0], v_c:
    [496], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [8, 182, 171, 226] }
545 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2131],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [848], q_ia: [0], i_b: [-888], q_ib: [0], i_c: [48], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [8405], q_va: [0], v_b: [-8895], q_vb: [0], v_c:
    [496], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [8, 182, 171, 226] }
546 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] System ticked
547 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] State: Get Sample
548 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Verify Quality of the Sample
549 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Logical Node : 0
550 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Get Sample -> Valid
551 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] System ticked
552 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] State: Valid
553 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 0
    value: 848
554 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 1
    value: -888
555 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 2
    value: 48
556 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 3
    value: 0
557 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 4
    value: 8405
558 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 5
    value: -8895

```

```

559 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 6
    value: 496
560 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 7
    value: 0
561 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU2: 5
562 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Valid ->
    CheckErrorPercentage
563 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] System ticked
564 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] State: CheckErrorPercentage
565 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] buffer_mu1: [[-841, -393,
    -97, 69, 627], [893, 992, 907, 827, 350], [-57, -601, -817, -899,
    -986], [0, 0, 0, 0, 0], [-8355, -3904, -906, 720, 6363], [8937, 9924,
    9077, 8276, 3495], [-589, -6023, -8172, -8999, -9860], [0, 0, 0, 0, 0]]
566 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] buffer_mu2: [[-13, 561, 818,
    999, 848], [869, 431, 81, -477, -888], [-862, -997, -903, -521, 48],
    [0, 0, 0, 0, 0], [-76, 5657, 8226, 9996, 8405], [8697, 4308, 808,
    -4781, -8895], [-8623, -9969, -9035, -5214, 496], [0, 0, 0, 0, 0]]
567 [2024-07-14T18:22:54Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
568 [2024-07-14T18:22:54Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
569 [2024-07-14T18:22:54Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
570 [2024-07-14T18:22:54Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
571 [2024-07-14T18:22:54Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
572 [2024-07-14T18:22:54Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
573 [2024-07-14T18:22:54Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
574 [2024-07-14T18:22:54Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
575 [2024-07-14T18:22:54Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
576 [2024-07-14T18:22:54Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
577 [2024-07-14T18:22:54Z INFO sub_with_fsm_iec] Value of the sum of MU1:
    13.774796
578 [2024-07-14T18:22:54Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
579 [2024-07-14T18:22:54Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
580 [2024-07-14T18:22:54Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
581 [2024-07-14T18:22:54Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
582 [2024-07-14T18:22:54Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
583 [2024-07-14T18:22:54Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
584 [2024-07-14T18:22:54Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
585 [2024-07-14T18:22:54Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
586 [2024-07-14T18:22:54Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2

```



```

587 [2024-07-14T18:22:54Z WARN  sub_with_fsm_iec] Failed acquisition value in
    the MU2
588 [2024-07-14T18:22:54Z INFO  sub_with_fsm_iec] Value of the sum of MU2:
    135.66617
589 [2024-07-14T18:22:54Z INFO  sub_with_fsm_iec] Value of error of MU1:
    0.3443699
590 [2024-07-14T18:22:54Z INFO  sub_with_fsm_iec] Value of error of MU2:
    3.3916543
591 [2024-07-14T18:22:54Z INFO  sub_with_fsm_iec] Value of the error:
    3.3916543
592 [2024-07-14T18:22:54Z INFO  sub_with_fsm_iec] Actual State: CompleteCycle
593 [2024-07-14T18:22:54Z INFO  sub_with_fsm_iec] System ticked
594 [2024-07-14T18:22:54Z INFO  sub_with_fsm_iec] State: CompleteCycle
595 [2024-07-14T18:22:54Z INFO  sub_with_fsm_iec] CompleteCycle -> GetSample
596 [2024-07-14T18:22:54Z INFO  sub_with_fsm_iec] Mu0 after evaluation
597 [2024-07-14T18:22:54Z INFO  sub_with_fsm_iec] Time of work of thread is:
    82.687632ms
598 [2024-07-14T18:22:54Z INFO  sub_with_fsm_iec] Mu0 before evaluation
599 [2024-07-14T18:22:54Z INFO  sub_with_fsm_iec] Mu0 after evaluation
600 [2024-07-14T18:22:54Z INFO  sub_with_fsm_iec] Time of work of thread is:
    109.291529ms
601 [2024-07-14T18:22:54Z INFO  sub_with_fsm_iec] Mu0 before evaluation
602 [2024-07-14T18:22:55Z INFO  sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2128],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [871], q_ia: [0], i_b: [-27], q_ib: [0], i_c: [-851], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [8800], q_va: [0], v_b: [-291], q_vb: [0], v_c:
    [-8508], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [251, 186, 141, 48]
    }
603 [2024-07-14T18:22:55Z INFO  sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2128],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [871], q_ia: [0], i_b: [-27], q_ib: [0], i_c: [-851], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [8800], q_va: [0], v_b: [-291], q_vb: [0], v_c:
    [-8508], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [251, 186, 141, 48]
    }
604 [2024-07-14T18:22:55Z INFO  sub_with_fsm_iec] System ticked
605 [2024-07-14T18:22:55Z INFO  sub_with_fsm_iec] State: Get Sample
606 [2024-07-14T18:22:55Z INFO  sub_with_fsm_iec] Verify Quality of the Sample
607 [2024-07-14T18:22:55Z INFO  sub_with_fsm_iec] Logical Node : 0
608 [2024-07-14T18:22:55Z INFO  sub_with_fsm_iec] Get Sample -> Valid
609 [2024-07-14T18:22:55Z INFO  sub_with_fsm_iec] System ticked
610 [2024-07-14T18:22:55Z INFO  sub_with_fsm_iec] State: Valid
611 [2024-07-14T18:22:55Z INFO  sub_with_fsm_iec] Value of Buffer MU 1 fase: 0
    value: 871
612 [2024-07-14T18:22:55Z INFO  sub_with_fsm_iec] Value of Buffer MU 1 fase: 1
    value: -27

```

```

613 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 2
    value: -851
614 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 3
    value: 0
615 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 4
    value: 8800
616 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 5
    value: -291
617 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 6
    value: -8508
618 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 7
    value: 0
619 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU1: 1
620 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Valid -> CompleteSample
621 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] System ticked
622 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] State: CompleteSample
623 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
624 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Mu0 after evaluation
625 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Time of work of thread is:
    304.907186ms
626 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Mu0 before evaluation
627 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2132],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [314], q_ia: [0], i_b: [-978], q_ib: [0], i_c: [668], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [3097], q_va: [0], v_b: [-9782], q_vb: [0], v_c:
    [6691], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [239, 127, 56, 162]
    }
628 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2132],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [314], q_ia: [0], i_b: [-978], q_ib: [0], i_c: [668], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [3097], q_va: [0], v_b: [-9782], q_vb: [0], v_c:
    [6691], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [239, 127, 56, 162]
    }
629 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] System ticked
630 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] State: Get Sample
631 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Verify Quality of the Sample
632 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Logical Node : 0
633 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Get Sample -> Valid
634 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] System ticked
635 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] State: Valid
636 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 0
    value: 314
637 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 1
    value: -978

```

```

638 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 2
    value: 668
639 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 3
    value: 0
640 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 4
    value: 3097
641 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 5
    value: -9782
642 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 6
    value: 6691
643 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 7
    value: 0
644 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU2: 1
645 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Valid -> CompleteSample
646 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] System ticked
647 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] State: CompleteSample
648 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
649 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Mu0 after evaluation
650 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Time of work of thread is:
    84.460747ms
651 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Mu0 before evaluation
652 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2129],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [984], q_ia: [0], i_b: [-353], q_ib: [0], i_c: [-632], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [9870], q_va: [0], v_b: [-3551], q_vb: [0], v_c:
    [-6315], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [71, 34, 159, 108]
    }
653 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2129],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [984], q_ia: [0], i_b: [-353], q_ib: [0], i_c: [-632], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [9870], q_va: [0], v_b: [-3551], q_vb: [0], v_c:
    [-6315], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [71, 34, 159, 108]
    }
654 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] System ticked
655 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] State: Get Sample
656 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Verify Quality of the Sample
657 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Logical Node : 0
658 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Get Sample -> Valid
659 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] System ticked
660 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] State: Valid
661 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 0
    value: 984
662 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 1
    value: -353

```

```

663 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 2
    value: -632
664 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 3
    value: 0
665 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 4
    value: 9870
666 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 5
    value: -3551
667 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 6
    value: -6315
668 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 7
    value: 0
669 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU1: 2
670 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Valid -> CompleteSample
671 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] System ticked
672 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] State: CompleteSample
673 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
674 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Mu0 after evaluation
675 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Time of work of thread is:
    412.952982ms
676 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Mu0 before evaluation
677 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2133],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [-82], q_ia: [0], i_b: [-818], q_ib: [0], i_c: [907], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [-892], q_va: [0], v_b: [-8178], q_vb: [0], v_c:
    [9073], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [93, 17, 93, 25] }
678 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2133],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [-82], q_ia: [0], i_b: [-818], q_ib: [0], i_c: [907], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [-892], q_va: [0], v_b: [-8178], q_vb: [0], v_c:
    [9073], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [93, 17, 93, 25] }
679 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] System ticked
680 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] State: Get Sample
681 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Verify Quality of the Sample
682 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Logical Node : 0
683 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Get Sample -> Valid
684 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] System ticked
685 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] State: Valid
686 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 0
    value: -82
687 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 1
    value: -818
688 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 2
    value: 907

```

```

689 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 3
    value: 0
690 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 4
    value: -892
691 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 5
    value: -8178
692 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 6
    value: 9073
693 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 7
    value: 0
694 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU2: 2
695 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Valid -> CompleteSample
696 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] System ticked
697 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] State: CompleteSample
698 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
699 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Mu0 after evaluation
700 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Time of work of thread is:
    84.613805ms
701 [2024-07-14T18:22:55Z INFO sub_with_fsm_iec] Mu0 before evaluation
702 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2130],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [995], q_ia: [0], i_b: [-585], q_ib: [0], i_c: [-409], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [9947], q_va: [0], v_b: [-5863], q_vb: [0], v_c:
    [-4080], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [55, 241, 85, 161]
    }
703 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2130],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [995], q_ia: [0], i_b: [-585], q_ib: [0], i_c: [-409], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [9947], q_va: [0], v_b: [-5863], q_vb: [0], v_c:
    [-4080], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [55, 241, 85, 161]
    }
704 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] System ticked
705 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] State: Get Sample
706 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Verify Quality of the Sample
707 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Logical Node : 0
708 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Get Sample -> Valid
709 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] System ticked
710 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] State: Valid
711 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 0
    value: 995
712 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 1
    value: -585
713 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 2
    value: -409

```

```

714 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 3
    value: 0
715 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 4
    value: 9947
716 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 5
    value: -5863
717 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 6
    value: -4080
718 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 7
    value: 0
719 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU1: 3
720 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Valid -> CompleteSample
721 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] System ticked
722 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] State: CompleteSample
723 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
724 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Mu0 after evaluation
725 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Time of work of thread is:
    414.937207ms
726 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Mu0 before evaluation
727 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2134],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [-381], q_ia: [0], i_b: [-607], q_ib: [0], i_c: [991], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [-3844], q_va: [0], v_b: [-6071], q_vb: [0], v_c:
    [9917], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [28, 107, 96, 103] }
728 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2134],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [-381], q_ia: [0], i_b: [-607], q_ib: [0], i_c: [991], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [-3844], q_va: [0], v_b: [-6071], q_vb: [0], v_c:
    [9917], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [28, 107, 96, 103] }
729 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] System ticked
730 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] State: Get Sample
731 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Verify Quality of the Sample
732 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Logical Node : 0
733 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Get Sample -> Valid
734 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] System ticked
735 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] State: Valid
736 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 0
    value: -381
737 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 1
    value: -607
738 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 2
    value: 991
739 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 3
    value: 0

```

```

740 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 4
    value: -3844
741 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 5
    value: -6071
742 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 6
    value: 9917
743 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 7
    value: 0
744 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU2: 3
745 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Valid -> CompleteSample
746 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] System ticked
747 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] State: CompleteSample
748 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
749 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Mu0 after evaluation
750 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Time of work of thread is:
    83.379774ms
751 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Mu0 before evaluation
752 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Mu0 after evaluation
753 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Time of work of thread is:
    92.178706ms
754 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Mu0 before evaluation
755 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Mu0 after evaluation
756 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Time of work of thread is:
    243.278937ms
757 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Mu0 before evaluation
758 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2131],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [922], q_ia: [0], i_b: [-798], q_ib: [0], i_c: [-121], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [9204], q_va: [0], v_b: [-7988], q_vb: [0], v_c:
    [-1213], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [98, 161, 157, 210]
    }
759 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2131],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [922], q_ia: [0], i_b: [-798], q_ib: [0], i_c: [-121], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [9204], q_va: [0], v_b: [-7988], q_vb: [0], v_c:
    [-1213], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [98, 161, 157, 210]
    }
760 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] System ticked
761 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] State: Get Sample
762 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Verify Quality of the Sample
763 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Logical Node : 0
764 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Get Sample -> Valid
765 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] System ticked
766 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] State: Valid

```

```

767 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 0
    value: 922
768 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 1
    value: -798
769 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 2
    value: -121
770 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 3
    value: 0
771 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 4
    value: 9204
772 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 5
    value: -7988
773 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 6
    value: -1213
774 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 7
    value: 0
775 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU1: 4
776 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Valid -> CompleteSample
777 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] System ticked
778 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] State: CompleteSample
779 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
780 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Mu0 after evaluation
781 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Time of work of thread is:
    75.982875ms
782 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Mu0 before evaluation
783 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2135],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [-623], q_ia: [0], i_b: [-359], q_ib: [0], i_c: [987], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [-6285], q_va: [0], v_b: [-3592], q_vb: [0], v_c:
    [9878], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [117, 36, 168, 137]
    }
784 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2135],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [-623], q_ia: [0], i_b: [-359], q_ib: [0], i_c: [987], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [-6285], q_va: [0], v_b: [-3592], q_vb: [0], v_c:
    [9878], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [117, 36, 168, 137]
    }
785 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] System ticked
786 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] State: Get Sample
787 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Verify Quality of the Sample
788 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Logical Node : 0
789 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Get Sample -> Valid
790 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] System ticked
791 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] State: Valid

```



```

792 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 0
    value: -623
793 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 1
    value: -359
794 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 2
    value: 987
795 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 3
    value: 0
796 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 4
    value: -6285
797 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 5
    value: -3592
798 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 6
    value: 9878
799 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 7
    value: 0
800 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU2: 4
801 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Valid -> CompleteSample
802 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] System ticked
803 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] State: CompleteSample
804 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
805 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Mu0 after evaluation
806 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Time of work of thread is:
    83.372299ms
807 [2024-07-14T18:22:56Z INFO sub_with_fsm_iec] Mu0 before evaluation
808 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2132],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [525], q_ia: [0], i_b: [-999], q_ib: [0], i_c: [476], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [5226], q_va: [0], v_b: [-9996], q_vb: [0], v_c:
    [4772], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [242, 100, 169, 122]
    }
809 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2132],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [525], q_ia: [0], i_b: [-999], q_ib: [0], i_c: [476], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [5226], q_va: [0], v_b: [-9996], q_vb: [0], v_c:
    [4772], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [242, 100, 169, 122]
    }
810 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] System ticked
811 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] State: Get Sample
812 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Verify Quality of the Sample
813 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Logical Node : 0
814 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Get Sample -> Valid
815 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] System ticked
816 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] State: Valid

```

```

817 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 0
      value: 525
818 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 1
      value: -999
819 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 2
      value: 476
820 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 3
      value: 0
821 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 4
      value: 5226
822 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 5
      value: -9996
823 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 6
      value: 4772
824 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 7
      value: 0
825 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] The value of
      counter_sample_valid_of_sv_id_MU1: 5
826 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Valid -> CompleteSample
827 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] System ticked
828 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] State: CompleteSample
829 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
830 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Mu0 after evaluation
831 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Time of work of thread is:
      416.174097ms
832 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Mu0 before evaluation
833 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Mu0 after evaluation
834 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Time of work of thread is:
      40.586331ms
835 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Mu0 before evaluation
836 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Received Ethernet Frame:
      EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
        17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
        SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
          [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
            no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
              [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2136],
                conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
                  smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
                    [-958], q_ia: [0], i_b: [235], q_ib: [0], i_c: [724], q_ic: [0], i_n:
                      [0], q_in: [0], v_a: [-9593], q_va: [0], v_b: [2355], q_vb: [0], v_c:
                        [7237], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [86, 167, 2, 210] }
837 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] frame inside FSM
      EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
        17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
        SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
          [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
            no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
              [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2136],
                conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
                  smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
                    [-958], q_ia: [0], i_b: [235], q_ib: [0], i_c: [724], q_ic: [0], i_n:
                      [0], q_in: [0], v_a: [-9593], q_va: [0], v_b: [2355], q_vb: [0], v_c:
                        [7237], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [86, 167, 2, 210] }
838 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] System ticked
839 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] State: Get Sample
840 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Verify Quality of the Sample
841 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Logical Node : 0
842 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Get Sample -> Valid

```

```

843 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] System ticked
844 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] State: Valid
845 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 0
      value: -958
846 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 1
      value: 235
847 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 2
      value: 724
848 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 3
      value: 0
849 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 4
      value: -9593
850 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 5
      value: 2355
851 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 6
      value: 7237
852 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 7
      value: 0
853 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] The value of
      counter_sample_valid_of_sv_id_MU2: 5
854 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Valid ->
      CheckErrorPercentage
855 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] System ticked
856 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] State: CheckErrorPercentage
857 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] buffer_mu1: [[871, 984, 995,
      922, 525], [-27, -353, -585, -798, -999], [-851, -632, -409, -121,
      476], [0, 0, 0, 0, 0], [8800, 9870, 9947, 9204, 5226], [-291, -3551,
      -5863, -7988, -9996], [-8508, -6315, -4080, -1213, 4772], [0, 0, 0, 0,
      0]]
858 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] buffer_mu2: [[314, -82,
      -381, -623, -958], [-978, -818, -607, -359, 235], [668, 907, 991, 987,
      724], [0, 0, 0, 0, 0], [3097, -892, -3844, -6285, -9593], [-9782,
      -8178, -6071, -3592, 2355], [6691, 9073, 9917, 9878, 7237], [0, 0, 0,
      0, 0]]
859 [2024-07-14T18:22:57Z WARN sub_with_fsm_iec] Failed acquisition value in
      the MU1
860 [2024-07-14T18:22:57Z WARN sub_with_fsm_iec] Failed acquisition value in
      the MU1
861 [2024-07-14T18:22:57Z WARN sub_with_fsm_iec] Failed acquisition value in
      the MU1
862 [2024-07-14T18:22:57Z WARN sub_with_fsm_iec] Failed acquisition value in
      the MU1
863 [2024-07-14T18:22:57Z WARN sub_with_fsm_iec] Failed acquisition value in
      the MU1
864 [2024-07-14T18:22:57Z WARN sub_with_fsm_iec] Failed acquisition value in
      the MU1
865 [2024-07-14T18:22:57Z WARN sub_with_fsm_iec] Failed acquisition value in
      the MU1
866 [2024-07-14T18:22:57Z WARN sub_with_fsm_iec] Failed acquisition value in
      the MU1
867 [2024-07-14T18:22:57Z WARN sub_with_fsm_iec] Failed acquisition value in
      the MU1
868 [2024-07-14T18:22:57Z WARN sub_with_fsm_iec] Failed acquisition value in
      the MU1
869 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of the sum of MU1:
      19.150064
870 [2024-07-14T18:22:57Z WARN sub_with_fsm_iec] Failed acquisition value in
      the MU2

```

```

871 [2024-07-14T18:22:57Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
872 [2024-07-14T18:22:57Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
873 [2024-07-14T18:22:57Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
874 [2024-07-14T18:22:57Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
875 [2024-07-14T18:22:57Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
876 [2024-07-14T18:22:57Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
877 [2024-07-14T18:22:57Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
878 [2024-07-14T18:22:57Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
879 [2024-07-14T18:22:57Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
880 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of the sum of MU2:
    -61.57344
881 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of error of MU1:
    0.4787516
882 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of error of MU2:
    1.539336
883 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of the error: 1.539336
884 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Actual State: CompleteCycle
885 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] System ticked
886 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] State: CompleteCycle
887 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] CompleteCycle -> GetSample
888 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Mu0 after evaluation
889 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Time of work of thread is:
    41.759234ms
890 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Mu0 before evaluation
891 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2133],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [235], q_ia: [0], i_b: [-957], q_ib: [0], i_c: [728], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [2294], q_va: [0], v_b: [-9576], q_vb: [0], v_c:
    [7284], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [133, 0, 24, 75] }
892 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2133],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [235], q_ia: [0], i_b: [-957], q_ib: [0], i_c: [728], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [2294], q_va: [0], v_b: [-9576], q_vb: [0], v_c:
    [7284], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [133, 0, 24, 75] }
893 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] System ticked
894 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] State: Get Sample

```

```

895 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Verify Quality of the Sample
896 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Logical Node : 0
897 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Get Sample -> Valid
898 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] System ticked
899 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] State: Valid
900 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 0
    value: 235
901 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 1
    value: -957
902 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 2
    value: 728
903 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 3
    value: 0
904 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 4
    value: 2294
905 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 5
    value: -9576
906 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 6
    value: 7284
907 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 7
    value: 0
908 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU1: 1
909 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Valid -> CompleteSample
910 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] System ticked
911 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] State: CompleteSample
912 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
913 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Mu0 after evaluation
914 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Time of work of thread is:
    414.905567ms
915 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Mu0 before evaluation
916 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2137],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [-950], q_ia: [0], i_b: [748], q_ib: [0], i_c: [199], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [-9475], q_va: [0], v_b: [7507], q_vb: [0], v_c:
    [1963], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [124, 8, 229, 226] }
917 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2137],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [-950], q_ia: [0], i_b: [748], q_ib: [0], i_c: [199], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [-9475], q_va: [0], v_b: [7507], q_vb: [0], v_c:
    [1963], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [124, 8, 229, 226] }
918 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] System ticked
919 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] State: Get Sample
920 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Verify Quality of the Sample
921 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Logical Node : 0

```

```

922 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Get Sample -> Valid
923 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] System ticked
924 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] State: Valid
925 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 0
    value: -950
926 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 1
    value: 748
927 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 2
    value: 199
928 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 3
    value: 0
929 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 4
    value: -9475
930 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 5
    value: 7507
931 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 6
    value: 1963
932 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 7
    value: 0
933 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU2: 1
934 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Valid -> CompleteSample
935 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] System ticked
936 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] State: CompleteSample
937 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
938 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Mu0 after evaluation
939 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Time of work of thread is:
    85.699797ms
940 [2024-07-14T18:22:57Z INFO sub_with_fsm_iec] Mu0 before evaluation
941 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2134],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [-270], q_ia: [0], i_b: [-695], q_ib: [0], i_c: [969], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [-2748], q_va: [0], v_b: [-6950], q_vb: [0], v_c:
    [9702], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [31, 142, 241, 254]
    }
942 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2134],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [-270], q_ia: [0], i_b: [-695], q_ib: [0], i_c: [969], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [-2748], q_va: [0], v_b: [-6950], q_vb: [0], v_c:
    [9702], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [31, 142, 241, 254]
    }
943 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] System ticked
944 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] State: Get Sample
945 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Verify Quality of the Sample
946 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Logical Node : 0

```

```

947 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Get Sample -> Valid
948 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] System ticked
949 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] State: Valid
950 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 0
    value: -270
951 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 1
    value: -695
952 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 2
    value: 969
953 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 3
    value: 0
954 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 4
    value: -2748
955 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 5
    value: -6950
956 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 6
    value: 9702
957 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 7
    value: 0
958 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU1: 2
959 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Valid -> CompleteSample
960 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] System ticked
961 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] State: CompleteSample
962 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
963 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Mu0 after evaluation
964 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Time of work of thread is:
    414.437569ms
965 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Mu0 before evaluation
966 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2138],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [-596], q_ia: [0], i_b: [993], q_ib: [0], i_c: [-400], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [-5934], q_va: [0], v_b: [9937], q_vb: [0], v_c:
    [-4005], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [73, 239, 55, 38] }
967 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2138],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [-596], q_ia: [0], i_b: [993], q_ib: [0], i_c: [-400], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [-5934], q_va: [0], v_b: [9937], q_vb: [0], v_c:
    [-4005], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [73, 239, 55, 38] }
968 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] System ticked
969 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] State: Get Sample
970 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Verify Quality of the Sample
971 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Logical Node : 0
972 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Get Sample -> Valid
973 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] System ticked

```

```

974 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] State: Valid
975 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 0
    value: -596
976 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 1
    value: 993
977 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 2
    value: -400
978 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 3
    value: 0
979 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 4
    value: -5934
980 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 5
    value: 9937
981 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 6
    value: -4005
982 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 7
    value: 0
983 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU2: 2
984 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Valid -> CompleteSample
985 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] System ticked
986 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] State: CompleteSample
987 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
988 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Mu0 after evaluation
989 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Time of work of thread is:
    85.223941ms
990 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Mu0 before evaluation
991 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Received Ethernet Frame:
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2135],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [-808], q_ia: [0], i_b: [-90], q_ib: [0], i_c: [907], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [-8180], q_va: [0], v_b: [-887], q_vb: [0], v_c:
    [9068], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [26, 149, 85, 246] }
992 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
    17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
    SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
    [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
    no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
    [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2135],
    conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
    smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
    [-808], q_ia: [0], i_b: [-90], q_ib: [0], i_c: [907], q_ic: [0], i_n:
    [0], q_in: [0], v_a: [-8180], q_va: [0], v_b: [-887], q_vb: [0], v_c:
    [9068], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [26, 149, 85, 246] }
993 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] System ticked
994 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] State: Get Sample
995 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Verify Quality of the Sample
996 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Logical Node : 0
997 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Get Sample -> Valid
998 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] System ticked
999 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] State: Valid

```



```

1000 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 0
      value: -808
1001 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 1
      value: -90
1002 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 2
      value: 907
1003 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 3
      value: 0
1004 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 4
      value: -8180
1005 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 5
      value: -887
1006 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 6
      value: 9068
1007 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 7
      value: 0
1008 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] The value of
      counter_sample_valid_of_sv_id_MU1: 3
1009 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Valid -> CompleteSample
1010 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] System ticked
1011 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] State: CompleteSample
1012 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
1013 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Mu0 after evaluation
1014 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Time of work of thread is:
      415.63286ms
1015 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Mu0 before evaluation
1016 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Received Ethernet Frame:
      EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
      17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
      SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
      [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
      no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
      [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2139],
      conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
      smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
      [-53], q_ia: [0], i_b: [888], q_ib: [0], i_c: [-842], q_ic: [0], i_n:
      [0], q_in: [0], v_a: [-455], q_va: [0], v_b: [8878], q_vb: [0], v_c:
      [-8426], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [57, 212, 78, 221]
      }
1017 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] frame inside FSM
      EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
      17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
      SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
      [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
      no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
      [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2139],
      conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
      smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
      [-53], q_ia: [0], i_b: [888], q_ib: [0], i_c: [-842], q_ic: [0], i_n:
      [0], q_in: [0], v_a: [-455], q_va: [0], v_b: [8878], q_vb: [0], v_c:
      [-8426], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [57, 212, 78, 221]
      }
1018 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] System ticked
1019 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] State: Get Sample
1020 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Verify Quality of the Sample
1021 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Logical Node : 0
1022 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Get Sample -> Valid
1023 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] System ticked
1024 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] State: Valid

```

```

1025 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 0
      value: -53
1026 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 1
      value: 888
1027 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 2
      value: -842
1028 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 3
      value: 0
1029 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 4
      value: -455
1030 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 5
      value: 8878
1031 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 6
      value: -8426
1032 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 7
      value: 0
1033 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] The value of
      counter_sample_valid_of_sv_id_MU2: 3
1034 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Valid -> CompleteSample
1035 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] System ticked
1036 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] State: CompleteSample
1037 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
1038 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Mu0 after evaluation
1039 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Time of work of thread is:
      83.993118ms
1040 [2024-07-14T18:22:58Z INFO sub_with_fsm_iec] Mu0 before evaluation
1041 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Mu0 after evaluation
1042 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Time of work of thread is:
      278.510854ms
1043 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Mu0 before evaluation
1044 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Mu0 after evaluation
1045 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Time of work of thread is:
      16.962microseconds
1046 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Mu0 before evaluation
1047 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Mu0 after evaluation
1048 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Time of work of thread is:
      4.279195ms
1049 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Mu0 before evaluation
1050 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Received Ethernet Frame:
      EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
      17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
      SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
      [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
      no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
      [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2136],
      conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
      smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
      [-999], q_ia: [0], i_b: [499], q_ib: [0], i_c: [499], q_ic: [0], i_n:
      [0], q_in: [0], v_a: [-9999], q_va: [0], v_b: [5007], q_vb: [0], v_c:
      [4987], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [225, 211, 40, 158]
      }

```

```

1051 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] frame inside FSM
    EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
      17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
      SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
        [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
        no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
        [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2136],
        conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
        smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
        [-999], q_ia: [0], i_b: [499], q_ib: [0], i_c: [499], q_ic: [0], i_n:
        [0], q_in: [0], v_a: [-9999], q_va: [0], v_b: [5007], q_vb: [0], v_c:
        [4987], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [225, 211, 40, 158]
    }
1052 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] System ticked
1053 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] State: Get Sample
1054 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Verify Quality of the Sample
1055 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Logical Node : 0
1056 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Get Sample -> Valid
1057 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] System ticked
1058 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] State: Valid
1059 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 0
    value: -999
1060 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 1
    value: 499
1061 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 2
    value: 499
1062 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 3
    value: 0
1063 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 4
    value: -9999
1064 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 5
    value: 5007
1065 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 6
    value: 4987
1066 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 7
    value: 0
1067 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] The value of
    counter_sample_valid_of_sv_id_MU1: 4
1068 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Valid -> CompleteSample
1069 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] System ticked
1070 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] State: CompleteSample
1071 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
1072 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Mu0 after evaluation
1073 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Time of work of thread is:
    129.567503ms
1074 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Mu0 before evaluation
1075 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Mu0 after evaluation
1076 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Time of work of thread is:
    10.144637ms
1077 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Mu0 before evaluation
1078 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Mu0 after evaluation
1079 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Time of work of thread is:
    1.35792ms
1080 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Mu0 before evaluation
1081 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Mu0 after evaluation
1082 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Time of work of thread is:
    3.24933ms
1083 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Mu0 before evaluation
1084 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Mu0 after evaluation

```

```

1085 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Time of work of thread is:
      10.81microseconds
1086 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Mu0 before evaluation
1087 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Received Ethernet Frame:
      EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
        17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
        SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
          [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
            no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
              [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2140],
                conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
                  smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
                    [553], q_ia: [0], i_b: [441], q_ib: [0], i_c: [-997], q_ic: [0], i_n:
                      [0], q_in: [0], v_a: [5567], q_va: [0], v_b: [4407], q_vb: [0], v_c:
                        [-9977], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [149, 110, 218, 79]
              }
1088 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] frame inside FSM
      EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
        17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
        SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
          [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
            no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
              [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2140],
                conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
                  smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
                    [553], q_ia: [0], i_b: [441], q_ib: [0], i_c: [-997], q_ic: [0], i_n:
                      [0], q_in: [0], v_a: [5567], q_va: [0], v_b: [4407], q_vb: [0], v_c:
                        [-9977], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [149, 110, 218, 79]
              }
1089 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] System ticked
1090 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] State: Get Sample
1091 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Verify Quality of the Sample
1092 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Logical Node : 0
1093 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Get Sample -> Valid
1094 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] System ticked
1095 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] State: Valid
1096 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 0
      value: 553
1097 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 1
      value: 441
1098 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 2
      value: -997
1099 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 3
      value: 0
1100 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 4
      value: 5567
1101 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 5
      value: 4407
1102 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 6
      value: -9977
1103 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 7
      value: 0
1104 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] The value of
      counter_sample_valid_of_sv_id_MU2: 4
1105 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Valid -> CompleteSample
1106 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] System ticked
1107 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] State: CompleteSample
1108 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
1109 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Mu0 after evaluation

```

```

1110 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Time of work of thread is:
      67.900748ms
1111 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Mu0 before evaluation
1112 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Received Ethernet Frame:
      EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
      17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
      SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
      [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
      no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
      [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2137],
      conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
      smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
      [-812], q_ia: [0], i_b: [913], q_ib: [0], i_c: [-105], q_ic: [0], i_n:
      [0], q_in: [0], v_a: [-8086], q_va: [0], v_b: [9138], q_vb: [0], v_c:
      [-1054], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [81, 228, 146, 142]
      }
1113 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] frame inside FSM
      EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
      17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
      SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
      [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
      no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
      [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2137],
      conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
      smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
      [-812], q_ia: [0], i_b: [913], q_ib: [0], i_c: [-105], q_ic: [0], i_n:
      [0], q_in: [0], v_a: [-8086], q_va: [0], v_b: [9138], q_vb: [0], v_c:
      [-1054], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [81, 228, 146, 142]
      }
1114 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] System ticked
1115 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] State: Get Sample
1116 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Verify Quality of the Sample
1117 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Logical Node : 0
1118 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Get Sample -> Valid
1119 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] System ticked
1120 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] State: Valid
1121 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 0
      value: -812
1122 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 1
      value: 913
1123 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 2
      value: -105
1124 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 3
      value: 0
1125 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 4
      value: -8086
1126 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 5
      value: 9138
1127 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 6
      value: -1054
1128 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 7
      value: 0
1129 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] The value of
      counter_sample_valid_of_sv_id_MU1: 5
1130 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Valid -> CompleteSample
1131 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] System ticked
1132 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] State: CompleteSample
1133 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
1134 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Mu0 after evaluation

```

```

1135 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Time of work of thread is:
      411.944223ms
1136 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Mu0 before evaluation
1137 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Received Ethernet Frame:
      EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
        17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
        SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
          [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
            no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
              [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2141],
                conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
                  smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
                    [935], q_ia: [0], i_b: [-167], q_ib: [0], i_c: [-769], q_ic: [0], i_n:
                      [0], q_in: [0], v_a: [9376], q_va: [0], v_b: [-1678], q_vb: [0], v_c:
                        [-7697], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [34, 206, 122, 81]
        }
1138 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] frame inside FSM
      EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
        17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
        SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
          [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
            no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
              [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2141],
                conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
                  smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
                    [935], q_ia: [0], i_b: [-167], q_ib: [0], i_c: [-769], q_ic: [0], i_n:
                      [0], q_in: [0], v_a: [9376], q_va: [0], v_b: [-1678], q_vb: [0], v_c:
                        [-7697], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [34, 206, 122, 81]
        }
1139 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] System ticked
1140 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] State: Get Sample
1141 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Verify Quality of the Sample
1142 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Logical Node : 0
1143 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Get Sample -> Valid
1144 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] System ticked
1145 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] State: Valid
1146 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 0
      value: 935
1147 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 1
      value: -167
1148 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 2
      value: -769
1149 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 3
      value: 0
1150 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 4
      value: 9376
1151 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 5
      value: -1678
1152 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 6
      value: -7697
1153 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 7
      value: 0
1154 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] The value of
      counter_sample_valid_of_sv_id_MU2: 5
1155 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Valid ->
      CheckErrorPercentage
1156 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] System ticked
1157 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] State: CheckErrorPercentage

```

```

1158 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] buffer_mu1: [[235, -270,
    -808, -999, -812], [-957, -695, -90, 499, 913], [728, 969, 907, 499,
    -105], [0, 0, 0, 0, 0], [2294, -2748, -8180, -9999, -8086], [-9576,
    -6950, -887, 5007, 9138], [7284, 9702, 9068, 4987, -1054], [0, 0, 0, 0,
    0]]
1159 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] buffer_mu2: [[-950, -596,
    -53, 553, 935], [748, 993, 888, 441, -167], [199, -400, -842, -997,
    -769], [0, 0, 0, 0, 0], [-9475, -5934, -455, 5567, 9376], [7507, 9937,
    8878, 4407, -1678], [1963, -4005, -8426, -9977, -7697], [0, 0, 0, 0,
    0]]
1160 [2024-07-14T18:22:59Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
1161 [2024-07-14T18:22:59Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
1162 [2024-07-14T18:22:59Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
1163 [2024-07-14T18:22:59Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
1164 [2024-07-14T18:22:59Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
1165 [2024-07-14T18:22:59Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
1166 [2024-07-14T18:22:59Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
1167 [2024-07-14T18:22:59Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
1168 [2024-07-14T18:22:59Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
1169 [2024-07-14T18:22:59Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU1
1170 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of the sum of MU1:
    -51.52102
1171 [2024-07-14T18:22:59Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
1172 [2024-07-14T18:22:59Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
1173 [2024-07-14T18:22:59Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
1174 [2024-07-14T18:22:59Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
1175 [2024-07-14T18:22:59Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
1176 [2024-07-14T18:22:59Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
1177 [2024-07-14T18:22:59Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
1178 [2024-07-14T18:22:59Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
1179 [2024-07-14T18:22:59Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
1180 [2024-07-14T18:22:59Z WARN sub_with_fsm_iec] Failed acquisition value in
    the MU2
1181 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of the sum of MU2:
    -14.840608
1182 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of error of MU1:
    1.2880255
1183 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of error of MU2:
    0.3710152

```

```

1184 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Value of the error:
      1.2880255
1185 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Actual State: ToogleMU
1186 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] System ticked
1187 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] State: ToogleMU
1188 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Toogle_MU before is : false
1189 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Toogle_MU after is : true
1190 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] ToogleMU -> CompleteCycle
1191 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] System ticked
1192 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] State: CompleteCycle
1193 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] CompleteCycle -> GetSample
1194 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Mu0 after evaluation
1195 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Time of work of thread is:
      87.513681ms
1196 [2024-07-14T18:22:59Z INFO sub_with_fsm_iec] Mu1 before evaluation
1197 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Received Ethernet Frame:
      EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
        17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
        SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
          [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
            no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
              [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2138],
                conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
                  smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
                    [-327], q_ia: [0], i_b: [980], q_ib: [0], i_c: [-660], q_ic: [0], i_n:
                      [0], q_in: [0], v_a: [-3201], q_va: [0], v_b: [9804], q_vb: [0], v_c:
                        [-6610], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [178, 253, 62, 186]
        }
1198 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] frame inside FSM
      EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
        17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
        SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
          [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
            no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
              [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2138],
                conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
                  smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
                    [-327], q_ia: [0], i_b: [980], q_ib: [0], i_c: [-660], q_ic: [0], i_n:
                      [0], q_in: [0], v_a: [-3201], q_va: [0], v_b: [9804], q_vb: [0], v_c:
                        [-6610], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [178, 253, 62, 186]
        }
1199 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] System ticked
1200 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] State: Get Sample
1201 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Verify Quality of the Sample
1202 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Logical Node : 0
1203 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Get Sample -> Valid
1204 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] System ticked
1205 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] State: Valid
1206 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 0
      value: -327
1207 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 1
      value: 980
1208 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 2
      value: -660
1209 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 3
      value: 0
1210 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 4
      value: -3201

```



```

1211 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 5
      value: 9804
1212 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 6
      value: -6610
1213 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 7
      value: 0
1214 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] The value of
      counter_sample_valid_of_sv_id_MU1: 1
1215 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Valid -> CompleteSample
1216 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] System ticked
1217 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] State: CompleteSample
1218 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
1219 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Mu1 after evaluation
1220 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Time of work of thread is:
      413.770782ms
1221 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Mu1 before evaluation
1222 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Received Ethernet Frame:
      EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
      17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
      SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
      [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
      no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
      [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2142],
      conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
      smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
      [994], q_ia: [0], i_b: [-588], q_ib: [0], i_c: [-405], q_ic: [0], i_n:
      [0], q_in: [0], v_a: [9943], q_va: [0], v_b: [-5893], q_vb: [0], v_c:
      [-4045], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [130, 133, 232, 46]
      }
1223 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] frame inside FSM
      EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
      17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
      SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
      [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
      no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
      [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2142],
      conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
      smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
      [994], q_ia: [0], i_b: [-588], q_ib: [0], i_c: [-405], q_ic: [0], i_n:
      [0], q_in: [0], v_a: [9943], q_va: [0], v_b: [-5893], q_vb: [0], v_c:
      [-4045], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [130, 133, 232, 46]
      }
1224 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] System ticked
1225 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] State: Get Sample
1226 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Verify Quality of the Sample
1227 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Logical Node : 0
1228 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Get Sample -> Valid
1229 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] System ticked
1230 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] State: Valid
1231 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 0
      value: 994
1232 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 1
      value: -588
1233 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 2
      value: -405
1234 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 3
      value: 0
1235 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 4
      value: 9943

```

```

1236 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 5
      value: -5893
1237 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 6
      value: -4045
1238 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 7
      value: 0
1239 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] The value of
      counter_sample_valid_of_sv_id_MU2: 1
1240 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Valid -> CompleteSample
1241 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] System ticked
1242 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] State: CompleteSample
1243 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
1244 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Mu1 after evaluation
1245 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Time of work of thread is:
      84.714773ms
1246 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Mu1 before evaluation
1247 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Received Ethernet Frame:
      EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
        17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
        SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
          [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
            no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
              [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2139],
                conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
                  smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
                    [312], q_ia: [0], i_b: [659], q_ib: [0], i_c: [-980], q_ic: [0], i_n:
                      [0], q_in: [0], v_a: [3215], q_va: [0], v_b: [6590], q_vb: [0], v_c:
                        [-9809], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [247, 57, 60, 246]
        }
1248 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] frame inside FSM
      EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
        17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
        SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
          [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
            no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
              [128, 4], sv_id: [875573296], smp_cnt_asn: [130, 2], smp_cnt: [2139],
                conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
                  smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
                    [312], q_ia: [0], i_b: [659], q_ib: [0], i_c: [-980], q_ic: [0], i_n:
                      [0], q_in: [0], v_a: [3215], q_va: [0], v_b: [6590], q_vb: [0], v_c:
                        [-9809], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [247, 57, 60, 246]
        }
1249 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] System ticked
1250 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] State: Get Sample
1251 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Verify Quality of the Sample
1252 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Logical Node : 0
1253 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Get Sample -> Valid
1254 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] System ticked
1255 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] State: Valid
1256 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 0
      value: 312
1257 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 1
      value: 659
1258 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 2
      value: -980
1259 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 3
      value: 0
1260 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 4
      value: 3215

```

```

1261 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 5
      value: 6590
1262 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 6
      value: -9809
1263 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 1 fase: 7
      value: 0
1264 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] The value of
      counter_sample_valid_of_sv_id_MU1: 2
1265 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Valid -> CompleteSample
1266 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] System ticked
1267 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] State: CompleteSample
1268 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
1269 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Mu1 after evaluation
1270 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Time of work of thread is:
      412.867674ms
1271 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Mu1 before evaluation
1272 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Received Ethernet Frame:
      EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
        17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
        SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
          [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
            no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
              [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2143],
                conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
                  smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
                    [913], q_ia: [0], i_b: [-816], q_ib: [0], i_c: [-90], q_ic: [0], i_n:
                      [0], q_in: [0], v_a: [9075], q_va: [0], v_b: [-8176], q_vb: [0], v_c:
                        [-892], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [139, 13, 105, 218]
        }
1273 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] frame inside FSM
      EthernetFrame { destination: [1, 12, 205, 4, 255, 255], source: [0, 26,
        17, 0, 0, 1], tpid: 33024, tci: 32768, ethertype: 35002, payload:
        SvPDU { appid: [64, 1], length: [0, 102], reserved1: [0, 0], reserved2:
          [0, 0], apdu: SmvData { sav_pdu_asn: [96, 92], no_asdu_asn: [128, 1],
            no_asdu: 1, seq_asdu_asn: [162, 87], asdu_asn: [48, 85], sv_id_asn:
              [128, 4], sv_id: [875573297], smp_cnt_asn: [130, 2], smp_cnt: [2143],
                conf_rev_asn: [131, 4], conf_rev: [1], smp_synch_asn: [133, 1],
                  smp_synch: 1, seq_data: [135, 64], logical_node: LogicalNode { i_a:
                    [913], q_ia: [0], i_b: [-816], q_ib: [0], i_c: [-90], q_ic: [0], i_n:
                      [0], q_in: [0], v_a: [9075], q_va: [0], v_b: [-8176], q_vb: [0], v_c:
                        [-892], q_vc: [0], v_n: [0], q_vn: [0] } } }, fcs: [139, 13, 105, 218]
        }
1274 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] System ticked
1275 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] State: Get Sample
1276 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Verify Quality of the Sample
1277 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Logical Node : 0
1278 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Get Sample -> Valid
1279 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] System ticked
1280 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] State: Valid
1281 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 0
      value: 913
1282 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 1
      value: -816
1283 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 2
      value: -90
1284 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 3
      value: 0
1285 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 4
      value: 9075

```

```

1286 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 5
      value: -8176
1287 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 6
      value: -892
1288 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Value of Buffer MU 2 fase: 7
      value: 0
1289 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] The value of
      counter_sample_valid_of_sv_id_MU2: 2
1290 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Valid -> CompleteSample
1291 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] System ticked
1292 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] State: CompleteSample
1293 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] CompleteSample -> GetSample
1294 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Mu1 after evaluation
1295 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Time of work of thread is:
      86.007624ms
1296 [2024-07-14T18:23:00Z INFO sub_with_fsm_iec] Mu1 before evaluation
1297 ^C[2024-07-14T18:23:01Z ERROR sub_with_fsm_iec] An error occurred while
      reading: Interrupted system call (os error 4)
1298 [2024-07-14T18:23:01Z INFO sub_with_fsm_iec] Mu1 after evaluation
1299 [2024-07-14T18:23:01Z INFO sub_with_fsm_iec] Time of work of thread is:
      333.169445ms
1300 [2024-07-14T18:23:01Z INFO sub_with_fsm_iec] Received Ctrl+C, shutting
      down.

```

ch6/assets/test_of_sub_with_fsm_iec61850_9_2.txt

Chapter 7

Conclusion

7.1 Limitations

This project has its limitations, as the typical environment for a Merging Unit involves fiber optic communications at rates of 1 Gbps or higher, along with switches capable of high transfer rates and extremely low latencies. These conditions are crucial because Merging Units need to deliver samples every 250 microseconds. As a result, the latency must be less than this value to ensure timely packet delivery. However, in this setup, the time between sending and receiving packets exceeds 250 microseconds. Although the publisher transmits information every 250 microseconds, the subscriber receives it after a longer delay due to the latency of the setup I was able to develop. While no packets are lost, the reading speed is slower than desired, with the subscriber receiving data beyond the 250-microsecond target.

Another limitation is the synchronization between the publisher and the subscriber. Currently, the devices are synchronized via Network Time Protocol (NTP), providing minimal synchronization. However, the error margin with NTP is about 1 millisecond. Since we are dealing with samples in the microsecond range, NTP does not offer the precision required for accurate synchronization. Achieving higher precision would require the implementation of Precision Time Protocol (PTP), which provides resolution in the nanosecond range.

Finally, there is a hardware platform limitation. The devices used were a Jetson Nano 4GB and a personal computer, both of which come with inherent performance constraints, especially concerning Ethernet network performance. In both cases, it was necessary to add a USB-to-Ethernet adapter to provide two Ethernet ports for communication between the publisher/algorithm and the algorithm/subscriber.

7.2 Conclusions and Final Considerations

This project originated from a critical need in the energy industry. As substations evolve into the digital age, merging units have been introduced to digitize the acquisition of current and voltage measurements. Today, redundancy in communication networks ensures that if one network fails, data samples and communications seamlessly continue over an alternate network, safeguarding the integrity of the substation's protection systems.

Similarly, the concept of redundancy was applied to Sampled Values (SVs). Two different devices acquire the same analog data and publish it digitally. In this setup, two merging units simultaneously measure the same current and voltage transformers and publish

the data. This enables the protection system to select one of the two samples for its algorithms, discarding the other. Currently, no selection mechanism exists, and only the first merging unit's sample is used. The second unit's sample is only considered if the first fails.

In response to these market challenges, this thesis focused on developing an algorithm that selects the best sample from two merging units measuring the same physical quantities, such as current and voltage, rather than defaulting to one unit. By comparing and choosing the optimal signal, the system not only provides a reliable backup but also improves the accuracy and efficiency of protective relays. This approach enhances decision-making in electrical protection systems, ultimately improving overall reliability and performance.

The development of a publisher and subscriber became necessary due to the lack of existing libraries for the IEC61850 protocol. This project opens the door for the use of the RUST programming language in creating digital-era equipment like Merging Units and Protection Relays. During my research, I found libraries available in languages such as C/C++, C#, Java, Python, and Go. However, since no library existed for RUST, it was essential to build these components from the ground up, resulting in a solid and well-structured foundation that adheres to the IEC61850 standard.

The features implemented cover the core functionality of a Merging Unit, including the reading of analog values, which are automatically generated based on time with a fixed amplitude. This allows for value emulation, with the possibility of integrating an ADC (Analog to Digital Converter) in the future for real analog acquisition. The system also includes the creation and transmission of SV packets, though it currently lacks a more accurate time synchronization protocol. Presently, the setup uses NTP for time acquisition, but PTP, which offers greater precision and complies with IEC61850-9-2, would be the ideal solution.

In terms of protection relays, basic functionality was established, including the reception of SV packets. However, further development is needed to create a fully functional protection relay. The starting point for such a device is acquiring the SVs, after which data processing, protection algorithms, and the necessary actions, like operating the circuit breaker, can be applied.

In summary, this project represents a major step toward developing a system that, with further refinement, could be transformed into a product ready for use in the energy industry. These two components play key roles in the operation, maintenance, and prevention of issues within substations. This project introduces a new way of developing products using a previously untapped language in this domain, offering substantial value to the broader community.

7.3 Future Work

7.3.1 Add an ADC to acquire values of Voltage Transformer and Current Transformer

According to (Laporte-Fauret et al. 2018), the authors examine the challenge of determining the appropriate resolution for an Analog-to-Digital Converter (ADC) when simultaneously receiving two signals of varying power levels—one weak and one strong.

Traditionally, ADC performance is evaluated based on the digitization of a single signal, where quantization noise and the signal-to-noise ratio (SNR) are the primary concerns. However, this approach does not fully capture the complexity of scenarios where two signals with a large dynamic range are present, which is increasingly relevant in modern communication systems like the Internet of Things (IoT).

The (Laporte-Fauret et al. 2018) critiques previous methods of evaluating ADC resolution, particularly formulas designed for single-signal reception, which often underestimate the impact of a second, stronger signal on the ADC's performance. It also evaluates an existing technique that provides overestimated resolution requirements when two signals are processed, indicating a gap in accuracy. To address these limitations, the authors propose a novel method to calculate the required ADC resolution, focusing on how the interaction between the weak and strong signals can actually enhance the dynamic range, allowing for better performance than predicted by older models.

Through mathematical analysis and simulations, the paper demonstrates that the required resolution for an ADC increases when dealing with two signals compared to a single signal. This is because the weaker signal must be accurately detected in the presence of the stronger one, a task complicated by the ADC's finite dynamic range. The authors show that their proposed method provides a more accurate evaluation of the necessary resolution, resulting in a dynamic range that exceeds the theoretical limits for a single-tone signal(Laporte-Fauret et al. 2018).

Furthermore, the paper discusses how this enhanced dynamic range, though beneficial, is still not sufficient for many modern applications, particularly in the IoT domain, where systems may require dynamic ranges of up to 130 dB. Current ADC technology, limited to 12 or 14 bits of resolution, cannot achieve such high performance. The authors suggest that alternative methods, such as companding techniques, might be necessary to overcome these limitations in future ADC designs(Laporte-Fauret et al. 2018).

This article provides a comprehensive analysis of ADC resolution in dual-signal scenarios, offering valuable guidance for designing ADCs with improved dynamic range performance, especially in systems where both weak and strong signals are processed simultaneously, which has application in our scenario(Laporte-Fauret et al. 2018).

7.3.2 Add a PTP server regarding the IEC61850-9-3-PTP

Substations have evolved over the years and transitioned into the digital era, synchronization protocols have become increasingly essential to ensure the proper alignment of IED (Intelligent Electronic Device) events. This synchronization allows for an accurate understanding of the event sequence in case of a fault, providing clarity on what occurred at the substation. When all devices are synchronized to a common time source, it becomes possible to interpret events chronologically. The introduction of the IEC 61850 protocol established several options for generating the master clock, including IRIG-B, DCF 77, 1PPS, Serial ASCII, NTP, and PTP.

Among these, only NTP and PTP can use the existing Ethernet network for synchronization, while the others require separate electrical wiring. This made NTP popular and widely adopted as a "standard" synchronization protocol because it leverages the same Ethernet network used by IEC 61850 and offers sufficient resolution with millisecond accuracy, which was adequate for most substation applications before the advent of

Merging Units. NTP was sufficient for other substation events like GOOSE, MMS, and signaling.

However, the introduction of PTP (Precision Time Protocol) brought higher precision, which became necessary with the use of Sampled Values, Synchrophasor measurements, and Travelling Wave Fault Location. These applications demand precision at the level of 100 microseconds or better, down to 1 microsecond, with PTP providing nanosecond-level accuracy. Consequently, PTP became essential for synchronization only after these advanced applications were implemented, and it was incorporated into the IEC 61850 standard starting in 2015. Further improvements were made with PTPv3 in 2019, which is compatible with PTPv2.

Looking ahead, there is an opportunity to enhance this project by implementing PTP to align the publisher with the IEC 61850-9-3 protocol. This will ensure the required time resolution for the Sampled Values published by the merging unit developed in this thesis (Baumgartner, Riesch, and Schenk n.d.).

7.3.3 Implement a more secure Sampled Value (SV) packet in modern substations

SV packets are critical in IEC 61850 substation automation systems (SAS), used to transmit digitized current and voltage measurements between various devices, such as Merging Units (MUs), Protection IEDs, and Control IEDs. These packets enable real-time decision-making to protect and control the grid infrastructure. However, as modern substations adopt networked communication, SV packets are exposed to various cybersecurity risks. Vulnerabilities, such as replay attacks and masquerade attacks, pose significant threats to the integrity of these messages, potentially leading to malfunctions in protection relays and equipment failures(Hussain et al. 2023).

The need for secure SV messages in automated substations stems from the following requirements:

- Confidentiality: Ensuring that the data in SV packets cannot be accessed or altered by unauthorized entities.
- Integrity: Guaranteeing that the SV packet content has not been tampered with during transmission.
- Authentication: Confirming that the SV message originated from a legitimate source.
- Timeliness: Ensuring that security measures do not introduce delays that would impact the system's ability to respond to faults in real-time(Hussain et al. 2023).

So implement a more secure way the SV packets is possible thorough this 4 principles, Message Authentication Code (MAC), Encryption of SV Payload, Timestamping for replay attack mitigation and extension fields for security mechanism following by order:

- Message Authentication Codes (MAC): A Message Authentication Code (MAC) provides a way to ensure both the integrity and authentication of SV messages. A MAC is generated using a cryptographic algorithm based on the contents of the message and a shared secret key between the publisher (Merging Unit) and subscriber (Protection IED)(Hussain et al. 2023).

- **Encryption of SV Payload:** Encryption ensures confidentiality, preventing unauthorized entities from reading the SV message contents. Advanced Encryption Standard (AES-GCM) is recommended for securing SV messages, as it supports both encryption and authentication in one operation(Hussain et al. 2023).
- **Timestamping for Replay Attack Mitigation:** Replay attacks involve capturing legitimate SV packets and resending them to trick the system into accepting outdated data as current. To mitigate this, each SV message must carry a timestamp that reflects the time the message was created(Hussain et al. 2023).
- **Extension Fields for Security Mechanisms:** Modifications to the SV message frame are required to support these security mechanisms. The IEC 61850-9-2 message format allows for an Extension field, which can be used to carry MAC values, encrypted payloads, and timestamps(Hussain et al. 2023).

Implementing a secure SV messaging scheme in IEC 61850 substations is essential to protect against modern cyber threats like replay and masquerade attacks. The combination of MAC for integrity and authentication, AES-GCM for encryption, and timestamping for replay attack prevention ensures that SV packets are protected against tampering and unauthorized access. While these enhancements increase the packet size and computational overhead, tests show that they can be implemented without compromising the real-time performance of protection systems. With the right key management practices and adherence to the IEC 62351 standard, secure SV messaging can significantly enhance the resilience and safety of automated substations(Hussain et al. 2023).

Bibliography

- Adamiak, Mark, Drew Baigent, and Ralph Mackiewicz (2009). "IEC 61850 Communication Networks and Systems In Substations: An Overview for Users". In: *Protection & Control Journal*. URL: <https://www.gegridsolutions.com/multilin/journals/issues/spring09/iec61850.pdf>.
- (n.d.). "IEC 61850 Communication Networks and Systems in Substations: An Overview for Users". In: (). URL: <https://www.gevernova.com/grid-solutions/multilin/journals/issues/spring09/iec61850.pdf>.
- Baumgartner, Bernhard, Christian Riesch, and Wolfgang Schenk (n.d.). "IEC 61850-9-3: Will Simplicity Supersede Complexity?" In: (). URL: https://www.omicron-lab.com/fileadmin/assets/Precision-Timing/Knowledge_Applications/Article_IEC_61850-9-3/IEC_61850-9-3_-_Will_simplicity_supersede_complexity_.pdf.
- Bettler, John, Ryan Mcdaniel, and David Bowen (2022). "Performance of IEC 61850 Sampled Values Relays for a Real-World Fault". In: *49th Annual Western Protective Relay Conference*. URL: <https://esic.wsu.edu/documents/2023/10/western-protective-relay-conference-2022-performance-of-iec-61850-sampled-values-relays-for-a-real-world-fault.pdf/>.
- Blair, Steven M. et al. (2013). "An Open Platform for Rapid-Prototyping Protection and Control Schemes with IEC 61850". In: URL: <https://ieeexplore.ieee.org/document/6479251>.
- Blog, Tekvel (2024). *Disrespectful Sampled Values subscriber behaviour*. Accessed: 2024-08-15. URL: <https://tekvel.com/en/web/blog/post/disrespectful-sv-subscriber-behaviour/>.
- Chen, Xi (2016). "Performance Analysis of IEC 61850 Process Bus and Interoperability Test among Multi-Vendor System". PhD thesis. URL: <https://research.manchester.ac.uk/en/studentTheses/performance-analysis-of-iec-61850-process-bus-and-interoperabilit>.
- Comission, International Electrotechnical (2003). *IEC 61850 Communication Networks and Systems for Power Utility Automation*. Tech. rep. International Electrotechnical Commission (IEC). URL: <https://webstore.iec.ch/publication/6028>.
- Galkin, Nikolai et al. (2023). "Microcomputer Prototyping of IEC61850-9-2 with Performance Analysis". In: URL: <https://ltu.diva-portal.org/smash/record.jsf?pid=diva2%3A1825382%5C&dswid=-5158>.
- Hariri, Mohamad El et al. (2019). "The IEC 61850 Sampled Measured Values Protocol: Analysis, Threat Identification, and Feasibility of Using NN Forecasters to Detect Spoofed Packets". In: URL: <https://ieeexplore.ieee.org/document/8783253>.
- Hussain, S. M. Suhail et al. (2023). "An Effective Security Scheme for Attacks on Sample Value Messages in IEC 61850 Automated Substations". In: *IEEE Open Access Journal of Power and Energy* 10, pp. 304–315. DOI: 10.1109/OAJPE.2023.3255790.
- Konka, Jakub W. et al. (2011). "Traffic Generation of IEC 61850 Sampled Values". In: URL: <https://personal.strath.ac.uk/robert.c.atkinson/papers/sgms2011.pdf>.

- Kumar, Shantanu et al. (2023). "Review of the Legacy and Future of IEC 61850 Protocols Encompassing Substation Automation System". In: *Electronics* 12.15. ISSN: 2079-9292. DOI: 10.3390/electronics12153345. URL: <https://www.mdpi.com/2079-9292/12/15/3345>.
- Laporte-Fauret, Baptiste et al. (2018). "ADC Resolution for Simultaneous Reception of Two Signals with High Dynamic Range". In: *2018 25th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, pp. 729–732. DOI: 10.1109/ICECS.2018.8617945.
- Leupp, Peter and Claes Ryttoft (2010). *Special Report IEC61850*. Tech. rep. Zurich, Switzerland: ABB. URL: https://library.e.abb.com/public/a56430e1e7c06fdcf12577a00043ab8b/3BSE063756_en_ABB_Review_Special_Report_IEC_61850.pdf.
- Mackiewicz, R.E. (2006). "Overview of IEC 61850 and Benefits". In: *2006 IEEE PES Power Systems Conference and Exposition*, pp. 623–630. DOI: 10.1109/PSCE.2006.296392.
- Ren, Xiang et al. (2022). "A New Differential Protection for Transmission Lines Connecting Renewable Energy Sources to MMC-HVDC Converter Stations Based on Dynamic Time Warping Algorithm". In: URL: <https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=%5C&arnumber=9952282>.
- Ribeiro, R.R.R. (2010). *Estudo da Norma IEC 61850*. Tech. rep. Campina Grande, Brazil: Universidade Federal de Campina Grande. URL: <http://dspace.sti.ufcg.edu.br:8080/jspui/bitstream/riufcg/18130/1/RODOLPHO%20RATHGE%20RANGEL%20RIBEIRO%20-%20TCC%20ENG.%20EL%C3%89TRICA%202010.pdf>.
- Saraiva, Diogo Emanuel Morgado (2018). "IEC 61850 Routable GOOSE and SV profiles over IP Telecom Networks". MA thesis. Aveiro, Portugal: Universidade de Aveiro. URL: <https://ria.ua.pt/handle/10773/25970>.
- Skendzic, Veselin, Ian Ender, Greg Zweigle, et al. (2007). "IEC 61850-9-2 process bus and its impact on power system protection and control reliability". In: *proceedings of the 9th Annual Western Power Delivery Automation Conference, Spokane, WA*. URL: <https://selinc.com/api/download/3479/>.
- Starck, Janne, Wolfgang Wimmer, and Karol Majer (2013). "Switchgear optimization using IEC 61850-9-2". In: *22nd International Conference and Exhibition on Electricity Distribution (CIRED 2013)*, pp. 1–4. DOI: 10.1049/cp.2013.0616.
- Stéphane, M. and T. Jean-Marc (2021). "Real-Time Performance and Security of IEC 61850 Process Bus Communications". In: URL: <https://hal.science/hal-03192264/file/5711-Research%20Article-23495-1-10-20210407.pdf>.
- Tibor, C. (2022). *History of IEC 61850 Sampled Values*. URL: <https://www.linkedin.com/pulse/history-iec-61850-sampled-values-tibor-congo/>.
- UCA International Users Group (2024). *Implementation Guideline for Digital Interface to Instrument Transformers Using IEC 61850-9-2*. Tel: +919-847-2241, Fax: +919-847-2939. UCA International Users Group. 10604 Candler Falls Court, Raleigh, NC 27614. URL: <http://www.ucainternational.org>.
- Wannous, Kinan and Petr Toman (2019). "Sharing Sampled Values Between Two Protection Relays According to Standard IEC 61850-9-2LE". In: URL: <https://www.mdpi.com/1996-1073/12/9/1618>.
- Wannous, Kinan, Petr Toman, Viktor Jurák, et al. (2019a). "Analysis of IEC 61850-9-2LE Measured Values Using a Neural Network". In: URL: <https://www.mdpi.com/1996-1073/12/9/1618>.

- (2019b). “Analysis of IEC 61850-9-2LE Measured Values Using a Neural Network”. In: *Energies* 12.9. DOI: 10.3390/en12091618. URL: <https://www.mdpi.com/1996-1073/12/9/1618>.
- Wei-ming, Wang, Duan Xiong-ying, and Luo Yan (2011). “The Research and Development of an Intelligent Merging Unit Based on IEC61850-9-2”. In: URL: <https://ieeexplore.ieee.org/document/5994084>.
- Yang, Qiaoyin et al. (2017). “Testing IEC 61850 Merging Units”. In: *44th Annual Western Protective Relay Conference*.
- Yang, Yanting et al. (2015). “Asynchronous Track-to-Track Association Algorithm Based on Dynamic Time Warping Distance”. In: *Journal of Information Fusion*. URL: <https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=%5C&arnumber=7260378>.
- Zhao, Pengcheng (2012). “IEC 61850-9-2 Process Bus Communication Interface for Light Weight Merging Unit Testing Environment”. MA thesis. Stockholm, Sweden: KTH Royal Institute of Technology.