The Research and Development of an Intelligent Merging Unit Based on IEC61850-9-2

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Abstract—**Merging unit (MU) is an important intelligent electronic device (IED) in digital substation and becomes research emphasis. The function of an MU is to collect multi-channel digital signals output by electronic current transformers (ECT) and electronic voltage transformers (EVT) synchronously, and transmit these signals with the protocol of IEC61850 to protective devices and measure-control devices. Compared with IEC61850-9-1, IEC61850-9-2 has more flexible frame format. It means the meaning of each channel and the quantity of the channels can be both customized. Moreover, 9-2 supports not only unicast but also multicast. This paper gives an information model of merging unit which informs us how the MU operates. Besides, it introduces a realization method of sample pulse synchronization, sample values (SV) receiving, processing and transmitting based on Field-Programmable Gate Array (FPGA) EP3C25Q240C8, 10/100 Mbps Ethernet controller LAN9215 and 100 Mbps integrated physical layer chip ICS1889 in detail. This method simplifies circuit design and enhances circuit stability. Data frames transmitted by the MU follow the protocol of 9-2 and can be switched between the interfaces of fiber optic with ST connector and electrical system with RJ45 connector in terms of actual needs. The data frames can be captured and analyzed by MMS ethereal software which supports 9-2 protocol. The test results demonstrate the utility and flexibility of the MU.**

Keywords-merging unit; FPGA; information model; IEC61850-9-2; function test

I. INTRODUCTION

Smart grid has been the developing direction around the world, and has been followed with extensive interest and research for the past few years. It contains power generation, power transformation, power transmission, power distribution and so on. Smart grid takes advantage of new technologies to meet the needs of security, reliability, economy, power quality, environmental protection and so on for power supply.

Digital substation which is an important part of smart grid adopts intelligent electronic devices to achieve digitization of information, network of communication platform and standardization of information sharing.

With the development of large capacity, extra-high voltage and ultra-high voltage power system, the conventional electromagnetic transformers which have many weak points are difficult to meet the application needs of power system. As the intelligent electronic devices of digital substation, the new electronic transformers have broad application prospects[1]. Compared with conventional electromagnetic transformers, electronic transformers have the excellent features of small cubage, light weight, excellent insulation, non saturation, wide-band response, digitization and so on. At the present time, electronic transformers based on optics and Rogowski coil have entered a practical stage.

Merging unit which is the applied foundation of electronic transformer in intelligent substation has become research emphasis and realized. The core foundation of digital substation is IEC61850 communication protocol. This protocol divides digital substation into three levels: station level, bay level and process level. High-speed Ethernet is used inner level and between the levels[2]. IEC61850-9 deepens the concept of MU, and takes it as a logic device in the system of IEC61850[3]. The main function of MU is to collect 12 channels sampled values from electronic current transformers (ECT) and electronic voltage transformers (EVT), and transmit these data to secondary protective devices and measure-control devices in a specified package format synchronously[4]. Compared with IEC61850-9-1, IEC61850-9-2 has more flexible data frame format.

Based on modular design concept, the MU introduced in this paper mainly uses FPGA, Ethernet controller and integrated physical layer chip to transmit data frames which follow IEC61850-9-2. The data frames can be switched between the interfaces of fiber optic with ST connector and electrical system with RJ45 connector in terms of actual needs. This design method simplifies circuit design and enhances circuit stability. Moreover, this MU has high flexibility and practicability.

II. MODEL OF MERGING UNIT

IEC61850-7-2 defines the Abstract Communication Service Interface (ACSI). And ACSI formulates the structure of digital substation and communication function. Transmission model of sampled values which described by ACSI is the function that the merging unit needs to realized. Transmission model of sampled values formulates three communication services: Send-Sample-Value-Message (SendSVMessage), Get-Sample-Value-Control-Block-Values (GetSVCBValues) and Set-Sample-Value-Control-Block-Values (SetSVCBValues). There are two methods to exchange sampled values between one sender and one or more receivers. One is Multicast-Sample-Value-Control-Block (MSVCB), and the other is Unicast-Sample-Value-Control-Block (USVCB).

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According to IEC61850-9-2, besides the SendSVMessage service function, MU should also have the GetSVCBValues and SetSVCBValues service functions which map to Manufacturing Message Specification (MMS). These two services can configure data sampling frequency, data input channel quantity of MU and so on on-line. Moreover, the format of the data frames output by MU can be changed if needed. Meanwhile, MU which follows IEC61850-9-2 supports the sample-value transmission method of MSVCB.

At the present stage, there are some problems in realizing MMS communication stack. Based on the protocol of 9-2LE, MU only needs to support SendSVMessage service function. And through pre-configuration, the MU realizes MSVCB methods. As a consequence, MMS stack does not need to be supported by the MU.

According to the description of the MU function above, build the information model of the MU as Fig. 1 shown. E1Q1SB1 is the server which represents the external visible behavior of a device. E1Q1SB1Munn is the logical device (LD) which contains the information produced and consumed by a group of domain-specific application functions, and each function is defined as a logical node(LN).

As a LN, LLN0 represents a group of common data. LPHD indicates the nameplate information of primary equipments. I11ATCTR1-I11NTCTR4 represent 4 channels ECTs which are used to detect protection currents. I22ATCTR1-I22NTCTR4 represent 4 channels ECTs which are used to detect measuring currents. U11ATVTR1-U11NTVTR4 represent 4 channels EVTs which are used to detect voltages. Amp and Vol are data objects that represent current sampled values and voltage sampled values separately.

On the basis of IEC60044[5], in order to meet the different accuracy of protection values and measuring values, different sampling frequencies was adopted for protection values and measuring values. As a result, two modules were designed for controlling sampled values transmission. PhsMeas1 and MSVCB01 are merged together to control 4-channel protection values transmission, and sampling frequency is 4 kHz. Phsmeas2 and MSVCB02 are merged together to control 8-channel measuring values transmission, and sampling frequency is 10 kHz.

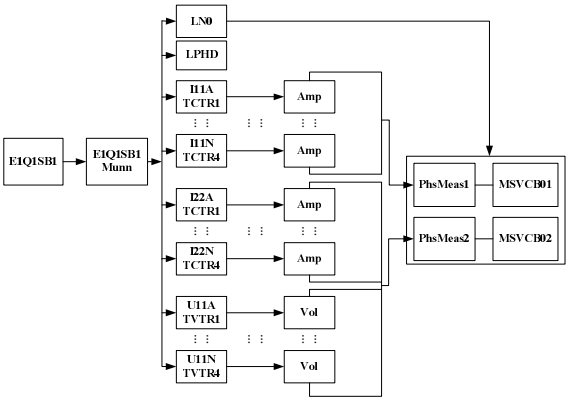

Figure 1.Information model of the merging unit

III. DESIGN OF MERGING UNIT

In order to meet the need of reliability, real-time and flexibility of the MU, this design simplifies the hardware circuit. The FPGA called EP3C25Q240C8 which is produced by Altera was selected as the core chip. This chip has abundant logical resources and can meet the need of multi-tasking. According to modular design, synchronous finite state machine of VerilogHDL was mainly used for programming. This design realized sampling pulse synchronization, sampled values receiving, sampled values processing, Ethernet controller driving, and sampled values transmission in single chip FPGA. Meanwhile, input crystal oscillator frequency of the FPGA is 50 MHz (20ns cycle). The programs in FPGA are run in parallel, so more tasks can be accomplished in one cycle. Therefore, it is very efficient. Besides, modular VerilogHDL programs are easy to maintain and upgrade.

As Fig.2 shown, the function of the MU is divided into three modules: sampling pulse synchronization module, sampled values processing module and data frames transmission module.

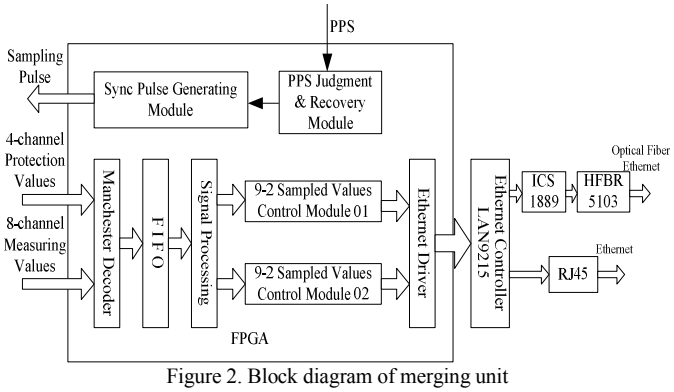

Figure 2. Block diagram of merging unit

A. Sampling Pulse Synchronization Module

This section is divided into two modules: PPS judgment and recovery module and sync pulse generating module[6].

The correct PPS needs to meet three requirements:

- The PPS cycle is 1s.
- The PPS high level width of is greater than 10μs.
- The PPS interval is greater than 500ms.

First, PPS judgment module judges whether the input PPS conforms to the three requirements above. If the PPS is correct three times consecutively, it is considered to be normal. When PPS judgment module (take sampling frequency 4 kHz as example) detects the fourth PPS, sync pulse generating module sends the first sampling pulse immediately. Meanwhile, the sync pulse generating module divides the input crystal oscillator of 50 MHz into sampling pulse of 4 kHz, and counts the sampling pulses. When the number of the sampling pulses reaches 4000, PPS judgment module detects the PPS and sync pulse generating module sends the sampling pulse again. It runs in loops, and the sampling pulse is corrected per second.

If the PPS is wrong, PPS recovery module start to run. This module which is similar to PPS judgment module judges whether the PPS is back to normal. Sync pulse generating module divides the input crystal oscillator of 50 MHz to generate sampling pulse of 4 kHz directly until the PPS is back to normal.

B. Sampled Values Processing Module

This section is divided into three modules: Manchester decoding module, FIFO module and signal processing module.

1) Manchester decoding and FIFO module

12 channels power grid data are transmitted in accordance with Manchester encoding rules, and the transmission speed is 2.5Mbit/s. So the MU needs Manchester decoding module to decode the 12 channels power grid data.

Manchester encoding principle: a 0 to 1 transition represents logic 1; a 1 to 0 transition represents logic 0, as Fig.3 shown. Conversely, it is decoding. Note that at the front of Manchester encoding data, there must be a synchronization word[7]. It is the key for decoding. Manchester decoding module detects the synchronization word continuously, and if the synchronization word is discovered, decoding begins.

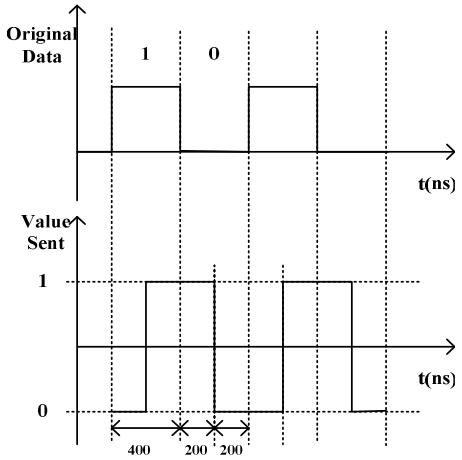

Figure 3. Principle of Manchester encoding

Decoded data are stored in the FIFO module. FIFO is the IP core that Altera designed for its FPGA. The IP core is a module which was tested rigorously and optimized. Furthermore, it is can be customized. IP core can improve development efficiency. The FIFO module in this design does not occupy logic elements, so it can save a lot of logic resources and facilitate expansion of other programs.

2) Signal processing module

This module reads 12 channels data from the FIFO module. Then a cyclic redundancy check (CRC) is performed to determine the validity of the data. After that, the data validity of each channel is written to the corresponding bits of Quality according to 9-2LE.

Compared with 9-1, 9-2 does not use digital rating data to calibrate the input data, because the sampled values are of 32-bit, that means higher accuracy. The sampled values are transmitted directly in 9-2. The current accuracy is 1mA, and the voltage accuracy is 10mV.

C. Data Frames Transmission Module

This section was divided into two sections: sampled values control module and Ethernet drive module.

1) Sampled values control module

The function of this module is to frame the processed data from the last module. It means to concatenate several ASDU into one APDU. Basic encoding rule (BER) of ASN.1 is used to encode APDU, as Fig.4 shown. The BER has the format of a triplet TLV (Tag, Length and Value). 4-channel protection values and 8-channel measuring values are framed separately, so protection values and measuring values need to form two APDU for transmission. The initial tags of the two APDU are both 0x60. The ASDU number of protection values is 1. The ASDU number of measuring values is 8.

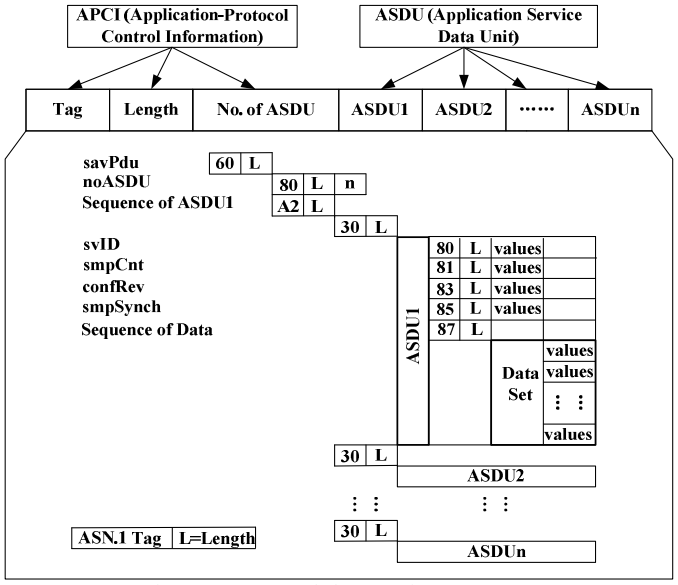

Figure 4. ASN.1 coded APDU frame structure

2) Ethernet drive module

The main function of this module is to drive the Ethernet controller LAN92215, and package the APDU on ISO/IEC8802-3 frame format[8] for Ethernet transmission. Use finite state machine of VerilogHDL to access the registers of LAN9215, and set it to 100M full duplex mode. Then access HW_CFG register of LAN9215 to switch between internal PHY (physical layer controller) and external PHY. If it is internal PHY, LAN9215 drives RJ45 to transmit data frames directly. If it is external PHY, LAN9215 accesses ICS1889 which is external PHY through MII interface, and ICS1889 drives HFBR5103 which is fiber optic Ethernet transceiver with ST connector to transmit data frames.

IV. MERGING UNIT FUNCTION TEST

The data frames transmitted by this MU were captured and analyzed by MMS Ethereal software. The results are shown in Fig.5 and Fig.6. MMS Ethereal identified the data frames correctly.

Fig.5 shows protection data frame. It can be seen that:

- The number of ASDUs is 1.
- smvID is E1Q1SB1Munn01.

- Sample count is 25618.
- Config Rev is 1.
- Sample Synched is true.
- Samples are preset to be 0.

Fig.6 shows measuring data frame. The results are almost the same as Fig.5 except that the number of ASDUs is 8, and the sample count is 64040.

The results demonstrate the data frames transmitted by this MU follow IEC61850-9-2 protocol.

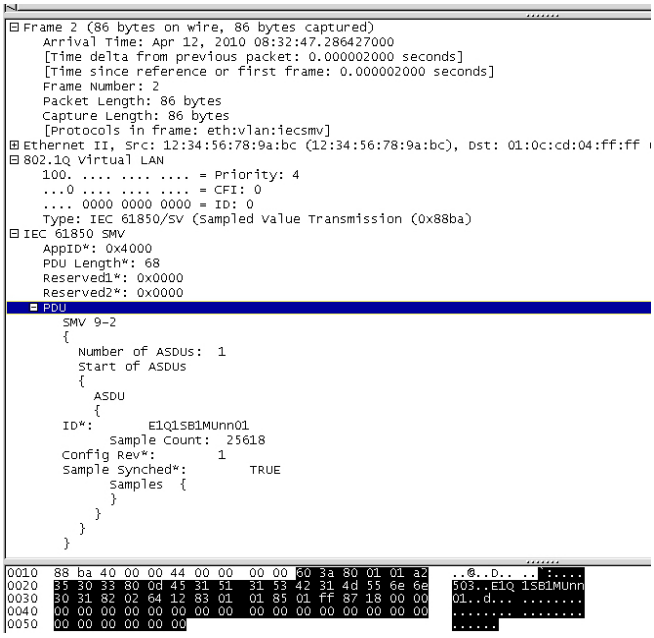

Figure 5. Protection data frame analyzed by MMS Ethereal

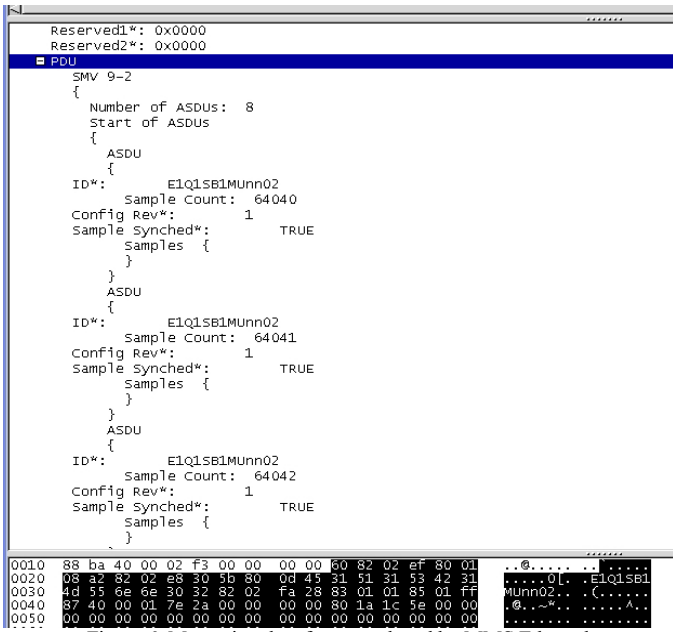

Figure 6. Measuring data frame analyzed by MMS Ethereal

V. CONCLUSION

This paper describes a realization method of intelligent merging unit based on single chip FPGA. This method takes full advantage of fast-speed, multi-task and modularization features of FPGA to make merging unit transmit data frames following IEC61850-9-2. Besides, the data frames can be switched between the interfaces of RJ45 and HFBR5103 according to actual needs. The results demonstrate this MU has high practicality in digital substation which is on the basis of IEC61850.

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