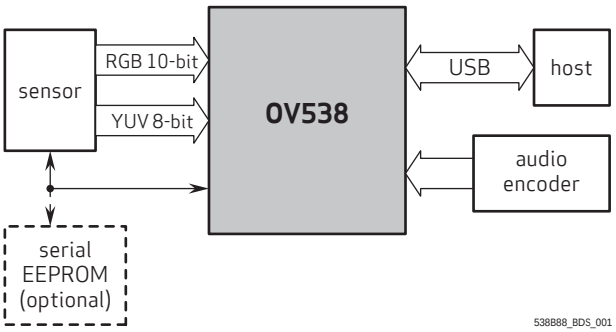
OV538-B88 Camera Bridge Processor

General Description

The OV538 Camera Bridge Processor is a low cost, enhanced single-chip processor for USB 2.0 PC camera applications, capable of supporting up to 2.0 Megapixel sensors for game console applications. When combined with an OmniVision VGA, 1.3 Mpixel, or 2.0 Mpixel digital CAMERACHIP™ sensor, the OV538 comprises an integrated USB 2.0 camera system, with no additional USB transceiver or DRAM required. The OV538 also supports audio input for full audio/video operation.

Note: The OV538-B88 is available in a lead-free package.

Figure 1 OV538 Attached to Application Engine



Ordering Information

Product	Package
OV0538-LB50 (lead-free)	BGA-88

Key Specifications

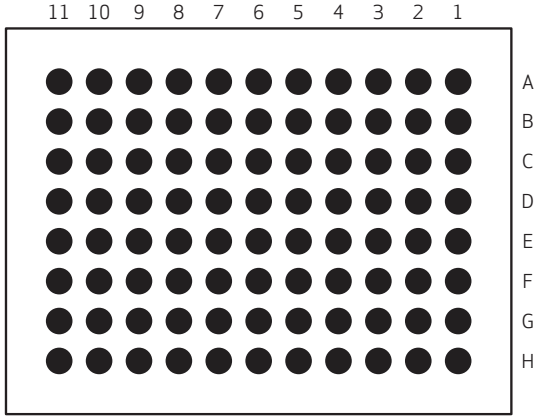
Power Supply	**Core**	1.8 V
	I/O	3.3V
	Regulator Input	3.3V
Power Requirements	**Active**	82 mA
	Standby	230 µA
Temperature Range		0 - 70°C
Package Dimensions		8.00 mm x 6.00 mm

Applications

- USB 2.0 applications combined with the following OmniVision CAMERACHIP families:
  - OV26xx (2.0 MegaPixel)
  - OV96xx (1.3 MegaPixel)
  - OV86xx (SVGA)
  - OV76xx (VGA)
  - OV66xx (CIF)

NOTE: The OV538 supports digital image sensors up to 2.0 Megapixel resolution. However, it will not support analog image sensors (OVx9xx or OVx4xx products).

Figure 2 OV538-B88 Pin Diagram (Bottom View)



	11	10	9	8	7	6	5	4	3	2	1
A	P_TCLK	P_BIAS	P_LPDEV	P_TM	P_OSC_EN	P_Y[5]	P_GPIO[0]	P_C_SDA	R25O	R25G	R25I
B	NC	NC	P_GPIO[6]	P_GPIO[8]	CORE_VSS2	P_CCLK	IO_VDD1	P_Y[1]	P_GPIO[1]	P_GPIO[2]	P_C_SCL
C	IO_VDD2	IO_VSS2	P_RESET_N	NC	NC	NC	NC	NC	P_Y[3]	IO_VSS1	P_Y[0]
D	P_GPIO[7]	P_ACLK	NC	NC	NC	NC	NC	NC	NC	P_Y[4]	P_Y[2]
E	CORE_VDD2	P_CLKI	NC	NC	NC	NC	NC	NC	NC	CORE_VDD1	P_Y[6]
F	VSSU	REXT	P_GPIO[9]	NC	NC	NC	NC	NC	P_Y[7]	P_Y[8]	P_Y[9]
G	VD33P	VDDU	VD33	VS33P	P_GPIO[10]	P_CLKO	P_PCLK	P_HREF	P_VSYNC	P_PWDN	P_GPIO[5]
H	RPU	DP	DM	VS33P	VD33P	CORE_VSS1	P_GPIO[3]	P_GPIO[4]	R18I	R18G	R18O

Features

General Features

- Low cost, low powered image processor that supports up to 2.0 Megapixel sensors
- Maximum pixel clock running at 48 MHz
- Supports USB Video Class
- Supports USB Audio Class
- Serial Camera Control Bus (SCCB) Master

CAMERACHIP Interfaces

- Up to 2 Megapixel
- 10-bit RGB interface
- 8-bit YUV interface
- Horizontal mirror image of RGB raw data

Image Signal Processor (ISP)

- Raw RGB data to YUV processing
- Edge enhancement
- Hue and saturation control
- Down-sampling, clamping and windowing (DCW)
- Digital 8x up-scaling (zoom in) for compressed images and down-scaling (zoom out) for previewing images at various steps
- Lens shading compensation
- Digital effects including:
  - Gray mode
  - Negative mode
  - Sepia mode
- Contrast and Brightness
- White pixel correction
- Image enhancement

Compression Encoder

- Embedded compression encoder for YUV 422 of up to 2 Megapixel resolution (YUV420 of up to 800x600 pixels)

Host Interface - USB 2.0

- Supports USB Video Class
- Supports USB Audio Class

Embedded 8-bit Microcontroller

- Embedded 512-Byte data memory
- Embedded 16KB program memory

Miscellaneous

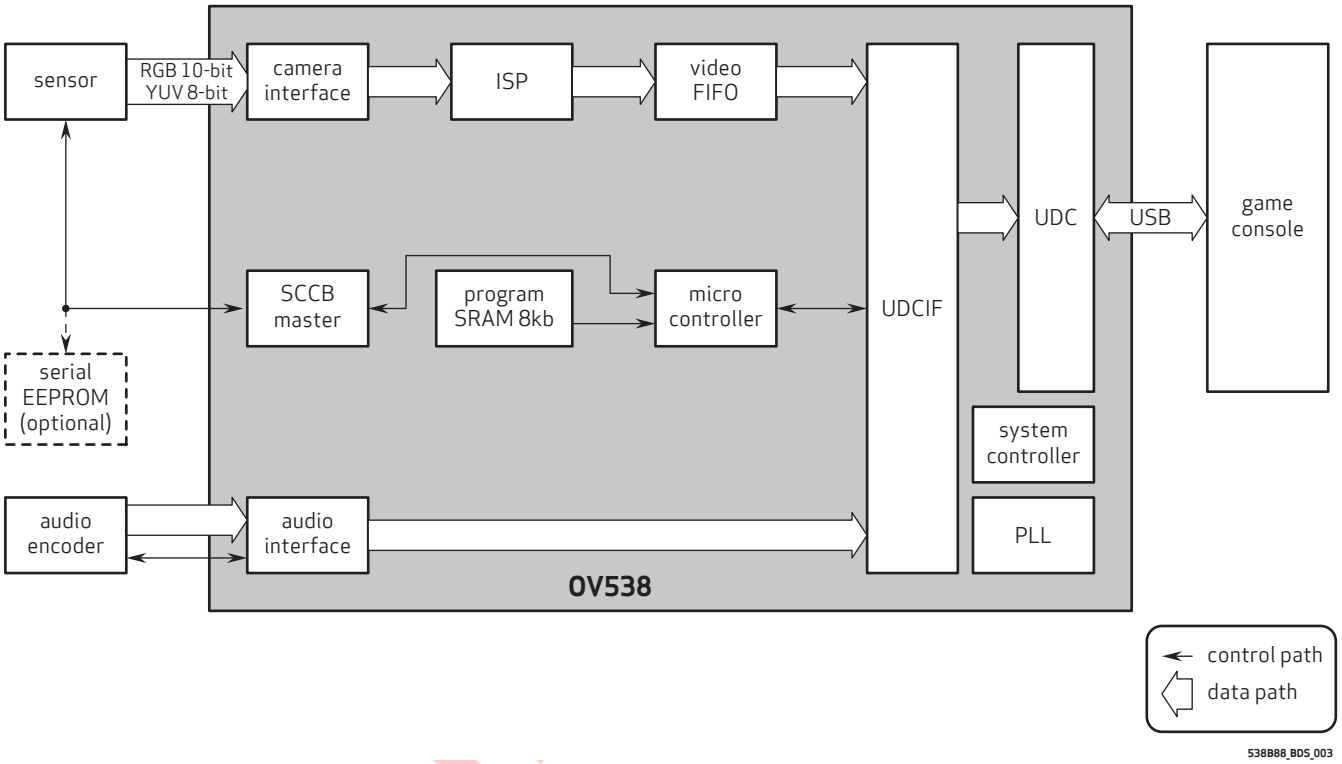
- Embedded 3.3V to 2.5V and 3.3V to 1.8V regulators
- Embedded PLL
- Optional external serial EEPROM
- General Purpose I/O (GPIO)
- Power-down control

Functional Description

Figure 3 shows the functional block diagram of the OV538 processor. The OV538 includes:

- Camera Interface
- Image Signal Processor
- Encoder
- Color Converter
- Host Controller
- SCCB Master Controller
- Microcontroller
- System Controller

Figure 3 Functional Block Diagram



Camera Interface

The Camera Interface takes either 10-bit RGB raw data or 8-bit YUV data from a maximum 2 Megapixel image sensor. The maximum pixel clock accepted by the Camera Interface is 48MHz.

The Camera Interface can interface with image sensor 656 and 601 modes, as well as HREF and HSYNC modes. It also supports mirror imaging of RGB raw data.

Image Signal Processor

The Image Signal Processor (ISP) can process both synchronized RGB raw data and YUV data, as well as bypass all processing for YUV data. Functions of the ISP include:

- Raw to YUV processing
- Edge enhancement
- Hue and saturation control
- Contrast and saturation control
- Down-sampling, clamping and windowing
- Digital 8x up-scaling (zoom in) for compressed images and down-scaling (zoom out) for previewing images at various steps
- Lens shading
- Digital effects including:
  - Gray mode
  - Negative mode
  - Sepia mode
- White pixel correction

Encoder

The Encoder can support real-time video compression for YUV 422 of up to 2.0 Megapixel resolution or YUV420 of up to 800 x 600 resolution.

Color Converter

The Color Converter can convert processed YUV422 to YUV411 or RGB565 formats. It can also bypass YUV422, RAW8 and RAW10 formats.

Host Controller

The OV538 uses USB 2.0 to communicate with the host controller. The USB video and audio classes are supported.

SCCB Master Controller

The SCCB Master Controller controls sensor registers. It is possible for the SCCB Master Controller to interface with an optional external EEPROM for downloading firmware to the program memory of the Microcontroller when the system is powered up.

Microcontroller

The OV538 embeds an 8-bit microcontroller with 512-byte data memory and 16KB program memory. It provides the flexibility of decoding protocol commands from the host for controlling the system, as well as the ability to fine tune image quality.

System Controller

The System Controller provides some system functions, such as GPIO and power-down functions.

Pin Description

Table 1 Pin Description by Function (Sheet 1 of 3)

Ball Number	Name	Pin Type	Function/Description
System Control			
G2	P_PWDN	I/O	Sensor Power Down General Purpose I/O Default: Output 1
A5	P_GPIO[0]	I/O	General Purpose I/O Audio interface synchronization signal Default: Input
B3	P_GPIO[1]	I/O	General Purpose I/O Audio interface clock signal Default: Input
B2	P_GPIO[2]	I/O	General Purpose I/O Audio interface data pin 1
H5	P_GPIO[3]	I/O	General Purpose I/O Audio interface data pin 2
H4	P_GPIO[4]	I/O	General Purpose I/O Audio interface data pin 3
G1	P_GPIO[5]	I/O	General Purpose I/O Audio interface data pin 4
B9	P_GPIO[6]	I/O	General Purpose I/O
D11	P_GPIO[7]	I/O	General Purpose I/O
B8	P_GPIO[8]	I/O	General Purpose I/O
F9	P_GPIO[9]	I/O	General Purpose I/O
G7	P_GPIO[10]	I/O	General Purpose I/O
C9	P_RESET_N	Input	Power On Reset 0: Reset
G6	P_CLKO	Output	Crystal Output
E10	P_CLKI	Input	Crystal Input
D10	P_ACLK	Output	Audio interface output clock
A8	P_TM	Output	Test Mode Enable
A7	P_OSC_EN	Output	Crystal Enable
A11	P_TCLK	Input	Test Mode Clock
A9	P_LPDEV	Input	Low Power Device Indicator
Camera Interface			
C1	P_Y[0]	I/O	Sensor Data Y[0] General Purpose I/O Default: Input of sensor data Y[0]
B4	P_Y[1]	I/O	Sensor Data Y[1] General Purpose I/O Default: Input of sensor data Y[1]

Table 1 Pin Description by Function (Sheet 2 of 3)

Ball Number	Name	Pin Type	Function/Description
D1	P_Y[2]	I/O	Sensor Data Y[2] General Purpose I/O
C3	P_Y[3]	I/O	Sensor Data Y[3] General Purpose I/O Default: Input of sensor data Y[3]
D2	P_Y[4]	I/O	Sensor Data Y[4] General Purpose I/O Default: Input of sensor data Y[4]
A6	P_Y[5]	I/O	Sensor Data Y[5] General Purpose I/O Default: Input of sensor data Y[5]
E1	P_Y[6]	I/O	Sensor Data Y[6] General Purpose I/O Default: Input of sensor data Y[6]
F3	P_Y[7]	I/O	Sensor Data Y[7] General Purpose I/O Default: Input of sensor data Y[7]
F2	P_Y[8]	I/O	Sensor Data Y[8] General Purpose I/O Default: Input of sensor data Y[8]
F1	P_Y[9]	I/O	Sensor Data Y[9] General Purpose I/O Default: Input of sensor data Y[9]
B6	P_CCLK	I/O	Camera Clock to Sensor General Purpose I/O Default: Output of camera clock
G5	P_PCLK	I/O	Pixel Clock from Sensor General Purpose I/O Default: Input of pixel clock
G4	P_HREF	I/O	Horizontal Reference/Sync from Sensor General Purpose I/O Default: Input of sensor HREF
G3	P_VSYNC	I/O	Vertical Sync from Sensor General Purpose I/O Default: Input of sensor VSYNC
A4	P_C_SDA	I/O	Master SCCB Data Default: Input
B1	P_C_SCL	I/O	Master SCCB Clock Default: Input
USB 2.0 Interface			
F10	REXT	Input	Reference Input
H10	DP	I/O	USB DP
H9	DM	I/O	USB DM

Table 1 Pin Description by Function (Sheet 3 of 3)

Ball Number	Name	Pin Type	Function/Description
Power and Ground			
A1	R25I	Power	3.3V to 2.5V Regulator Input
A2	R25G	Ground	3.3V to 2.5V Regulator Ground
A3	R25O	Power	3.3V to 2.5V Regulator Output
B5	IO_VDD1	Power	I/O Power
C2	IO_VSS1	Ground	I/O Ground
E2	CORE_VDD1	Power	1.8V Core Power
H6	CORE_VSS1	Ground	1.8V Core Ground
H3	R18I	Power	3.3V to 1.8V Regulator Input
H2	R18G	Ground	3.3V to 1.8V Regulator Ground
H1	R18O	Power	3.3V to 1.8V Regulator Output
C11	IO_VDD2	Power	IO Power
C10	IO_VSS2	Ground	IO Ground
E11	CORE_VDD2	Power	1.8 V Core Power
B7	CORE_VSS2	Ground	1.8 V Core Ground
F11	VSSU	Ground	1.8V USB Core Ground
G10	VDDU	Power	1.8V USB Core Ground
H8/G8	VS33P	Ground	3.3V USB Ground
G11/H7	VD33P	Power	3.3V USB Power
G9	VD33	Power	3.3V USB Digital Power
Unused Pins			
B10-B11	NC	–	No connection

Electrical Characteristics

Table 2 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
T_{STG}	Ambient storage temperature[a]	TBD	TBD	°C
V_{SUP}	All I/O supply voltage	–	TBD	V
T_{JUNC}	Junction temperature	–	TBD	°C

a. Exceeding the stresses listed may permanently damage the device. This is a stress rating only and functional operation of the device at these and any other condition above those indicated in this specification is not implied. Exposure to absolute maximum rating conditions for any extended period may affect reliability.

Table 3 DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD_IO}	DC supply voltage - I/O	3.3V ± 10%	3.0	3.3	3.6	V
V_{DD_CORE}	DC supply voltage - Core	1.8V ± 5%	1.7	1.8	2.0	V
V_{IH}	Input voltage HIGH	CMOS	2.3			V
V_{IL}	Input voltage LOW	CMOS			0.7	V
V_{OH}	Output voltage HIGH	I_{OH} = 4mA	2.4			V
V_{OL}	Output voltage LOW	I_{OL} = 4mA			0.5	V
I_S	Suspend current			230	350	µA
I_{DDA}	Operating current	1600 x 1200, 7.5 fps[a]		82		mA

a. ISP: On, Compression: On

Timing Specifications

Table 4 1.8V Regulator Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OUT}	Output voltage	I_{OUT} = 1mA, Typ=3.3V I_{OUT} = 40mA, Typ=3.3V I_{OUT} = 80mA, Typ=3.3V I_{OUT} = 100mA, Typ=3.3V		1.82 1.81 1.80 1.79		V
ΔV_{LINE}	Line regulation	2.7V<V_{IN}<3.6V	–	–	20	mV
ΔV_{LOAD}	Load regulation	1mA<I_{OUT} <100mA	–	–	65	mV
V_{DROP}	Dropout voltage		–	–	900	mV
I_{LIMIT}	Current limit		–	–	100	mA
I_{MIN}	Min current load		0	–	–	µA
I_{OPER}	Operating current	I_{OUT} = 100mA	–	1	–	mA
I_{QUIE}	Quiescent current	I_{OUT} = 0mA	–	1	–	mA

Table 5 2.5V Regulator Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OUT}	Output voltage	I_{OUT} = 1mA, Typ=3.3V I_{OUT} = 20mA, Typ=3.3V I_{OUT} = 40mA, Typ=3.3V I_{OUT} = 50mA, Typ=3.3V		2.50 2.49 2.48 2.47		V
ΔV_{LINE}	Line regulation	3.0V<V_{IN}<3.6V			20	mV
ΔV_{LOAD}	Load regulation	1mA<I_{OUT} <50mA			60	mV
V_{DROP}	Dropout voltage	3.0V<V_{IN}<3.6V, 0mA<I_{OUT} <50mA			500	mV
I_{LIMIT}	Current limit				80	mA
I_{MIN}	Min current load		0			µA
I_{OPER}	Operating current	I_{OUT} = 50mA		1		mA
I_{QUIE}	Quiescent current	I_{OUT} = 0mA		1		mA

Timing Specifications

SCCB Timing Specifications

Master SCCB Timing

The master SCCB is a two-wire SCCB bus, including SIO_D and SIO_C.

Figure 4 Master SCCB Timing Diagram

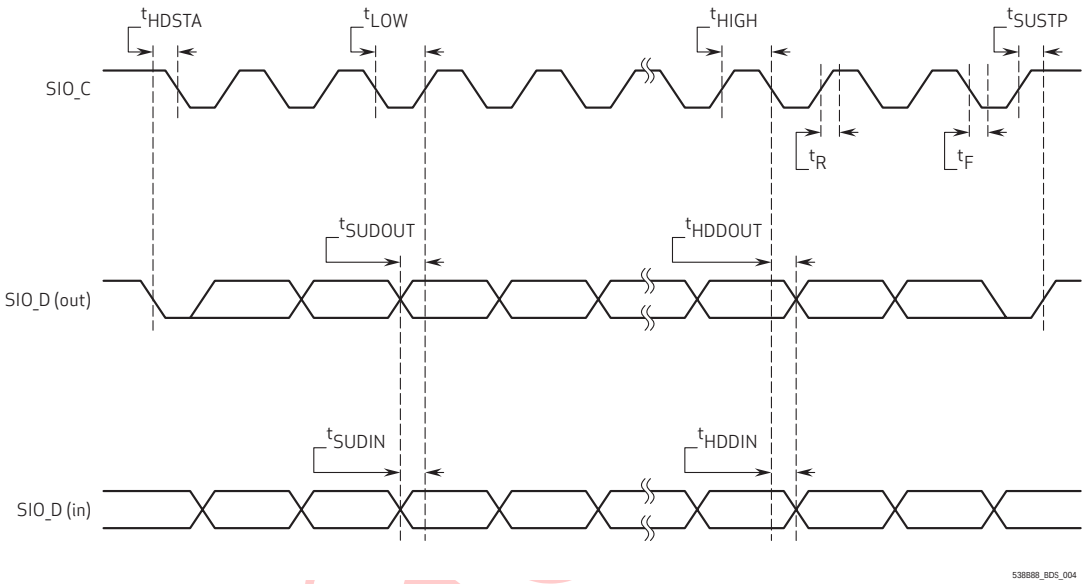


Table 6 Master SCCB Timing Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{SIO_C}	SIO_C clock frequency			395		KHz
t_{HIGH}	SIO_C clock high time			1.09		us
t_{LOW}	SIO_C clock low time			1.28		us
t_{HDSTA}	Start of transmission hold time			1.27		us
t_{SUSTP}	Stop of transmission setup time			0.64		us
t_{SUDOUT}	Output data transmission setup time			0.62		us
t_{HDDOUT}	Output data transmission hold time			0.62		us
t_R	SIO_C clock rising time[a]			300		ns
t_F	SIO_C clock failing time[a]			12		ns
t_{SUDIN}	Input data setup time		0.5			us
t_{HDDIN}	Input data hold time		0			us

a. R_{pup}=3.3K

3-wire Audio Interface Timing

The slave audio interface is a 3-wire audio bus. It has one clock signal ACLK, one synchronous signal ASYN and one audio data signal ADAT. The audio bus can be extended to 4-wire, 5-wire or 6-wire by including more audio data pins.

Figure 5 Slave Audio Interface AC Timing Diagram

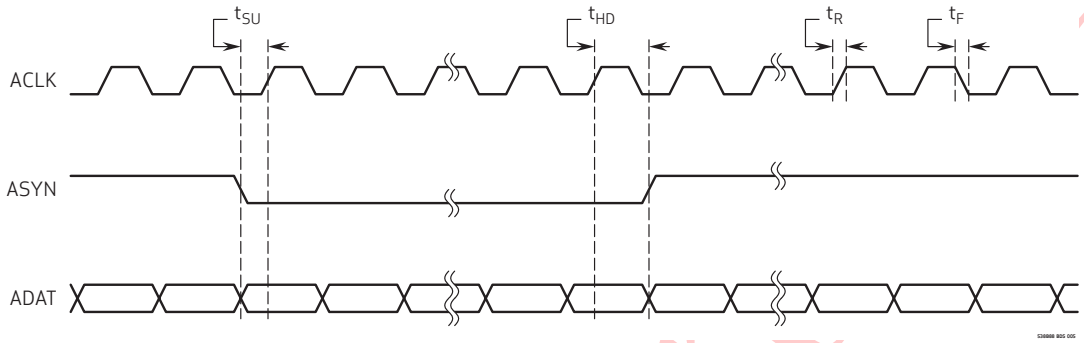


Table 7 Slave Audio Interface AC Timing Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_R	ACLK clock rise time		–	4.2	–	ns
t_F	ACLK clock fall time		–	3.75	–	ns
t_{SU}	Data setup time		4	–	–	ns
t_{HD}	Data hold time		37	–	–	ns

Figure 6 3-wire Slave Audio Interface Timing Diagram

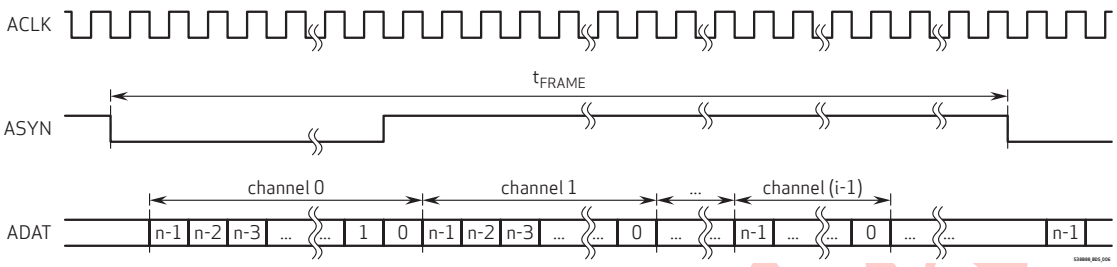


Figure 7 Extended 6-wire Slave Audio Interface Timing Diagram

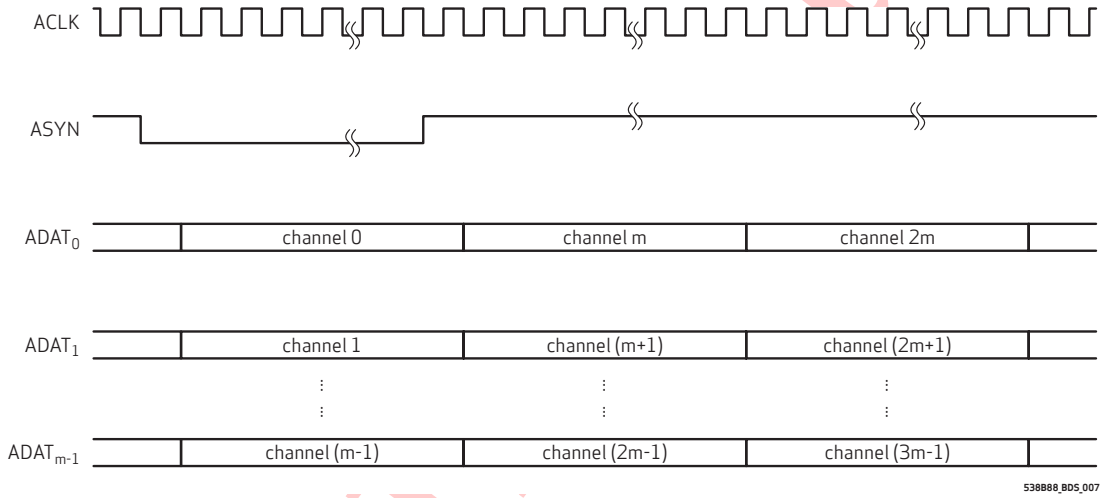


Table 8 Slave Audio Interface Timing Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{FRAME}	ASYN to ASYN		–	–	128	bit
n	Audio data resolution		–	–	24	bit
i	Channel number		–	–	8	bit
m	Audio data pin number		–	–	4	bit

Clock Timing Specifications

Table 9 Input Clock X_IN Timing Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{X_IN}	Input clock frequency			12.0		MHz
$t_{X\_IN\_DCY}$	Input clock duty cycle		40	50	60	%

Table 10 Input Clock PCLK Timing Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PCK}	Input clock frequency			24	48	MHz
t_{PCK_DCY}	Input clock duty cycle		40	50	60	%

Table 11 Output Clock CCLK Timing Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{CCK}	Output clock frequency			24		MHz
t_{CCK_DCY}	Output clock duty cycle		40	50	60	%

Register Set

Table 12 provides a list and description of the Device Control registers contained in the OV538.

Table 12 Register List of SCCB and Micro-Controller (Sheet 1 of 2)

Address (Hex)	Register Name	Default Value	R/W	Description
0xF0	MS_SP	8'h13	RW	SCCB Master Speed
0xF1	MS_ID	8'h60	RW	SCCB Master ID
0xF2	MS_ADDRESS	8'h5A	RW	SCCB Master Address
0xF3	MS_DO	8'hF1	RW	SCCB Master Data Out
0xF4	MS_DI	–	R	SCCB Master Data In
0xF5	MS_CTRL	8'h00	RW	SCCB Master Command Control Bit[7]: Send NAK/ACK in acknowledge phase of data in cycle Bit[6]: Use read ID (bit[0] of MS_ID: 1) Bit[5]: Launch stop bit cycle Bit[4]: Launch start bit cycle Bit[3]: Launch data in cycle Bit[2]: Launch data out cycle Bit[1]: Launch address cycle Bit[0]: Launch ID cycle 8'h37: 3-byte write 8'h33: 2-byte write 8'hF9: 2-byte read Burst write: 8'h13: Launch start-id-address cycle 8'h02: Launch data out cycle, n times 8'h20: Launch stop bit cycle Burst read: 8'h33: Launch 2-byte write for address 8'h51: Launch start-id with read ID 8'h04: Launch data in cycle with ACK 8'hA4: Launch last data in cycle with NAK, then stop bit
0xF6	MS_STATUS	–	R	Status of SCCB Master Bit[7:3]: Reserved Bit[2]: Slave status 0: ACK 1: NAK Bit[1]: Cycle completed for burst mode Bit[0]: Command busy
0xF7-0xF8	RSVD	XX	–	Reserved

Table 12 Register List of SCCB and Micro-Controller (Sheet 2 of 2)

Address (Hex)	Register Name	Default Value	R/W	Description
0xF9	MC_BIST	–	RW	Bit[7]: Microcontroller Bit[6]: Boot ROM select Bit[5]: R/W 1 error for 12K-byte memory Bit[4]: R/W 0 error for 12K-byte memory Bit[3]: R/W 1 error for 512-byte memory Bit[2]: R/W 0 error for 512-byte memory Bit[1]: BIST busy bit for read; One-shot reset of microcontroller for write Bit[0]: Launch BIST
0xFA	MC_AL	–	RW	Program Memory Pointer Address Low Byte
0xFB	MC_AH	–	RW	Program Memory Pointer Address High Byte
0xFC	MC_D	8'h80	R	Program Memory Pointer Access Address
0xFD	SAMPLE	8'h00	RW	Audio Comb filter control Bit[4]: 32/64 select Bit[3:0]: Step
0xFe	AC_BIST	8'h00	RW	Bit[7:5]: Reserved Bit[4]: Mute Bit[3]: R/W 1 error Bit[2]: R/W 0 error Bit[1]: BIST busy bit Bit[0]: Launch BIST
0xFF	RSVD	XX	–	Reserved

Table 13 Register List of System Controller (Sheet 1 of 4)

Address (Hex)	Register Name	Default Value	R/W	Description
0xE0	RESET0	8'h00	RW	Reset Bit[7]: SCCB Bit[6]: Audio interface Bit[5]: DIF Bit[4]: Audio Bit[3]: VFIFO Bit[2]: Compression Bit[1]: ISP Bit[0]: CIF
0xE1	RESET1	8'h00	RW	Clock Enable Bit[2]: UDCIF Bit[1]: UDC Bit[0]: Microcontroller

Table 13 Register List of System Controller (Sheet 2 of 4)

Address (Hex)	Register Name	Default Value	R/W	Description
0xE2	CLOCK0	8'h2F	RW	Clock Control (1: OFF, 0: ON) Bit[7]: SCCB Bit[6]: Audio interface Bit[5]: DIF Bit[4]: Audio Bit[3]: VFIFO Bit[2]: Compression Bit[1]: ISP Bit[0]: CIF
0xE3	CLOCK1	8'h00	RW	Clock Control (1: OFF, 0: ON) Bit[0]: Sensor power down in suspend mode enable Bit[3]: Reserved Bit[2]: PLL disable Bit[1]: Microcontroller
0xE4	RSVD	XX	–	Reserved
0xE5	CAMERA_CLK	8'h04	RW	Bit[7]: Drive 0 to SRAM output 0: Normal 1: Driver 0 Bit[6]: SRAM input force to 0 0: Normal mode 1: Force to 0 Bit[5]: SRAM CEN Bit[4:0]: Camera clock select
0xE6	USER	8'h00	RW	User defined
0xE7	SYS_CTRL	8'h3b	RW	System Control Bit[7]: Launch suspend Bit[6]: Launch register reset Bit[5]: Reserved Bit[4]: Microcontroller wakeup reset enable Bit[3]: Reserved Bit[2]: Wakeup enable Bit[1]: Suspend enable Bit[0]: Camera power ON/OFF 0: Power ON camera 1: Power down camera
0xE8	Step[7:0]	8'h80	R	Audio clock parameter0 Bit[7:0]: Reserved
0xE9	Step[10:8]	8'h00	R	Audio clock parameter0 Bit[10:8]: Reserved
0xEA	Max[7:0]	8'h53	R	Audio clock parameter1 Bit[7:0]: Reserved
0xEB	Max[10:8]	8'h07	R	Audio clock parameter1 Bit[10:8]: Reserved

Table 13 Register List of System Controller (Sheet 3 of 4)

Address (Hex)	Register Name	Default Value	R/W	Description
0xEC	IRQ_M0	–	–	Interrupt Mask Bit[7]: UDC Bit[6]: USB enumeration done Bit[5]: USB suspend Bit[4]: USB early suspend Bit[3]: USB SOF Bit[2]: UDCIF interrupt Bit[1]: AEC Bit[0]: AWB
0xED	IRQ_M1	–	–	Interrupt Mask Bit[7]: Line interrupt Bit[6]: ATG Bit[5]: Compression EOF Bit[4]: Compression SOF Bit[3]: Compression overflow Bit[2]: VSYNC Bit[1]: ISP EOF Bit[0]: ISP SOF
0xEE	IRQ0	–	–	Interrupt Status Bit[7]: UDC Bit[6]: USB enumeration done Bit[5]: USB suspend Bit[4]: USB early suspend Bit[3]: USB SOF Bit[2]: UDCIF interrupt Bit[1]: AEC Bit[0]: AWB
0xEF	IRQ1	–	–	Interrupt Status Bit[7]: Line interrupt Bit[6]: ATG Bit[5]: Compression EOF Bit[4]: Compression SOF Bit[3]: Compression overflow Bit[2]: VSYNC Bit[1]: ISP EOF Bit[0]: ISP SOF
0x35	DIF	8'h00	RW	Bit[2]: Select RGB mode Bit[1]: Select Compression mode Bit[0]: Debug port enable
0x3B	CIF_FRAME	6'h10	RW	Bit[7:6]: Number of frame for output Bit[5]: Enable/disable CIF output after (Bit[3:0]) frames Bit[4]: Enable CIF output Bit[3:0]: Number of frames for CIF output

Table 13 Register List of System Controller (Sheet 4 of 4)

Address (Hex)	Register Name	Default Value	R/W	Description
0x3C	IPU_FRAME	6'h10	RW	Bit[7:6]: Number of frame for output Bit[5]: Enable/disable IPU output after (Bit[3:0]) frames Bit[4]: Enable IPU output Bit[3:0]: Number of frames for IPU output
0x3D	PHY_BIST0	8'h00	RW	Bit[7:0]: BIST data
0x3E	PHY_BIST1	8'h00	RW	Bit[15:8]: BIST data
0x3F	PHY_BIST2	–	RW	Bit[7]: BIST transceiver select Bit[6]: BIST termination select Bit[5:4]: BIST OP mode Bit[3]: BIST suspendm Bit[2]: BIST on Bit[1]: BIST txvalidh Bit[0]: BIST txvalid

Table 14 Register List of GPIO (Sheet 1 of 4)

Address (Hex)	Register Name	Default Value	R/W	Description
0x20	GPIO_N0	8'h6C	RW	PHY Control Bit [7:6]: PHY input clock reference Bit [5]: PHY data bus 16/8 select Bit [4:0]: Reserved
0x21	GPIO_C0	8'h00	RW	I/O pad in/out control: 0 input; 1 output
0x22	GPIO_I0	–	R	I/O Pad Input
0x23	GPIO_V0	8'h02	RW	I/O Pad Output
0x24	GPIO_N1	8'h7F	RW	I/O Pad (1: Normal mode, 0: Register control) Bit[4]: SIO_C Bit[3]: SIO_D Bit[2:0]: Reserved
0x25	GPIO_C1	8'h43	RW	I/O Pad In/Out Control Bit[6]: P_OSCEN Bit[5]: Reserved Bit[4]: P_SIO_C Bit[3]: P_SDA_D Bit[2:0]: GPIO[10:8]
0x26	GPIO_I1	–	R	I/O Pad Input Bit[6]: OSCEN Bit[5:4]: Reserved Bit[3]: PHY BIST fail Bit[2:0]: GPIO[10:8]

Table 14 Register List of GPIO (Sheet 2 of 4)

Address (Hex)	Register Name	Default Value	R/W	Description
0x27	GPIO_V1	8'h00	RW	I/O Pad Output Bit[7]: Reserved Bit[6]: P_OSCEN Bit[5]: Reserved Bit[4]: P_SIO_C Bit[3]: P_SIO_D Bit[2:0]: GPIO[10:8]
0x28	SENSOR_S1	8'h00	RW	I/O Pad Driving Strength Bit[7]: P_Y[7] Bit[6]: P_Y[6] Bit[5]: P_Y[5] Bit[4]: P_Y[4] Bit[3]: P_Y[3] Bit[2]: P_Y[2] Bit[1]: P_Y[1] Bit[0]: P_Y[0]
0x29	SENSOR_C1	8'h00	RW	I/O Pad Output Bit[7]: P_Y[7] Bit[6]: P_Y[6] Bit[5]: P_Y[5] Bit[4]: P_Y[4] Bit[3]: P_Y[3] Bit[2]: P_Y[2] Bit[1]: P_Y[1] Bit[0]: P_Y[0]
0x2A	SENSOR_I1	8'h60	RW	I/O Pad In/Out Control Bit[7]: P_Y[7] Bit[6]: P_Y[6] Bit[5]: P_Y[5] Bit[4]: P_Y[4] Bit[3]: P_Y[3] Bit[2]: P_Y[2] Bit[1]: P_Y[1] Bit[0]: P_Y[0]
0x2B	SENSOR_V1	8'h00	RW	I/O Pad Output Bit[7]: P_Y[7] Bit[6]: P_Y[6] Bit[5]: P_Y[5] Bit[4]: P_Y[4] Bit[3]: P_Y[3] Bit[2]: P_Y[2] Bit[1]: P_Y[1] Bit[0]: P_Y[0]

Table 14 Register List of GPIO (Sheet 3 of 4)

Address (Hex)	Register Name	Default Value	R/W	Description
0x2C	SENSOR_S0	8'h00	RW	I/O Pad Driving Strength Bit[7]: P_ACLK Bit[6]: P_CCLK Bit[5]: P_PWDN Bit[4]: P_HREF Bit[3]: P_VSYNC Bit[2]: P_PCLK Bit[1]: P_Y[9] Bit[0]: P_Y[8]
0x2D	SENSOR_C0	8'h60	RW	I/O Pad In/Out Control Bit[7]: P_YACLK Bit[6]: P_YCCLK Bit[5]: P_YSPWDN Bit[4]: P_YHREF Bit[3]: P_YVSYNC Bit[2]: P_YPCLK Bit[1]: P_Y[9] Bit[0]: P_Y[8]
0x2E	SENSOR_I0	–	R	I/O Pad Input Bit[7]: P_ACLK Bit[6]: P_CCLK Bit[5]: P_PWDN Bit[4]: P_HREF Bit[3]: P_VSYNC Bit[2]: P_PCLK Bit[1]: P_Y[9] Bit[0]: P_Y[8]
0x2F	SENSOR_V0	8'h00	RW	I/O Pad Output Bit[7]: P_ACLK Bit[6]: P_CCLK Bit[5]: P_PWDN Bit[4]: P_HREF Bit[3]: P_VSYNC Bit[2]: P_PCLK Bit[1]: P_Y[9] Bit[0]: P_Y[8]
0x30	REGULATOR_C0	8'hE9	RW	2.5V Regulator control Bit[7] PDENI Bit[6] PDI Bit[5] PD_REG Bit[4]: DIO2 Bit[3:0]: PVREF

Table 14 Register List of GPIO (Sheet 4 of 4)

Address (Hex)	Register Name	Default Value	R/W	Description
0x31	REGULATOR_C1	8'hE9	RW	1.8V Regulator control Bit[7] PDENI Bit[6] PDI Bit[5] PD_REG Bit[4]: DIO2 Bit[3:0]: PVREF
0x32	SD_PGA	8'h24	RW	SD PGA[7:0]
0x33	SD_C0	8'h29	RW	SD Control Bit[7]: RSWi Bit[6:4]: SD_RI Bit[3:0]: BGI
0x34	SD_C1	8'h04	RW	SD Control Bit[2]: SD PGA[8] Bit[1]: PWDNI Bit[0]: PDENI
0x39	GPIO_S0	8'h00	RW	I/O Pad Driving Strength Bit[7:0]: GPIO[7:0]
0x3A	GPIO_S1	8'h00	RW	I/O Pad (1: Normal mode, 0: Register control) Bit[7]: Reserved Bit[6]: P_OSCEN Bit[5]: P_RESET_ Bit[4]: P_SIO_C Bit[3]: P_SIO_D Bit[2:0]: GPIO[10:8]

Table 15 Register List of Video Data[a]

Address (Hex)	Register Name	Default Value	R/W	Description
0x00	V_FMT	8'h40	RW	Bit[7]: Swap even byte and odd byte Bit[6:5]: Video Format 000: RAW8 001: RAW10 010: RAW16 011: Reserved 100: YUV422 101: YUV411, first line is YYYY, second line is YUYV 110: YUV411, first line is YUYV, second line is YYYY 111: YUV411, first line is UYY, second line is VYY Bit[3]: Transfer select 0: BULK transfer 1: ISO transfer Bit[2]: Still image header for USB video class Bit[1:0]: Reserved
0x01	PLOAD_H	8'h00	RW	Bit[15:8]: Of pay load size, divided by 4
0x02	PLOAD_L	8'h80	RW	Bit[7:0]: Of pay load size, divided by 4
0x03	FRAME_H	8'h0A	RW	Bit[23:16]:Of frame size, divided by 4
0x04	FRAME_M	8'h00	RW	Bit[15:8]: Of frame size, divided by 4
0x05	FRAME_L	8'h00	RW	Bit[7:0]: Of frame size, divided by 4
0x06	HEADER3	8'hFF	RW	Input header byte 3 for Internal use
0x07	HEADER2	8'h5A	RW	Input header byte 2 for Internal use
0x08	HEADER1	8'hA5	RW	Input header byte 1 for Internal use
0x09	HEADER0	8'h00	RW	Input header byte 0 for Internal use
0x0A	V_CNTL0	8'h08	RW	Bit[7]: Reserved Bit[6]: Internal video RAM BIST enable Bit[5:4]: Reserved Bit[3]: Compression Header Format enable Bit[2]: Reserved Bit[1]: Header End for USB video class Bit[0]: Header Reserved for USB video class
0x0B	V_CNTL1	8'h0E	RW	Bit[7]: Internal video RAM BIST OK Bit[6]: Internal video RAM BIST ERR Bit[5:4]: Reserved Bit[3]: Auto Frame size Bit[2:0]: Reserved

a. The video data registers are indirectly controlled by 0x1C and 0x1D registers.

Package Specifications

The OV538-B88 uses a 64-pin BGA package. Refer to Figure 8 for package information.

Figure 8 OV538-B88 Package Specifications

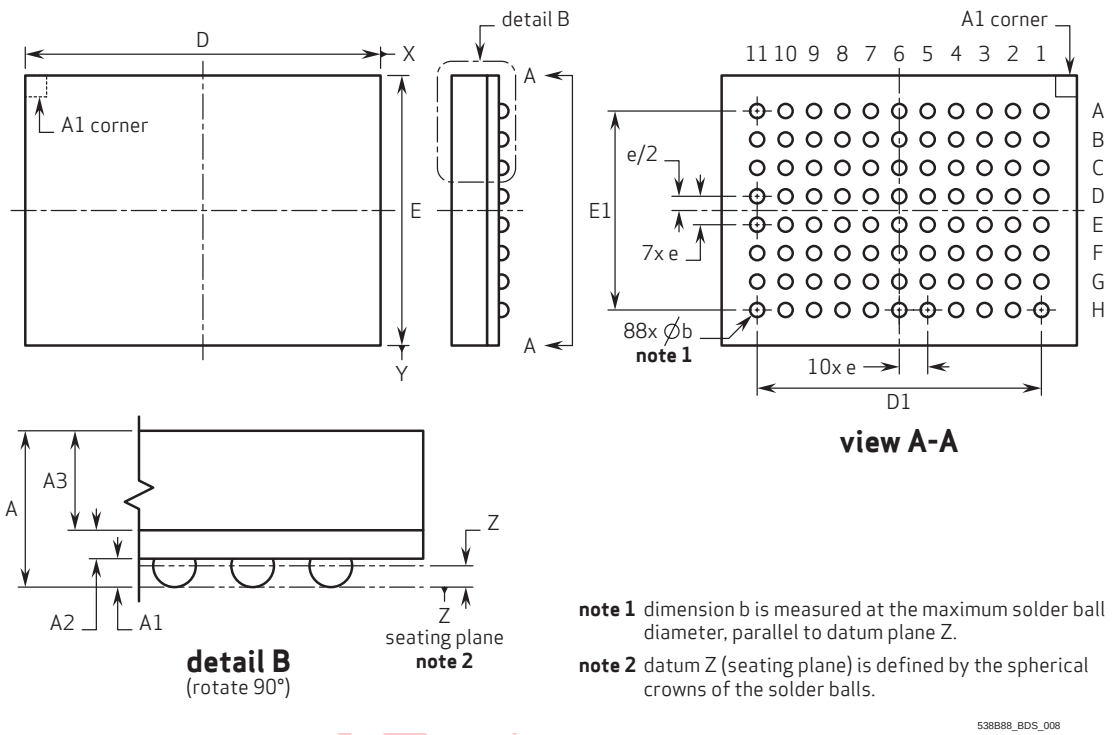


Table 16 88-Pin BGA Package Dimensions

Dimension	Symbol	Minimum	Nominal	Maximum	Units
Package Height	A			1.3	mm
Ball Height	A1	0.16		0.26	mm
	A2		0.32 REF		
	A3		0.7 REF		
Ball Diameter	b	0.27		0.37	mm
Package Body Dimension Y	D		8 BSC		mm
Ball Center-to-Center Y-axis	D1	5.50	6.5 BSC	5.70	mm
Package Body Dimension X	E		6 BSC		mm
Ball Center-to-Center X-axis	E1		4.55 BSC		mm
Ball Pitch	e		0.65 BSC		mm

Note:

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For further information, please feel free to contact OmniVision at info@ovt.com.

OmniVision Technologies, Inc.
1341 Orleans Drive
Sunnyvale, CA USA
(408) 542-3000

REVISION CHANGE LIST

Document Title: OV538-B88 Datasheet **Version:** 1.0

DESCRIPTION OF CHANGES

- Initial Release

REVISION CHANGE LIST

Document Title: OV538-B88 Datasheet **Version:** 1.1

DESCRIPTION OF CHANGES

The following changes were made to version 1.0.

- Updated Key Specifications: Power Requirements on page 1, changed values from (Active: TBD, Standby: TBD); changed values to (Active: 82 mA, Standby: 230 µA)
- Updated Table 1: Pin Description on page 7, changed values:

Ball Number	Name	Pin Type	Function/Description
Power and Ground			
C11	IO_VDD2	Power	3.3V Audio Power
C10	IO_VSS2	Ground	Audio Ground
E11	CORE_VDD2	Power	I/O Power
B7	CORE_VSS2	Ground	I/O Ground
F11	VSSU	Ground	1.8V Core Power
G10	VDDU	Power	1.8V Core Ground
H8/G8	VS33P	Ground	USB Analog Ground
G11/H7	VD33P	Power	3.3V USB Analog Power
G9	VD33	Power	USB Digital Ground

values updated to:

Ball Number	Name	Pin Type	Function/Description
Power and Ground			
C11	IO_VDD2	Power	IO Power
C10	IO_VSS2	Ground	IO Ground
E11	CORE_VDD2	Power	1.8 V Core Power
B7	CORE_VSS2	Ground	1.8 V Core Ground
F11	VSSU	Ground	1.8V USB Core Ground
G10	VDDU	Power	1.8V USB Core Ground
H8/G8	VS33P	Ground	3.3V USB Ground
G11/H7	VD33P	Power	3.3V USB Power
G9	VD33	Power	3.3V USB Digital Power

- Updated Table 3: DC Electrical Characteristics on page 8, values changed from:

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD_IO}	DC supply voltage - I/O	3.3V ± 10%	TBD	TBD	TBD	V
V_{DD_CORE}	DC supply voltage - Core	1.8V ± 5%	TBD	TBD	TBD	V
V_{IH}	Input voltage HIGH	CMOS	TBD			V
V_{IL}	Input voltage LOW	CMOS			TBD	V
V_{OH}	Output voltage HIGH	$I_{OH = 4mA}$	TBD			V
V_{OL}	Output voltage LOW	$I_{OL = 4mA}$			TBD	V
I_S	Suspend current			TBD	TBD	µA
I_{DDA}	Operating current			TBD		mA

changed to:

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD_IO}	DC supply voltage - I/O	3.3V ± 10%	3.0	3.3	3.6	V
V_{DD_CORE}	DC supply voltage - Core	1.8V ± 5%	1.7	1.8	2.0	V
V_{IH}	Input voltage HIGH	CMOS	2.3			V
V_{IL}	Input voltage LOW	CMOS			0.7	V
V_{OH}	Output voltage HIGH	$I_{OH = 4mA}$	2.4			V
V_{OL}	Output voltage LOW	$I_{OL = 4mA}$			0.5	V
I_S	Suspend current			230	350	µA
I_{DDA}	Operating current	1600 x 1200, 7.5 fps[a]		82		mA

a. ISP: On, JPG: On

- Updated Table 4: 1.8 Regulator Electrical Characteristics on page 9, values changed from:

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OUT}	Output voltage	I_{OUT} = 1mA, Typ=3.3V I_{OUT} = 40mA, Typ=3.3V I_{OUT} = 80mA, Typ=3.3V I_{OUT} = 100mA, Typ=3.3V		TBD TBD TBD TBD		V
ΔV_{LINE}	Line regulation	2.7V<V_{IN}<3.6V	–	–	TBD	mV
ΔV_{LOAD}	Load regulation	1mA<I_{OUT} <100mA	–	–	TBD	mV
V_{DROP}	Dropout voltage		–	–	TBD	mV
I_{LIMIT}	Current limit		–	–	TBD	mA
I_{MIN}	Min current load		TBD	–	–	µA
I_{OPER}	Operating current	I_{OUT} = 100mA	–	TBD	–	mA
I_{QUIE}	Quiescent current	I_{OUT} = 0mA	–	TBD	–	mA

changed to:

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OUT}	Output voltage	I_{OUT} = 1mA, Typ=3.3V I_{OUT} = 40mA, Typ=3.3V I_{OUT} = 80mA, Typ=3.3V I_{OUT} = 100mA, Typ=3.3V		1.82 1.81 1.80 1.79		V
ΔV_{LINE}	Line regulation	2.7V<V_{IN}<3.6V	–	–	20	mV
ΔV_{LOAD}	Load regulation	1mA<I_{OUT} <100mA	–	–	65	mV
V_{DROP}	Dropout voltage		–	–	900	mV
I_{LIMIT}	Current limit		–	–	100	mA
I_{MIN}	Min current load		0	–	–	µA
I_{OPER}	Operating current	I_{OUT} = 100mA	–	1	–	mA
I_{QUIE}	Quiescent current	I_{OUT} = 0mA	–	1	–	mA

- Updated Table 5: 2.5V Regulator Electrical Characteristics on page 9, values changed from:

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OUT}	Output voltage	I_{OUT} = 1mA, Typ=3.3V I_{OUT} = 20mA, Typ=3.3V I_{OUT} = 40mA, Typ=3.3V I_{OUT} = 50mA, Typ=3.3V		TBD TBD TBD TBD		V
ΔV_{LINE}	Line regulation	3.0V<V_{IN}<3.6V			TBD	mV
ΔV_{LOAD}	Load regulation	1mA<I_{OUT} <50mA			TBD	mV
V_{DROP}	Dropout voltage	3.0V<V_{IN}<3.6V, 0mA<I_{OUT} <50mA			TBD	mV
I_{LIMIT}	Current limit				TBD	mA
I_{MIN}	Min current load		TBD			µA
I_{OPER}	Operating current	I_{OUT} = 50mA		TBD		mA
I_{QUIE}	Quiescent current	I_{OUT} = 0mA		TBD		mA

- Changed to:

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OUT}	Output voltage	I_{OUT} = 1mA, Typ=3.3V I_{OUT} = 20mA, Typ=3.3V I_{OUT} = 40mA, Typ=3.3V I_{OUT} = 50mA, Typ=3.3V		2.50 2.49 2.48 2.47		V
ΔV_{LINE}	Line regulation	3.0V<V_{IN}<3.6V			20	mV
ΔV_{LOAD}	Load regulation	1mA<I_{OUT} <50mA			60	mV
V_{DROP}	Dropout voltage	3.0V<V_{IN}<3.6V, 0mA<I_{OUT} <50mA			500	mV
I_{LIMIT}	Current limit				80	mA
I_{MIN}	Min current load		0			µA
I_{OPER}	Operating current	I_{OUT} = 50mA		1		mA
I_{QUIE}	Quiescent current	I_{OUT} = 0mA		1		mA

- Updated Table 6: Master SCCB Timing Specifications on page 10, values changed from:

Symbol	Parameter	Condition	Min	Typ	Max
f_{SIO_C}	SIO_C clock frequency			TBD	
t_{HIGH}	SIO_C clock high time			TBD	
t_{LOW}	SIO_C clock low time			TBD	
t_{HDSTA}	Start of transmission hold time			TBD	
t_{SUSTP}	Stop of transmission setup time			TBD	
t_{SUDOUT}	Output data transmission setup time			TBD	
t_{HDDOUT}	Output data transmission hold time			TBD	
t_R	SIO_C clock rising time[a]			TBD	
t_F	SIO_C clock failing time[a]			TBD	
t_{SUDIN}	Input data setup time		TBD		
t_{HDDIN}	Input data hold time		TBD		

a. R_{pup}=10KΩ

Changed to:

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{SIO_C}	SIO_C clock frequency			395		KHz
t_{HIGH}	SIO_C clock high time			1.09		us
t_{LOW}	SIO_C clock low time			1.28		us
t_{HDSTA}	Start of transmission hold time			1.27		us
t_{SUSTP}	Stop of transmission setup time			0.64		us
t_{SUDOUT}	Output data transmission setup time			0.62		us
t_{HDDOUT}	Output data transmission hold time			0.62		us
t_R	SIO_C clock rising time[a]			300		ns
t_F	SIO_C clock failing time[a]			12		ns
t_{SUDIN}	Input data setup time		0.5			us
t_{HDDIN}	Input data hold time		0			us

a. R_{pup}=3.3K

- Updated Table 7: Slave Audio Interface AC Timing Specifications on page 11, values changed from:

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_R	ACLK clock rise time		–	TBD	–	us
t_F	ACLK clock fall time		–	TBD	–	us
t_{SU}	Data setup time		–	–	TBD	us
t_{HD}	Data hold time		–	–	TBD	us

Changed to:

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_R	ACLK clock rise time		–	4.2	–	ns
t_F	ACLK clock fall time		–	3.75	–	ns
t_{SU}	Data setup time		4	–	–	ns
t_{HD}	Data hold time		37	–	–	ns

- Updated Table 9: Input Clock X_IN Timing Specifications on page 11, values changed from:

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{X_IN}	Input clock frequency		TBD	TBD	TBD	MHz
$t_{X\_IN\_DCY}$	Input clock duty cycle		TBD	TBD	TBD	%

Changed to:

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{X_IN}	Input clock frequency			12.0		MHz
$t_{X\_IN\_DCY}$	Input clock duty cycle		40	50	60	%

- Updated Table 10: Input PCLK Timing Specifications on page 11, values changed from:

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PCK}	Input clock frequency		TBD	TBD	TBD	MHz
t_{PCK_DCY}	Input clock duty cycle		TBD	TBD	TBD	%

Changed to:

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PCK}	Input clock frequency			24	48	MHz
t_{PCK_DCY}	Input clock duty cycle		40	50	60	%

- Updated Table 11: Output CCLK Timing Specifications on page 13, values changed from:

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{CCK}	Output clock frequency		TBD	TBD	TBD	MHz
t_{CCK_DCY}	Output clock duty cycle		TBD	TBD	TBD	%

Changed to:

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{CCK}	Output clock frequency			24		MHz
t_{CCK_DCY}	Output clock duty cycle		40	50	60	%