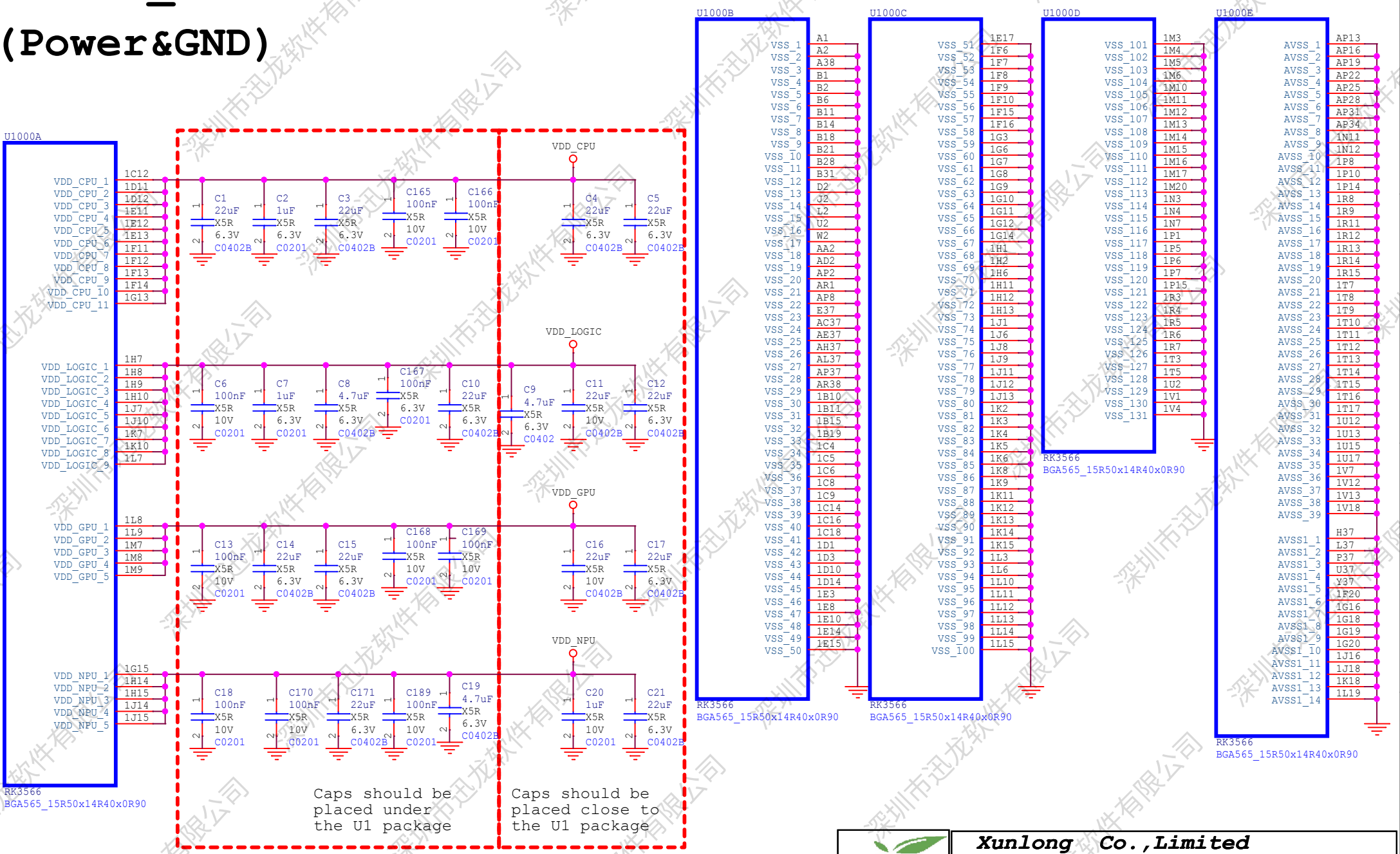
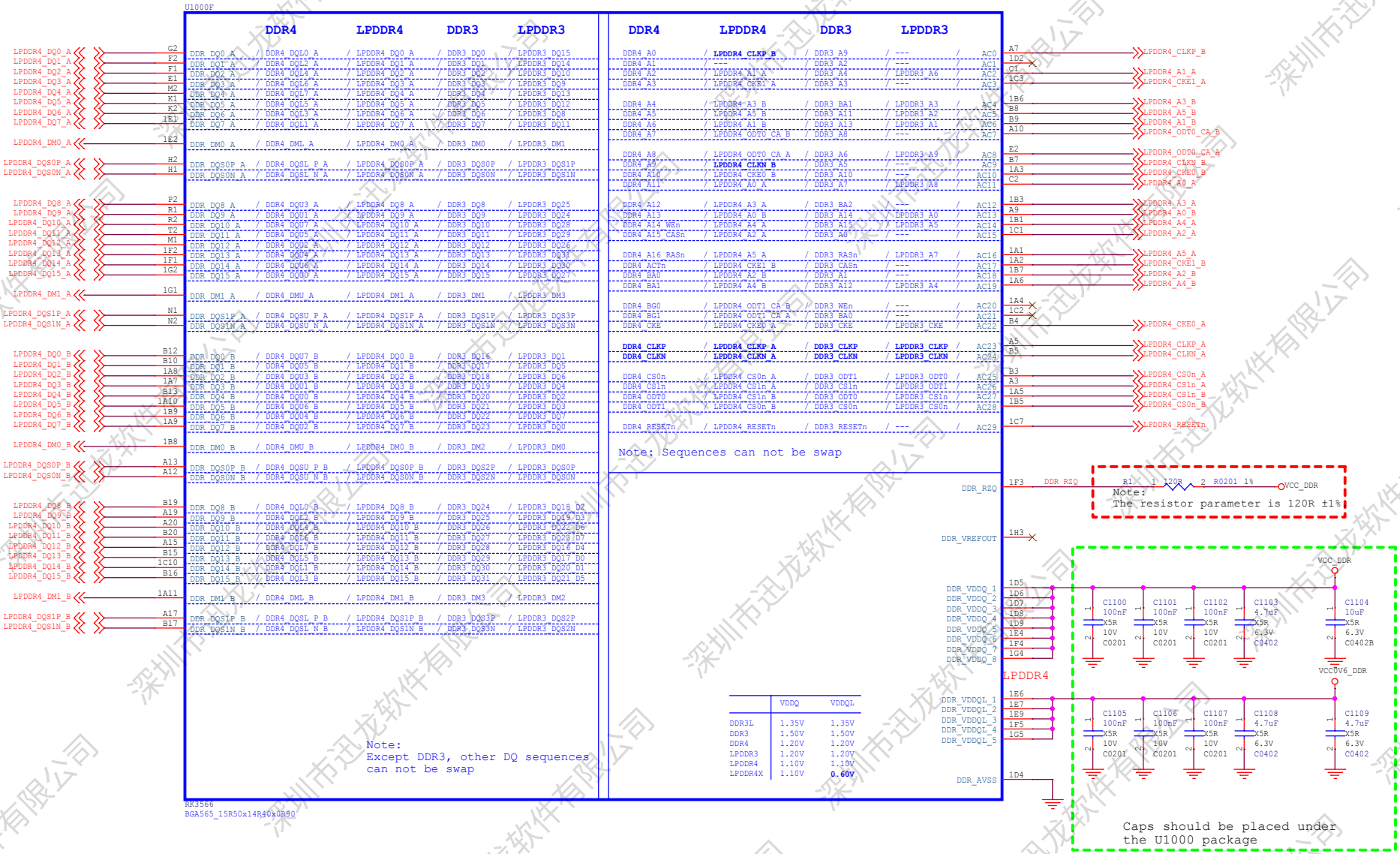
RK3566_ABCDE

(Power&GND)



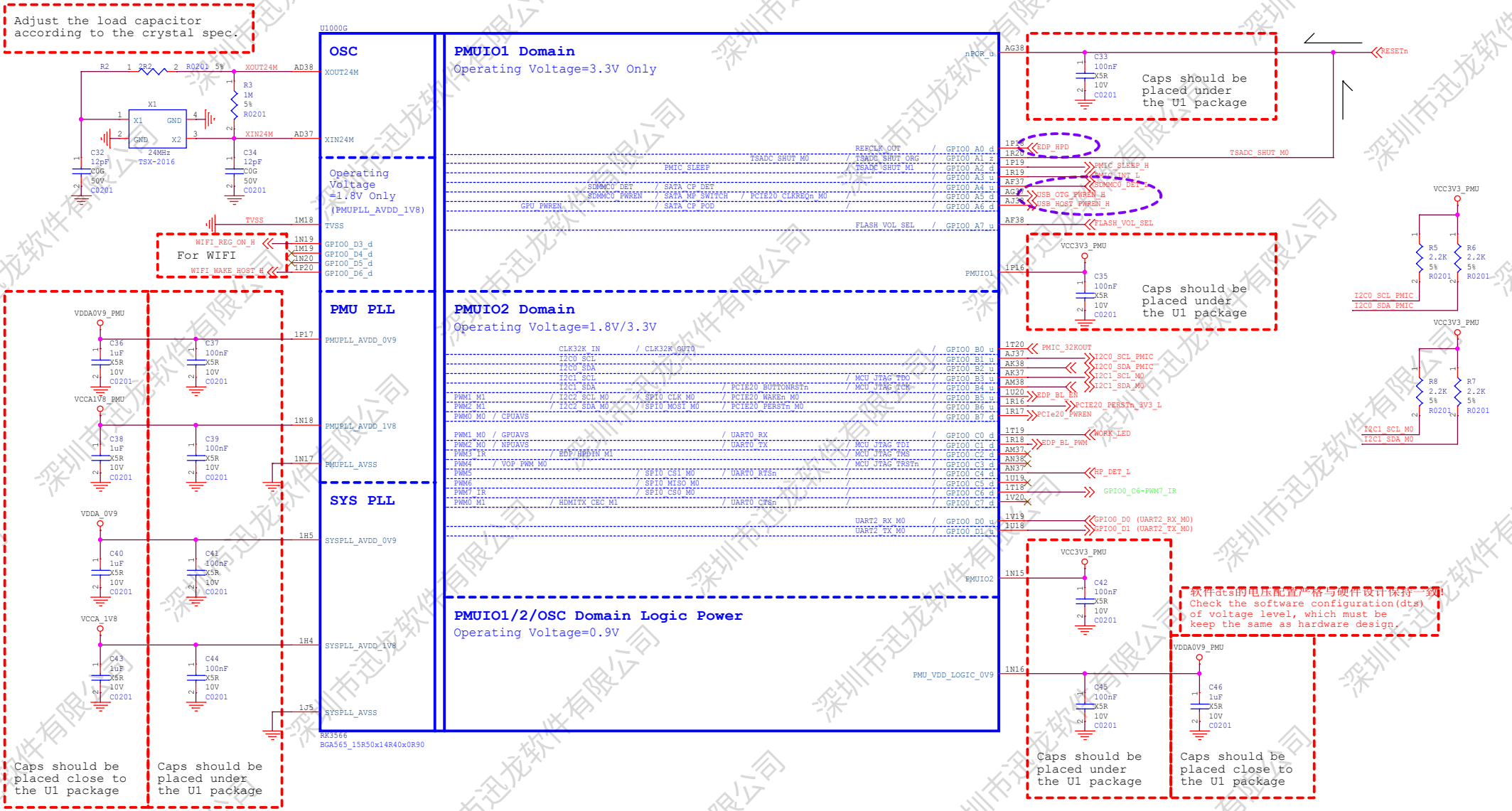
Xunlong Co.,Limited			
Design Name: OPi3B			
Size: A4	Page Name: 08RK3566_Power/GND		Rev: 1.0
Date: Monday, August 14, 2023	Sheet 8 of 28		

RK3566_F(DDR PHY)



Xunlong Co.,Limited		
Design Name	OPi3B	
Size A3	Page Name 09RK3566_DDR_PHY	Rev 1.0
Date: Monday, August 14, 2023	Sheet 9 of 28	

RK3566_G(OSC/PLL/PMUIO1/2)



Xunlong Co.,Limited		
Design Name: OPi3B		
Size: A3	Page Name: 10.RK3566_OSC/PLL/PMUIO	Rev: 1.0
Date: Monday, August 14, 2023	Sheet 10 of 28	

RK3566_I(VCCIO2 Domain)

U1000I

VCCIO2 Domain

Operating Voltage=1.8V/3.3V

EMMC_D0	/ FLASH_D0	/ GPIO1_B4_u	A32	eMMC_D0/FLASH_D0
EMMC_D1	/ FLASH_D1	/ GPIO1_B5_u	B27	eMMC_D1/FLASH_D1
EMMC_D2	/ FLASH_D2	/ GPIO1_B6_u	B32	eMMC_D2/FLASH_D2
EMMC_D3	/ FLASH_D3	/ GPIO1_B7_u	B29	eMMC_D3/FLASH_D3
EMMC_D4	/ FLASH_D4	/ GPIO1_C0_u	B33	eMMC_D4/FLASH_D4
EMMC_D5	/ FLASH_D5	/ GPIO1_C1_u	A30	eMMC_D5/FLASH_D5
EMMC_D6	/ FLASH_D6	/ GPIO1_C2_u	B30	eMMC_D6/FLASH_D6
EMMC_D7	/ FLASH_D7	/ GPIO1_C3_u	A33	eMMC_D7/FLASH_D7
EMMC_CMD	/ FLASH_WRn	/ GPIO1_C4_u	A27	eMMC_CMD/FLASH_WRn
EMMC_CLKOUT	/ FLASH_DQS	/ GPIO1_C5_d	A29	eMMC_CLKOUT/FLASH_DQS
EMMC_DATA_STROBE	/ FSPI_CS1n / FLASH_CLE	/ GPIO1_C6_d	1A16	eMMC_DATA_STROBE/FLASH_CLE
EMMC_RSTn	/ FSPI_D2 / FLASH_WPn	/ GPIO1_C7_d	1B16	eMMC_RSTn/FSPI_D2/FLASH_WPn
	FSPI_CLK / FLASH_ALE	/ GPIO1_D0_d	1A15	FSPI_CLK/FLASH_ALE
	FSPI_D0 / FLASH_RDY	/ GPIO1_D1_u	1A17	FSPI_D0/FLASH_RDY
	FSPI_D1 / FLASH_RDn	/ GPIO1_D2_u	1A18	FSPI_D1/FLASH_RDn
	FSPI_CS0n / FLASH_CS0n	/ GPIO1_D3_u	1B17	FSPI_CS0n/FLASH_CS0n
	FSPI_D3 / FLASH_CS1n	/ GPIO1_D4_u	1C15	FSPI_D3/FLASH_CS1n

Default is determined by Pin
FLASH_VOL_SEL/GPIO0_A7_u:
L:VCCIO2 must supply 3.3V
H:VCCIO2 must supply 1.8V

VCCIO2 — 1C13

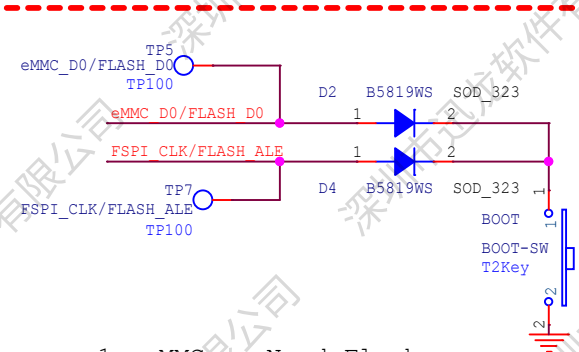
RK3566
BGA565_15R50x14R40x0R90

VCCIO_FLASH — 1.8V

C47 100nF X5R 10V C0201

Caps should be placed under the U1 package

软件dts的电压配置严格与硬件设计保持一致!
Check the software configuration(dts) of voltage level, which must be keep the same as hardware design.



1. eMMC or Nand Flash:
   Short 'eMMC_D0/FLASH_D0' and GND to enter Maskrom Mode.

2. SPI Flash:
   Short 'FSPI_CLK/FLASH_ALE' and GND to enter Maskrom Mode.

Be sure to reserve the testpoints for firmware burning or update.

RK3566_J(VCCIO3 Domain)

U1000J

VCCIO3 Domain

Operating Voltage=1.8V/3.3V

PWM8_M1 / SDMMC0_D0	/ UART2_TX_M1 / UART6_TX_M1	/ GPIO1_D5_u	1E20	SDMMC0_D0
PWM9_M1 / SDMMC0_D1	/ UART2_RX_M1 / UART6_RX_M1	/ GPIO1_D6_u	1F19	SDMMC0_D1
SDMMC0_D2	/ ARM_JTAG_TCK/ UART5_CTSn_M0	/ GPIO1_D7_u	1D20	SDMMC0_D2
SDMMC0_D3	/ ARM_JTAG_TMS/ UART5_RTSn_M0	/ GPIO2_A0_u	1F18	SDMMC0_D3
PWM10_M1 / SDMMC0_CMD	/ UART5_RX_M0	/ GPIO2_A1_u	1E19	SDMMC0_CMD
SDMMC0_CLK / TEST_CLKOUT	/ UART5_TX_M0	/ GPIO2_A2_d	G38	SDMMC0_CLK

VCCIO3 — 1F17

VCCIO_SD

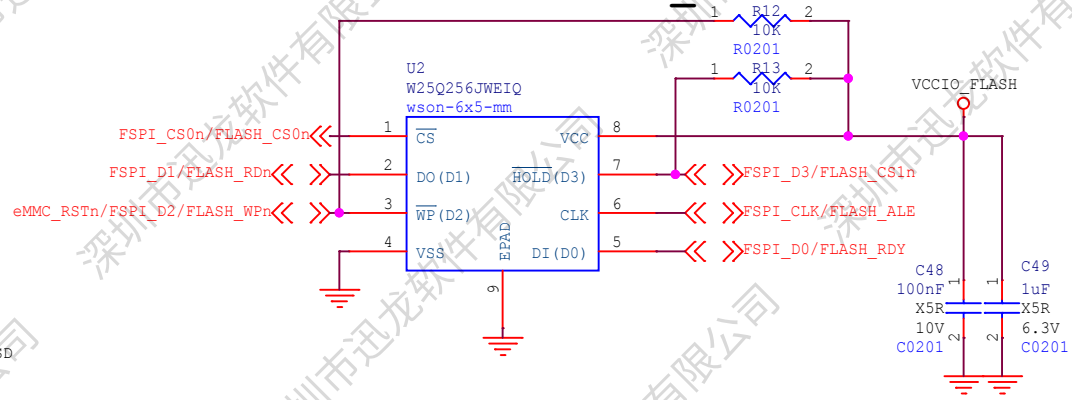
C50 100nF X5R 10V C0201

Caps should be placed under the U1 package

RK3566
BGA565_15R50x14R40x0R90

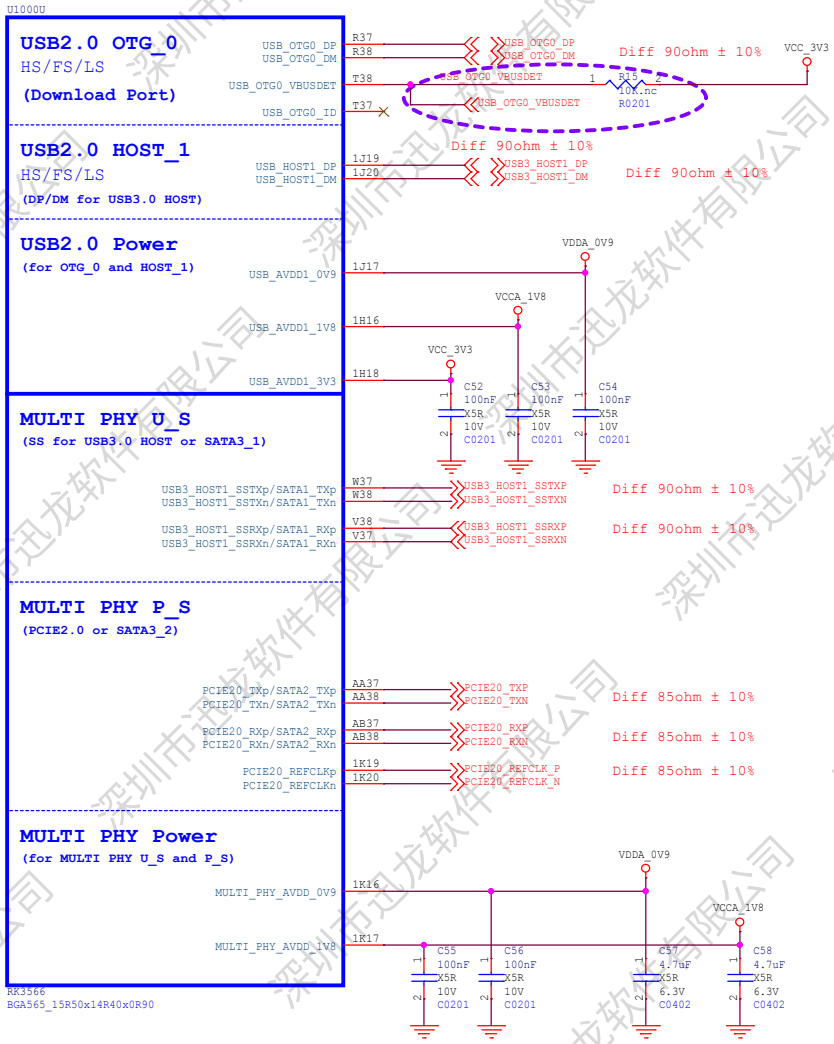
软件dts的电压配置严格与硬件设计保持一致!
Check the software configuration(dts) of voltage level, which must be keep the same as hardware design.

default VCC = VCCIO_FLASH 1.8V

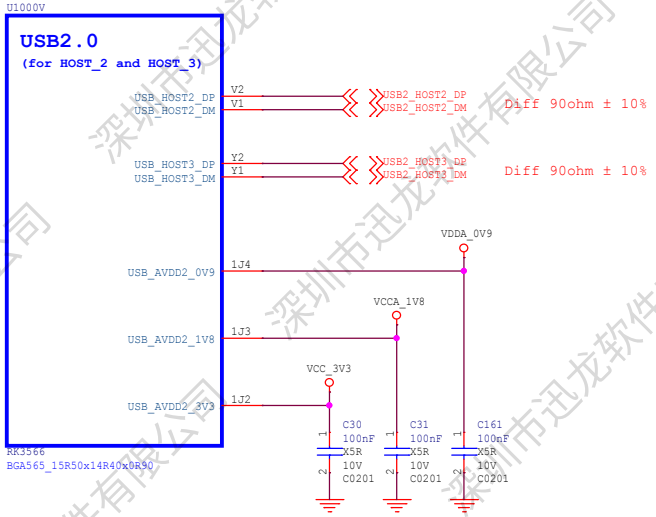


Xunlong Co.,Limited		
Design Name: OPi3B		
Size: A4	Page Name: 11RK3566_Flash/SD_Contr	Rev: 1.0
Date: Monday, August 14, 2023	Sheet 11 of 28	

RK3566_U(USB3.0/PCIe2.0x1/SATA)

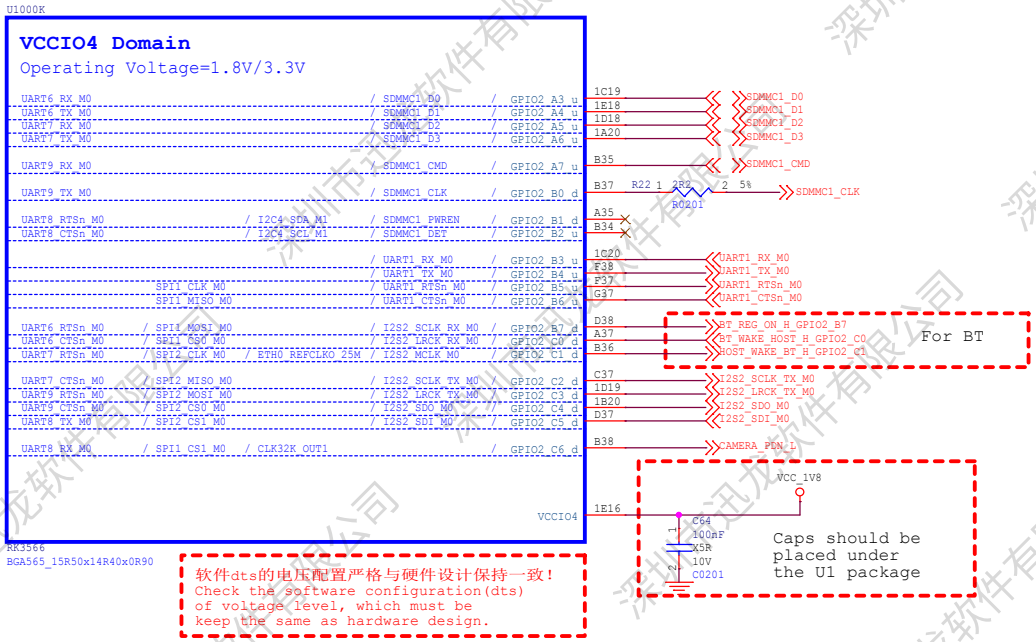


RK3566_V(USB2.0 HOST)



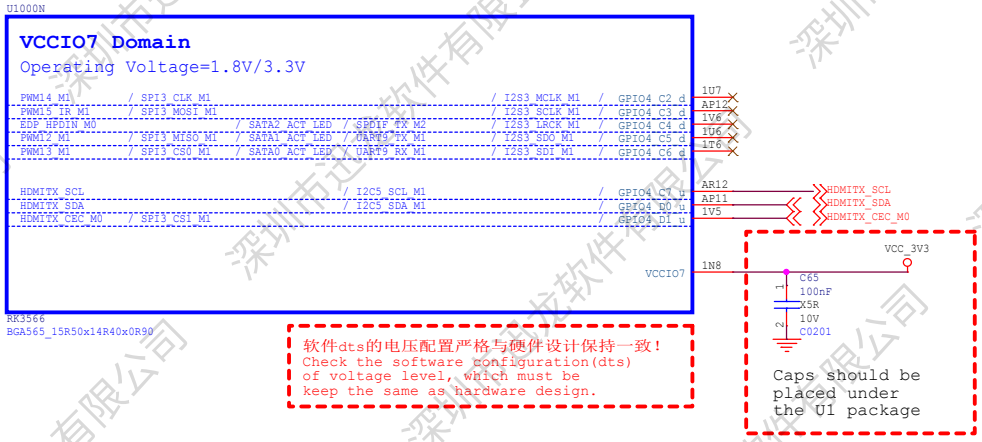
Xunlong Co.,Limited		
Design Name	OPi3B	
Size A3	Page Name 12.RK3566_USB/PCIe/SATA_PHY	Rev 1.0
Date: Monday, August 14, 2023	Sheet 12 of 28	

RK3566_K(VCCIO4 Domain)



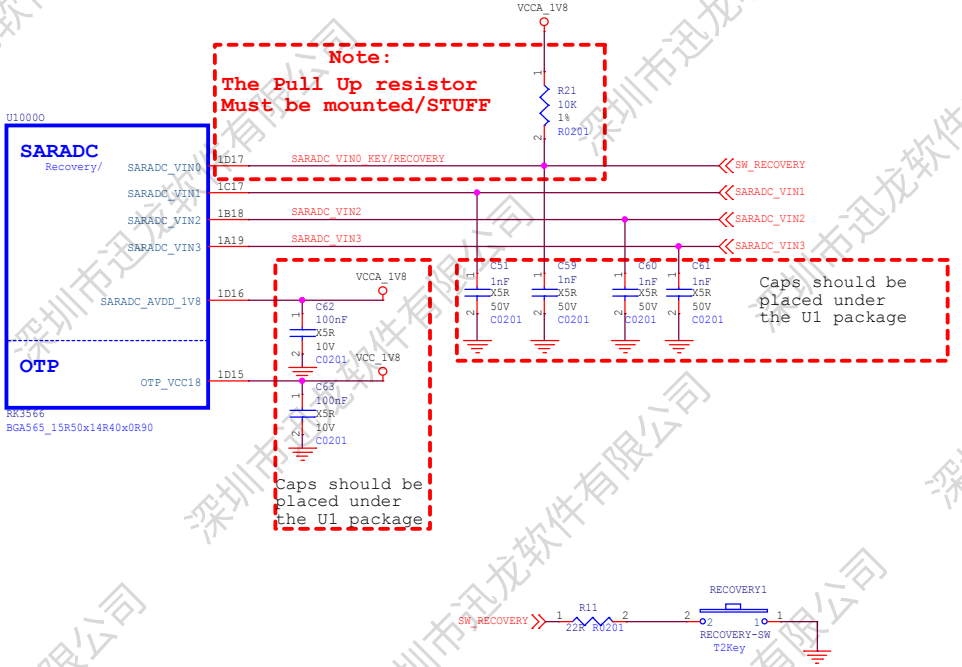
软件dts的电压配置严格与硬件设计保持一致!
Check the software configuration(dts) of voltage level, which must be keep the same as hardware design.

RK3566_N(VCCIO7 Domain)



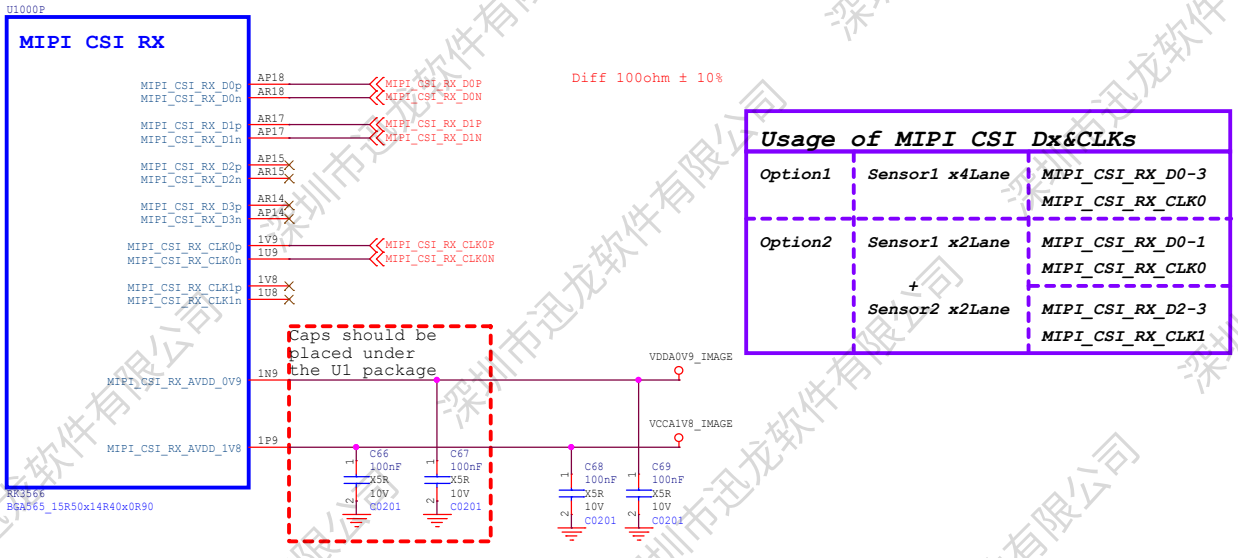
软件dts的电压配置严格与硬件设计保持一致!
Check the software configuration(dts) of voltage level, which must be keep the same as hardware design.

RK3566_O(SARADC/OTP)



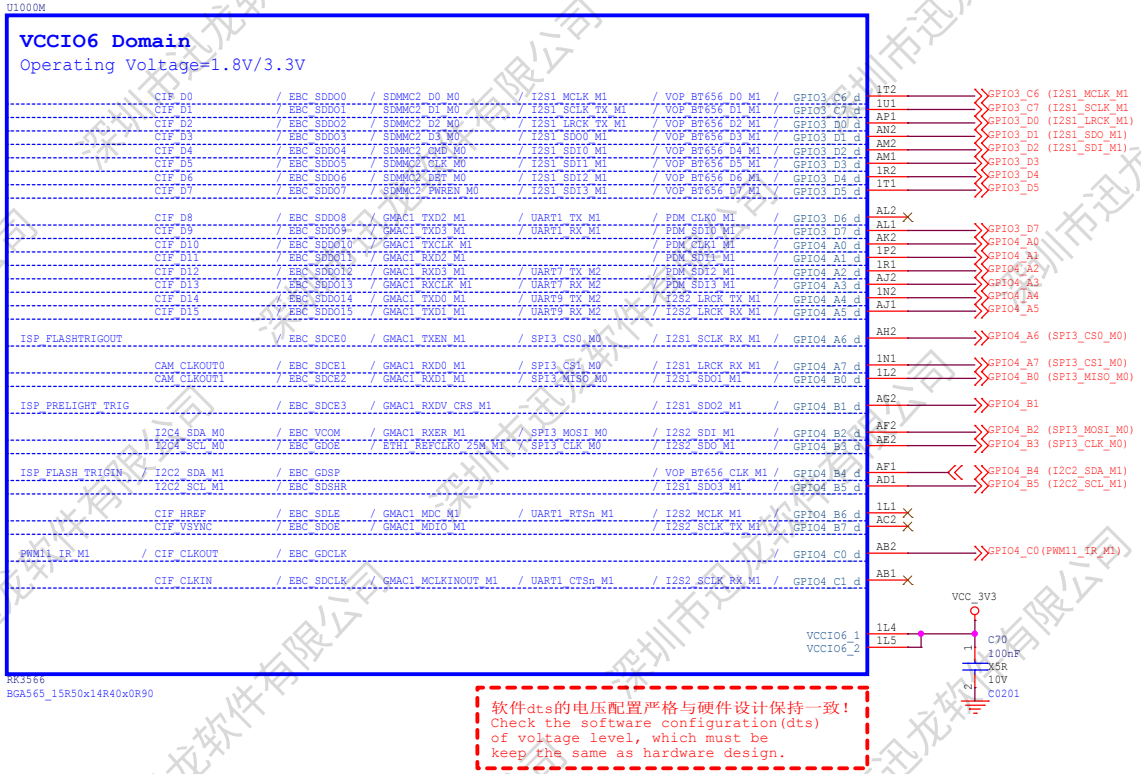
Xunlong Co.,Limited		
Design Name: OPi3B		
Size: A3	Page Name: 13.RK3566_SARADC/GPIO	Rev: 1.0
Date: Monday, August 14, 2023	Sheet 13 of 28	

RK3566_P(MIPI_CSI_RX)

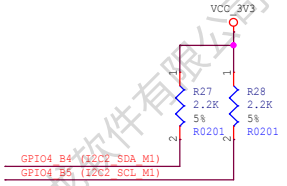


Usage of MIPI CSI Dx&CLKs		
Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

RK3566_M(VCCIO6 Domain)



软件dts的电压配置严格与硬件设计保持一致!
Check the software configuration(dts) of voltage level, which must be keep the same as hardware design.



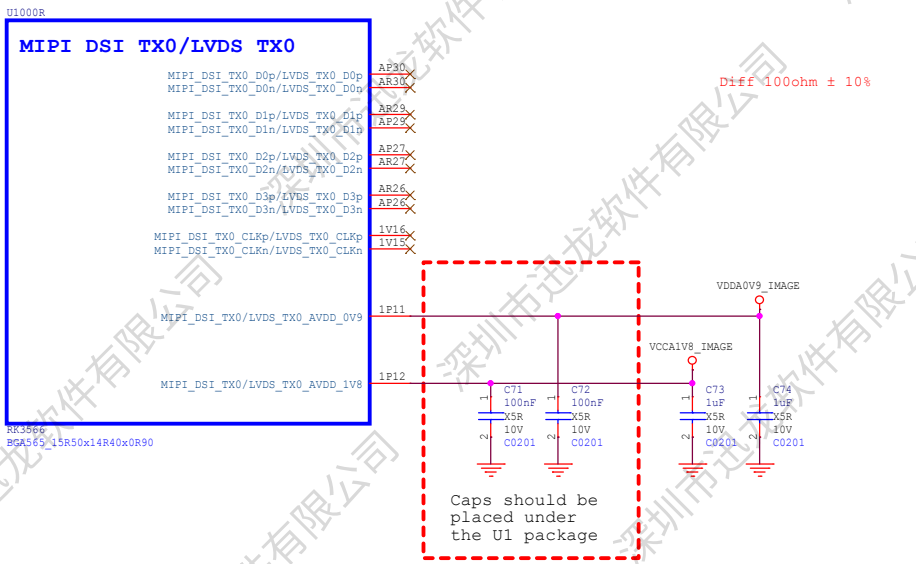
Xunlong Co.,Limited

Design Name: OPi3B

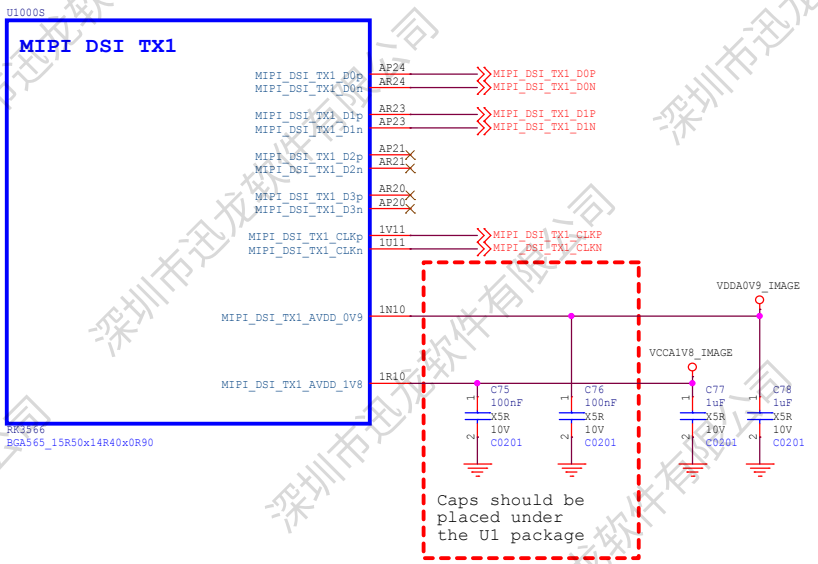
Size: A3 | Page Name: 14RK3566_CSI/GPIO | Rev: 1.0

Date: Monday, August 14, 2023 | Sheet 14 of 28

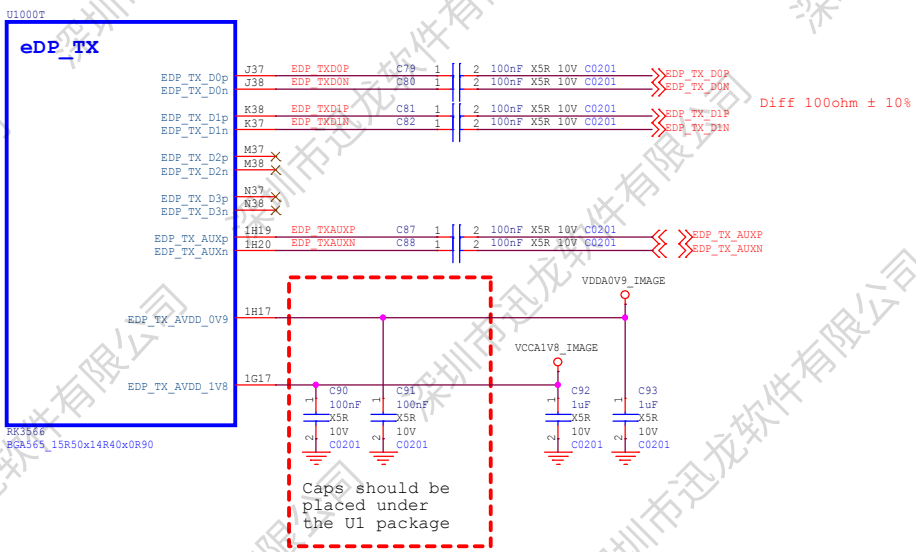
RK3566_R(MIPI_DSI_TX0/LVDS_TX0)



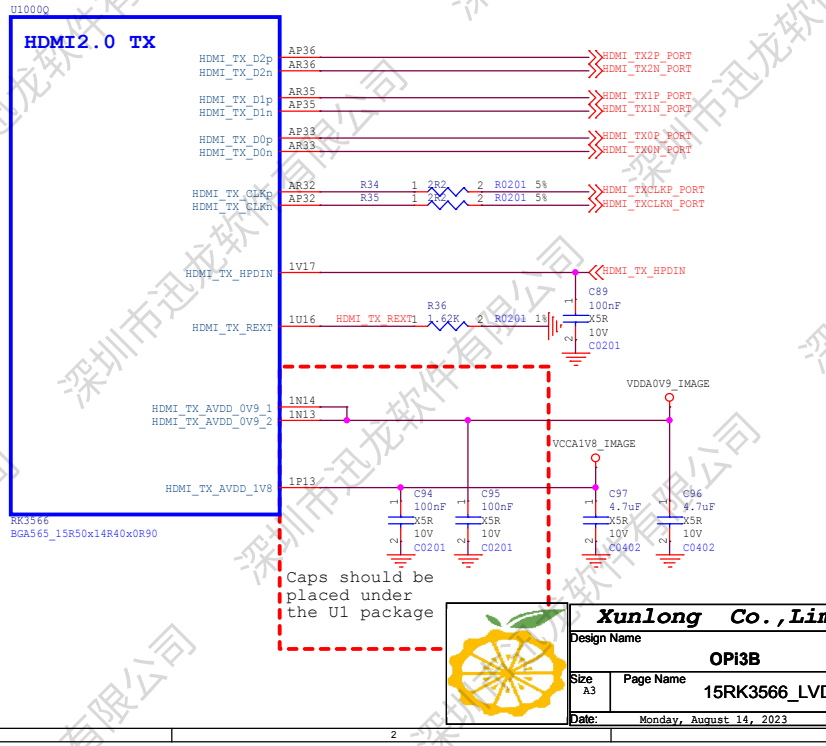
RK3566_S(MIPI_DSI_TX1)



RK3566_T(eDP TX)



RK3566_Q(HDMI2.0 TX)



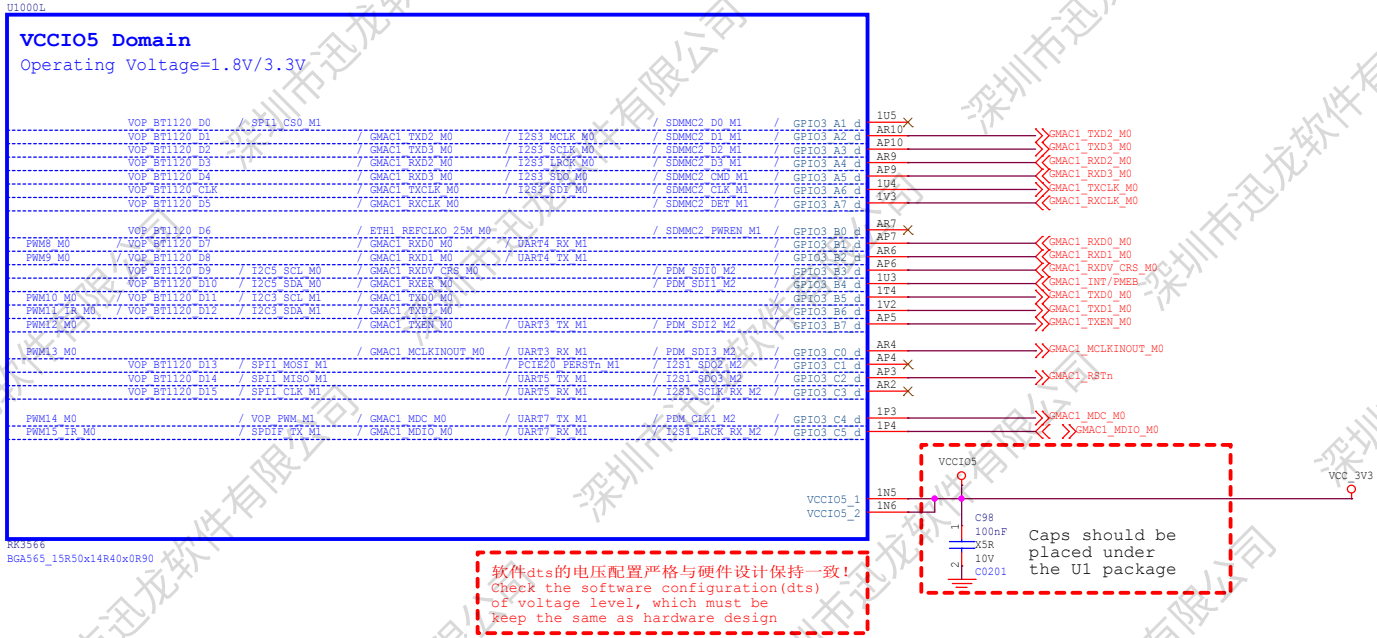
Xunlong Co.,Limited

Design Name: OPi3B

Size: A3 | Page Name: 15RK3566_LVDS_MIPI | Rev: 1.0

Date: Monday, August 14, 2023 | Sheet 15 of 28

RK3566_L(VCCIO5 Domain)



GMAC	Direction	GEPHY	GMAC	Direction	FEPHY
GMACx_TXD0	------>	PHYx_TXD0	GMACx_TXD0	------>	PHYx_TXD0
GMACx_TXD1	------>	PHYx_TXD1	GMACx_TXD1	------>	PHYx_TXD1
GMACx_TXD2	------>	PHYx_TXD2			
GMACx_TXD3	------>	PHYx_TXD3			
GMACx_TXEN	------>	PHYx_TXEN	GMACx_TXEN	------>	PHYx_TXEN
GMACx_TXCLK	------>	PHYx_TXCLK			
GMACx_RXD0	<------	PHYx_RXD0	GMACx_RXD0	<------	PHYx_RXD0
GMACx_RXD1	<------	PHYx_RXD1	GMACx_RXD1	<------	PHYx_RXD1
GMACx_RXD2	<------	PHYx_RXD2			
GMACx_RXD3	<------	PHYx_RXD3			
GMACx_RXDV	<------	PHYx_RXDV	GMACx_RXDV	<------	PHYx_CRS_DV
GMACx_RXCLK	<------	PHYx_RXCLK			
GMACx_RXER			GMACx_RXER	<------	PHYx_RXER
GMACx_MDC	------>	PHYx_MDC	GMACx_MDC	------>	PHYx_MDC
GMACx_MDIO	<----->	PHYx_MDIO	GMACx_MDIO	<----->	PHYx_MDIO
ETHx_REFCLKO_25M	------>	PHYx_XTALIN			
GMACx_MCLKINOUT	<------	PHYx_CLKOUT125 (Option)	GMACx_MCLKINOUT	------>	PHYx_XTALIN/REFCLK
GPIO	------>	PHYx_RSTn	GPIO	------>	PHYx_RSTn
GPIO	<------	PHYx_INT/PMEB	GPIO	<------	PHYx_INT/PMEB

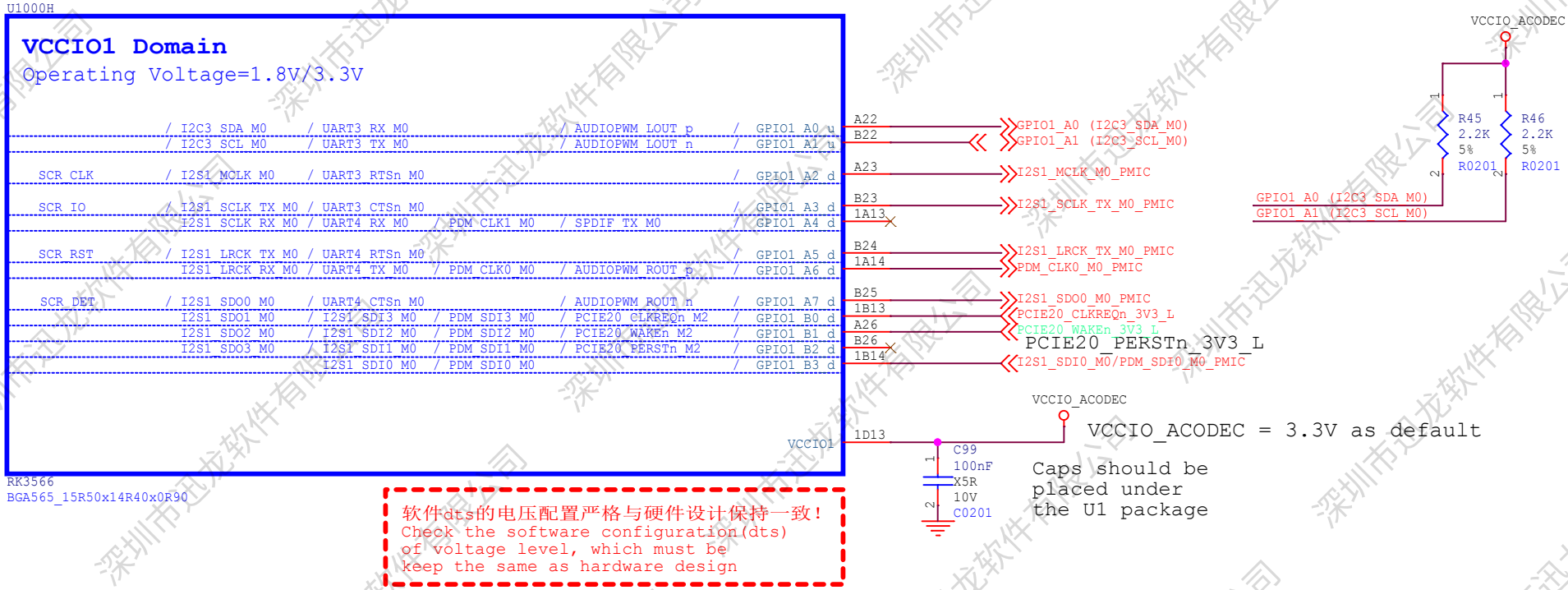
Xunlong Co.,Limited

Design Name: OPi3B

Size: A3 | Page Name: 16RK3566_GMAC | Rev: 1.0

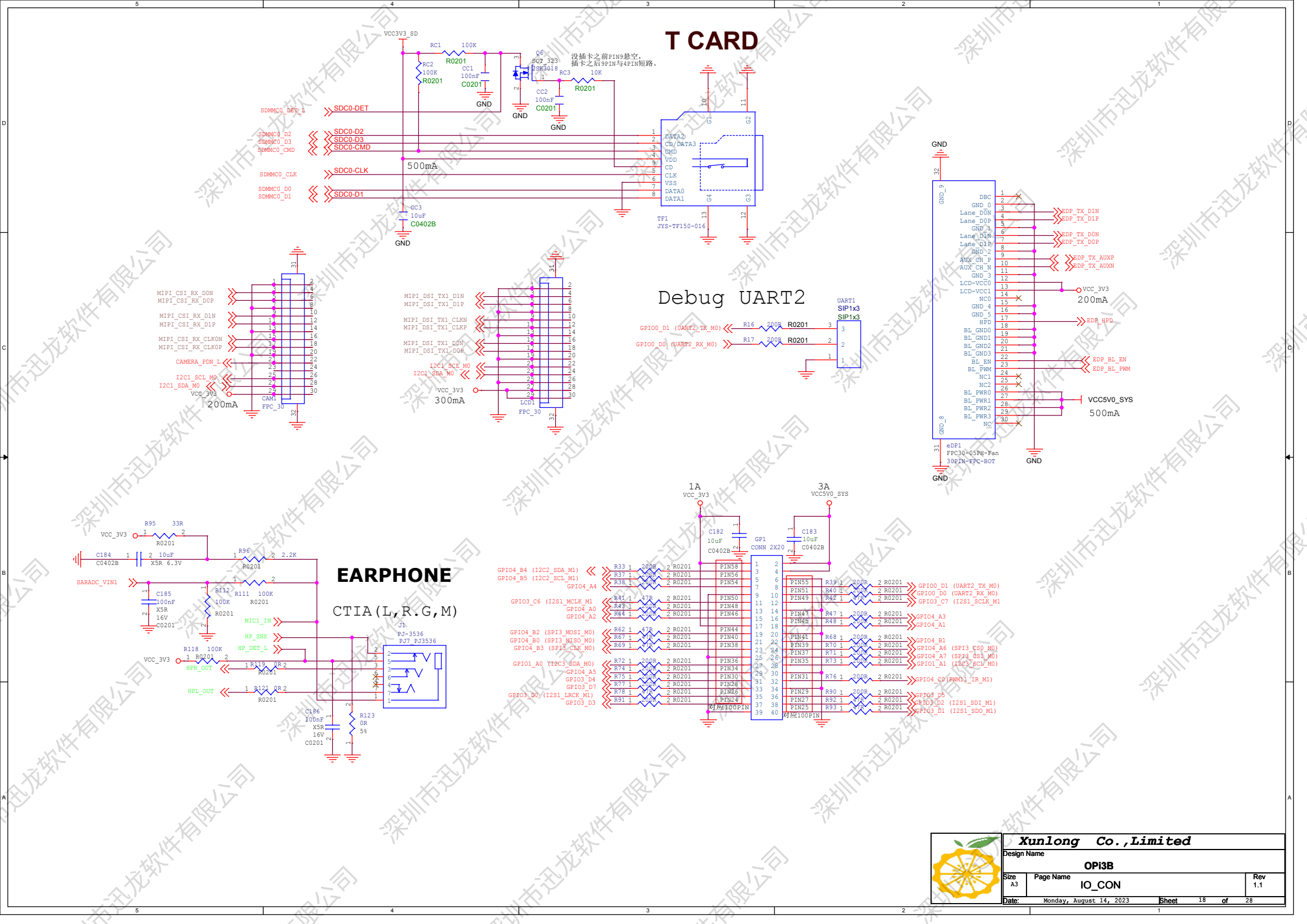
Date: Monday, August 14, 2023 | Sheet 16 of 28

RK3566_H(VCCIO1 Domain)



软件dts的电压配置严格与硬件设计保持一致！
Check the software configuration(dts)
of voltage level, which must be
keep the same as hardware design

Xunlong Co.,Limited		
Design Name: OPi3B		
Size: A4	Page Name: 17RK3566_Audio_Interface	Rev: 1.0
Date: Monday, August 14, 2023	Sheet 17 of 28	


T CARD
VCC3V3_SD
RC1 100K
R0201
RC2 100K
R0201
CC1 100nF
C0201
GND
Q6 SOT_323 2SK3018
没插卡之前PIN9悬空，
插卡之后9PIN与4PIN短路。
RC3 10K
R0201
CC2 100nF
C0201
SDMMC0_DET_L
SDC0-DET
SDMMC0_D2
SDMMC0_D3
SDMMC0_CMD
SDC0-D2
SDC0-D3
SDC0-CMD
SDMMC0_CLK
SDC0-CLK
SDMMC0_D0
SDMMC0_D1
SDC0-D1
500mA
CC3 10uF
C0402B
TF1
JYS-TF150-016
DATA2
CD/DATA3
CMD
VDD
CD
CLK
VSS
DATA0
DATA1
MIPI_CSI_RX_D0N
MIPI_CSI_RX_D0P
MIPI_CSI_RX_D1N
MIPI_CSI_RX_D1P
MIPI_CSI_RX_CLK0N
MIPI_CSI_RX_CLK0P
CAMERA_PDN_L
I2C1_SCL_M0
I2C1_SDA_M0
VCC_3V3
200mA
CAM1
FPC_30
MIPI_DSI_TX1_D1N
MIPI_DSI_TX1_D1P
MIPI_DSI_TX1_CLKN
MIPI_DSI_TX1_CLKP
MIPI_DSI_TX1_D0N
MIPI_DSI_TX1_D0P
I2C1_SCL_M0
I2C1_SDA_M0
VCC_3V3
300mA
LCD1
FPC_30
Debug UART2
GPIO0_D1 (UART2_TX_M0)
GPIO0_D0 (UART2_RX_M0)
R16 200R R0201
R17 200R R0201
UART1
SIP1x3
SIP1x3
GND
DBC
GND_0
Lane_D0N
Lane_D0P
GND_1
Lane_D1N
Lane_D1P
GND_2
AUX_CH_P
AUX_CH_N
GND_3
LCD-VCC0
LCD-VCC1
NC0
GND_4
GND_5
HPD
BL_GND0
BL_GND1
BL_GND2
BL_GND3
BL_EN
BL_PWM
NC1
NC2
BL_PWR0
BL_PWR1
BL_PWR2
BL_PWR3
NC
eDP_TX_D1N
eDP_TX_D1P
eDP_TX_D0N
eDP_TX_D0P
eDP_TX_AUXP
eDP_TX_AUXN
VCC_3V3
200mA
eDP_HPD
eDP_BL_EN
eDP_BL_PWM
VCC5V0_SYS
500mA
eDP1
FPC30-05PH-Fan
30PIN-FPC-BOT
EARPHONE
CTIA(L,R.G,M)
R95 33R
R0201
C184 10uF
C0402B
X5R 6.3V
R96 2.2K
R0201
SARADC_VIN1
C185 100nF
X5R 16V
C0201
R112 100K
R0201
R111 100K
R0201
MIC1_IN
HP_SNS
HP_DET_L
R118 100K
R0201
HPR_OUT
R119 0R
R0201
HPL_OUT
R121 0R
R0201
J1
PJ-3536
PJ7_PJ3536
C186 100nF
X5R 16V
C0201
R123 0R 5%
1A
3A
C182 10uF
C0402B
C183 10uF
C0402B
GP1
CONN 2X20
XJ双100PIN
GPIO4_B4 (I2C2_SDA_M1)
GPIO4_B5 (I2C2_SCL_M1)
GPIO4_A4
GPIO3_C6 (I2S1_MCLK_M1)
GPIO4_A0
GPIO4_A2
GPIO4_B2 (SPI3_MOSI_M0)
GPIO4_B0 (SPI3_MISO_M0)
GPIO4_B3 (SPI3_CLK_M0)
GPIO1_A0 (I2C3_SDA_M0)
GPIO4_A5
GPIO3_D4
GPIO3_D7
GPIO3_D0 (I2S1_LRCK_M1)
GPIO3_D3
GPIO0_D1 (UART2_TX_M0)
GPIO0_D0 (UART2_RX_M0)
GPIO3_C7 (I2S1_SCLK_M1)
GPIO4_A3
GPIO4_A1
GPIO4_B1
GPIO4_A6 (SPI3_CS0_M0)
GPIO4_A7 (SPI3_CS1_M0)
GPIO1_A1 (I2C3_SCL_M0)
GPIO4_C0(PWM11_IR_M1)
GPIO3_D5
GPIO3_D2 (I2S1_SDI_M1)
GPIO3_D1 (I2S1_SDO_M1)
Xunlong Co.,Limited
Design Name
OPi3B
Size A3
Page Name
IO_CON
Rev 1.1
Date: Monday, August 14, 2023
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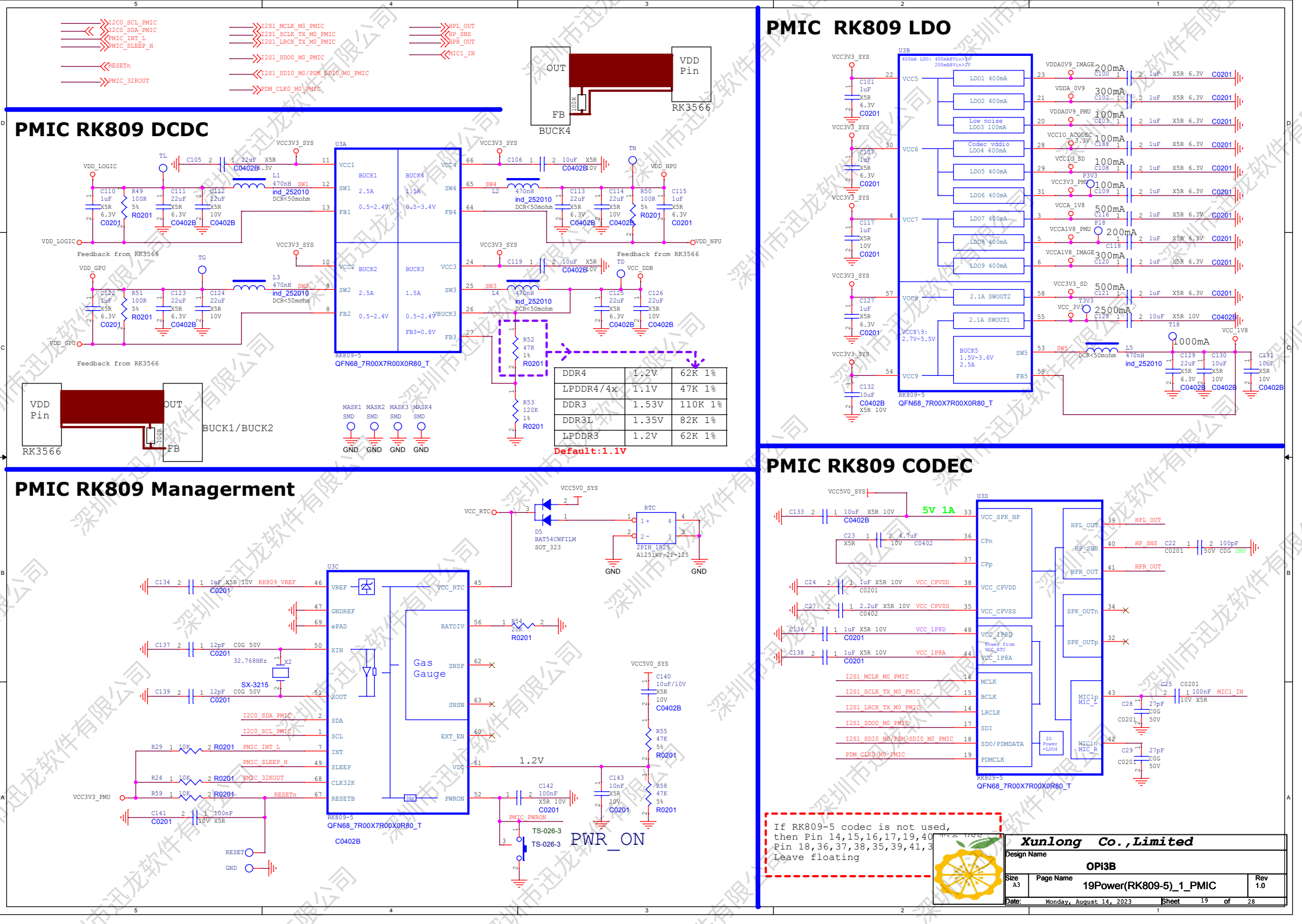
I2C0_SCL_PMIC
I2C0_SDA_PMIC
PMIC_INT_L
PMIC_SLEEP_H
RESETn
PMIC_32KOUT
I2S1_MCLK_M0_PMIC
I2S1_SCLK_TX_M0_PMIC
I2S1_LRCK_TX_M0_PMIC
I2S1_SDO0_M0_PMIC
I2S1_SDI0_M0/PDM_SDI0_M0_PMIC
PDM_CLK0_M0_PMIC
HPL_OUT
HP_SNS
HPR_OUT
MIC1_IN
OUT
FB
100R
VDD Pin
RK3566
BUCK4
PMIC RK809 DCDC
VDD_LOGIC
VDD_GPU
VDD_NPU
VCC_DDR
VCC3V3_SYS
U3A
RK809-5
QFN68_7R00X7R00X0R80_T
Feedback from RK3566
BUCK1
BUCK2
BUCK3
BUCK4
2.5A
1.5A
0.5-2.4V
0.5-3.4V
FB3=0.8V
ind_252010
DCR<50mohm
MASK1 MASK2 MASK3 MASK4
GND
DDR4 1.2V 62K 1%
LPDDR4/4x 1.1V 47K 1%
DDR3 1.53V 110K 1%
DDR3L 1.35V 82K 1%
LPDDR3 1.2V 62K 1%
Default:1.1V
PMIC RK809 LDO
U3B
400mA LDO: 400mA@Vin>3V
200mA@Vin>2V
LDO1 400mA
LDO2 400mA
Low noise LDO3 100mA
Codec vddio LDO4 400mA
LDO5 400mA
LDO6 400mA
LDO7 400mA
LDO8 400mA
LDO9 400mA
2.1A SWOUT2
2.1A SWOUT1
BUCK5 1.5V-3.6V 2.5A
VDDA0V9_IMAGE 200mA
VDDA_0V9 300mA
VDDA0V9_PMU 100mA
VCCIO_ACODEC 100mA
VCCIO_SD 100mA
VCC3V3_PMU 100mA
VCCA_1V8 500mA
VCCA1V8_PMU 200mA
VCCA1V8_IMAGE 300mA
VCC3V3_SD 500mA
VCC_3V3 2500mA
VCC_1V8 1000mA
PMIC RK809 Managerment
VCC5V0_SYS
VCC_RTC
RTC
D5
BAT54CWFILM
SOT_323
2PIN_1R25
A1251WF-2P-125
U3C
Gas Gauge
VREF
GNDREF
ePAD
XIN
XOUT
SDA
SCL
INT
SLEEP
CLK32K
RESETB
BATDIV
SNSP
SNSN
EXT_EN
VDC
PWRON
32.768HKz
SX-3215
RESETn
PMIC_INT_L
PMIC_SLEEP_H
PMIC_32KOUT
I2C0_SDA_PMIC
I2C0_SCL_PMIC
1.2V
PMIC_PWRON
TS-026-3
PWR_ON
PMIC RK809 CODEC
U3D
5V 1A
VCC_SPK_HP
CPn
CPp
VCC_CPVDD
VCC_CPVSS
VCC_1P8D
VCC_1P8A
MCLK
BCLK
LRCLK
SDI
SDO/PDMDATA
PDMCLK
HPL_OUT
HP_SNS
HPR_OUT
SPK_OUTn
SPK_OUTp
MIC1p MIC_L
MIC1n MIC_R
If RK809-5 codec is not used,
then Pin 14,15,16,17,19,40 ...
Pin 18,36,37,38,35,39,41,3...
Leave floating
Xunlong Co.,Limited
Design Name
OPi3B
Page Name
19Power(RK809-5)_1_PMIC
Rev
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A3
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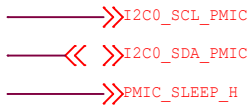
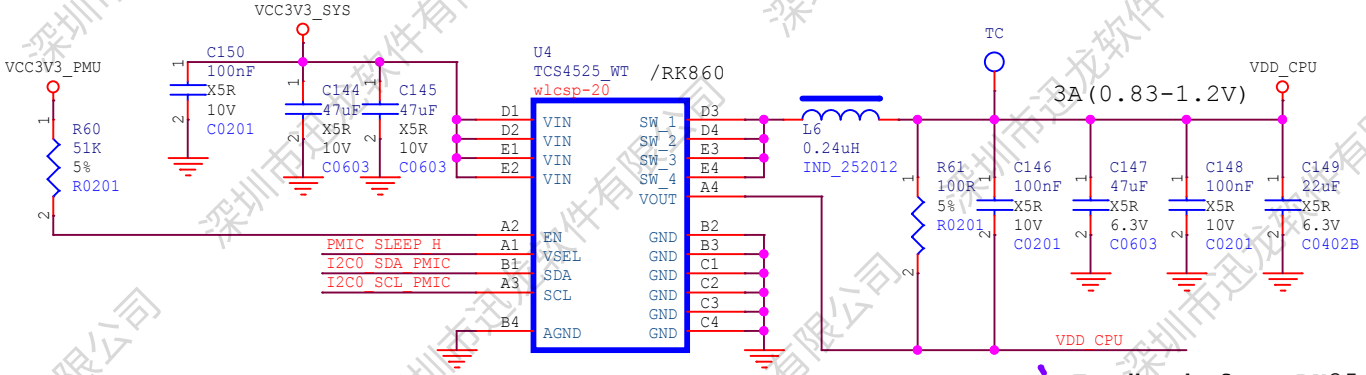
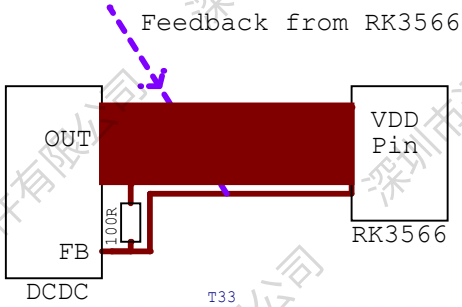
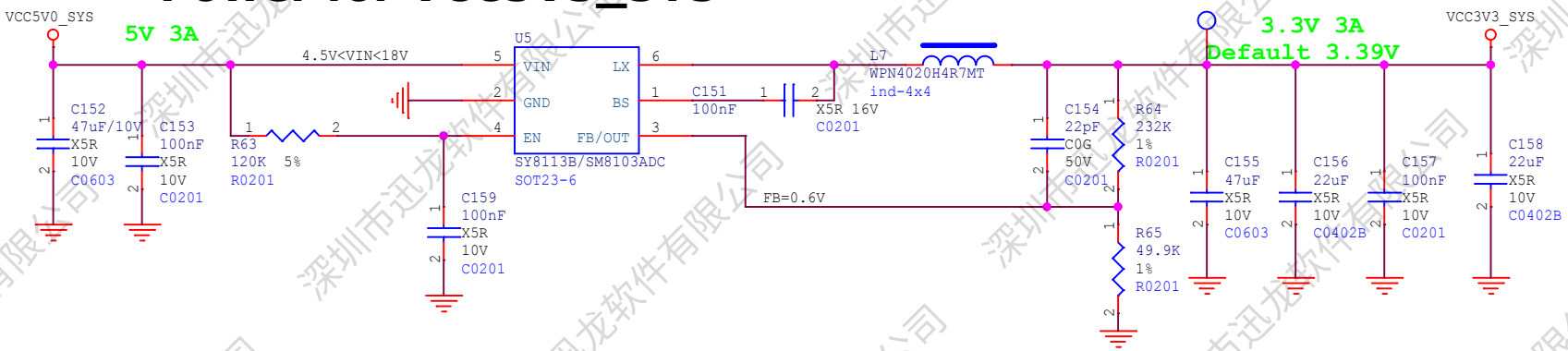


VDD_CPU_EXT





Power for VCC3V3_SYS



Xunlong Co.,Limited		
Design Name: OPi3B		
Size: A4	Page Name: 20Power(RK809-5)_2_Ext	Rev: 1.0
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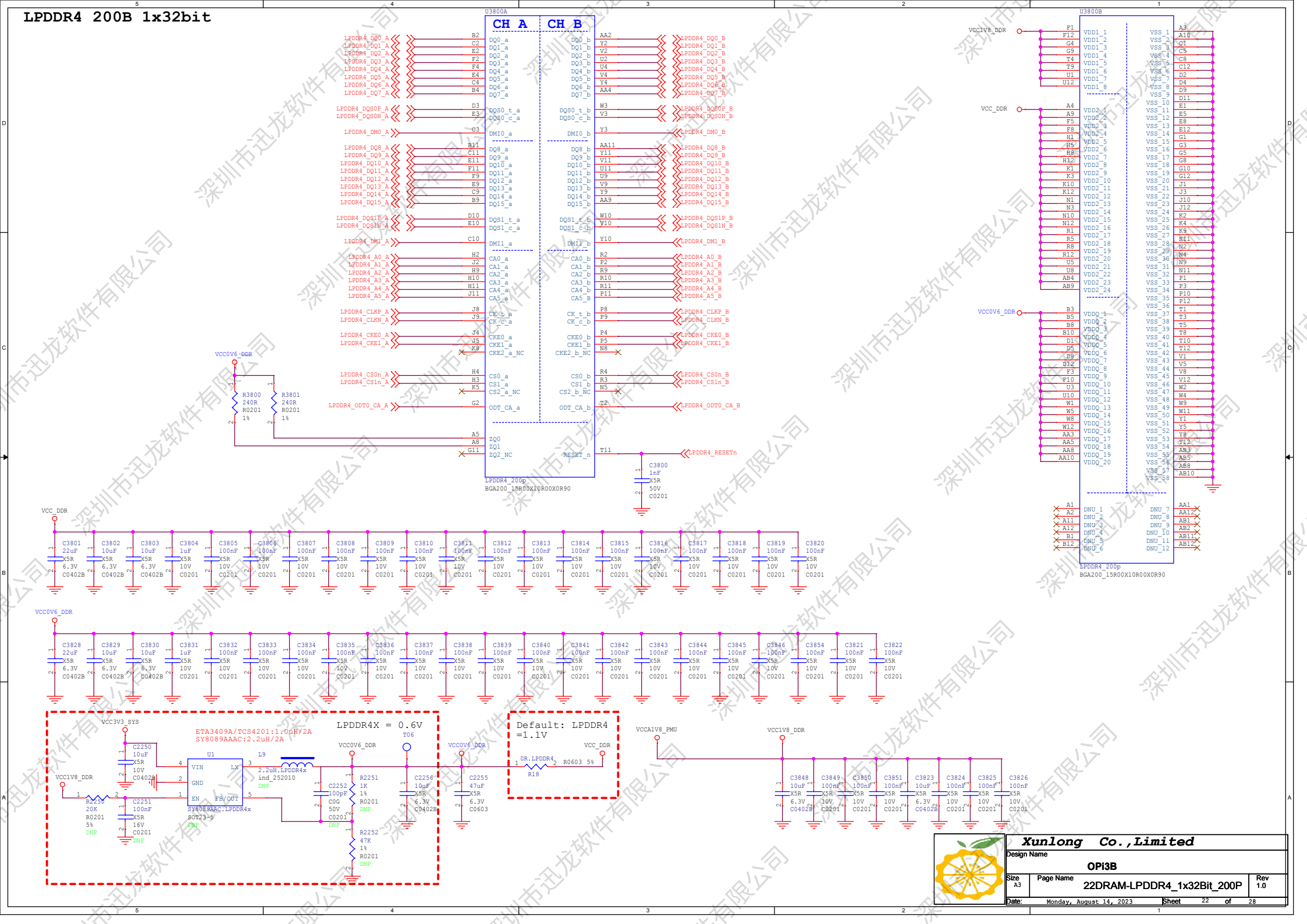
LPDDR4 200B 1x32bit



Xunlong Co.,Limited

Design Name: OPi3B

Size: A3 | Page Name: 22DRAM-LPDDR4_1x32Bit_200P | Rev: 1.0

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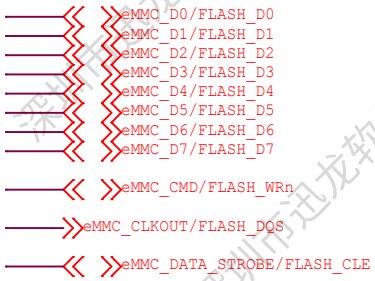
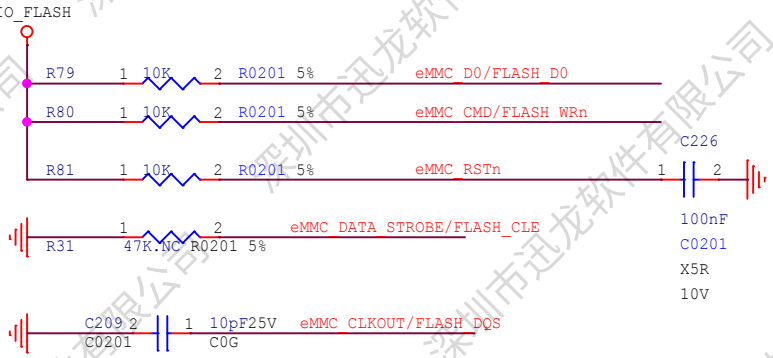
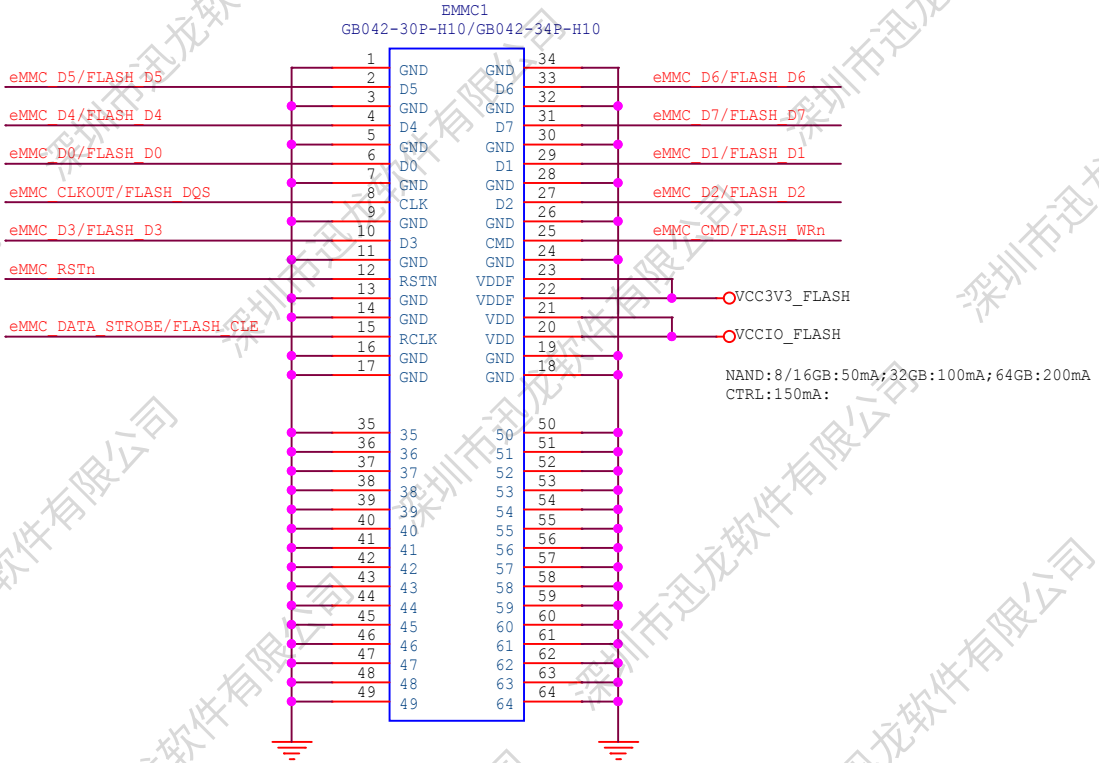
eMMC







Xunlong Co.,Limited		
Design Name: OPi3B		
Size: A4	Page Name: 23Flash-eMMC_Flash	Rev: 1.0
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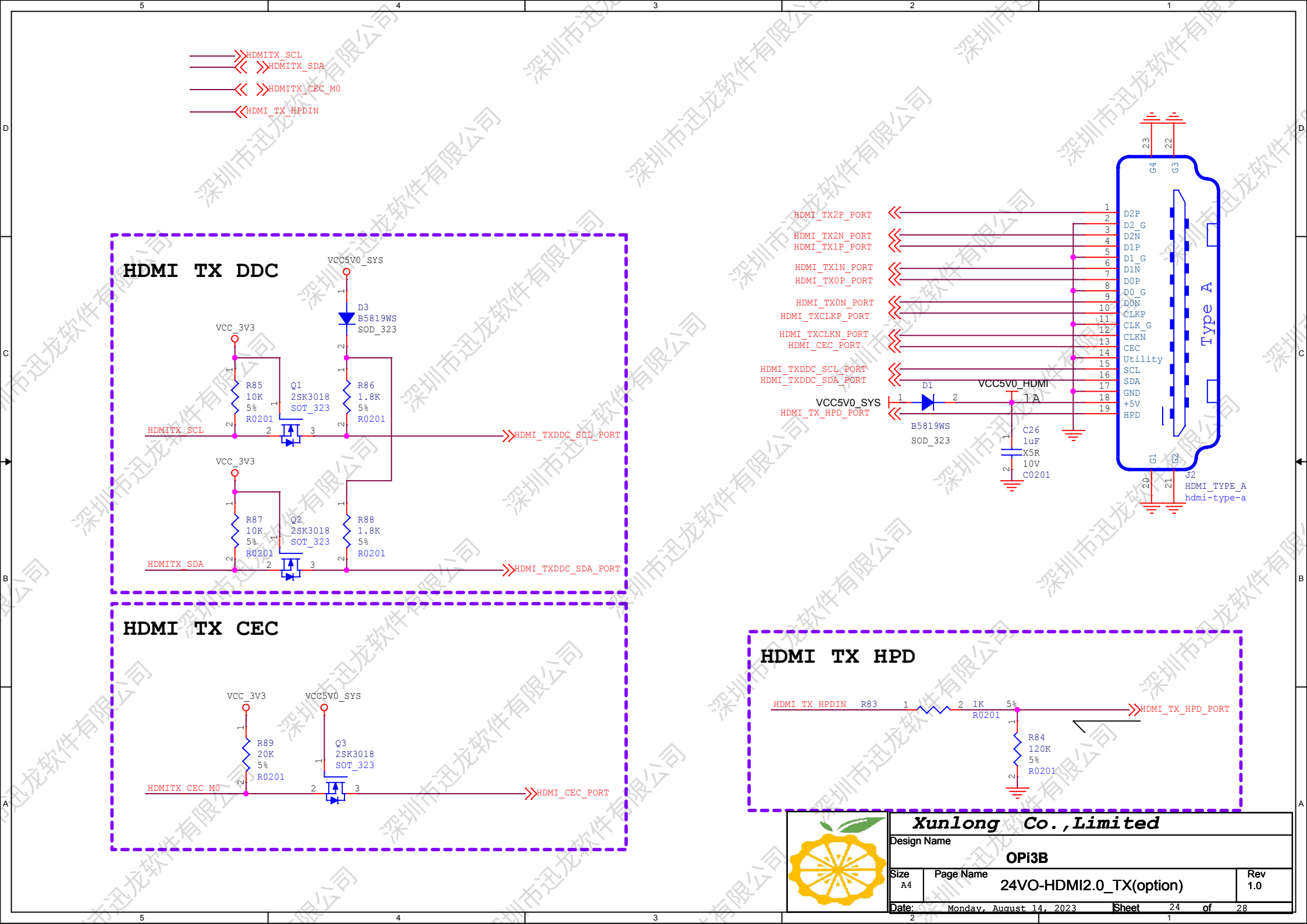
HDMITX_SCL
HDMITX_SDA
HDMITX_CEC_M0
HDMI_TX_HPDIN
HDMI TX DDC
VCC5V0_SYS
D3
B5819WS
SOD_323
VCC_3V3
R85
10K
5%
R0201
Q1
2SK3018
SOT_323
R86
1.8K
5%
R0201
HDMITX_SCL
HDMI_TXDDC_SCL_PORT
VCC_3V3
R87
10K
5%
R0201
Q2
2SK3018
SOT_323
R88
1.8K
5%
R0201
HDMITX_SDA
HDMI_TXDDC_SDA_PORT
HDMI TX CEC
VCC_3V3
VCC5V0_SYS
R89
20K
5%
R0201
Q3
2SK3018
SOT_323
HDMITX_CEC_M0
HDMI_CEC_PORT
HDMI_TX2P_PORT
HDMI_TX2N_PORT
HDMI_TX1P_PORT
HDMI_TX1N_PORT
HDMI_TX0P_PORT
HDMI_TX0N_PORT
HDMI_TXCLKP_PORT
HDMI_TXCLKN_PORT
HDMI_CEC_PORT
HDMI_TXDDC_SCL_PORT
HDMI_TXDDC_SDA_PORT
VCC5V0_SYS
HDMI_TX_HPD_PORT
D1
B5819WS
SOD_323
VCC5V0_HDMI
1 A
C26
1uF
X5R
10V
C0201
D2P
D2_G
D2N
D1P
D1_G
D1N
D0P
D0_G
D0N
CLKP
CLK_G
CLKN
CEC
Utility
SCL
SDA
GND
+5V
HPD
Type A
J2
HDMI_TYPE_A
hdmi-type-a
HDMI TX HPD
HDMI_TX_HPDIN
R83
1K
5%
R0201
HDMI_TX_HPD_PORT
R84
120K
5%
R0201
Xunlong Co.,Limited
Design Name
OPi3B
Size
A4
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24VO-HDMI2.0_TX(option)
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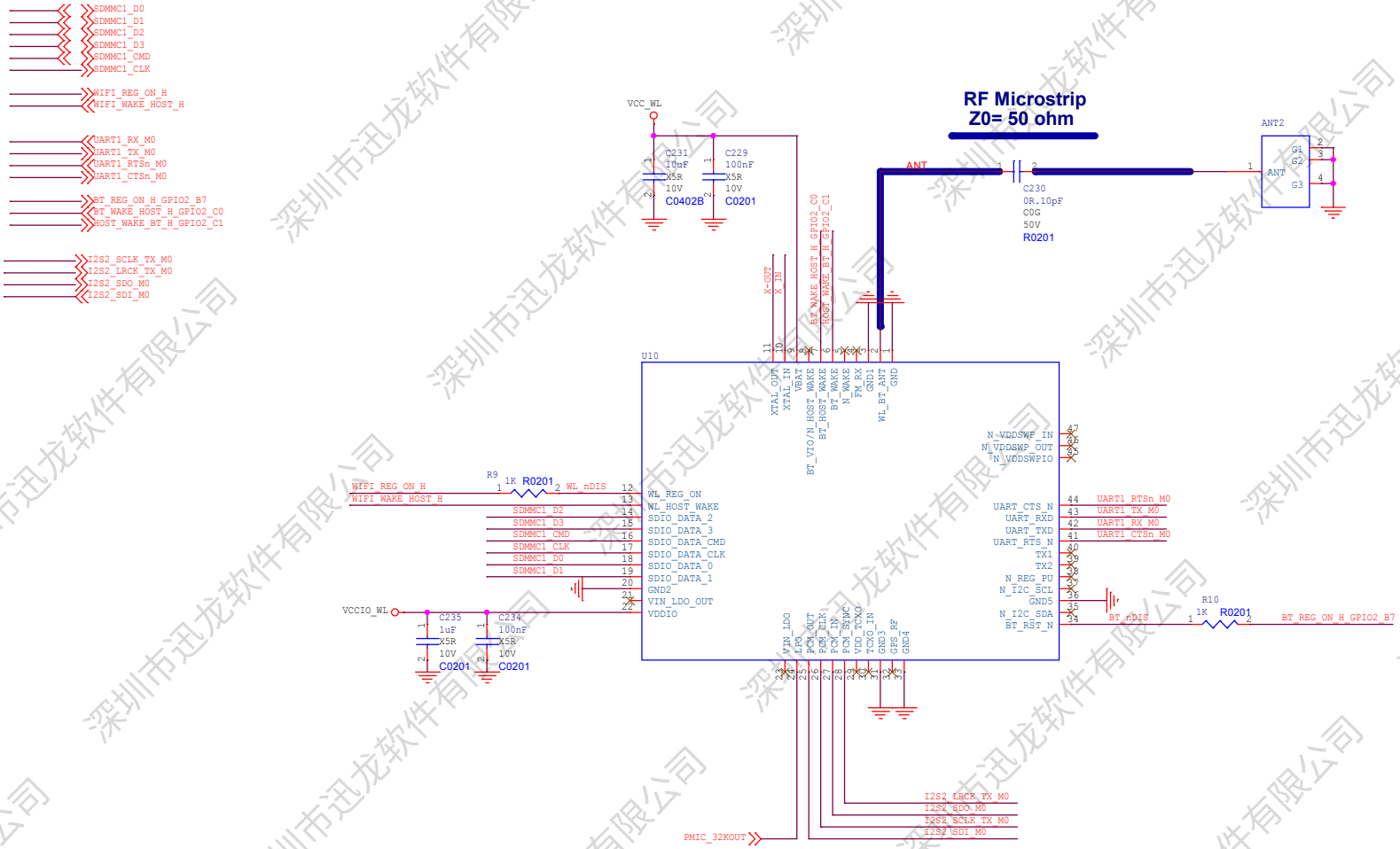
SDIO WIFI/BT Module-1T1R



Xunlong Co.,Limited		
Design Name	OPi3B	
Size A3	Page Name 25WIFI/BT-SDIO_1T1R+UART	Rev 1.0
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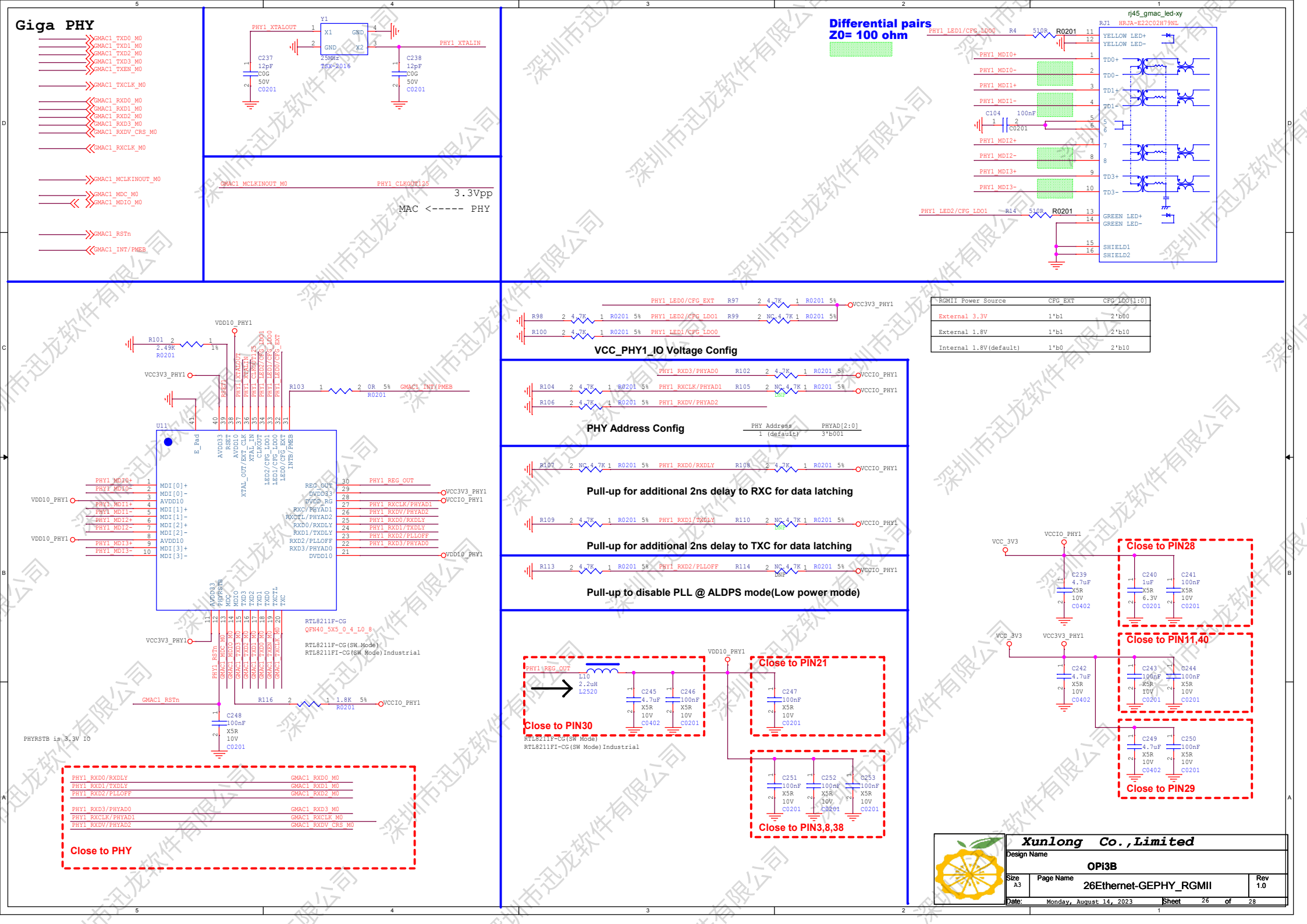
Giga PHY
GMAC1_TXD0_M0
GMAC1_TXD1_M0
GMAC1_TXD2_M0
GMAC1_TXD3_M0
GMAC1_TXEN_M0
GMAC1_TXCLK_M0
GMAC1_RXD0_M0
GMAC1_RXD1_M0
GMAC1_RXD2_M0
GMAC1_RXD3_M0
GMAC1_RXDV_CRS_M0
GMAC1_RXCLK_M0
GMAC1_MCLKINOUT_M0
GMAC1_MDC_M0
GMAC1_MDIO_M0
GMAC1_RSTn
GMAC1_INT/PMEB
PHY1_XTALOUT
PHY1_XTALIN
Y1
25MHz
TSX-2016
C237
12pF
C0G
50V
C0201
C238
12pF
C0G
50V
C0201
GMAC1_MCLKINOUT_M0
PHY1_CLKOUT125
3.3Vpp
MAC <----- PHY
Differential pairs
Z0= 100 ohm
rj45_gmac_led-xy
RJ1 HRJA-E22C02H79NL
PHY1_LED1/CFG_LDO0
R4
510R
R0201
YELLOW LED+
YELLOW LED-
PHY1_MDI0+
PHY1_MDI0-
PHY1_MDI1+
PHY1_MDI1-
C104
100nF
C0201
PHY1_MDI2+
PHY1_MDI2-
PHY1_MDI3+
PHY1_MDI3-
TD0+
TD0-
TD1+
TD1-
TD3+
TD3-
PHY1_LED2/CFG_LDO1
R14
510R
R0201
GREEN LED+
GREEN LED-
SHIELD1
SHIELD2
VDD10_PHY1
R101
2.49K
R0201
VCC3V3_PHY1
R103
0R
R0201
GMAC1_INT/PMEB
U11
E_Pad
MDI[0]+
MDI[0]-
MDI[1]+
MDI[1]-
MDI[2]+
MDI[2]-
MDI[3]+
MDI[3]-
AVDD10
AVDD33
DVDD33
DVDD_RG
DVDD10
REG_OUT
RXC/PHYAD1
RXCTL/PHYAD2
RXD0/RXDLY
RXD1/TXDLY
RXD2/PLLOFF
RXD3/PHYAD0
PHY1_REG_OUT
PHY1_RXCLK/PHYAD1
PHY1_RXDV/PHYAD2
PHY1_RXD0/RXDLY
PHY1_RXD1/TXDLY
PHY1_RXD2/PLLOFF
PHY1_RXD3/PHYAD0
RTL8211F-CG
QFN40_5X5_0_4_L0_8
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
PHYRSTB is 3.3V IO
C248
100nF
X5R
10V
C0201
R116
1.8K
R0201
VCCIO_PHY1
PHY1_RXD0/RXDLY
PHY1_RXD1/TXDLY
PHY1_RXD2/PLLOFF
PHY1_RXD3/PHYAD0
PHY1_RXCLK/PHYAD1
PHY1_RXDV/PHYAD2
GMAC1_RXD0_M0
GMAC1_RXD1_M0
GMAC1_RXD2_M0
GMAC1_RXD3_M0
GMAC1_RXCLK_M0
GMAC1_RXDV_CRS_M0
Close to PHY
PHY1_LED0/CFG_EXT
R97
R98
PHY1_LED2/CFG_LDO1
R99
R100
PHY1_LED1/CFG_LDO0
VCC_PHY1_IO Voltage Config
RGMII Power Source
CFG_EXT
CFG_LDO[1:0]
External 3.3V
1'b1
2'b00
External 1.8V
1'b1
2'b10
Internal 1.8V(default)
1'b0
2'b10
PHY1_RXD3/PHYAD0
R102
R104
PHY1_RXCLK/PHYAD1
R105
R106
PHY1_RXDV/PHYAD2
VCCIO_PHY1
PHY Address Config
PHY Address
PHYAD[2:0]
1 (default)
3'b001
R107
PHY1_RXD0/RXDLY
R108
Pull-up for additional 2ns delay to RXC for data latching
R109
PHY1_RXD1/TXDLY
R110
Pull-up for additional 2ns delay to TXC for data latching
R113
PHY1_RXD2/PLLOFF
R114
Pull-up to disable PLL @ ALDPS mode(Low power mode)
PHY1_REG_OUT
L10
2.2uH
L2520
C245
4.7uF
X5R
10V
C0402
C246
100nF
X5R
10V
C0201
Close to PIN30
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
VDD10_PHY1
C247
100nF
X5R
10V
C0201
Close to PIN21
C251
100nF
X5R
10V
C0201
C252
100nF
X5R
10V
C0201
C253
100nF
X5R
10V
C0201
Close to PIN3,8,38
VCC_3V3
VCCIO_PHY1
C239
4.7uF
X5R
10V
C0402
C240
1uF
X5R
6.3V
C0201
C241
100nF
X5R
10V
C0201
Close to PIN28
VCC_3V3
VCC3V3_PHY1
C242
4.7uF
X5R
10V
C0402
C243
100nF
X5R
10V
C0201
C244
100nF
X5R
10V
C0201
Close to PIN11,40
C249
4.7uF
X5R
10V
C0402
C250
100nF
X5R
10V
C0201
Close to PIN29
Xunlong Co.,Limited
Design Name
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A3
Page Name
26Ethernet-GEPHY_RGMII
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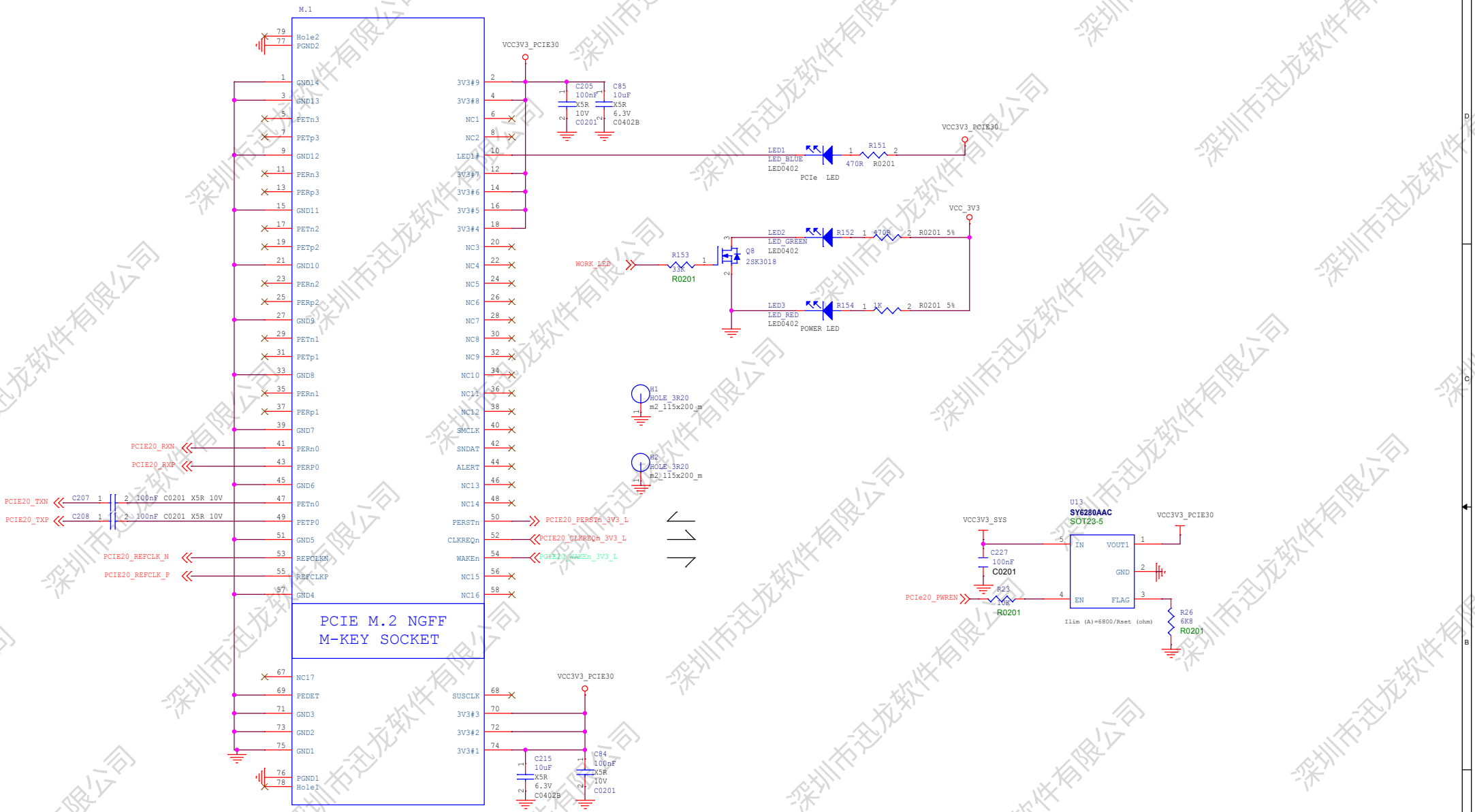

Xunlong Co.,Limited		
Design Name	OPi3B	
Size A3	Page Name 27.M.2 M key PCIe/LED	Rev 1.0
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