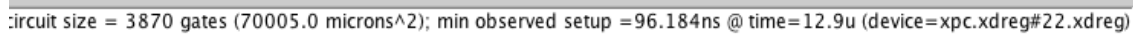


## ECPE 173 – Spring 2013

### Lab Project 6

In this lab project, we will fix any existing errors with Lab Project 5 and optimize our Beta.

1. Start a new Word document report for this project. Create appropriate document headings and write a short Problem section describing the goals of this lab (in your own words – not mine!).
2. Create a new folder for this lab and copy your lab project 5 files there. Do not overwrite the original lab project 5.
3. In your Word document, create a “Current Design” section and describe the current state of your Beta (working or not). From the gate level compilation, determine the size and speed of your design (see Figure 1). Include this information in this section.



circuit size = 3870 gates (70005.0 microns^2); min observed setup = 96.184ns @ time=12.9u (device=xpc.xdreg#22.xdreg)

Figure 1: Example of Size and Speed data

4. If your design still does not work, fix it. Create a “Functional Design” section and explain how you fixed the design.
5. Once your design works, optimize it. Clean up the code and modify the logic to reduce the size and speed up the system. Create an “Optimization” section and document all your modifications. For each reasonable modification (use your judgment on reasonable), document the size and speed.
6. Create a “Future Work” section and outline any additional changes you would make to your design.
7. Submit via Sakai.