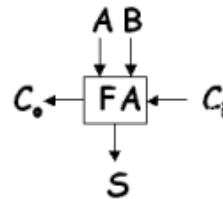


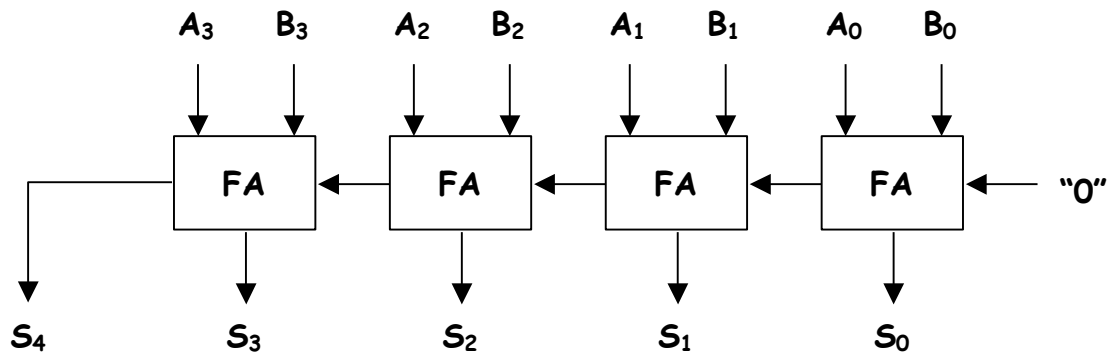
$$S = A \oplus B \oplus C_{in} \quad C_o = A \cdot B + A \cdot C_{in} + B \cdot C_{in}$$

$C_i$	A	B	S	$C_o$
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



Typically S is implemented using two cascaded 2-input XOR gates. One can use three 2-input NANDs and one 3-input NAND to implement  $C_o$  (remember that by Demorgan's Law two cascaded NANDs is logically equivalent to a cascade of AND/OR).

The module performs the addition of two one-bit inputs (A and B) incorporating the carry in from the previous stage ( $C_i$ ). The result appears on the S output and a carry ( $C_o$ ) is generated for the next stage. A possible schematic for the 4-bit adder is shown below:



## 2: XOR/XNOR Gates

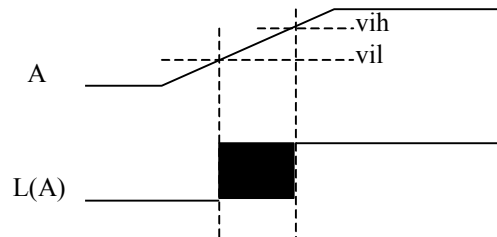
Since we're using individual gates to implement the logic, a good place to start is to build your own gate library (e.g., inverter, 2-input NAND, 2-input NOR, 2-input XOR), test them individually, and then use them to implement your design. It's much easier to debug your circuit module-by-module rather than as one big lump. XOR/XNOR can be challenging gates to design; here's one suggestion for how they might be implemented:

## 4: Plotting Results

Interpreting analog signal levels as logic values can be tedious. JSim will do it for you automatically if you ask to plot “L(a)” instead of just “a”. The logic-high and logic-thresholds are determined by the “vih” and “vil” options:

```
.options vih=2.6 vil=0.6
```

Initial values are specified in “/mit/6.004/jsim/nominal.jsim”, but you can respecify them in your own netlist. Voltages between vil and vih are displayed as a filled-in rectangle to indicate that the logic value cannot be determined. For example:



You can also ask for the values of a set of signals to be displayed as a bus, e.g., “L(a3,a2,a1,a0)”. The signals should be listed most-significant bit first. A bus waveform is displayed as a filled-rectangle if any of the component signals has an invalid logic level or as a hexadecimal value otherwise. In the following plot the four signals a3, a2, a1 and a0 are interpreted as a 4-bit integer where the high-order bit (a3) is making a 1→0 transition. The filled-in rectangle represents the period of time during which a3 transitions from  $V_{IH}$  to  $V_{IL}$ .

L(a3,a2,a1,a0)	0xF		0x7
----------------	-----	--	-----

## 5: Design Guidelines

Here’s a list of design tasks you might use to organize your approach to the lab:

1. Draw a gate-level schematic for the full-adder module. XOR gates can be used to implement the S output; two levels of NAND gates are handy for implementing  $C_o$  as a sum of products.
2. Create a MOSFET circuit for each of the logic gates you used in step 1.
3. Enter .subckt definitions in your netlist for each of the logic gates. Use Jsim to test each logic gate with all possible combinations of inputs. Debugging your gate designs one-by-one will be much easier than trying to debug them as part of the adder circuit. Here’s a sample netlist for testing a 2-input NAND gate called nand2:

```
.include "/mit/6.004/jsim/nominal.jsim"  
.include "/mit/6.004/jsim/8clocks.jsim"
```

```
.subckt nand2 a b z
... internals of nand2 circuit here
.ends
Xtest clk1 clk2 z nand2
.tran 20ns
.plot clk1
.plot clk2
.plot z
```

4. Enter a .subckt definition for the full-adder, building it out of the gates you designed and tested above. Use Jsim to test your design with all 8 possible combinations of the three inputs. At this point you probably want to switch to using “Fast Transient Analysis” do to the simulations as it is much faster than “Device-level Simulation”.
5. Enter the netlist for the 4-bit adder and test the circuit using input waveforms supplied by lab2checkoff.jsim. Note that the checkoff circuitry expects your 4-bit adder to have exactly the terminals shown below – the inside circuitry is up to you, but the “.subckt ADDER4...” line in your netlist should match exactly the one shown below.

```
.include "/mit/6.004/jsim/nominal.jsim"
.include "/mit/6.004/jsim/lab2checkoff.jsim"

... subckt definitions of your logic gates

.subckt FA a b ci s co
... full-adder internals here
.ends

.subckt ADDER4 a3 a2 a1 a0 b3 b2 b1 b0 s4 s3 s2 s1 s0
* remember the node named "0" is the ground node
* nodes c0 through c3 are internal to the ADDER module
Xbit0 a0 b0 0 s0 c0 FA
Xbit1 a1 b1 c0 s1 c1 FA
Xbit2 a2 b2 c1 s2 c2 FA
Xbit3 a3 b3 c2 s3 s4 FA
.ends
```

lab2checkoff.jsim contains the necessary circuitry to generate the appropriate input waveforms to test your adder. It includes a .tran statement to run the simulation for the appropriate length of time and a few .plot statements showing the input and output waveforms for your circuit.

When debugging your circuits, you can plot additional waveforms by adding .plot statements to the end of your netlist. For example, to plot the carry-out signal from the first full adder, you could say

```
.plot Xtest.c0
```

where Xtest is the name lab2checkoff.jsim gave to the ADDER4 device it created and c0 is the name of the internal node that connects the carry-out of the low-order FA to the carry-in of the next FA.