ECPE 174 – Lab 8: Verilog

I. Objectives

Design a system using the Verilog HDL. Understand the basic syntax and structure along with the similarities and differences of using Verilog compared to VHDL.

II. Problem Statement

When designing complex digital circuits, whether for ASIC or FPGA development, two hardware description languages exist: VHDL and Verilog. Basic use and functionality are the same, but differences do exist and knowledge of both provides greater flexibility in digital design.

We will utilize a past lab to introduce Verilog and understand the differences between VDHL and Verilog.

Choose between any of the following past lab problems: Lab 1 (car taillights), Lab 3 (combination lock), Lab 4 (vending machine), or Lab 6/7 (the complete ALU).

III. Pre-Lab

Complete the following steps before lab and turn in by 2pm:

1. Having picked a lab, provide the lab problem description and your VHDL code.
2. Ensure the VHDL has at least one COMPONENT description (whether that is the masterclk, synchronizer logic, or datapath units). If code changes were required, state them and only include the final VHDL code.
3. Record the fitter summary, timing summary, Quartus-generated state diagram, and high-level RTL.
4. Design a Verilog solution to the same problem.
5. Simulate the solution (which will require removing any clock divide or modifying the divide value to not divide). Ensure the design works and provide both the functional waveform and final Verilog.
6. For the Verilog design, record the fitter summary, timing summary, Quartus-generated state diagram, and high-level RTL.

Submit electronically via Sakai by 2pm.

IV. In-Lab

Complete the following steps in lab:

1. Implement your Verilog design on the Cyclone 2.
2. Demonstrate for check-off.

V. Post-Lab

Discuss the following in your lab report:

- What, if any, differences do you see between the VHDL and Verilog designs based on the Quartus generated information? Explain these differences (or lack of them).
- What do you see as the advantages and disadvantages between VHDL and Verilog? Which do you prefer? Why?