Elizabeth Basha
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Lab Practical Objectives

Overview

ECPE 174 focuses on the practical engineering aspects of advanced digital design, preparing students to work on large-scale digital projects in industry and academic settings. Given this focus, the lab practical provides an ideal metric of a student's ability to use the design tools focused on in the class. This report provides an outline of the format of the practical, the topics covered by the practical, grading, and a summary of the specific objectives the exam covers.

Practical Format

The lab practical occurs on Tuesday, October 11 in Chambers 115 from 2-5pm. Students have the entire lab period to work on the practical although the design of it will ensure that those students who know the material finish in 1.5 hours.

Each student works independently on a computer in the lab with a Cyclone 2 board. Students can utilize any books, notes, or prior work during the exam. As everyone will have their own Internet-accessible computer, students can also access online resources and their *u* drive. Students cannot talk to other students, use their mobile phone, or chat online with anyone. Additionally, students cannot view or listen to any material requiring headphones. Anyone incorrectly utilizing materials or providing any distractions will receive one warning. Any further violations will result in the end of the exam for that student and dismissal from the lab.

Practical Topics and Coverage

The lab practical emphasizes those skills utilized in lab. However, in testing those skills, the exam can require design topics discussed in class such as finite state machine design (Mealy and Moore) and synchronizing logic.

All labs to date have required the use of VHDL coding; the practical may do so as well. This could include utilizing clock divider logic as well as testbenches. The exam will provide any extra code although students should know how to include such code in their design.

Labs have focused on Quartus and Cyclone 2 boards. Understanding Quartus consists of four areas: simulation, implementation verification, analysis, and programming. For simulation, students should know how to create a waveform simulation file, how to test a reasonable number of input cases, how to examine internal signals for debugging purposes, how to perform both functional and timing simulation, and how to determine the simulation coverage according to Quartus.

Implementation verification requires understanding the range of tools Quartus provides to explore the synthesized design. This includes the Equation Summary (demonstrated in Figure 1a), State Machine Viewer (shown in Figure 1b), and the RTL viewer (shown in Figure 2). For the State Machine Viewer, students should know how to find the transition table and encoding.

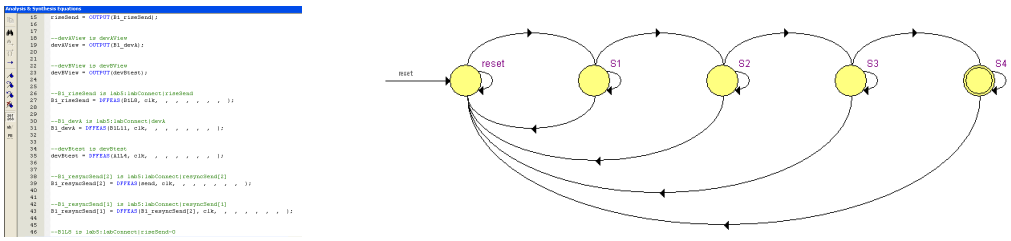

Figure 1: Output from (a) Equation Viewer and (b) State Machine Viewer.

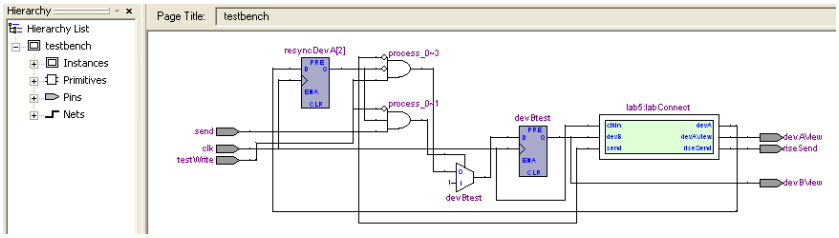

Figure 2: RTL Viewer Output.

Quartus also provides several analysis tools. Figures 3 and 4 show the two different tools we use regularly in lab: the Fitter Summary and Timing Summary, respectively. Students should know where to find this information.

Fitter Status	Successful - Sat Sep 18 01:10:29 2010
Quartus II Version	9.1 Build 304 01/25/2010 SP 1 SJ Web Edition
Revision Name	lab3
Top-level Entity Name	lab3
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Final
Total logic elements	24 / 18,752 (< 1 %)
Total combinational functions	15 / 18,752 (< 1 %)
Dedicated logic registers	20 / 18,752 (< 1 %)
Total registers	20
Total pins	5 / 315 (2 %)
Total virtual pins	0
Total memory bits	0 / 239,616 (0 %)
Embedded Multiplier 9-bit elements	0 / 52 (0 %)
Total PLLs	0 / 4 (0 %)

Figure 3: Fitter Summary.

Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time	From	To	From Clock	To Clock	Failed Paths
1	Worst-case tsu	N/A	None	3.508 ns	send	devBtest	--	clk	0
2	Worst-case tco	N/A	None	7.408 ns	lab5:labConnect|riseSend	riseSend	clk	--	0
3	Worst-case th	N/A	None	-2.828 ns	testWrite	devBtest	--	clk	0
4	Clock Setup: 'clk'	N/A	None	Restricted to 380.08 MHz (period = 2.631 ns)	lab5:labConnect|devBFF2	lab5:labConnect|devA	clk	clk	0
5	Total number of failed paths								0

Figure 4: Timing Summary.

Finally, students should know how to implement a design on the Cyclone 2 board. This entails pin assignment (requiring determining the correct pins for different on-board components), programming, and testing. Students should know the functionality of the different components including whether the component uses active high or active low logic. Students will not need to connect their board to any external hardware.

Grading

The lab practical counts as 10% of the course grade and will consist of 100 points. Each item will indicate its point value. Process counts so students may need to explain steps taken to achieve a goal. If any problems (such as the design does not work) or anomalies arise (for example, Quartus does not provide a state diagram or uses a large number of registers to implement the design), students should explain their steps to solve and to understand them. In these cases, we will only give partial credit if students document their debugging and thought processes.

Summary

This report outlined the structure, topics, and grading of the lab practical. Given its importance, we conclude by summarizing the objectives:

- Design VHDL code to solve a given problem
- Include code in higher level testbenches or add lower level components
- Simulate design with functional and timing simulation, providing a specified coverage level and testing the majority of input combinations
- View the synthesized design through equations, state machines, and RTL
- Analyze the timing and space requirements of the design
- Program a Cyclone board with the design and correctly implement design on board, using proper debugging skills