ECPE 174 – Lab 7
Timing, Placement, and Memory

I. Objectives

Design a memory system. Constrain timing. Explore placement. Resolve timing issues.

II. Problem Statement

In this lab, we will finalize our Lab 6 memory system design as described in the Lab 6 handout.

All output signals and input signals (except data in) must be viewable through seven-segment or LEDs.

III. Pre-Lab

Complete the following steps before lab and turn in by 2pm:

1. Determine how to connect to internal memory. Write a paragraph about the connection requirements. Draw a timing diagram of the memory read and write operations (specific to your problem constraints).
2. Draw a block diagram of your overall design, making sure to label all signals and their widths; you should modify your diagram from Lab 6 to reflect both the actual ALU design used and the memory system. Write several paragraphs outlining any design decisions and assumptions including justification. Indicate how you will input and output everything on the board.
3. Design the finite state machine necessary to control the system with memory. Draw a state diagram of the FSM.
4. If you did not get the system working in hardware already:
    a. Implement the finite state machine control in VHDL. Do not connect memory yet – just implement proper operation in talking to the memory.
    b. Simulate your code using the waveform editor and functional simulation. Ensure simulation covers 75% or greater of the test cases and use simulation to verify VHDL matches your state machine.
5. Read provided material on the placement editor.

Submit electronically via Sakai.

IV. In-Lab

Complete the following steps in lab:

1. Instantiate just the memory module on the Cyclone II. Connect inputs to toggle switches and outputs to LEDs. Demonstrate for check-off.
2. Instantiate complete system. Demonstrate for check-off.
3. Using the timing analyzer, constrain the clock frequency of the system to a reasonable value. Record the report results. If you receive any timing errors, modify your design to fix them. Record the updated report results and code modifications. Demonstrate for check-off.
4. Increase the clock frequency constraint until the design no longer functions (do not immediately jump to an impossible value but slowly skew the clock frequency range until it fails). Record all values tried and any warning/error messages received.

5. Using the placement editor, determine where the failing paths are in the system. Take a screenshot of one of the failing paths (include delay labels and anything indicating the path details).
6. Returning to your design, optimize your code.
7. Rerun the timing analyzer with the failing clock frequency. Record the report results. If you still receive timing errors, continue to modify your design to fix them. Record the updated report results and code modifications.
8. Once system works, demonstrate for check-off.

V. Post-Lab

Write one lab report for both Lab 6 and Lab 7. Describe your overall verification procedure over all three labs – this should be a thorough description and probably around 1-2 pages (not including figures and tables).

In addition to the Lab 6 post-lab questions, answer the following questions:

- Provide a table outlining your timing trials. Over what range of frequencies does your design work? Where did it fail the first time? What path(s) failed? Why do you think those paths failed?
- How did you optimize your design? What was your optimization process? Do you think your process was efficient? Why or why not? How would you change your process next time?