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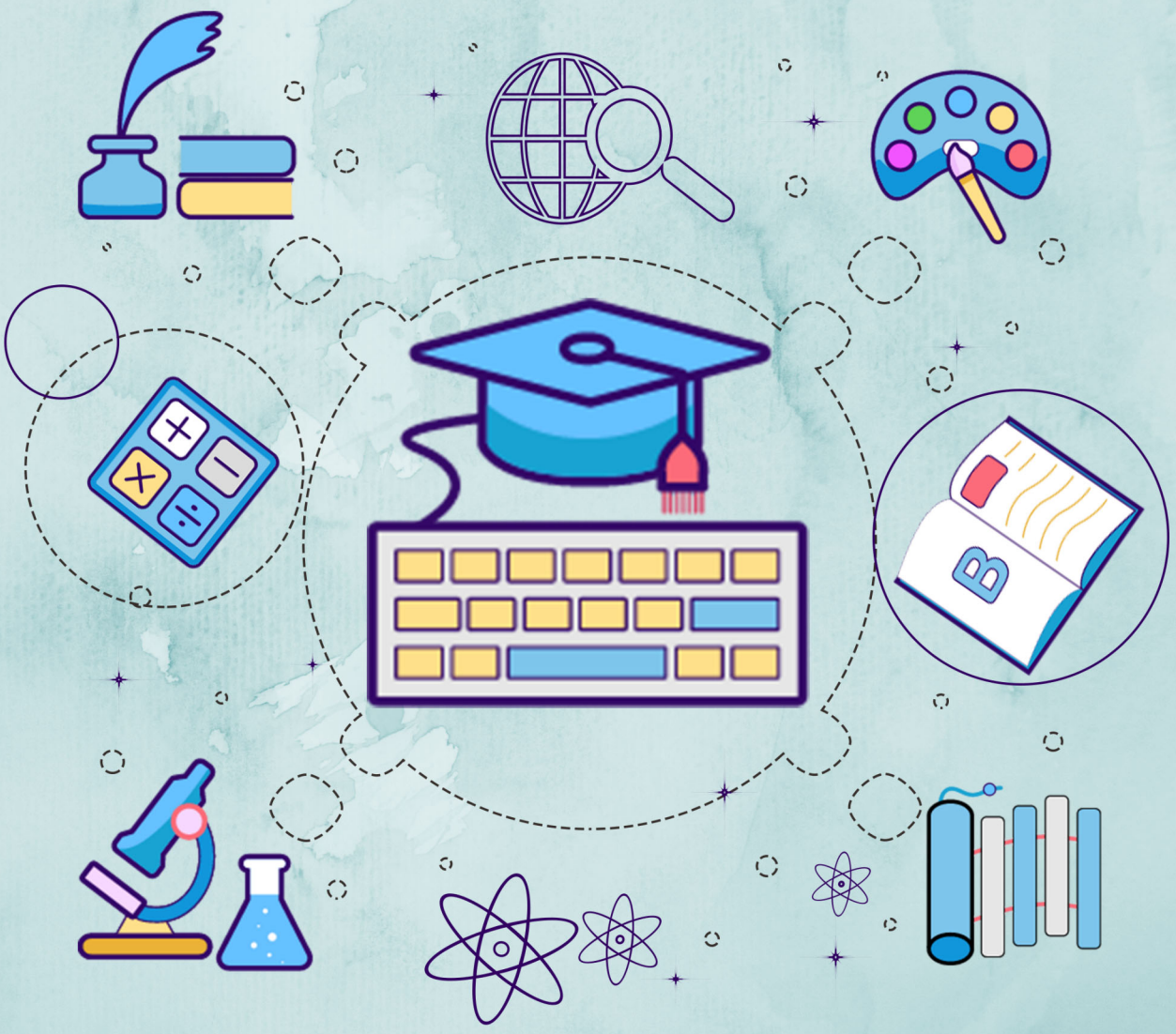

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KTU S4 CSE

COMPUTER ORGANIZATION AND ARCHITECTURE (CST 202)

QUESTION BANK

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KTU S4 CSE Computer Organization & Architecture (COA)

Module Wise Question Bank

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MODULE 1

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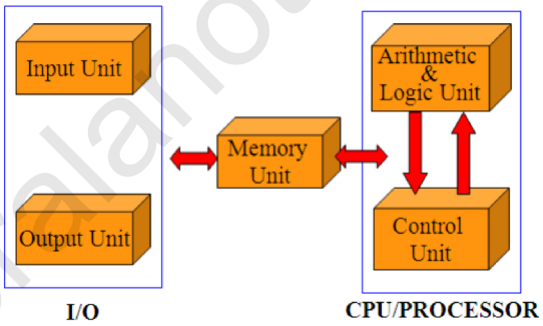
1. **Explain the functional units of computer**



- Input Unit: Data/ instructions are fed to a computer through input unit
  Examples: keyboard, mouse. Scanner, joystick
- Arithmetic & Logic Unit: ALU consist of necessary logic circuits like adder, comparator etc., to perform arithmetic and logic operations such as addition, multiplication, comparison of two numbers etc.
- Control Unit: Control unit co-ordinates activities of all units by issuing control signals. Control signals issued by control unit govern the data transfers and then appropriate operations take place. Control unit interprets or decides the operation/action to be performed.

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- ALU &Control Unit together called Central Processing Unit (CPU). CPU is the brain of a computer system.
- **Memory Unit**: Memory unit stores the program instructions (Code), data and results of computations etc

  Examples: ROM,RAM
- **Output Unit**: Computer after computation returns the computed results, error messages, etc. via output unit.

  Examples: Monitor, printer, speaker

2. **Describe the operational concepts of a computer.**
   - A set of instructions called a program reside in the main memory of computer. Data is also stored in the memory
   - The CPU fetches those instructions sequentially one-by-one from the main memory, decodes them and performs the specified operation on associated data operands in ALU.
   - Processed data and results will be stored in the memory and displayed on an output unit.
   - All activities pertaining to processing and data movement inside the computer machine are governed by control unit.

3. **What is a register? Describe the functions of various registers in CPU with a neat diagram./ Explain the internal architecture of a processor.**

   Registers are high-speed storage area within the CPU. All data must be stored in a register before it can be processed.

   In addition to ALU CPU also contains CPU also contains Instruction Register (IR), the Program Counter(PC), the general-purpose registers, the Memory Address Register(MAR) and Memory Data Register(MDR).

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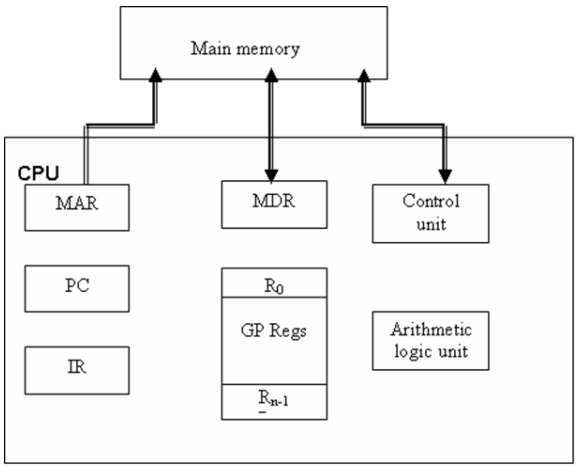

Functions

- **Instruction Register(IR)**: contains the instruction that is being executed. Its output is available to the control circuits, that generate the timing signals for control of the actual processing circuits needed to execute the instruction.
- **Program Counter(PC):** It contains the memory address of the next instruction to be fetched and executed
- **Memory Address Register (MAR):** holds the address of the memory location to or from which data is to be transferred.
- **Memory Data Register(MDR):** contains the data to be written into or read-out of the addressed memory location.
- **General- purpose Registers:** are used for holding data, intermediate results of operations. They are also known as scratch-pad registers.

4. Illustrate the basic operational concepts in transferring data between main memory and processor.

- Programs reside in the memory & usually get these through the input unit.
- Execution of the program starts when the PC is set to point at the first instruction of the program.
- Contents of PC are transferred to MAR and a Read Control Signal is sent to the memory.
- The addressed word is read out of the memory and loaded into the MDR.
- Now contents of MDR are transferred to the IR & now the instruction is ready to be decoded and executed.

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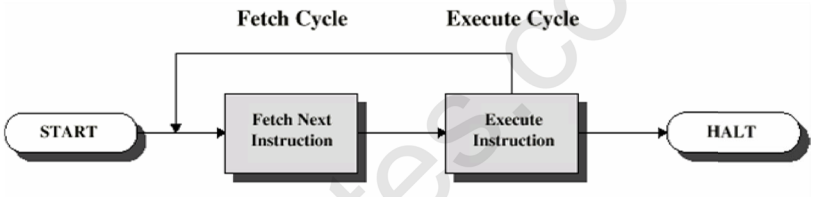
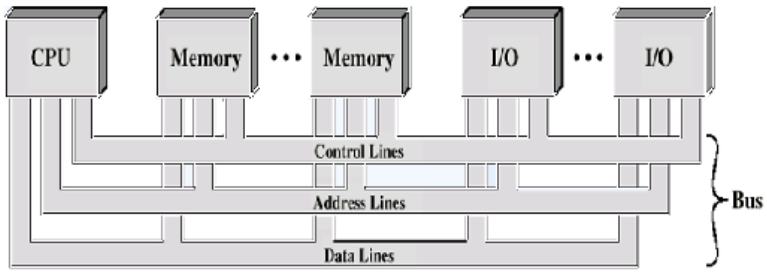
- If the instruction involves an operation by the ALU, it is necessary to obtain the required operands.
- An operand in the memory is fetched by sending its address to MAR & Initiating a read cycle.
- When the operand has been read from the memory to the MDR, it is transferred from MDR to the ALU.
- After one or two such repeated cycles, the ALU can perform the desired operation.
- If the result of this operation is to be stored in the memory, the result is sent to MDR.
- Address of location where the result is stored is sent to MAR & a write cycle is initiated.
- The contents of PC are incremented so that PC points to the next instruction that is to be executed.



5. **List different types of buses used to interconnect various functional units in a computer.**
   - **Data Bus**: It is used for transmission of data. The number of data lines corresponds to the number of bits in a word.
   - **Address Bus**: It carries the address of the main memory location from where the data can be accessed.
   - **Control Bus**: It is used to indicate the direction of data transfer and to coordinate the timing of events during the transfer.



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6. **Explain zero, one, two and three address instruction with an example for each.**

Three -address instruction format

This instruction format consists of three addresses along with an operation field. The three addresses include the address of the first operand, address of the second operand, address to store the result.

Format: Operation code Source1,source2, destination

Example: Add A,B,C

[C]← [A]+[B]

Two -address instruction format

This instruction format consists of two addresses along with an operation field. The two addresses include the address of the first operand, address of the second operand; the result is stored in one of the operand address.

Example: Add A, B

B← [A]+[B]

One -address instruction format

This instruction format consists of one address along with an operation field. The address is that of the first operand. The second operand and the result are stored in a CPU register called **accumulator**. A machine has only one accumulator; it need not be explicitly mentioned in the instruction.

Example: Add A

Zero -address instruction format

A **stack** is included in the CPU for performing arithmetic and logic instructions with no addresses. The operands are pushed onto the stack from memory and ALU operations are implicitly performed on the top elements of the stack.

Example: Add

Top of stack = top of stack + second top of stack

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7. **What is an addressing mode? List different addressing modes used in an instruction execution.**

   The address generated by the CPU in-order to access the operand in the memory is termed as an effective address. The methods used to provide an access path to operands in memory and CPU registers is addressing mode.

   Various addressing modes are

   - Immediate
   - Register
   - Direct(Absolute)
   - Indirect
   - Index (Displacement)
   - Base with index
   - Base with index and offset
   - Relative
   - Auto increment
   - Auto decrement

8. **Describe auto increment addressing mode with the help of an example.**

   After accessing the operand the content of this register is automatically incremented to point the next item in the list.

   Increment R_i

   Add (R1)+, R2

9. **Identify the following addressing modes.**

   Move #500,R0-Immediate Addressing mode

   Add 4(R0),R1-Index addressing mode

   Add #16,R0-Immediate addressing mode

   Add 12(R0),R3-Index addressing mode

   Move R1,Sum1-Combination of register and direct

   Add [R2],[R0]- Indirect addressing mode

   Add (R2)+,R0-Autoincrement mode

   Add Loc,R2- Direct addressing mode

   Add (R3),R2-Indirect addressing mode

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Add (R5),R1-Indirect addressing mode

Move R5, R4-Register Addressing mode

Move Loc1,Loc2-Direct addressing mode

Load 20(R1),R5-Index addressing mode

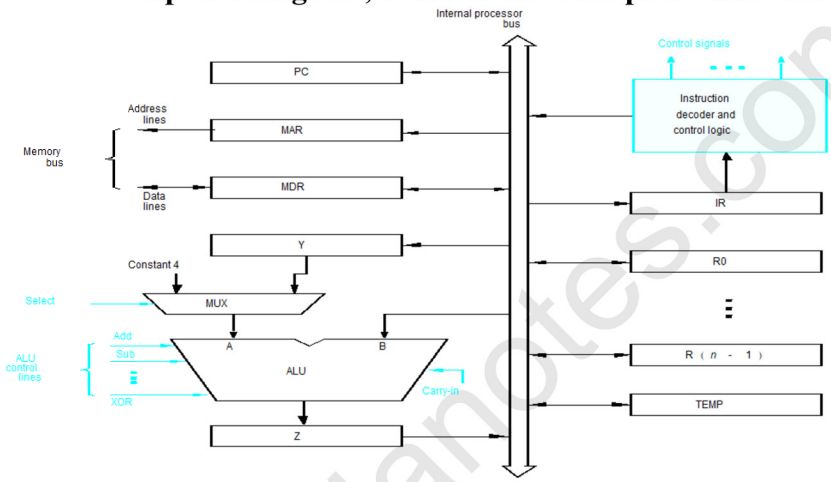
Store R5,30(R1,R2)-Base with index and offset

Sub (R1)+,R5-Autoincrement mode

Add (-R1),R5-Autodecrement mode

Jump 10(PC)- Relative addressing mode

10. With the help of a diagram, describe the data-path inside the processor.



- Processor fetches one instruction at a time and perform the operation specified.
- Instructions are fetched from successive memory locations until a branch or a jump instruction is encountered.
- Processor keeps track of the address of the memory location containing the next instruction to be fetched using Program Counter (PC).
- Fetch the contents of the memory location pointed to by the PC. The contents of this location are loaded into the IR (fetch phase).

$$IR \leftarrow [[PC]]$$

- Assuming that the memory is byte addressable(4 byte long), increment the contents of the PC by 4 (fetch phase).

$$PC \leftarrow [PC] + 4$$

  - PC Keeps track of execution of a program
  - Contains the memory address of the next instruction to be fetched and executed.

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- Constant 4 is used by the processor to increment the contents of PC.

- Carry out the actions specified by the instruction in the IR (execution phase).
- The data and address lines of external memory connected to the processor bus via MDR and MAR
- Register MDR has 2 inputs and 2 outputs.:
  - Contains data to be written into or read out of the addressed location.
  - Data can be loaded into MDR either from memory bus or from internal processor bus.
- MAR Holds the address of the location to be accessed.
  - I/P of MAR is connected to Internal bus and an O/p to external bus.
- The instruction decoder and control logic circuit is responsible for implementing the actions specified by the instruction loaded in IR
  - The decoder generate the control signals needed to select the registers
  - The registers, ALU and interconnecting bus are collectively referred to as the data path.
- MUX
  - Select either the output of the register Y or a constant value 4 to be provided as input A of the ALU.

11. Give the control sequence for execution of instruction Add[R3],R1 using a single bus organization

Step	Action
1	PC_{out} , MAR_{in} , Read, Select4,Add, Z_{in}
2	Z_{out} , PC_{in} , Y_{in} , WMF C
3	MDR_{out} , IR_{in}
4	$R3_{out}$, MAR_{in} , Read
5	$R1_{out}$, Y_{in} , WMF C
6	MDR_{out} , SelectY, Add, Z_{in}
7	Z_{out} , $R1_{in}$, End

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12. Write down the sequence of actions needed to fetch and execute the instruction

LOAD 10(R2),R1.

1. Pcout, MARin, Read,Select4,Add, Zin
2. Zout, Pcin, Yin,WMFC
3. MDRout, IRin
4. R2out,MARin, Read
5. WMFC, MDRout
6. IR10out,Yin
7. Select Y, Add, Zin
8. Zout, R1 in, End

13. Write down the sequence of actions needed to fetch and execute the instruction

STORE R1, 10(R2)

1. Pcout, MARin, Read,Select4,Add, Zin
2. Zout, Pcin, Yin,WMFC
3. MDRout, IRin
4. R2out,MARin, Read
5. WMFC, MDRout
6. IR10out,Yin
7. Select Y, Add, Zin
8. Zout, MARin
9. R1 out, MDRin, Write
10. WMFC, End

14. Give the sequence of control steps required to perform the operation ADD NUM, R1

1. Pcout, MARin, Read,Select4,Add, Zin
2. Zout, Pcin, Yin,WMFC
3. MDRout, IRin
4. IRNUMout,Yin,
5. SelectY, R1out, Add, Zin
6. Zout, R1in,End

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15. Give the sequence of control steps to perform the operation ADD (NUM),R1

1. Pcout, MARin, Read,Select4,Add, Zin
2. Zout, Pcin, Yin,WMFC
3. MDRout, IRin
4. IRNUMout,MARin, Read
5. WMFC, MDRout,MARin,Read
6. WMFC, MDRout,Yin
7. Select Y, R1out, Add,Zin
8. Zout,R1in,END

16. Give the sequence of control steps required to perform the operation ADD R1, NUM

1. PCout, MARin, Read,Select4,Add, Zin
2. Zout, Pcin, Yin,WMFC
3. MDRout, IRin
4. IRNUMout, MARin, Read
5. WMFC, MDRout, Yin,
6. Select Y, R1out,Add, Zin
7. Zout, MDRin, Write
8. WMFC, END

17. Illustrate the advantages of using multiple bus organization over single bus organization.

- Multiple Bus Organization Improves Efficiency.
- Additional Buses Allow Expansion.
- More Buses Means More Compatibility
- Processor speed is high in multiple bus organization

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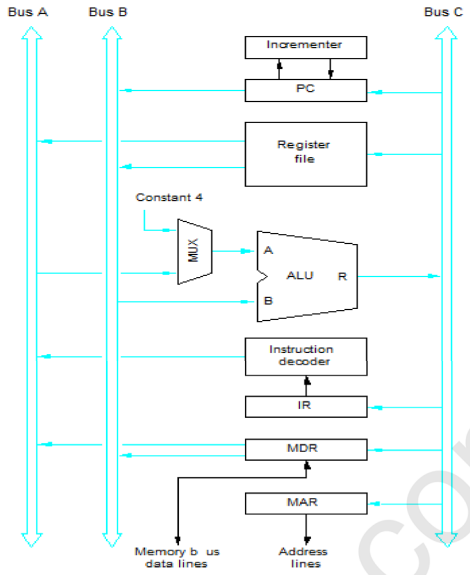
18. Draw the diagram of a multi-bus organization with 3 buses. Write the control sequence for the instruction Add R4, R5, R6 for the above mentioned multi-bus organization.



Step	Action
1	PC_{out}, R=B, MAR_{in}, Read, IncPC
2	WMFC
3	MDR_{outB}, R=B, IR_{in}
4	$R4_{outA}$, $R5_{outB}$, SelectA, Add, $R6_{in}$, End

19. How is a branching instruction executed?

A branch instruction replaces the contents of PC with the branch target address, which is usually obtained by adding an offset X given in the branch instruction. The offset X is usually the difference between the branch target address and the address immediately following the branch instruction

Control Sequence of a branch instruction

1. PC out, MKAR in, Read, Clear Y, Set carry in to ALU,ADD,Zin
2. Z out, PC in, WMFC
3. MDR out, IR in
4. PC out, Y in
5. Offset field of IR out, ADD, Zin
6. Zout, PC in ,End

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