CST 202	Computer Organization and Architecture	CATEGORY	L	T	P	CREDIT	YEAR OF INTRODUCTION
		PCC	3	1	0	4	2019

Preamble:

The course is prepared with the view of enabling the learners capable of understanding the fundamental architecture of a digital computer. Study of Computer Organization and Architecture is essential to understand the hardware behind the code and its execution at physical level by interacting with existing memory and I/O structure. It helps the learners to understand the fundamentals about computer system design so that they can extend the features of computer organization to detect and solve problems occurring in computer architecture.

Prerequisite : Topics covered under the course Logic System Design (CST 203)

Course Outcomes: After the completion of the course the student will be able to

CO#	CO
CO1	Recognize and express the relevance of basic components, I/O organization and pipelining schemes in a digital computer **(Cognitive knowledge: Understand)**
CO2	Explain the types of memory systems and mapping functions used in memory systems **(Cognitive Knowledge Level: Understand)**
CO3	Demonstrate the control signals required for the execution of a given instruction **(Cognitive Knowledge Level: Apply))**
CO4	Illustrate the design of Arithmetic Logic Unit and explain the usage of registers in it **(Cognitive Knowledge Level: Apply)**
CO5	Explain the implementation aspects of arithmetic algorithms in a digital computer **(Cognitive Knowledge Level:Apply)**
CO6	Develop the control logic for a given arithmetic problem **(Cognitive Knowledge Level: Apply)**

Mapping of course outcomes with program outcomes

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	✓	✓	✓	✓								✓
CO2	✓	✓	✓	✓						✓		✓
CO3	✓	✓	✓	✓						✓		✓
CO4	✓	✓	✓	✓						✓		✓
CO5	✓	✓	✓							✓		✓
CO6	✓	✓	✓	✓								✓

Abstract POs defined by National Board of Accreditation			
PO#	**Broad PO**	**PO#**	**Broad PO**
PO1	Engineering Knowledge	**PO7**	Environment and Sustainability
PO2	Problem Analysis	**PO8**	Ethics
PO3	Design/Development of solutions	**PO9**	Individual and team work
PO4	Conduct investigations of complex problems	**PO10**	Communication
PO5	Modern tool usage	**PO11**	Project Management and Finance
PO6	The Engineer and Society	**PO12**	Life long learning

Assessment Pattern

Bloom's Category	Continuous Assessment Tests		End Semester Examination Marks (%)
	Test1 (%)	Test2 (%)	
Remember	20	20	30
Understand	40	40	30
Apply	40	40	40
Analyze			

Evaluate			
Create			

Mark Distribution

Total Marks	CIE Marks	ESE Marks	ESE Duration
150	**50**	**100**	**3 hours**

Continuous Internal Evaluation Pattern:

Attendance : 10 marks

Continuous Assessment Tests : 25 marks

Continuous Assessment Assignment : 15 marks

Internal Examination Pattern:

Each of the two internal examinations has to be conducted out of 50 marks

First Internal Examination shall be preferably conducted after completing the first half of the syllabus and the Second Internal Examination shall be preferably conducted after completing remaining part of the syllabus.

There will be two parts: Part A and Part B. Part A contains 5 questions (preferably, 2 questions each from the completed modules and 1 question from the partly covered module), having 3 marks for each question adding up to 15 marks for part A. Students should answer all questions from Part A. Part B contains 7 questions (preferably, 3 questions each from the completed modules and 1 question from the partly covered module), each with 7 marks. Out of the 7 questions in Part B, a student should answer any 5.

End Semester Examination Pattern:

There will be two parts; Part A and Part B. Part A contains 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which a student should answer any one. Each question can have maximum 2 sub-divisions and carries 14 marks.

Syllabus

Module 1

Basic Structure of computers – functional units - basic operational concepts - bus structures. Memory locations and addresses - memory operations,Instructions and instruction sequencing , addressing modes.

Basic processing unit – fundamental concepts – instruction cycle – execution of a complete instruction - single bus and multiple bus organization

Module 2

Register transfer logic: inter register transfer – arithmetic, logic and shift micro operations.

Processor logic design: - processor organization – Arithmetic logic unit - design of arithmetic circuit - design of logic circuit - Design of arithmetic logic unit - status register – design of shifter - processor unit – design of accumulator.

Module 3

Arithmetic algorithms: Algorithms for multiplication and division (restoring method) of binary numbers. Array multiplier , Booth's multiplication algorithm.

Pipelining: Basic principles**,** classification of pipeline processors, instruction and arithmetic pipelines (Design examples not required), hazard detection and resolution.

Module 4

Control Logic Design: Control organization – Hard_wired control-microprogram control – control of processor unit - Microprogram sequencer,micro programmed CPU organization - horizontal and vertical micro instructions.

Module 5

I/O organization: accessing of I/O devices – interrupts, interrupt hardware -Direct memory access.

Memory system: basic concepts – semiconductor RAMs. memory system considerations – ROMs, Content addressable memory, cache memories - mapping functions.

Text Books

1. Hamacher C., Z. Vranesic and S. Zaky, Computer Organization ,5/e, McGraw Hill, 2011
2. Mano M. M., Digital Logic & Computer Design, PHI, 2004
3. KaiHwang, Faye Alye Briggs, Computer architecture and parallel processing McGraw-Hill, 1984

Reference Books

1. Mano M. M., Digital Logic & Computer Design, 3/e, Pearson Education, 2013.
2. Patterson D.A. and J. L. Hennessy, Computer Organization and Design, 5/e, Morgan Kaufmann Publishers, 2013.
3. William Stallings, Computer Organization and Architecture: Designing for Performance, Pearson, 9/e, 2013.
4. Chaudhuri P., Computer Organization and Design, 2/e, Prentice Hall, 2008.
5. Rajaraman V. and T. Radhakrishnan, Computer Organization and Architecture, Prentice Hall, 2011

Sample Course Level Assessment Questions

Course Outcome1(CO1): Which are the registers involved in a memory access operation and how are they involved in it?

Course Outcome 2(CO2): Explain the steps taken by the system to handle a write miss condition inside the cache memory.

Course Outcome 3(CO3): Generate the sequence of control signals required for the execution of the instruction MOV [R1],R2 in a threebus organization.

Course Outcome 4(CO4): Design a 4-bit combinational logic shifter with 2 control signals H0 and H1 that perform the following operations :

H1	H0	Operation
0	0	Transfer 1's to all output line
0	1	No shift operation
1	0	Shift left
1	1	Shift right

Course Outcome 5(CO5): Explain the restoring algorithm for binary division. Also trace the algorithm to divide $(1001)_2$ by $(11)_2$

Course Outcome 6(CO6): Design a software control logic based on microprogramed control to perform the addition of 2 signed numbers represented in sign magnitude form.

Model Question Paper

QP CODE: PAGES:2

Reg No:_____

Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION, MONTH & YEAR

Course Code: CST 202

Course Name: Computer organization and architecture

Max.Marks:100 **Duration: 3 Hours**

PART A

Answer all Questions. Each question carries 3 Marks

1. Give the significance of instruction cycle.
2. Distinguish between big endian and little endian notations. Also give the significance of these notations.
3. Compare I/O mapped I/O and memory mapped I/O.
4. Give the importance of interrupts in I/O interconnection.
5. Justify the significance of status register.
6. How does the arithmetic circuitry perform logical operations in an ALU.
7. Illustrate divide overflow with an example.
8. Write notes on arithmetic pipeline.
9. Briefly explain the role of micro program sequence.
10. Differentiate between horizontal and vertical micro instructions.

Part B

Answer any one Question from each module. Each question carries 14 Marks

11.

11.(a) What is the significance of addressing modes in computer architecture.

(4)

11.(b) Write the control sequence for the instruction DIV R1,[R2] in a three bus structure.

(10)

OR

12. Explain the concept of a single bus organization with help of a diagram. Write the control sequence for the instruction ADD [R1],[R2].

(14)

13. Explain various register transfer logics.

(14)

OR

14.

14.(a) Design a 4 bit combinational logic shifter with 2 control signals H1 and H2 that perform the following operations (bit values given in parenthesis are the values of control variable H1 and H2 respectively.) : Transfer of 0's to S (00), shift right (01), shift left (10), no shift (11).

(5)

14.(b) Design an ALU unit which will perform arithmetic and logic operation with a given binary adder.

(9)

15.

15.(a) Give the logic used behind Booth's multiplication algorithm.

(4)

15.(b) Identify the appropriate algorithm available inside the system to perform the multiplication between -14 and -9. Also trace the algorithm for the above input.

(10)

OR

16.

16.(a) List and explain the different pipeline hazards and their possible solutions

(10)

16.(b) Design a combinational circuit for 3x2 multiplication.

(4)

17. Design a hardwared control unit used to perform addition/subtraction of 2 numbers represented in sign magnitude form.

(14)

OR

18. Give the structure of the micro program sequencer and its role in sequencing the micro instructions.

(14)

19.

19.(a) Explain the different ways in which interrupt priority schemes can be implemented

(10)

19.(b) Give the structure of SRAM cell.

(4)

OR

20.

20.(a) Explain the various mapping functions available in cache memory.

(9)

20.(b) Briefly explain content addressable memory.

(5)

TEACHING PLAN		
No	**Contents**	**No of Lecture Hrs**
Module 1 : (Basic Structure of computers) (9 hours)		
1.1	Functional units,basic operational concepts,bus structures (introduction)	1
1.2	Memory locations and addresses , memory operations	1
1.3	Instructions and instruction sequencing	1
1.4	Addressing modes	1
1.5	Fundamental concepts of instruction execution, instruction cycle	1
1.6	Execution of a complete instruction - single bus organization (Lecture 1)	1
1.7	Execution of a complete instruction - single bus organization (Lecture 2)	1
1.8	Execution of a complete instruction - multiple bus organization (Lecture 1)	1
1.9	Execution of a complete instruction - multiple bus organization (Lecture 2)	1
Module 2 :(Register transfer logic and Processor logic design) (10 hours)		
2.1	Inter register transfer – arithmetic micro operations	1
2.2	Inter register transfer – logic and shift micro operations	1
2.3	Processor organization	1
2.4	Design of arithmetic circuit	1
2.5	Design of logic circuit	1
2.6	Design of arithmetic logic unit	1
2.7	Design of status register	1
2.8	Design of shifter - processor unit	1

2.9	Design of accumulator (Lecture 1)	1
2.10	Design of accumulator (Lecture 2)	1
Module 3 : (Arithmetic algorithms and Pipelining) (9 hours)		
3.1	Algorithm for multiplication of binary numbers	1
3.2	Algorithm for division (restoring method) of binary numbers	1
3.3	Array multiplier	1
3.4	Booth's multiplication algorithm	1
3.5	Pipelining: Basic principles	1
3.6	Classification of pipeline processors (Lecture 1)	1
3.7	Classification of pipeline processors (Lecture 2)	1
3.8	Instruction and arithmetic pipelines (Design examples not required)	1
3.9	Hazard detection and resolution	1
Module 4 :(Control Logic Design) (9 hours)		
4.1	Control organization –design of hardwired control logic (Lecture 1)	1
4.2	Control organization –design of hardwired control logic (Lecture 2)	1
4.3	Control organization –design of hardwired control logic (Lecture 3)	1
4.4	Design of microprogram control logic–control of processor unit (Lecture1)	1
4.5	Design of microprogram control logic–control of processor unit (Lecture2)	1
4.6	Design of microprogram control logic–control of processor unit (Lecture3)	1
4.7	Microprogram sequencer	1
4.8	Micro programmed CPU organization	1
4.9	Microinstructions –horizontal and vertical micro instructions	1
Module 5 : (Basic processing units, I/O and memory) (8 hours)		
5.1	Accessing of I/O devices –interrupts	1
5.2	Interrupt hardware	1

5.3	Direct memory access	1
5.4	Memory system: basic concepts –semiconductor RAMs	1
5.5	Memory system considerations – ROMs	1
5.6	Content addressable memory	1
5.7	Cache memories -mapping functions (Lecture 1)	1
5.8	Cache memories -mapping functions (Lecture 2)	1