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DRAFT Scheme of Valuation/Answer Key

(Scheme of evaluation (marks in brackets) and answers of problems/key)

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

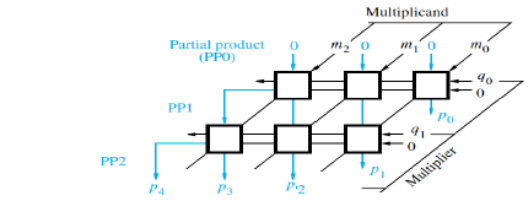
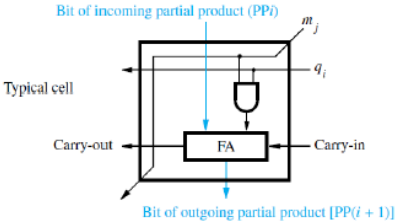
FOURTH SEMESTER B.TECH DEGREE EXAMINATION, **MAY 2021**

Course Code: CST202

Course Name: Computer Organization and Architecture

Max. Marks: 100		Duration: 3 Hours

PART A

		(Answer all questions; each question carries 3 marks)	Marks
1		Auto increment Mode = after operand addressing , the contents of the register is incremented.eg: (R4)+ (1.5 marks) Decrement Mode = before operand addressing, the contents of the register is decrement.eg: -(R4) (1.5 marks)	3
2		MAR, MDR (1 mark) 1) MAR_{in} , 2) MDR_{in} , MDR_{out}, MDR_{inE}, MDR_{outE}, (2 marks)	3
3		Example (1.5 marks) Explanation (1.5 marks)	3
4		Any binary data can be represented in the form of 2^k-2^m(1.5 marks) To multiply with 2 shift towards left (1.5 mark)	3
5		 (a)Array multiplication of positive binary operands  (b) Multiplier cell	3
6		Structural hazards, data hazards, control hazards (Each carries 1 mark)	3
7		A control unit whose binary control variables are stored in memory is called a micro programmed control unit.	3

8		Control organization 4 methods: 1. One flip flop per state method 2. Sequence register and decoder method 3. PLA control 4. Micro-program control	3
9		An **interrupt** is a signal to the processor emitted by hardware or software indicating an event that needs immediate attention. (1.5 marks) Steps (1.5 marks)	3
10		SRAM circuits require more area on a chip, because an SRAM memory cell requires four to six transistors compared to a single transistor and a capacitor for DRAM	3
PART B			
(Answer one full question from each module, each question carrie			
Module -1			
11	a)	**Single bus organization:** Allows only one transfer at a time. It costs very low It is flexible for attaching peripheral devices. Its performance is low **Multiple bus organization:** Allows two or more transfer at a time. It costs high It provides concurrency in operation. Its performance is high	4
	b)	**(A+B) * (C+D)** **(5 marks)** ● Three-Address 1. ADD A, B, R1 ; R1 ← M[A] + M[B] 2. ADD C, D, R2 ; R2 ← M[C] + M[D] 3. MUL R1, R2, X ; M[X] ← R1 * R2 ● Two-Address 1. MOV A, R1 ; R1 ← M[A] 2. ADD B, R1 ; R1 ← R1 + M[B] 3. MOV C, R2 ; R2 ← M[C] 4. ADD D, R2 ; R2 ← R2 + M[D]	10

		5. MUL R2, R1 ; R1 ← R1 * R2 6. MOV R1,X ; M[X] ← R1 ● One-Address [AC- ACCUMULATOR] 1. LOAD A ; AC ← M[A] 2. ADD B ; AC ← AC + M[B] 3. STORE T ; M[T] ← AC 4. LOAD C ; AC ← M[C] 5. ADD D ; AC ← AC + M[D] 6. MUL T ; AC ← AC * M[T] 7. STORE X ; M[X] ← AC **C← [A] + [B]** (5 marks) ● Three-Address 1. ADD A, B, C ; C ← M[A] + M[B] ● Two-Address 1. MOV A, R1 ; R1 ← M[A] 2. ADD B, R1 ; R1 ← R1 + M[B] 3. MOV R1,C ; M[C]← R1 ● One-Address [AC- ACCUMULATOR] 1. LOAD A ; AC ← M[A] 2. ADD B ; AC ← AC + M[B] 3. STORE C ; M[C] ← AC	
12	a)	Figure (3 marks) Explanation(3 marks)	6
	b)	Single bus organization figure (3 marks) Control sequences for instruction ADD [R2],R3 (5 marks)	8
		Module -2	
13	a)	Processor organization methods - (1 mark) i scratchpad memory (figure 1.5 marks explanation 1.5 marks) ii Two-port memory (figure 1.5 marks explanation 1.5 marks) iii Accumulator register (figure 1.5 marks explanation 1.5 marks)	10
	b)	True complement circuit - figure(2.5 marks) Explanation (1.5 marks)	4
14	a)	Diagram(4 marks)	8

		Explanation (4 marks)	
	b)	Shifter - Figure (4 marks) Explanation (2 marks)	6
Module -3			
15	a)	Restoring division - flowchart(3 marks) Explanation with example(3 marks)	6
	b)	Data hazards - A data hazard is any condition in which either the source or the destination operands of an instruction are not available at the time expected in the pipeline. As a result some operation has to be delayed, and the pipeline stalls. (1 marks) Mention various data hazards (3) Resolution techniques: internal forwarding ,short circuiting(4 marks)	8
16	a)	Booth's multiplication algorithm - flow chart(2 marks) -5 X 4 example(3 marks)	8
	b)	Draw time space diagram (1 marks) (minimum 5 hazards should be identified 1 mark for each) Between I_1 & I_3 structural Between I_1 & I_2 data(RAW) Between I_2 & I_3 data(RAW) Between I_1 & I_5 structural I_4 Control	6
Module -4			
17	a)	Micro-program sequencer - figure (4 marks) Detailed explanation (6 marks)	10
	b)	Vertical instruction format(2 marks) Horizontal instruction format(2 marks)	4
18	a)	Micro-programmed computer organization - figure (4marks) explanation (4 marks)	8
	b)	One flip-flop per method - figure (3marks) Explanation(3 marks)	6
Module -5			
19	a)	I/O accessing mechanisms A Program driven (3 marks)	7

		B, Interrupt initiated I/O (3 marks) C, DMA (3 marks)	
	b)	ROM explanation(1 mark) (Mention any four type one mark each) PROM: Allows data to be loaded by user, programmability is achieved by inserting a fuse at point P in a ROM cell. EPROM : In EPROM, one can program the memory chip and erase it thousands of times, erasure requires dissipating charges trapped in the transistor of memory cells. This can be done by exposing the chip to UV light. EEPROM : Its method of erasure is electrical, so requires different voltages for erasing, writing and reading stored data FLASH MEMORY : The erasure of the entire contents takes less than a second, or one might say in a flash, hence its name, Flash memory. (4X1.5=6 marks)	5
20	a)	Internal organization of 1K X 8 memory chip - Diagram - (3 marks) Explanation (2 marks)	5
	b)	Direct mapping (3 marks) Associative mapping (3 marks) Set associative mapping (3 marks)	9
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