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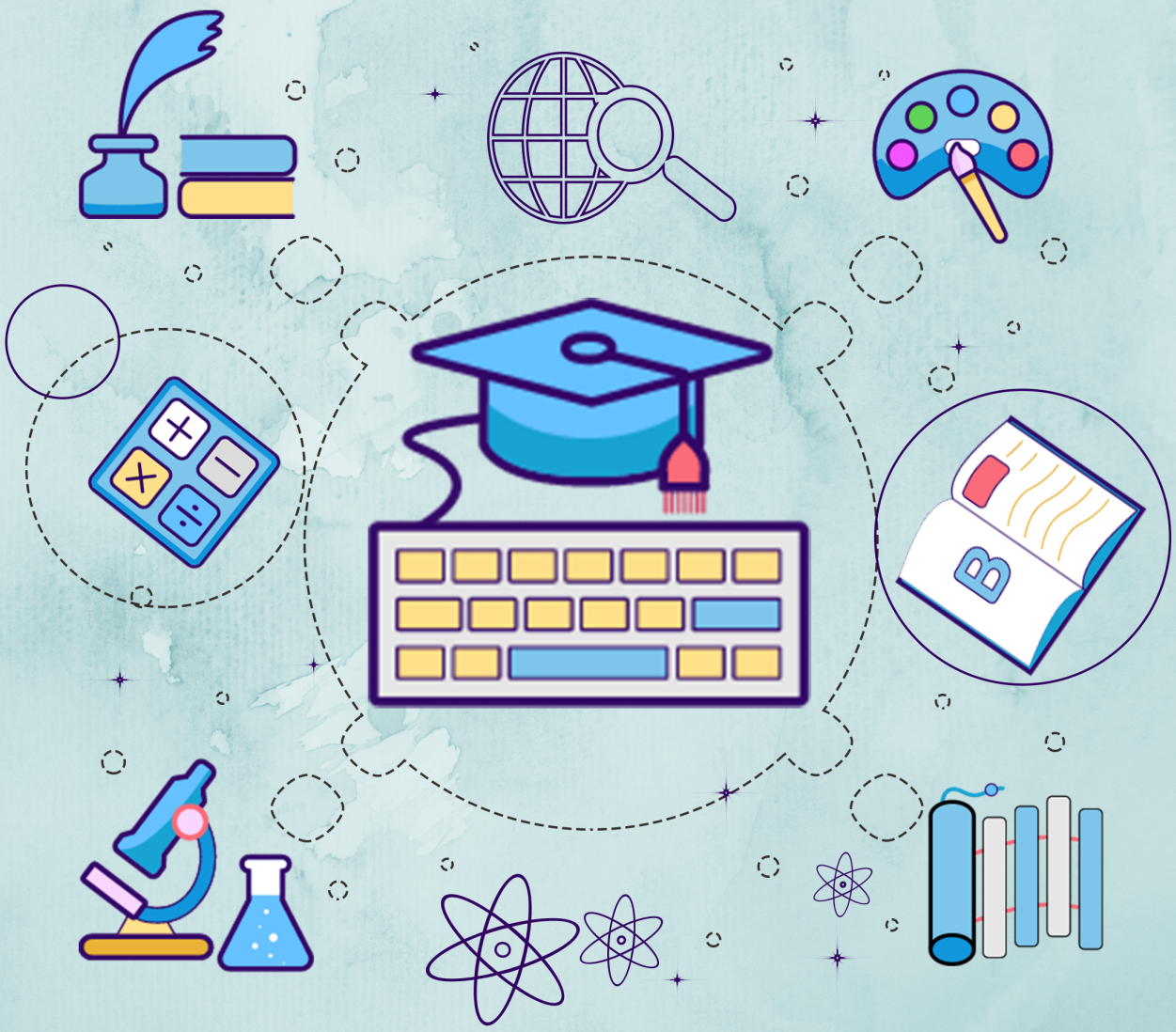

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KTU S4 CSE

COMPUTER ORGANIZATION AND ARCHITECTURE (CST 202)

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MODULE 2

20. List the components of register transfer logic.

The set of registers in the system and their functions: A register also encompasses all type of registers including shift registers, counters and memory units.

The binary-coded information stored in the registers: The binary information stored in registers may be binary numbers, binary coded decimal numbers, alphanumeric characters, control information or any other binary coded information.

The operations performed on the information stored in the registers: The operations performed on data stored in registers are called micro operations. Examples are shift, count, add, clear and load

The control functions that initiate the sequence of operations: The control functions that initiate the sequence of operations consists of timing signals that sequence the operations one at a time.

21. What is microoperation?

Micro-operations: operations executed on data stored in one or more registers. For any function of the computer, a sequence of micro-operations is used to describe it

Example: Shift, count, clear, add & load

22. What are the different types of micro operations?

a. Register transfer microoperations
b. Arithmetic microoperations (on numeric data stored in the registers)
c. Logic microoperations (bit manipulations on non-numeric data)
d. Shift microoperations

23. How do you represent register in resister transfer logic.

- Rectangular box with name of the register inside,
- The individual cells is assigned a letter with a subscript number,
- The numbering of cells from right to left can be marked on top of the box,
- 16 bit register is partitioned into 2 parts , bits 1 to 8 are assigned the letter L(for low) and bits 9 to 16 are assigned the letter H(for high)

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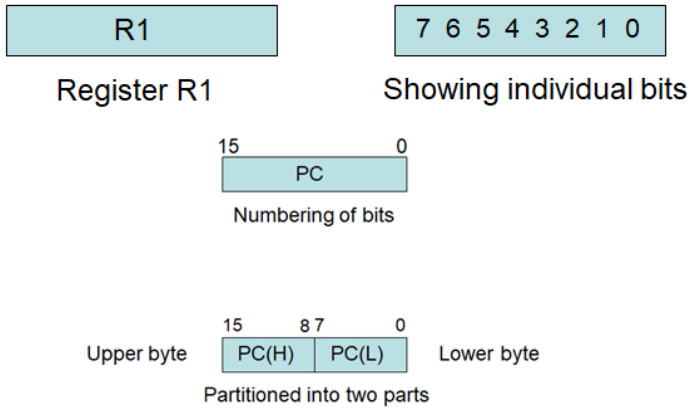

24. Explain the register transfer micro operation with the help of an example.

- Information transfer from one register to another is described by a *replacement operator:* R2 ← R1
- This statement denotes a transfer of the content of register R1 into register R2
- The transfer happens in one clock cycle
- The content of the R1 (source) does not change
- The content of the R2 (destination) will be lost and replaced by the new data transferred from R1
- We are assuming that the circuits are available from the outputs of the source register to the inputs of the destination register, and that the destination register has a parallel load capability

25. With a neat diagram explain how the the conditional transfer operation is implemented.

- Conditional transfer occurs only under a control condition
- Representation of a (conditional) transfer
  - X'T1: A ← B
- A binary condition (X'T1 equals to 0 or 1) determines when the transfer occurs
- The content of B is transferred into A only if if x is 0 and T_1 is 1`

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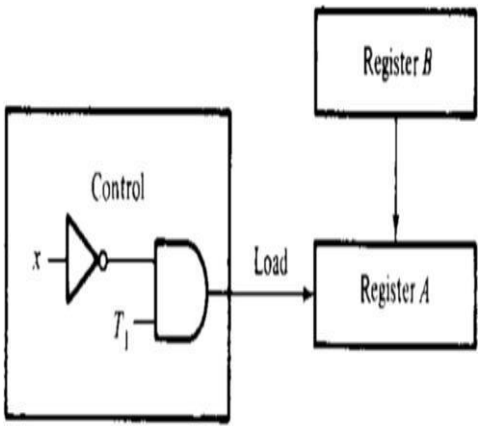

26. Illustrate the basic symbols used in register transfer operation with examples.

Basic Symbols for Register Transfers		
Symbol	Description	Examples
Letters & numerals	Denotes a register	MAR, R2
Parenthesis ( )	Denotes a part of a register	R2(0-7), R2(L)
Arrow ←	Denotes transfer of information	R2 ← R1
Comma ,	Separates two microoperations	R2 ← R1, R1 ← R2
Colon:	Terminates a control function	P:
Square Brackets [ ]	Specifies an address for memory transfer	MBR ← M [MAR]

27. List all possible arithmetic micro operations with an example.

- Addition Microoperation:R3 ←R1+R2
- Subtraction Microoperation: R3 ←R1-R2 OR R3 ←R1+R2'+1
- One's Complement Microoperation:R2 ←R2'
- Two's Complement Microoperation:R2 ←R2'+1
- Increment Microoperation:R2 ←R2+1
- Decrement Microoperation:R2 ←R2-1

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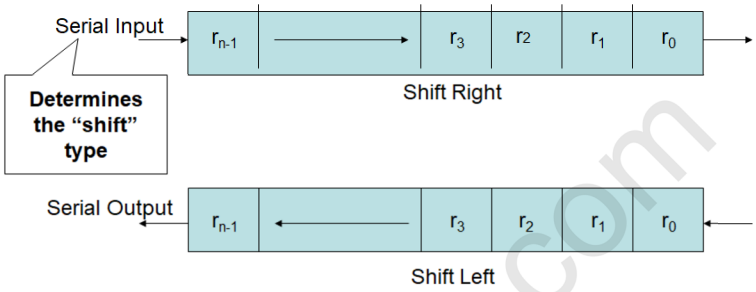
28. Explain logical, circular and arithmetic shift operations with example.

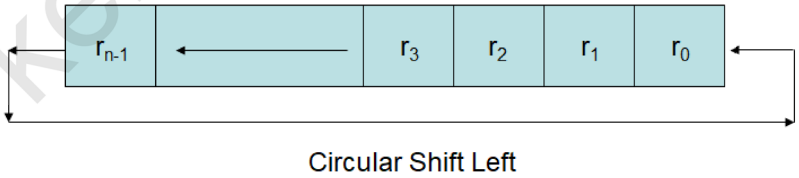
Logical Shift

- Transfers 0 through the serial input
- Logical Shift Right: R1 ← shr R1 — The same
- Logical Shift Left: R2 ← shl R2 — The same



Circular Shift

- Circulates the bits of the register around the two ends without loss of information
- Circular Shift Right: R1 ← cir R1 — The same
- Circular Shift Left: R2 ← cil R2 — The same



Arithmetic Shift

It is also called signed shift**.** When shifting right with an **arithmetic right shift**, the least-significant bit is lost and the most-significant bit is *copied*.

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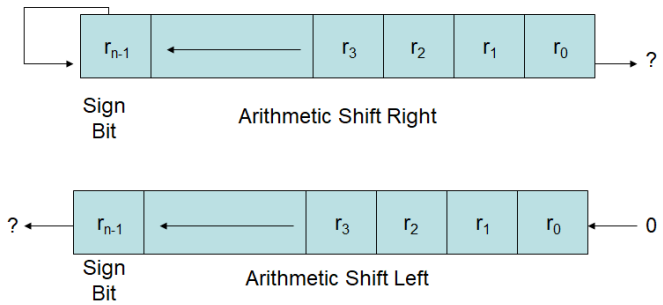


29. Describe various processor organization methods.

Different Processor Organization are:-

a. Bus Organization

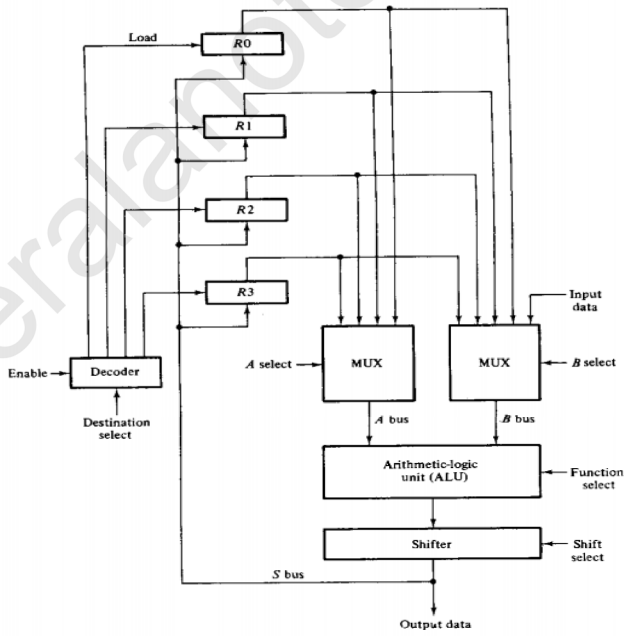
b. Scratchpad Memory

c. Processor with 2-port memory

d. Accumulator Register

Bus Organization

When a large number of registers are included in a processor, it is the most efficient way to connect them through common buses.



- Register connected to two MUX to form input buses A and B.
- The selection lines of each MUX select one register for the particular bus.
- The A and B buses are applied to a common ALU.

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- The function selected in the ALU determines the particular operation that is to be performed.
- The shift micro-operations are implemented in the shifter.
- The result of the micro-operation goes through the output bus S into the inputs of all registers.
- The destination register that receives the information from the output bus is selected by a decoder.
- When enabled, this decoder activates one of the register load inputs to provide a transfer path between the data on the S bus and the inputs of the selected destination register.
- The output bus S provides the terminals for transferring data to an external destination.
- One input of MUX A or B can receive data from the outside
- The control unit that supervises the processor bus system directs the information flow through the ALU by selecting the various components in the unit.

Scratch pad memory

- The register in a processor unit can be enclosed in a small memory unit.
- When included in a processor unit,a small memory is sometime called a scratchpad memory.
- The use of a small memory is a cheaper alternative to collecting processor registers through a bus system.
- The difference between the two system is the manner in which information is selected for transfer into the ALU

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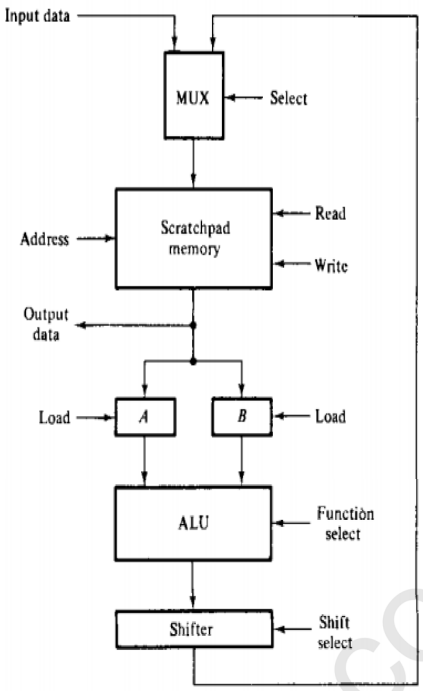
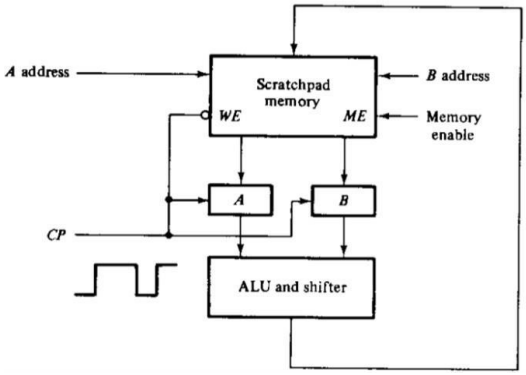


- Resource register is selected from memory and loaded into register A.
- A Second source register is selected from memory and loaded into register B.
- The information in A and B is manipulated in the ALU and shifter.
- Result of the operation is transferred to a memory register specifying its word address and activating the memory-write input control.
- Assume that the memory has eight words, so that an address must be specified with three bits.

Processor with 2- port memory



- Some processor employ a 2 port memory in order to **overcome the delay caused when reading two source registers**. A 2-port has two separate address lines to select two

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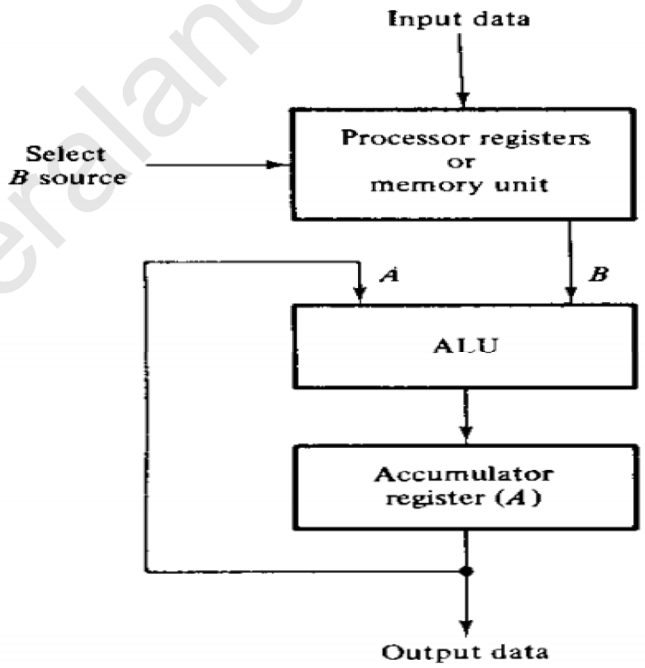
words of memory simultaneously. The organization of a processor unit with a 2-port scratchpad memory is shown in figure above.

- In this way the two source register can be read at the same time.
- Memory has 2 sets of addresses. One for port A and the other for Port B.Data from any word in the memory are read into the register A by specifying an A address . Likewise data from any word in memory are read into B register by specifying a B address. The same address can be applied to the A address and B address.
- When enabled by the Memory Enable (ME) input, new data can be written into the word specified byb the B address. Thus the A and B addresses specify two source registers simultaneously and the B address always specifies the destination register.
- A and B registers are latches that accepts new information as the clock pulse CP is in 1 -state . When CP goes to 0, the latches are disabled and hold the information that was stored when CP was 1.

Processor with Accumulator register

Accumulator is the intermediate storage of arithmetic and logic data in a computer's CPU



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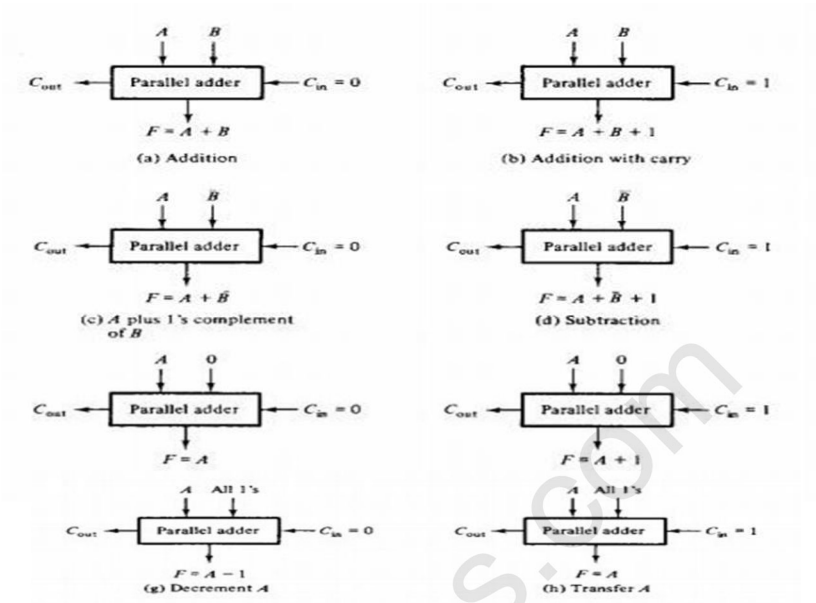
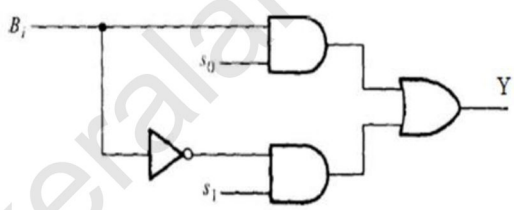
30. Describe the design of Arithmetic circuit

8 arithmetic operations acan be described in the following figure



By changing the B input and C_{in} we get 8 operaton. So the input B is applied in four different form by using following circuit.



S1	S0	Y
0	0	0
0	1	B
1	0	B'
1	1	1

Y=S0Bi+S1Bi'

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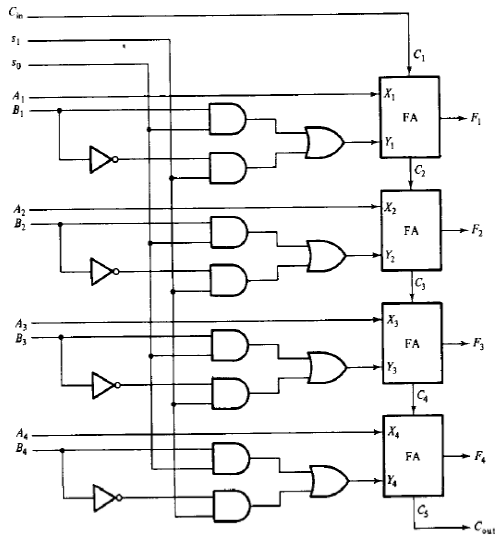

Function select			Y equals	Output equals	Function
s_1	s_0	C_{in}			
0	0	0	0	$F = A$	Transfer A
0	0	1	0	$F = A + 1$	Increment A
0	1	0	B	$F = A + B$	Add B to A
0	1	1	B	$F = A + B + 1$	Add B to A plus 1
1	0	0	$\bar{B}$	$F = A + \bar{B}$	Add 1's complement of B to A
1	0	1	$\bar{B}$	$F = A + \bar{B} + 1$	Add 2's complement of B to A
1	1	0	All 1's	$F = A - 1$	Decrement A
1	1	1	All 1's	$F = A$	Transfer A

31. Explain the design of logic circuit

16 logic operations can be generated in one circuit and selected by means of four selection lines.

Can be obtained by means of AND, OR, and NOT (complement) operations

For three operations, we need two selection variables

But two selection lines can select among four logic operations, so we choose also the exclusive-OR (XOR) function for the logic circuit to be designed

The diagram(next slide) shows one typical stage designated by subscript i. The circuit must be repeated n times for an n-bit logic circuit

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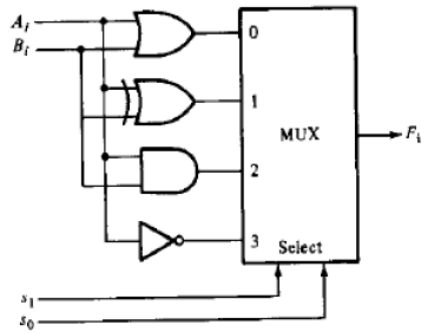


s_1	s_0	Output	Operation
0	0	$F_i = A_i + B_i$	OR
0	1	$F_i = A_i \oplus B_i$	XOR
1	0	$F_i = A_i B_i$	AND
1	1	$F_i = A_i'$	NOT

32. Give the function table and design of ALU

Function table

Selection				Output	Function
s_2	s_1	s_0	C_{in}		
0	0	0	0	$F = A$	Transfer A
0	0	0	1	$F = A + 1$	Increment A
0	0	1	0	$F = A + B$	Addition
0	0	1	1	$F = A + B + 1$	Add with carry
0	1	0	0	$F = A - B - 1$	Subtract with borrow
0	1	0	1	$F = A - B$	Subtraction
0	1	1	0	$F = A - 1$	Decrement A
0	1	1	1	$F = A$	Transfer A
1	0	0	X	$F = A \vee B$	OR
1	0	1	X	$F = A \oplus B$	XOR
1	1	0	X	$F = A \wedge B$	AND
1	1	1	X	$F = \bar{A}$	Complement A

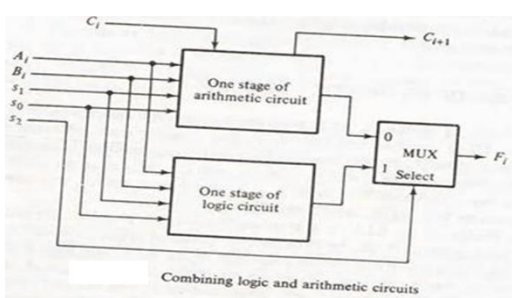
Design steps

1. Design the arithmetic section independent of the logic section.

2. Determine the logic operations obtained from the arithmetic circuit in step 1, assuming that the input carries to all stages are 0.

3. Modify the arithmetic circuit to obtain the required logic operations.

One bit ALU design



Combining logic and arithmetic circuits

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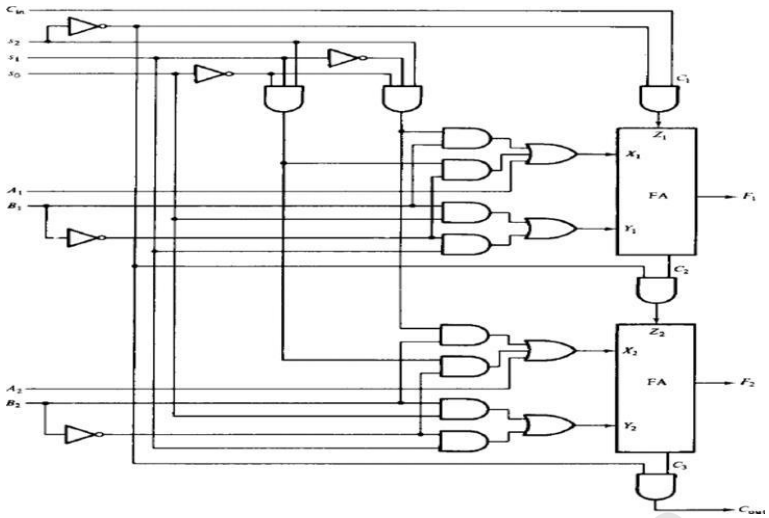
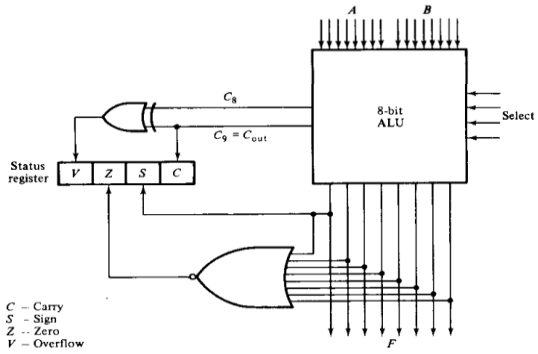


33. Implement the status register. Give its design and function table.

Status register is a 4 bit register. The four bits are C (carry), Z (zero),S (sign) and V (overflow).These bits are set or cleared as a result of an operation performed in the ALU.

- Bit C is set if the output carry of an ALU is 1.
- Bit S is set to 1 if the highest order bit of the result in the output of the ALU is 1.
- Bit Z is set to 1 if the output of the ALU contains all O's.
- Bit V is set if the exclusive —OR of carries C8 and C9 is 1, and cleared otherwise. This is the condition for overflow when the numbers are in signed 2's complement representation. For an 8 bit ALU, V is set if the result is greater than 127 or less than -128.



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Relation	Condition of status bits	Boolean function
$A > B$	$C = 1$ and $Z = 0$	CZ'
$A \geq B$	$C = 1$	C
$A < B$	$C = 0$	C'
$A \leq B$	$C = 0$ or $Z = 1$	$C' + Z$
$A = B$	$Z = 1$	Z
$A \neq B$	$Z = 0$	Z'

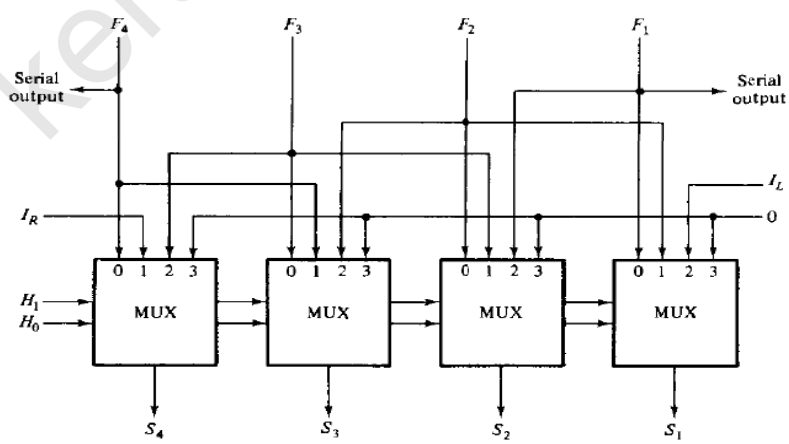
34. Explain the Design of a logic shifter circuit with diagram and function table.

Shifter may function in four different ways.

1. The shifter may transfer the information directly without a shift.
2. The shifter may shift the information to the right.
3. The shifter may shift the information to the left.
4. In some cases no transfer is made from ALU to the output bus.

Shifter operation can be selected by two variables H1 H0

- If H1 H0 = 0 0 No shift is executed and the signal from F go directly to S lines
- If H1 H0 = 0 1 Shift Right is executed
- If H1 H0 = 1 0 Shift Left is executed
- If H1 H0 = 1 1 No operations



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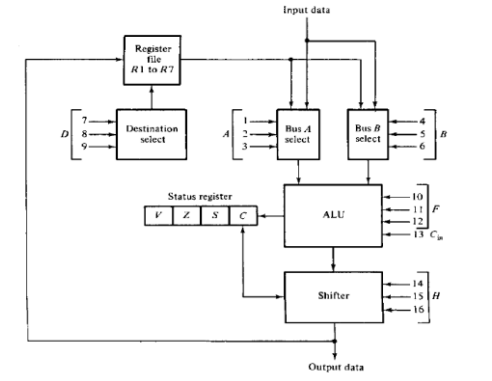
H1	H2	Operation	Function
0	0	S<--F	Transfer F to S
0	1	S←Shr F	Shift right F into S
1	0	S← Shl F	Shift left F into S
1	1	S←0	Transfer 0 into S

35. Design the complete Processor Unit

- The 3-bit binary code listed in the table specifies the code for each of the five fields A, B, D, input data, F, and H.
- The register selected by A, B, and D is the one whose decimal number is equivalent to the binary number in the code.
- When the A or B field is 000, the corresponding multiplexer selects the input data.
- When D = 000, no destination register is selected.
- The three bits in the F field, together with the input carry Cin, provide the 12 operations of the ALU
- There are two possibilities for F = A.
    - Carry bit C is cleared,
    - Carry bit C is set to 1.



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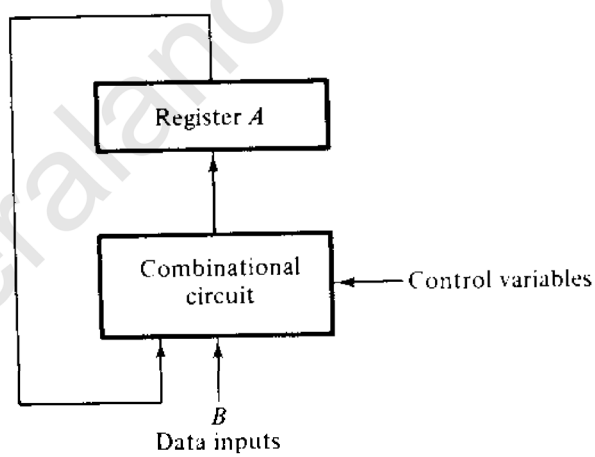
Binary code	Function of selection variables					
	A	B	D	F with $C_{in} = 0$	F with $C_{in} = 1$	H
0 0 0	Input data	Input data	None	$A, C \leftarrow 0$	$A + 1$	No shift
0 0 1	$R1$	$R1$	$R1$	$A + B$	$A + B + 1$	Shift-right, $I_R = 0$
0 1 0	$R2$	$R2$	$R2$	$A - B - 1$	$A - B$	Shift-left, $I_L = 0$
0 1 1	$R3$	$R3$	$R3$	$A - 1$	$A, C \leftarrow 1$	0's to output bus
1 0 0	$R4$	$R4$	$R4$	$A \vee B$	—	—
1 0 1	$R5$	$R5$	$R5$	$A \oplus B$	—	Circulate-right with C
1 1 0	$R6$	$R6$	$R6$	$A \wedge B$	—	Circulate-left with C
1 1 1	$R7$	$R7$	$R7$	$\bar{A}$	—	—

36. Explain the Design of accumulator

- Accumulator refers to both the A register and its associated combinational circuit.
- The external inputs to the accumulator are the data inputs from B and the control variables that determine the micro operations for the register.
- The next state of register A is a function of its present state and of the external inputs.
- Accumulator can also perform data processing operations.



Control variable	Microoperation	Name
p_1	$A \leftarrow A + B$	Add
p_2	$A \leftarrow 0$	Clear
p_3	$A \leftarrow \bar{A}$	Complement
p_4	$A \leftarrow A \wedge B$	AND
p_5	$A \leftarrow A \vee B$	OR
p_6	$A \leftarrow A \oplus B$	Exclusive-OR
p_7	$A \leftarrow \text{shr } A$	Shift-right
p_8	$A \leftarrow \text{shl } A$	Shift-left
p_9	$A \leftarrow A + 1$	Increment
	If $(A = 0)$ then $(Z = 1)$	Check for zero

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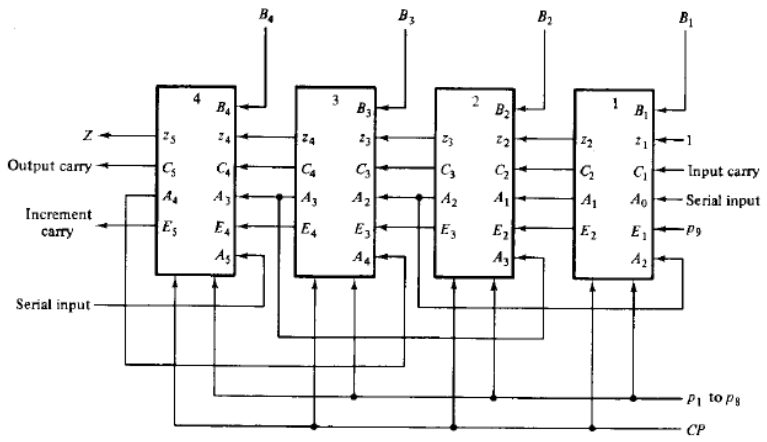

- The inputs and outputs of each stage can be connected in cascade to form a complete accumulator.
- The number on top of each block represents the bit position.
- All blocks receive 8 control variables P1 to P8 and the clock pulses from CP.
- The other six inputs and four outputs are same as with the typical stage.
- The zero detect chain is obtained by connecting the z variables in cascade, with the first block receiving a binary constant I .
- The last stage produces the zero detect variable Z.
- Total number of terminals in the 4 bit accumulator is 25, including terminals for the A outputs.
- Incorporating two more terminals for power supply, the circuit can be enclosed within one IC package having 27 or 28 pins.
- The number of terminals for the control variable can be reduced from 9 to 4 if a decoder is inserted in the IC.
- In such cases, IC pin count is also reduced to 22 and the accumulator can be extended to 16 microoperations without adding external pins (That is, with 4 bits we can identify 16 operations).

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