PHYS 605 Lab #9

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I. INTRODUCTION AND THEORY

A. Purpose

The goal was to build a 4-bit shift register using D flip-flops. This required application of logic concepts to understand the behavior of the D flip-flop.

B. Background / Theory

A set-reset flip-flop is made up of two NOR ("not or") gates whose output and inputs are connected as shown in figure (1).

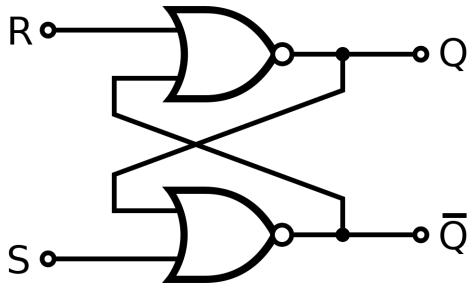

FIG. 1: A set-reset flip-flop.

The output of the set-reset flip-flop is low when S=0 and R=1, and high when S=1 and R=0. When its inputs are not opposite, its behavior is undefined. The SR flip-flop's truth table is shown below.

S	R	Q
0	0	X
0	1	0
1	0	1

A 555 timer is a device which produces timing pulses. The frequency of these pulses depend on the resistor values, R_a and R_b, and capacitor value, C.

$$f = \frac{1.4}{C(R_a + 2R_b)} \tag{1}$$

A D flip-flop, shown in figure (2), takes the data line at its D terminal, and a clock input at the CLK terminal. Internally, it is made up of two gated set-reset flip-flops. These gates enable the SR flip-flop only when E is high. In the D flip-flop, the clock input is what is connected

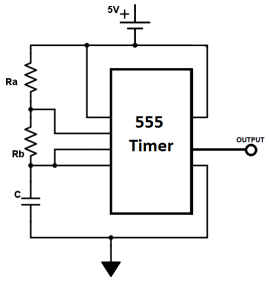

FIG. 2: The schematic of the 555 timer built for the lab.

to the second E, and the first takes E after it has gone through an inverter. This means that when the clock is low, the first SR flip-flop is enabled, and when the clock is high, the second SR flip-flop is enabled. The data line should be bits, so the D input will be either low or high. S1 takes D directly, and R1 takes D after it is inverted. This means that its output will always be 0 at one terminal and 1 at the other (as its terminals are "Q" and "not Q"). This means that the inputs to the second SR flip-flop will also be 0 at one terminal and 1 at the other. This is important because it ensures that the output of the SR flip-flops will have predictable output.

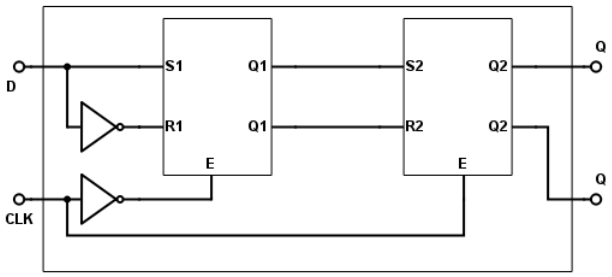

FIG. 3: Detailed view of a D flip-flop.

D	CLK	Q
0	rising edge	0
1	rising edge	1

A shift resistor is a circuit that propagates bits in support of memory management. It takes data in at one terminal, and shifts one bit on each clock pulse that is input to the other terminal. It is constructed by cascading flip-flops so that the output of one flip-flop is the

input of the next flip-flop. All are connected to the same clock.

A 4-bit shift register is made up of four flip-flops, as shown in figure (4).

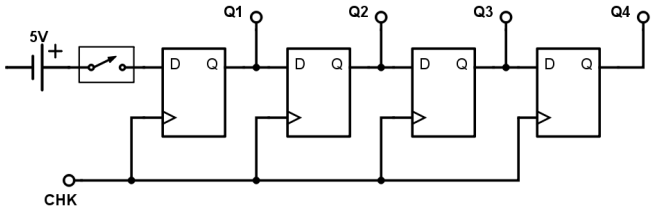

FIG. 4: The shift register schematic.

This kind of shift register is known as serial-in, parallel-out (SIPO), because the bits are provided in serial through the data line D, and then are pushed through the shift register one step at a time on each clock pulse. This means that after four clock pulses, four bits will have been loaded: one for each output Q. The information is then available in parallel.

II. METHODOLOGY

1. Using equation (1), select resistor and capacitor values that will create a frequency that makes the circuit behavior easy to observe.
2. Set up 555 timer.
3. Construct the shift registor circuit as shown in figure (2).
4. Connect an LED to each output Q.
5. Using the switch to change the input to the circuit and observe the behavior of the LEDS.

III. RESULTS AND ANALYSIS

In setting up the 555 timer, R_a was chosen to be 35.18kΩ, R_b was chosen to be 677kΩ, and C was chosen to be 0.947μF. Using equation (1), this gave an expected frequency of 1.98Hz.

$$\begin{aligned} f_{expected} &= \frac{1.4}{C(R_a + 2R_b)} \\ &= \frac{1.4}{0.947 \times 10^{-6}(35.18 \times 10^3 + 2(677 \times 10^3)} \\ &= 1.98Hz \end{aligned}$$

This was effective, as the clock pulses were slow enough that they were easy to observe.

When the "data" was given to the circuit by flipping the switch to provide the 5V input, the LED at Q1 lit up, followed by the LED at Q2, then Q3, then Q4; when Q4 lit up all four LEDs were lit. When the switch was opened so that no voltage was provided to the input D, the LED at Q4 dimmed first, then Q3, then Q2, and finally Q1.

This behavior was what was expected, as the bit register should push the bit forward a step on each clock pulse.

IV. CONCLUSION

The shift register was built successfully. The LEDs at each output lit as the "bit" was pushed through, then turned off one at a time beginning with Q4 and ending with Q1.