Evgeny Manzhosov

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CONTACT INFORMATION

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RESEARCH INTERESTS

I am interested in finding low-overhead solutions that secure computing systems, especially if those solutions require system design with multiple objectives in mind, e.g., reliability and security. In broad terms, I am interested in hardware security, computer architecture, hardware-software co-design (e.g., compiler-assisted), and power optimization.

EDUCATION

Fu Foundation School of Engineering and Applied Science, Columbia University, New York, NY, USA — 03/2019–*present*

- Ph.D. Candidate in Computer Science.
- Advisor: Prof. Simha Sethumadhavan.
- GPA: **4.04/4.00**

Fu Foundation School of Engineering and Applied Science, Columbia University, New York, NY, USA — 02/2023

- M.Phil. in Computer Science.

Fu Foundation School of Engineering and Applied Science, Columbia University, New York, NY, USA — 09/2017–02/2019

- M.Sc. in Electrical Engineering.
- Advisor: Prof. Keren Bergman.
- GPA: **4.05/4.00**.

Technion - Israel Institute of Technology, Haifa, Israel. — 10/2008–07/2014

- B.Sc. Electrical Engineering and B.Sc. Physics.
- GPA: **89.5/100**.

HONORS AND AWARDS

- My paper was selected as **Top Pick for the IEEE Micro Top Picks** — 01/2023
- **Winner** of **Qualcomm Innovation Fellowship** with proposal "Practical Security for Heterogeneous Systems". — 08/2020
- **Winner** of **RSA Security Scholar Pitch Off**. — 02/2020
- **Master of Science Award of Excellence**. — 02/2019

RESEARCH EXPERIENCE

Graduate Projects at Columbia University

- **MUSE ECC**: a novel error correction code designed to encode the metadata along with the data while providing ChipKill-level error correction over standard memory interfaces (DDR4, DDR5). For this project, I implemented in Verilog custom low latency (1-2 clock cycles), non-pipelined multipliers, and modulo units for 64 to 160-bit words. In addition, I implemented all the test benches in SystemVerilog, code profiling algorithms in C++, and modified the GEM5 simulator to support variable latency penalty on the memory interface to emulate the impact of ECC. — 2020-2022
- **NoFAT**: a novel technique to enable metadata-less memory bounds checks to ensure spatial and temporal memory safety. The NoFAT is built upon binning memory allocators. Hence, with NoFAT we are able to derive base-and-bounds for each object implicitly. To lower the overheads, we implemented custom hardware units to speed up the derivation of the base address for each dereferenced pointer. We use this address later to look up the size of the memory allocation and to determine the upper bound of the object in memory. — 2020-2021

- **ZeRO**: a novel technique to ensure pointer integrity with zero performance cost. In ZeRO, pointers are loaded/stored with special instructions and protected in caches with specially encoded metadata. 2020-2021
- **Name Confusion Architectures**: a novel mitigation for code-reuse attacks in resource-constrained devices (for example, IoT devices) using minimal micro-architectural adjustments and no software changes. For this project, I implemented micro-architectural changes required by the technique to the branch predictors and various pipeline stages of the Out-Of-Order CPU model in the GEM5 architectural simulator. 2019
- **Tapless Calibration Method**: a new calibration method for silicon photonics switches based on the MZI elements. This method, unlike prior work, does not require tapping the switches to monitor the power. Instead, we leverage the photo-conductance effect to both control and calibrate the switch elements. 2018

Undergraduate Projects at the Technion

- Investigating Zero-Temperature Coefficient behavior of CMOS-SOI devices. 2012-2013

Technical Skills

- **Programming Languages**: Rust, C/C++, Python, Tcl, PHP, Google OR-tools
- **HDL Languages**: Verilog, SystemVerilog, VHDL, SystemC
- **EDA Tools**: Synopsys: DC, ICC, ICC2, PrimeTime; Apache Redhawk; Cadence Virtuoso, Innovus; Xilinx Vivado
- **Compilers**: Clang/LLVM
- **ISA**: X86 and ARM assembly
- **Simulation Software**: MATLAB, Gem5, BookSim, ChampSim

Work Experience

- **Graduate Research Assistant** 02/2019–present
  Computer Architecture and Security Technologies Lab (CASTL)
  Department of Computer Science, Columbia University
  - [**CSEE 4824**] Computer Architecture, Teaching Assistant Fall 2021
  - [**COMS 6424**] Hardware Security, Teaching Assistant Spring 2021

- **Intern at Technology and Research Group** 05/2022–08/2022
  Office of the CTO, Microsoft, Redmond, WA, USA
  Reliability and scheduling of distributed AI jobs.

- **Graduate Research Assistant, Lightwave Research Laboratory** 09/2017–02/2019
  Department of Electrical Engineering, Columbia University
  - [**ELEN E3701**] Intro to Communication Systems, Teaching Assistant Spring 2018

- **Senior Physical Design Engineer** 05/2016–08/2017
  Cisco Inc., Caesarea, Israel

  1. I implemented critical path blocks with >10M cells, blocks with HBM2 PHY interfaces, and custom clock structures using ICC2 abstraction flow (divide design to sub-designs and top), Primetime Hyperscale flow, Apache Redhawk DMP flow.

  2. I developed from scratch a web-based system to monitor and collect the results for Place-and-Route runs. This system allowed engineers to track the impact of design changes on various metrics (e.g., timing closure, DRC errors, and others), compare design versions and create weekly reports in two clicks. Team leaders and management could monitor and track the status of chip implementation convergence in real-time.

  3. I mentored newly recruited engineers – walk-through Place-and-Route design implementation flows, helped to debug the designs, etc.

- **Physical Design Engineer** 03/2013–05/2016
  Apple Inc., Haifa, Israel

  During my time at Apple I was responsible for the following at the same time:

1. I implemented (RTL2GDS) low power and high std cell count designs with multiple voltage domains and clock domain crossings – floorplanning, placement, clock tree synthesis, timing closure, DRC/LVS clean up, formal verification, etc.

2. In addition, on a day-to-day basis, I was developing and supporting project Place-and-Route flows for the top and block levels. It included things such as power grid flow scripts, power switch and tap insertion flows for multi-voltage area designs, running regressions to validate flow stability, and helping team members with flow-related issues.

3. At last, I was responsible for Full Chip Power Delivery Analysis using Apache Redhawk suite. I was running Static/Dynamic IR Drop analysis, resolving full-chip, integration, and block-level issues, and support of partition owners.

- **Part Time Physical Design Engineer** 07/2011–03/2013
  Intel Inc., Haifa, Israel

  I set up and maintained simulation environments for Apache RedHawk: simulations scripts, scenarios, post-processing. In addition, I did Static IR Drop, Dynamic IR Drop, and Power-UP simulations on a block/full-chip level.

Conference Publications

1. **Manzhosov, E.**, Hastings, A., Pancholi, M., Piersma, R., Tarek Ibn Ziad, M., and Sethumadhavan, S., 2022, October. "Revisiting Residue Codes for Modern Memories". *2022 55th IEEE/ACM International Symposium on Microarchitecture (MICRO)*, 2022, pp. 73-90. **Top Pick in IEEE Micro Top Picks 2023.**
2. **Tarek Ibn Ziad, M., Arroyo, M.A., Manzhosov, E., Kemerlis, V.P., and Sethumadhavan, S., 2021, September. "WiP: Securing Resource-Constrained Processors with Name Confusion". In** *2021 IEEE Symposium on Secure and Private Execution Environment Design* **(SEED).**
3. **Tarek Ibn Ziad, M., Arroyo, M.A., Manzhosov, E., Kemerlis, V.P., and Sethumadhavan, S., 2021, September. "EPI: Efficient Pointer Integrity For Securing Embedded Systems". In** *2021 IEEE Symposium on Secure and Private Execution Environment Design* **(SEED).**
4. **Tarek Ibn Ziad, M., Arroyo, M.A., Manzhosov, E., Piersma, R. and Sethumadhavan, S., 2021, June. "No-FAT: Architectural support for low overhead memory safety checks". In** *2021 ACM/IEEE 48th Annual International Symposium on Computer Architecture* **(ISCA) (pp. 916-929). IEEE.**
5. **Tarek Ibn Ziad, M., Arroyo, M.A., Manzhosov, E. and Sethumadhavan, S., 2021, June. "ZeRØ: Zero-overhead resilient operation under pointer integrity attacks". In** *2021 ACM/IEEE 48th Annual International Symposium on Computer Architecture* **(ISCA) (pp. 999-1012). IEEE.**
6. **Abrams, N.C., Cheng, Q., Glick, M., Manzhosov, E., Jezzini, M., Morrissey, P., O'Brien, P. and Bergman, K., 2020. "Design considerations for multi-chip module silicon-photonic transceivers".** *In Metro and Data Center Optical Networks and Short-Reach Links III* **(Vol. 11308, p. 113080I). International Society for Optics and Photonics.**
7. **Gazman, A., Manzhosov, E., Bahadori, M., Anderson, E., Zhu, Z., Shen, Y. and Bergman, K., 2018, September. "Topology Agnostic Solution for Tapless Calibration of Silicon Photonic Mach-Zehnder Based Switches". In** *2018 European Conference on Optical Communication* **(ECOC) (pp. 1-3). IEEE.**
8. **Malits, M., Svetlitza, A., Manzhosov, E., Rotman, N. and Nemirovsky, Y., 2012, November. "The influence of thermoelectric effects on the self-heating of nanometer CMOS-SOI devices". In 2012 IEEE 27th Convention of Electrical and Electronics Engineers in Israel (pp. 1-5). IEEE.**

Journal Publications

1. Shen, Y., Meng, X., Cheng, Q., Rumley, S., Abrams, N., Gazman, A., **Manzhosov, E.**, Glick, M.S. and Bergman, K., 2019. "Silicon photonics for extreme scale systems". *Journal of Lightwave Technology*, 37(2), pp.245-259.
2. Gazman, A., **Manzhosov, E.**, Browning, C., Bahadori, M., London, Y., Barry, L. and Bergman, K., 2018. "Tapless and topology agnostic calibration solution for silicon photonic switches". *Optics express*, 26(25), pp.32662-32674.