

Example for \$readmemh



project\_2 - [C:/Users/ytian/project\_2/project\_2.xpr] - Vivado 2016.2

File Edit Flow Tools Window Layout View Run Help

Default Layout

Flow Navigator

#### Project Manager

- Project Settings
- Add Sources
- Language Templates
- IP Catalog

#### IP Integrator

- Create Block Design
- Open Block Design
- Generate Block Design

#### Simulation

- Simulation Settings
- Run Simulation

#### RTL Analysis

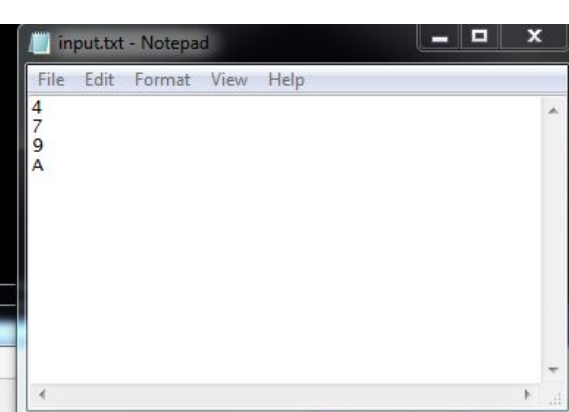
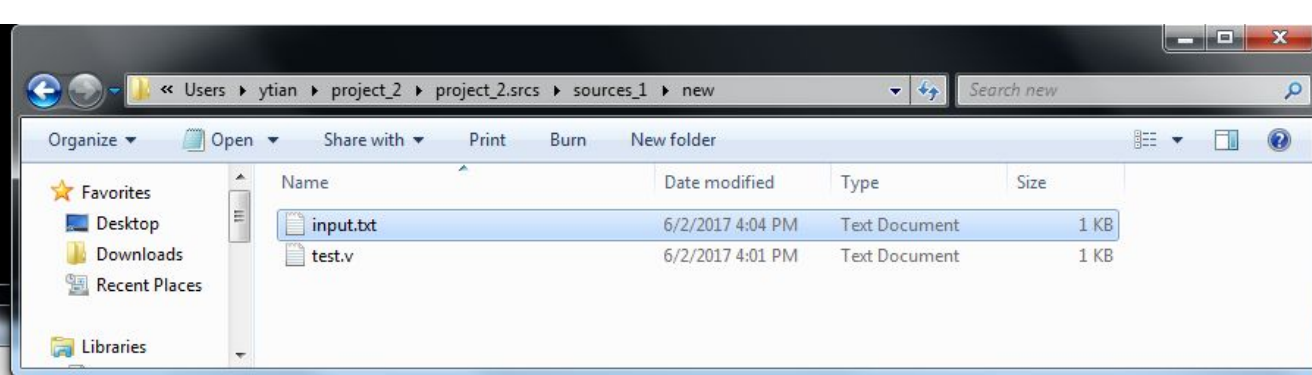
- Elaboration Settings
- Open Elaborated Design

#### Synthesis

- Synthesis Settings
- Run Synthesis
- Open Synthesized Design

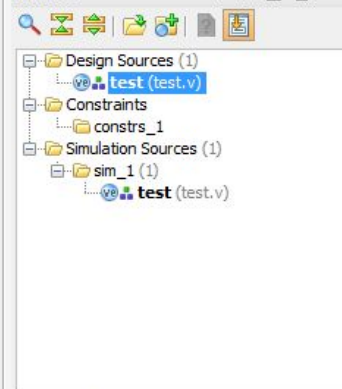
#### Implementation

- Implementation Settings
- Run Implementation
- Open Implemented Design



Behavioral Simulation - Functional - sim\_1 - test

Sources



Objects

Name	Value	Data Type
mem[0:3][7:0]	04,07,09,0a	Array
[0][7:0]	04	Array
[1][7:0]	07	Array
[2][7:0]	09	Array
[3][7:0]	0a	Array
i[31:0]	4	Array

Hierarchy Libraries Compile Order

Scope Sources

Tcl Console

```
# }
# run 1000ns
04
07
09
0a
INFO: [USF-XSim-96] XSim completed. Design snapshot 'test_beh'
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
```

Type a Tcl command here

Tcl Console Messages Log

test.v x

C:/Users/ytian/project\_2/project\_2.srscs/sources\_1/new/test.v

```
22
23 module test(
24
25 );
26 reg [7:0] mem[0:3];
27 integer i;
28 initial begin
29     $readmemh("c:/Users/ytian/project_2/project_2.srscs/sources_1/new/input.txt", mem);
30     for (i=0; i<4; i=i+1) begin
31         #10
32         $display("%h", mem[i]);
33     end
34 end
35 endmodule
36
```

Untitled 11

