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DS90LV031ATM/NOPB

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DS90LV031A 3V LVDS Quad CMOS Differential Line Driver

Check for Samples: DS90LV031A

FEATURES

- **>400 Mbps (200 MHz) switching rates**
- **0.1 ns typical differential skew**
- **0.4 ns maximum differential skew**
- **2.0 ns maximum propagation delay**
- **3.3V power supply design**
- **±350 mV differential signaling**
- **Low power dissipation (13mW at 3.3V static)**
- **Interoperable with existing 5V LVDS devices**
- **Compatible with IEEE 1596.3 SCI LVDS standard**
- **Compatible with TIA/EIA-644 LVDS standard**
- **Industrial operating temperature range**
- **Available in SOIC and TSSOP surface mount packaging**

DESCRIPTION

The DS90LV031A is a quad CMOS differential line driver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 400 Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90LV031A accepts low voltage LVTTL/LVCMOS input levels and translates them to low voltage (350 mV) differential output signals. In addition the driver supports a TRI-STATE® function that may be used to disable the output stage, disabling the load current, and thus dropping the device to an ultra low idle power state of 13 mW typical.

The EN and EN* inputs allow active Low or active High control of the TRI-STATE outputs. The enables are common to all four drivers. The DS90LV031A and companion line receiver (DS90LV032A) provide a new alternative to high power psuedo-ECL devices for high speed point-to-point interface applications.

Connection Diagram

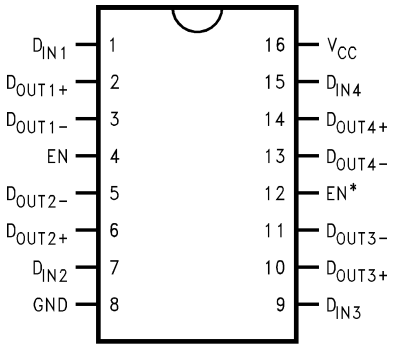

Figure 1. Dual-In-Line
See Package Number D (R-PDSO-G16) or PW (R-PDSO-G16)

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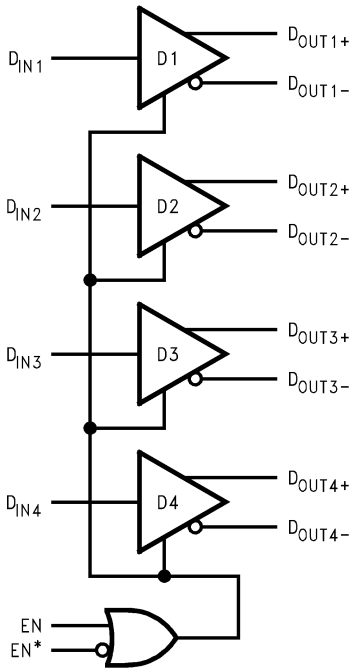
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Functional Diagram



Truth Table

Enables		Input	Outputs	
EN	**EN***	**D_{IN}**	**D_{OUT+}**	**D_{OUT-}**
L	H	X	Z	Z
All other combinations of ENABLE inputs		L	L	H
		H	H	L

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Supply Voltage (V_{CC})	−0.3V to +4V
Input Voltage (D_{IN})	−0.3V to (V_{CC} + 0.3V)
Enable Input Voltage (EN, EN*)	−0.3V to (V_{CC} + 0.3V)
Output Voltage (D_{OUT+}, D_{OUT-})	−0.3V to +3.9V
Short Circuit Duration	
(D_{OUT+}, D_{OUT-})	Continuous
Maximum Package Power Dissipation @ +25°C	
D Package	1088 mW
PW Package	866 mW
Derate D Package	8.5 mW/°C above +25°C
Derate PW Package	6.9 mW/°C above +25°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range	
Soldering (4 sec.)	+260°C
Maximum Junction Temperature	+150°C
ESD Rating (2)	
(HBM, 1.5 kΩ, 100 pF)	≥ 6 kV

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. Electrical Characteristics specifies conditions of device operation.
(2) ESD Ratings:
HBM (1.5 kΩ, 100 pF) ≥ 6 kV

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+3.0	+3.3	+3.6	V
Operating Free Air Temperature (T_A)				
Industrial	−40	+25	+85	°C

Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified. (1) (2) (3)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
V_{OD1}	Differential Output Voltage	R_L = 100Ω (Figure 2)	D_{OUT-} D_{OUT+}	250	350	450	mV
ΔV_{OD1}	Change in Magnitude of V_{OD1} for Complementary Output States				4	35	|mV|
V_{OS}	Offset Voltage			1.125	1.25	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States				5	25	|mV|
V_{OH}	Output Voltage High				1.38	1.6	V
V_{OL}	Output Voltage Low			0.90	1.03		V
V_{IH}	Input Voltage High		D_{IN}, EN, EN*	2.0		V_{CC}	V
V_{IL}	Input Voltage Low			GND		0.8	V
I_{IH}	Input Current	V_{IN} = V_{CC} or 2.5V		−10	±1	+10	µA
I_{IL}	Input Current	V_{IN} = GND or 0.4V		−10	±1	+10	µA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−1.5	−0.8		V
I_{OS}	Output Short Circuit Current	ENABLED, (4) D_{IN} = V_{CC}, D_{OUT+} = 0V or D_{IN} = GND, D_{OUT-} = 0V	D_{OUT-} D_{OUT+}		−6.0	−9.0	mA
I_{OSD}	Differential Output Short Circuit Current	ENABLED, V_{OD} = 0V (4)			−6.0	−9.0	mA
I_{OFF}	Power-off Leakage	V_{OUT} = 0V or 3.6V, V_{CC} = 0V or Open		−20	±1	+20	µA
I_{OZ}	Output TRI-STATE Current	EN = 0.8V and EN* = 2.0V V_{OUT} = 0V or V_{CC}		−10	±1	+10	µA
I_{CC}	No Load Supply Current Drivers Enabled	D_{IN} = V_{CC} or GND	V_{CC}		5.0	8.0	mA
I_{CCL}	Loaded Supply Current Drivers Enabled	R_L = 100Ω All Channels, D_{IN} = V_{CC} or GND (all inputs)			23	30	mA
I_{CCZ}	No Load Supply Current Drivers Disabled	D_{IN} = V_{CC} or GND, EN = GND, EN* = V_{CC}			2.6	6.0	mA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except: V_{OD1} and ΔV_{OD1}.
(2) All typicals are given for: V_{CC} = +3.3V, T_A = +25°C.
(3) The DS90LV031A is a current mode device and only functions within datasheet specifications when a resistive load is applied to the driver outputs typical range is (90Ω to 110Ω)
(4) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

Switching Characteristics - Industrial

V_{CC} = +3.3V ±10%, T_A = −40°C to +85°C (1) (2) (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100Ω, C_L = 10 pF (Figure 3 and Figure 4)	0.8	1.18	2.0	ns
t_{PLHD}	Differential Propagation Delay Low to High		0.8	1.25	2.0	ns
t_{SKD1}	Differential Pulse Skew $\|t_{PHLD} - t_{PLHD}\|$ (4)		0	0.07	0.4	ns
t_{SKD2}	Channel-to-Channel Skew (5)		0	0.1	0.5	ns
t_{SKD3}	Differential Part to Part Skew (6)		0		1.0	ns
t_{SKD4}	Differential Part to Part Skew (7)		0		1.2	ns
t_{TLH}	Rise Time			0.38	1.5	ns
t_{THL}	Fall Time			0.40	1.5	ns
t_{PHZ}	Disable Time High to Z	R_L = 100Ω, C_L = 10 pF (Figure 5 and Figure 6)			5	ns
t_{PLZ}	Disable Time Low to Z				5	ns
t_{PZH}	Enable Time Z to High				7	ns
t_{PZL}	Enable Time Z to Low				7	ns
f_{MAX}	Maximum Operating Frequency (8)		200	250		MHz

(1) All typicals are given for: V_{CC} = +3.3V, T_A = +25°C.
(2) Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50Ω, t_r ≤ 1 ns, and t_f ≤ 1 ns.
(3) C_L includes probe and jig capacitance.
(4) t_{SKD1}, $|t_{PHLD} - t_{PLHD}|$ is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
(5) t_{SKD2} is the Differential Channel-to-Channel Skew of any event on the same device.
(6) t_{SKD3}, Differential Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
(7) t_{SKD4}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max − Min| differential propagation delay.
(8) f_{MAX} generator input conditions: t_r = t_f < 1ns, (0% to 100%), 50% duty cycle, 0V to 3V. Output Criteria: duty cycle = 45%/55%, VOD > 250mV, all channels switching.

Parameter Measurement Information

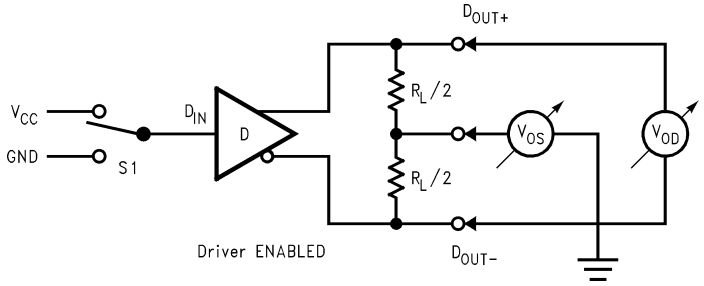


Figure 2. Driver V_{OD} and V_{OS} Test Circuit

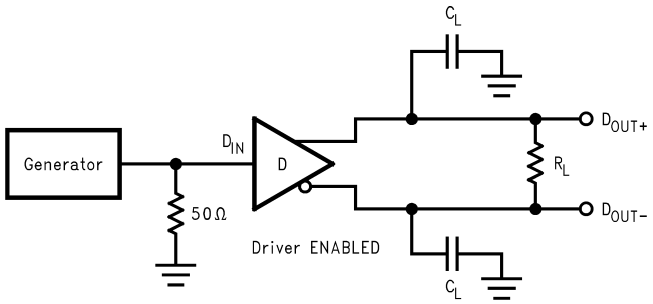


Figure 3. Driver Propagation Delay and Transition Time Test Circuit

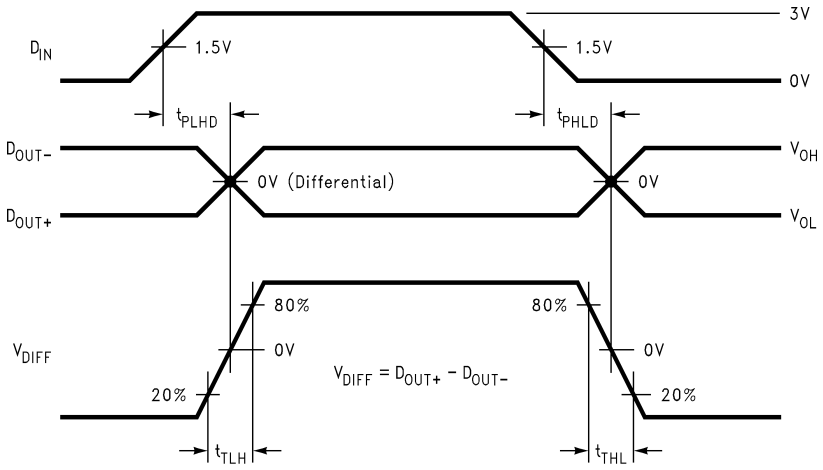


Figure 4. Driver Propagation Delay and Transition Time Waveforms

Parameter Measurement Information (continued)

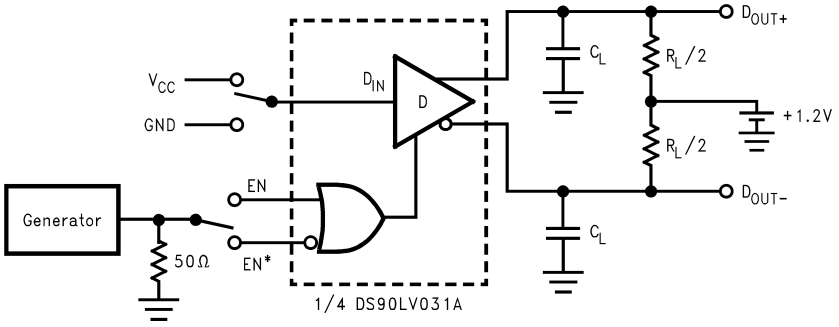


Figure 5. Driver TRI-STATE Delay Test Circuit

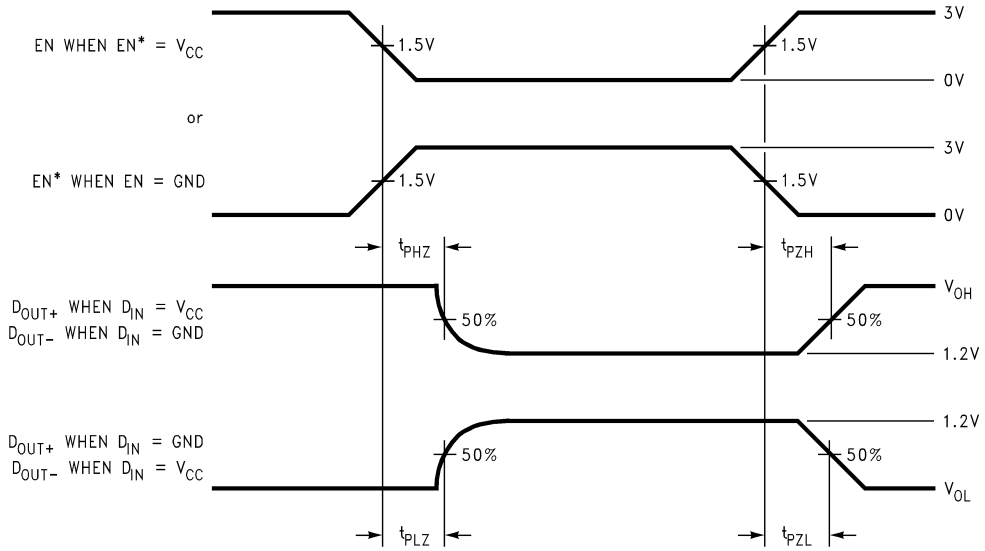


Figure 6. Driver TRI-STATE Delay Waveforms

APPLICATION INFORMATION

General application guidelines and hints for LVDS drivers and receivers may be found in the following application notes: LVDS Owner's Manual (SNLA187), AN-808 (SNLA028), AN-1035 (SNOA355), AN-977 (SNLA166), AN-971 (SNLA165), AN-916 (SNLA219), AN-805 (SNOA233), AN-903 (SNLA034).

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in Figure 8. This configuration provides a clean signaling environment for the quick edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic differential impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90LV031A differential line driver is a balanced current source design. A current mode driver, generally speaking has a high output impedance and supplies a constant current for a range of loads (a voltage mode driver on the other hand supplies a constant voltage for a range of loads). Current is switched through the load in one direction to produce a logic state and in the other direction to produce the other logic state. The output current is typically 3.5 mA, a minimum of 2.5 mA, and a maximum of 4.5 mA. The current mode **requires** (as discussed above) that a resistive termination be employed to terminate the signal and to complete the loop as shown in Figure 8. AC or unterminated configurations are not allowed. The 3.5 mA loop current will develop a differential voltage of 350 mV across the 100Ω termination resistor which the receiver detects with a 250 mV minimum differential noise margin neglecting resistive line losses (driven signal minus receiver threshold (350 mV – 100 mV = 250 mV)). The signal is centered around +1.2V (Driver Offset, V_{OS}) with respect to ground as shown in Figure 7. Note that the steady-state voltage (V_{SS}) peak-to-peak swing is twice the differential voltage (V_{OD}) and is typically 700 mV.

The current mode driver provides substantial benefits over voltage mode drivers, such as an RS-422 driver. Its quiescent current remains relatively flat versus switching frequency. Whereas the RS-422 voltage mode driver increases exponentially in most case between 20 MHz–50 MHz. This is due to the overlap current that flows between the rails of the device when the internal gates switch. Whereas the current mode driver switches a fixed current between its output without any substantial overlap current. This is similar to some ECL and PECL devices, but without the heavy static I_{CC} requirements of the ECL/PECL designs. LVDS requires > 80% less current than similar PECL devices. AC specifications for the driver are a tenfold improvement over other existing RS-422 drivers.

The TRI-STATE function allows the driver outputs to be disabled, thus obtaining an even lower power state when the transmission of data is not required.

The footprint of the DS90LV031A is the same as the industry standard 26LS31 Quad Differential (RS-422) Driver and is a step down replacement for the 5V DS90C031 Quad Driver.

Power Decoupling Recommendations

Bypass capacitors must be used on power pins. High frequency ceramic (surface mount is recommended) 0.1µF in parallel with 0.01µF, in parallel with 0.001µF at the power supply pin as well as scattered capacitors over the printed circuit board. Multiple vias should be used to connect the decoupling capacitors to the power planes. A 10µF (35V) or greater solid tantalum capacitor should be connected at the power entry point on the printed circuit board.

PC Board considerations

Use at least 4 PCB layers (top to bottom); LVDS signals, ground, power, TTL signals.

Isolate TTL signals from LVDS signals, otherwise the TTL may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by a power/ground plane(s).

Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

Differential Traces

Use controlled impedance traces which match the differential impedance of your transmission medium (ie. cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs should be < 10mm long). This will help eliminate reflections and ensure noise is coupled as common-mode. Lab experiments show that differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is greater with the closer traces. Plus, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result. (Note the velocity of propagation, v = c/Er where c (the speed of light) = 0.2997mm/ps or 0.0118 in/ps). Do not rely solely on the auto-route function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number of vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

Termination

Use a resistor which best matches the differential impedance of your transmission line. The resistor should be between 90Ω and 130Ω. Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work without resistor termination. Typically, connect a single resistor across the pair at the receiver end.

Surface mount 1% to 2% resistors are best. PCB stubs, component lead, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be < 10mm (12mm MAX).

Probing LVDS Transmission Lines

Always use high impedance (> 100kΩ), low capacitance (< 2pF) scope probes with a wide bandwidth (1GHz) scope. Improper probing will give deceiving results.

Cables and Connectors, General Comments

When choosing cable and connectors for LVDS it is important to remember:

Use controlled impedance media. The cables and connectors you use should have a matched differential impedance of about 100Ω. They should not introduce major impedance discontinuities.

Balanced cables (e.g. twisted pair) are usually better than unbalanced cables (ribbon cable, simple coax.) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common-mode (not differential mode) noise which is rejected by the receiver. For cable distances < 0.5M, most cables can be made to work effectively. For distances 0.5M ≤ d ≤ 10M, CAT 3 (category 3) twisted pair cable works well, is readily available and relatively inexpensive.

Fail-safe of an LVDS Interface

If the LVDS link as shown in Figure 8 needs to support the case where the Line Driver is disabled, powered off, or removed (un-plugged) and the Receiver device is powered on and enabled, the state of the LVDS bus is unknown and therefore the output state of the Receiver is also unknown. If this is of concern, please consult the respective LVDS Receiver data sheet for guidance on Failsafe Biasing options for the LVDS interface to set a known state on the inputs for these conditions.

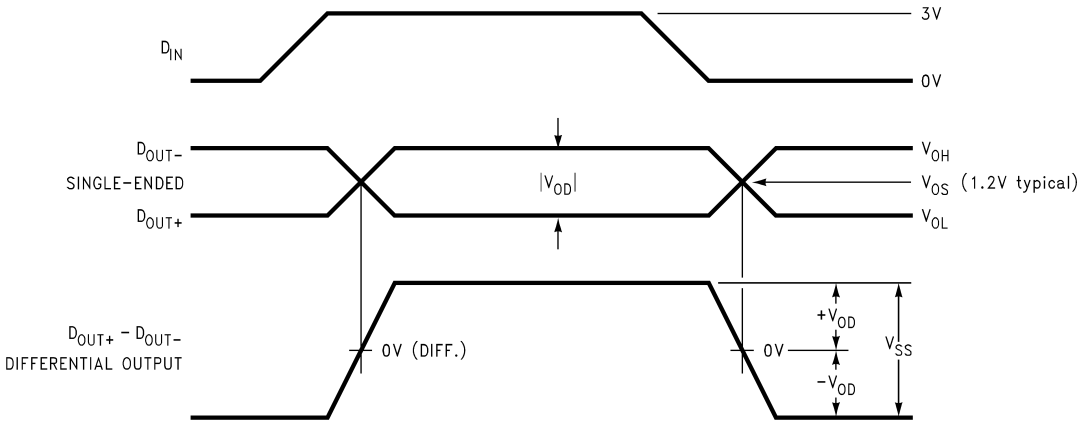


Figure 7. Driver Output Levels

TYPICAL APPLICATION

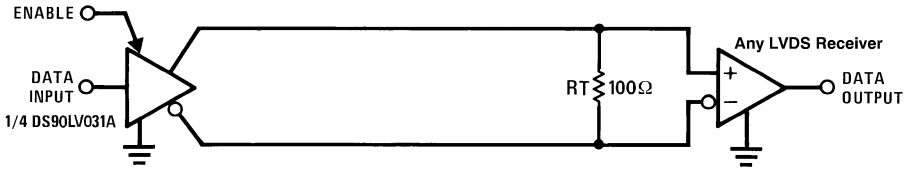


Figure 8. Point-to-Point Application

Typical Performance Curves

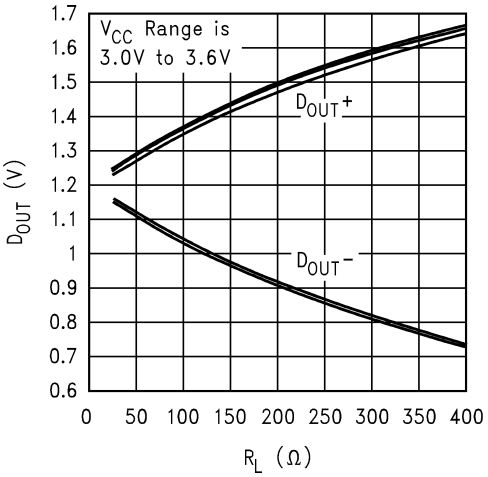


Figure 9. Typical DS90LV031A, D_{OUT} (single ended) vs R_L, T_A = 25°C

Typical Performance Curves (continued)

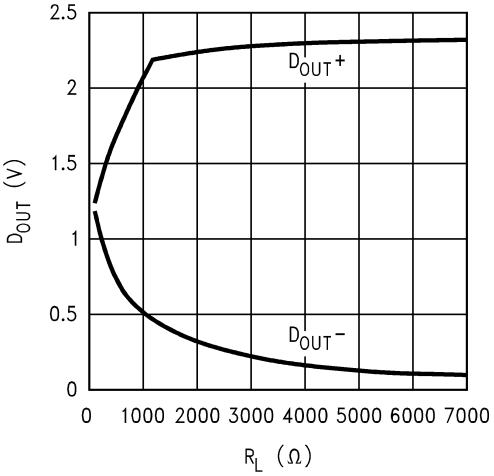


Figure 10. Typical DS90LV031A, D_{OUT} vs R_L, V_{CC} = 3.3V, T_A = 25°C

PIN DESCRIPTIONS

Pin No.	Name	Description
1, 7, 9, 15	D_{IN}	Driver input pin, TTL/CMOS compatible
2, 6, 10, 14	D_{OUT+}	Non-inverting driver output pin, LVDS levels
3, 5, 11, 13	D_{OUT-}	Inverting driver output pin, LVDS levels
4	EN	Active high enable pin, OR-ed with EN*
12	EN*	Active low enable pin, OR-ed with EN
16	V_{CC}	Power supply pin, +3.3V ± 0.3V
8	GND	Ground pin

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	11

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90LV031ATM	NRND	SOIC	D	16	48	TBD	Call TI	Call TI	-40 to 85	DS90LV031A TM	
DS90LV031ATM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS90LV031A TM	Samples
DS90LV031ATMTC	NRND	TSSOP	PW	16	92	TBD	Call TI	Call TI	-40 to 85	DS90LV 031AT	
DS90LV031ATMTC/NOPB	ACTIVE	TSSOP	PW	16	92	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS90LV 031AT	Samples
DS90LV031ATMTCX/NOPB	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS90LV 031AT	Samples
DS90LV031ATMX	NRND	SOIC	D	16	2500	TBD	Call TI	Call TI	-40 to 85	DS90LV031A TM	
DS90LV031ATMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN | Call TI	Level-1-260C-UNLIM	-40 to 85	DS90LV031A TM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

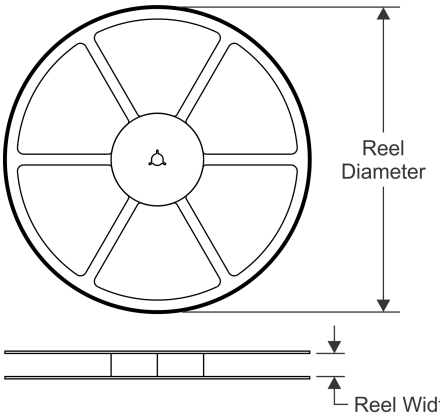
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

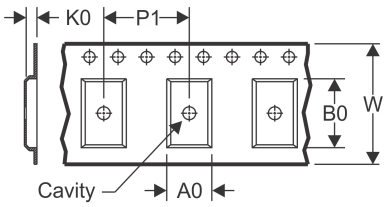
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

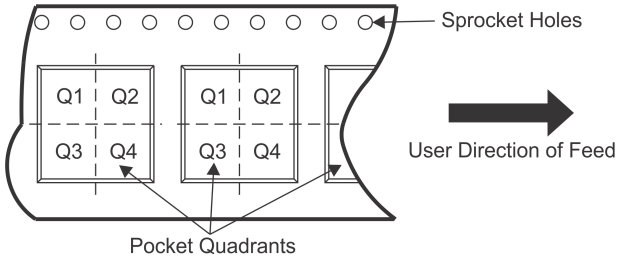


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

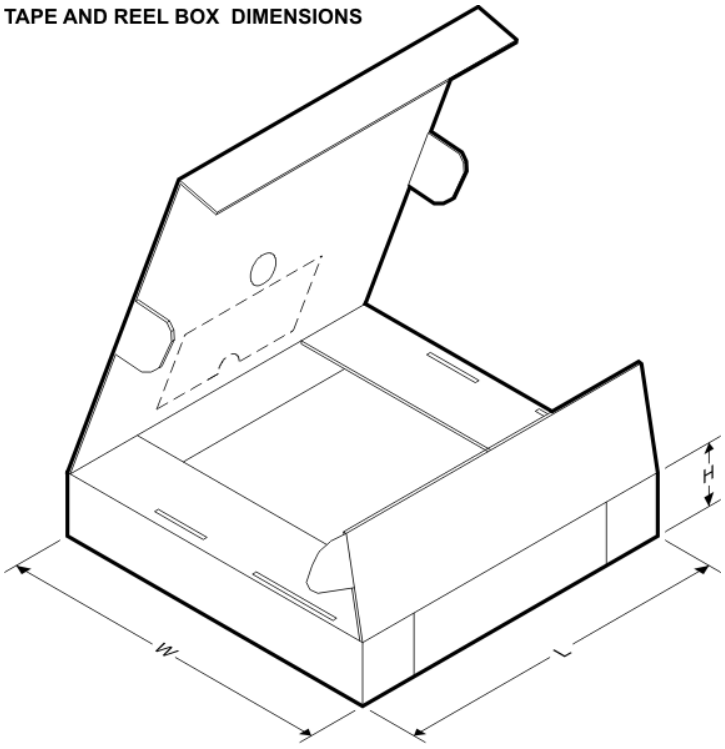


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90LV031ATMTCX/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
DS90LV031ATMX	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
DS90LV031ATMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

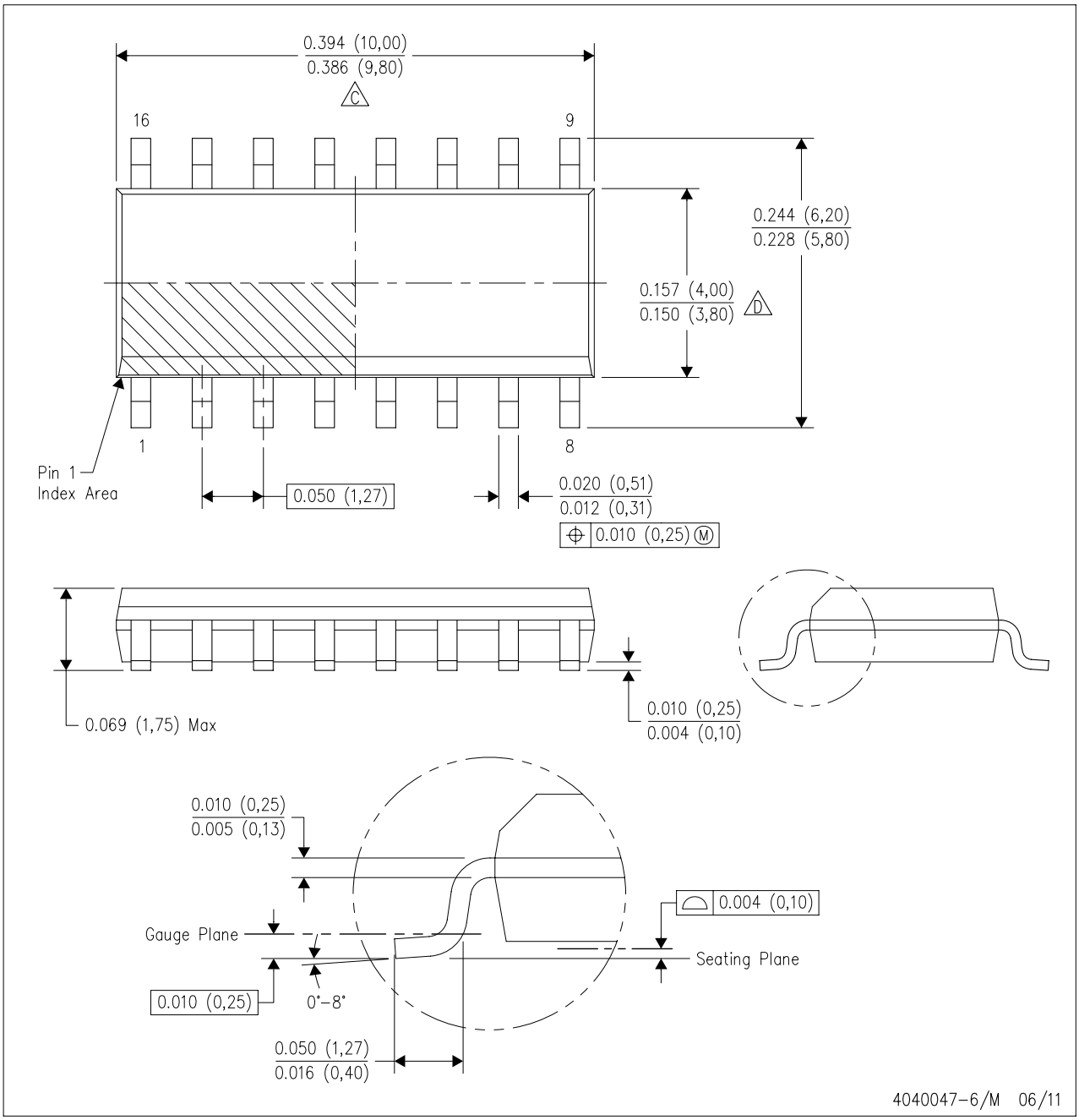


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90LV031ATMTCX/NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0
DS90LV031ATMX	SOIC	D	16	2500	367.0	367.0	35.0
DS90LV031ATMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

MECHANICAL DATA

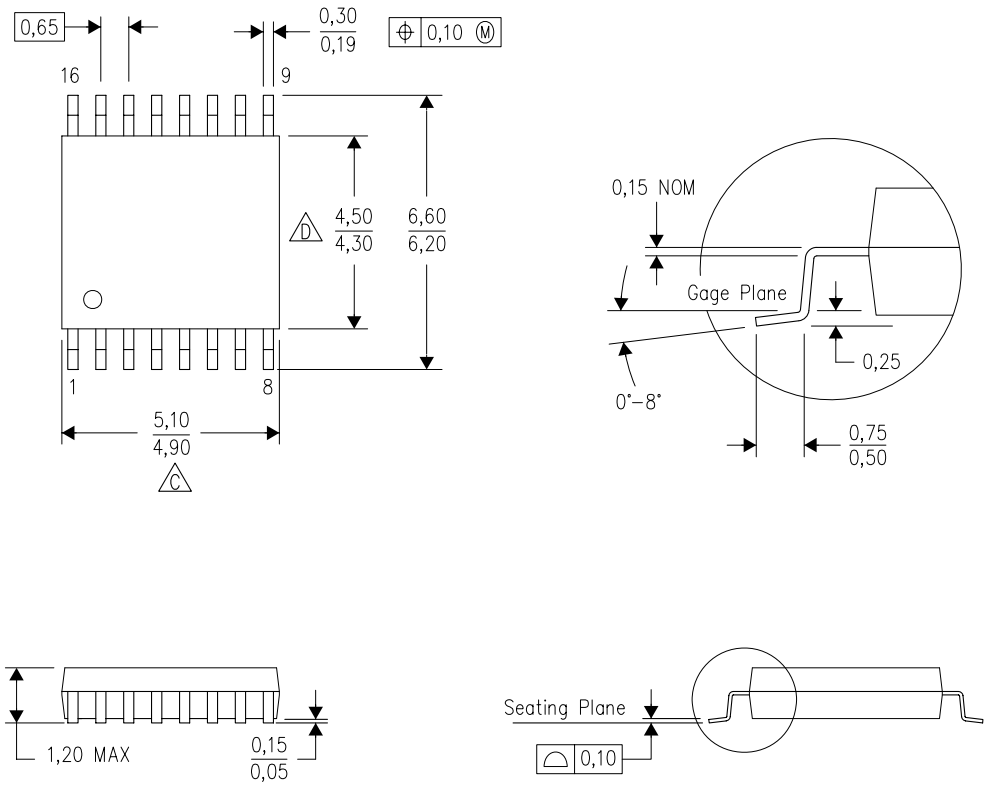
D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

MECHANICAL DATA

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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