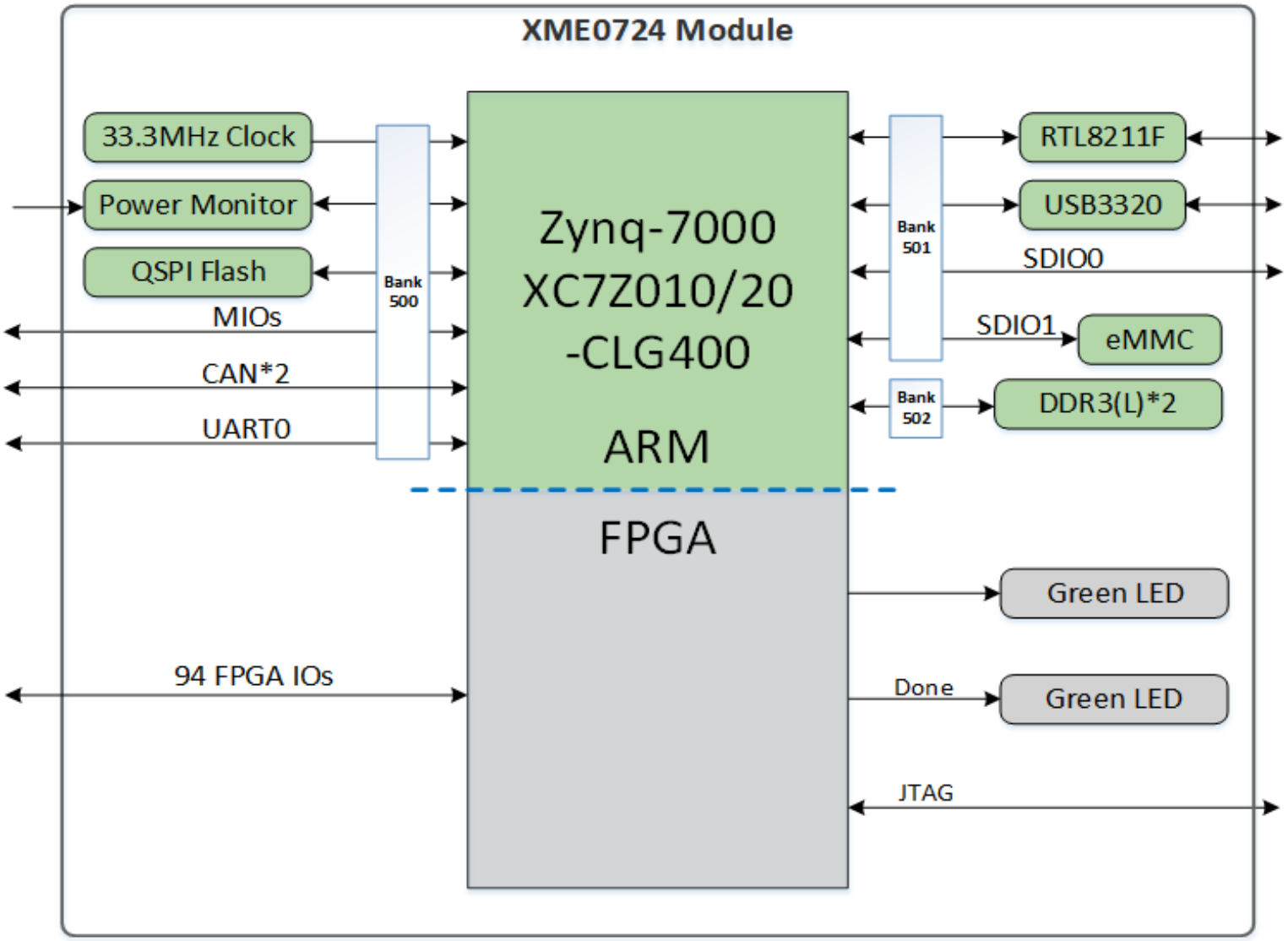
XME0724 Block Diagram

REV	DATE	PAGES	DESCRIPTION
1.0	02/12/2019	All	Rev 1.0 Release
2.0	01/04/2022	06,10	Rev 2.0 Release
3.0	09/06/2022	10	Rev 3.0 Release



PAGE	DESCRIPTION
1	Title, Notes, Block Diagram, Revision History
2	POWER
3	FPGA_POWER
4	FPGA_CONFIG
5	FPGA_IO_PL
6	FPGA_IO_PS
7	FPGA_DDR
8	DDR3
9	eMMC
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Title: XME0724 Schematic

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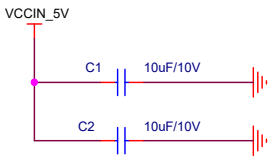
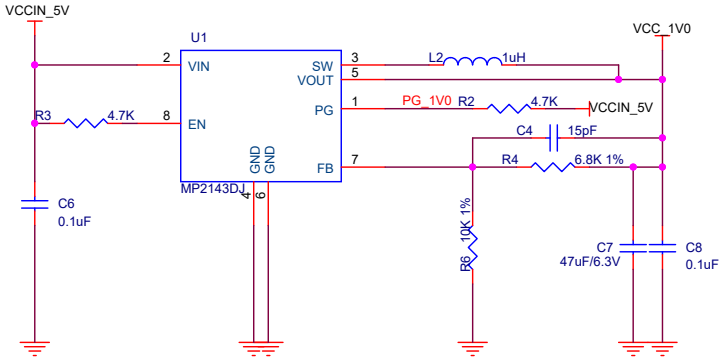
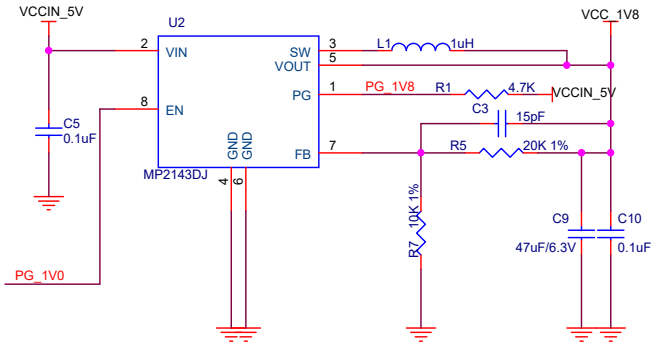
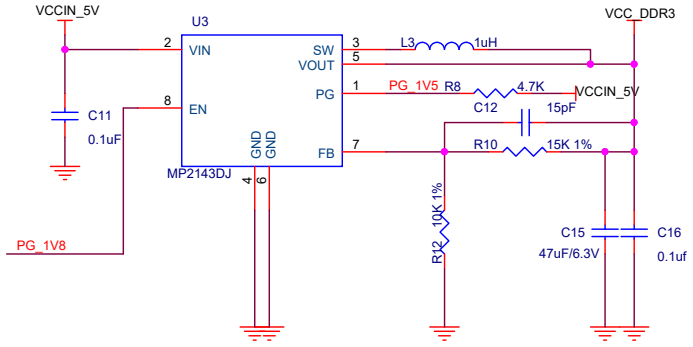




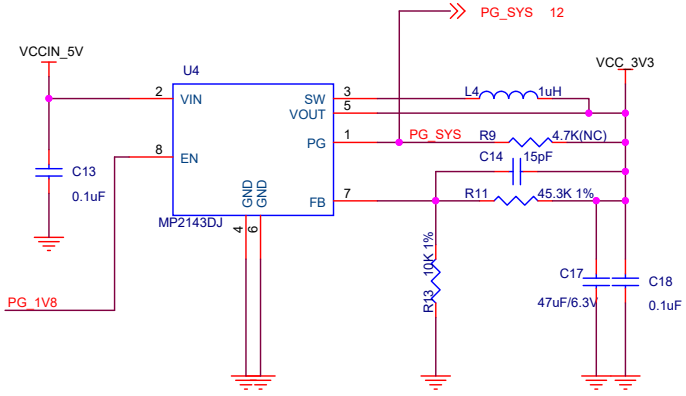
Vref = 0.6V VOUT = 1.0V



Vref = 0.6V VOUT = 1.8V



Vref = 0.6V VOUT = 1.5V



Vref = 0.6V VOUT = 3.3V

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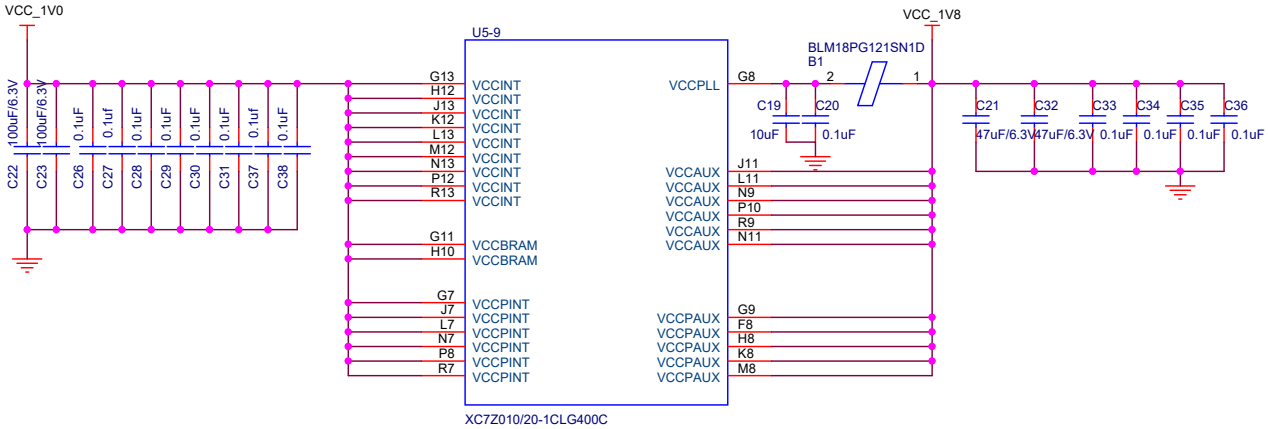

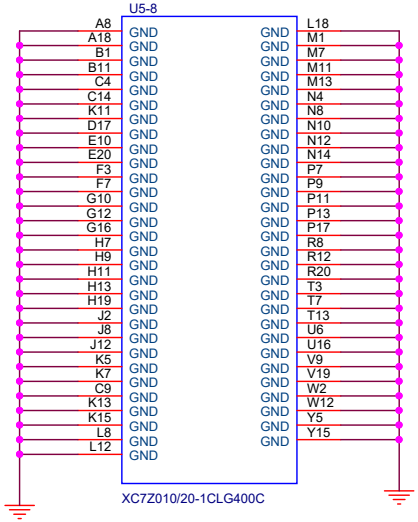

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Title: ZYNQ7010 FPGA_POWER

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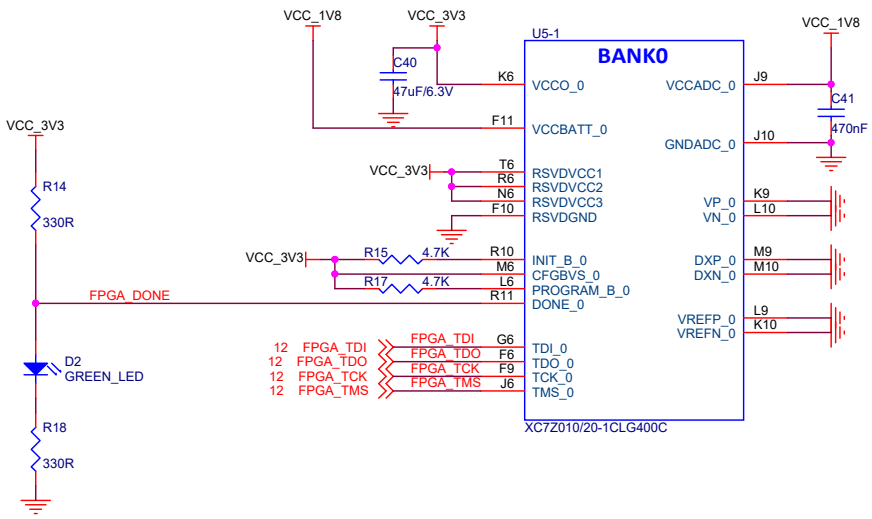
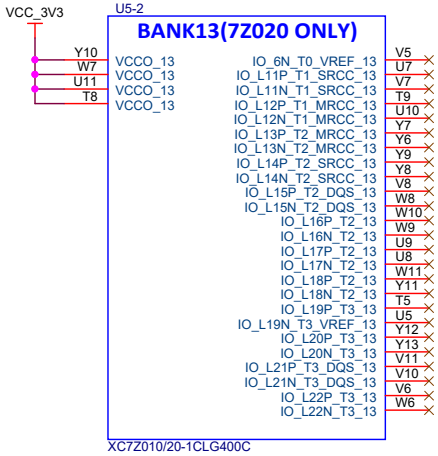
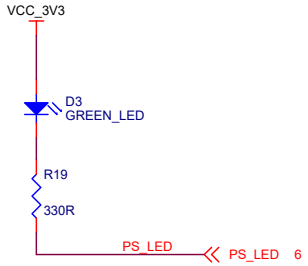
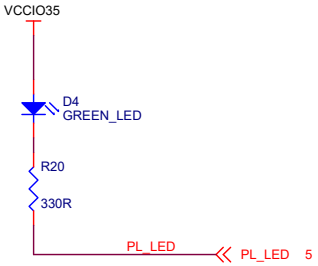
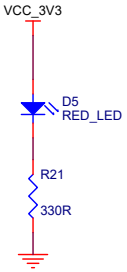
ZYNQ_CONFIG











Four LEDs:
1. Power LED: Red
2. DONE LED: Green
3. PS LED: Green
4. PL LED : Green
Layout Together

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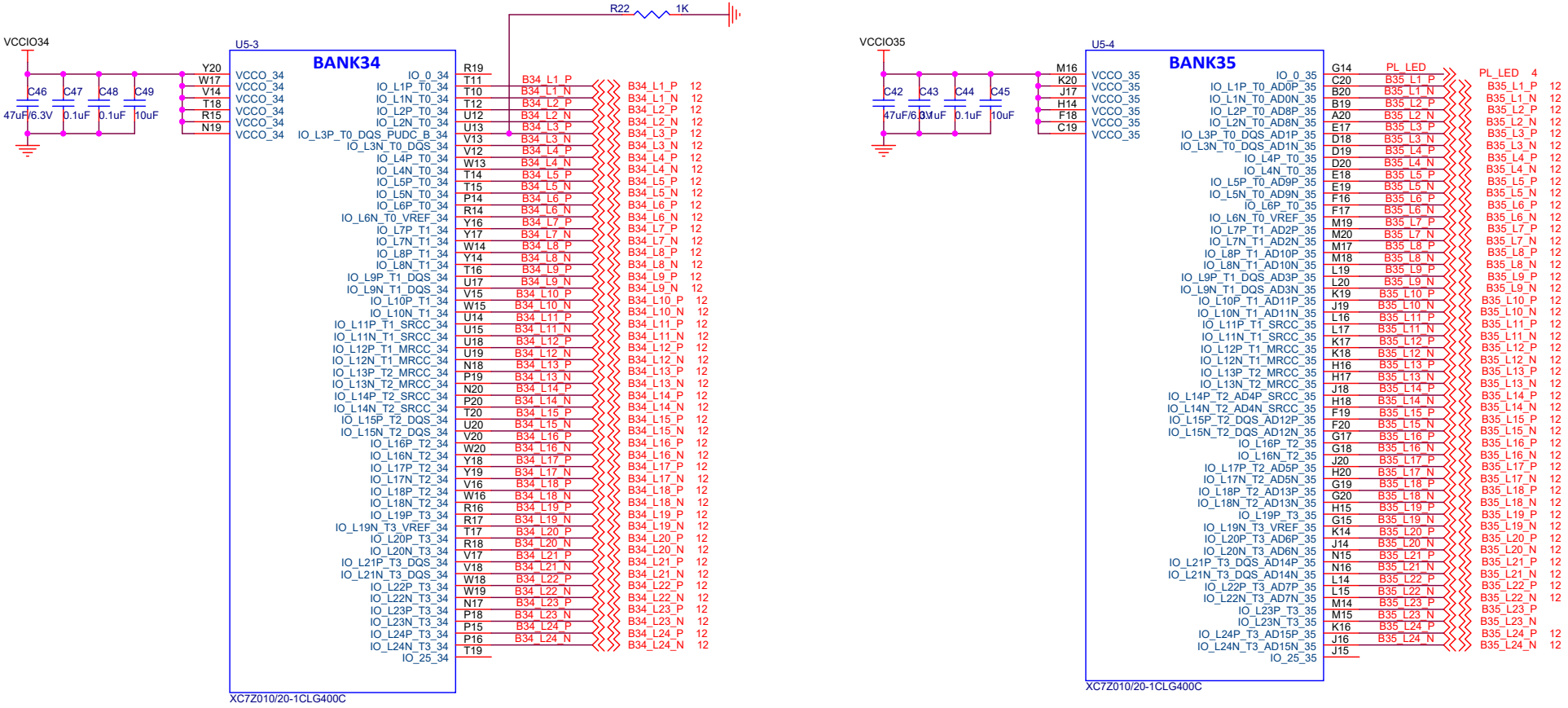
FPGA_PL



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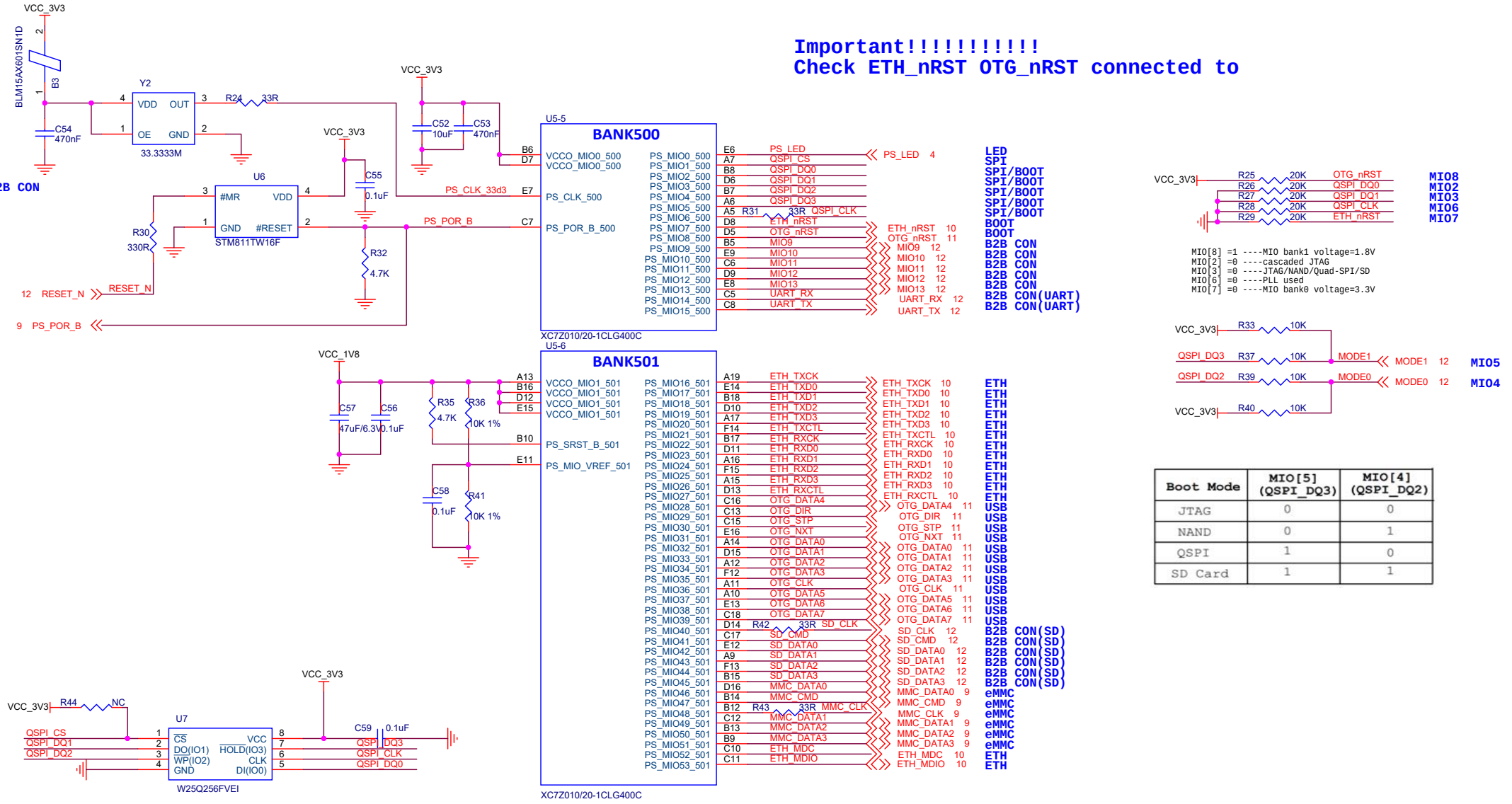
Important!!!!!!!!!!!
Check ETH_nRST OTG_nRST connected to
B2B CON
BANK500
XC7Z010/20-1CLG400C
BANK501
XC7Z010/20-1CLG400C
STM811TW16F
W25Q256FVEI
33.3333M
MIO[8] =1 ----MIO bank1 voltage=1.8V
MIO[2] =0 ----cascaded JTAG
MIO[3] =0 ----JTAG/NAND/Quad-SPI/SD
MIO[6] =0 ----PLL used
MIO[7] =0 ----MIO bank0 voltage=3.3V
Boot Mode | MIO[5] (QSPI_DQ3) | MIO[4] (QSPI_DQ2)
JTAG | 0 | 0
NAND | 0 | 1
QSPI | 1 | 0
SD Card | 1 | 1
MicroPhase Inc. www.microphase.cn
Title
ZYNQ PS
Size
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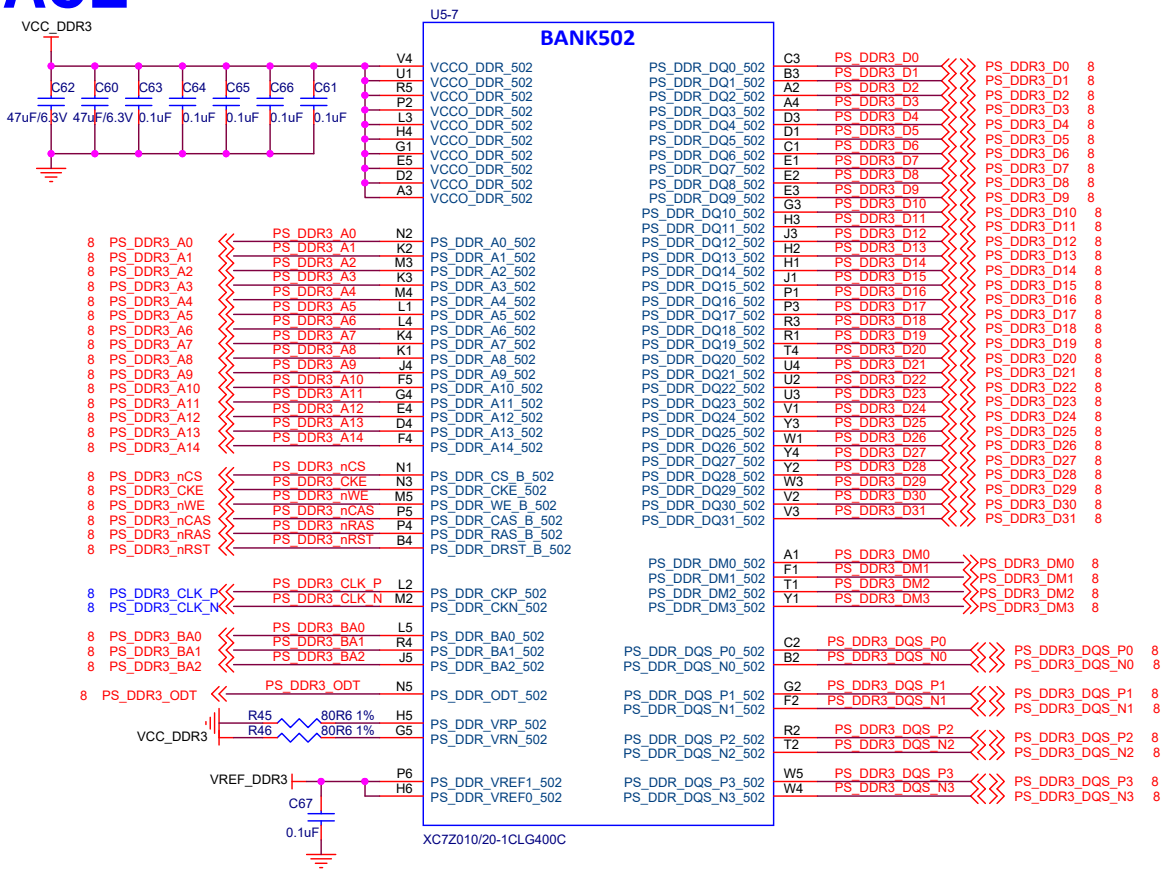
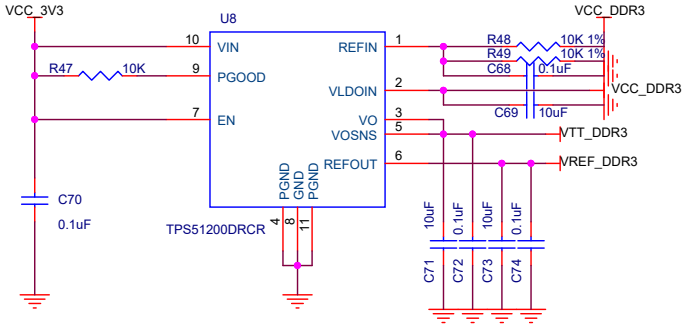
DDR_INTERFACE





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Title	ZYNQ DDR	
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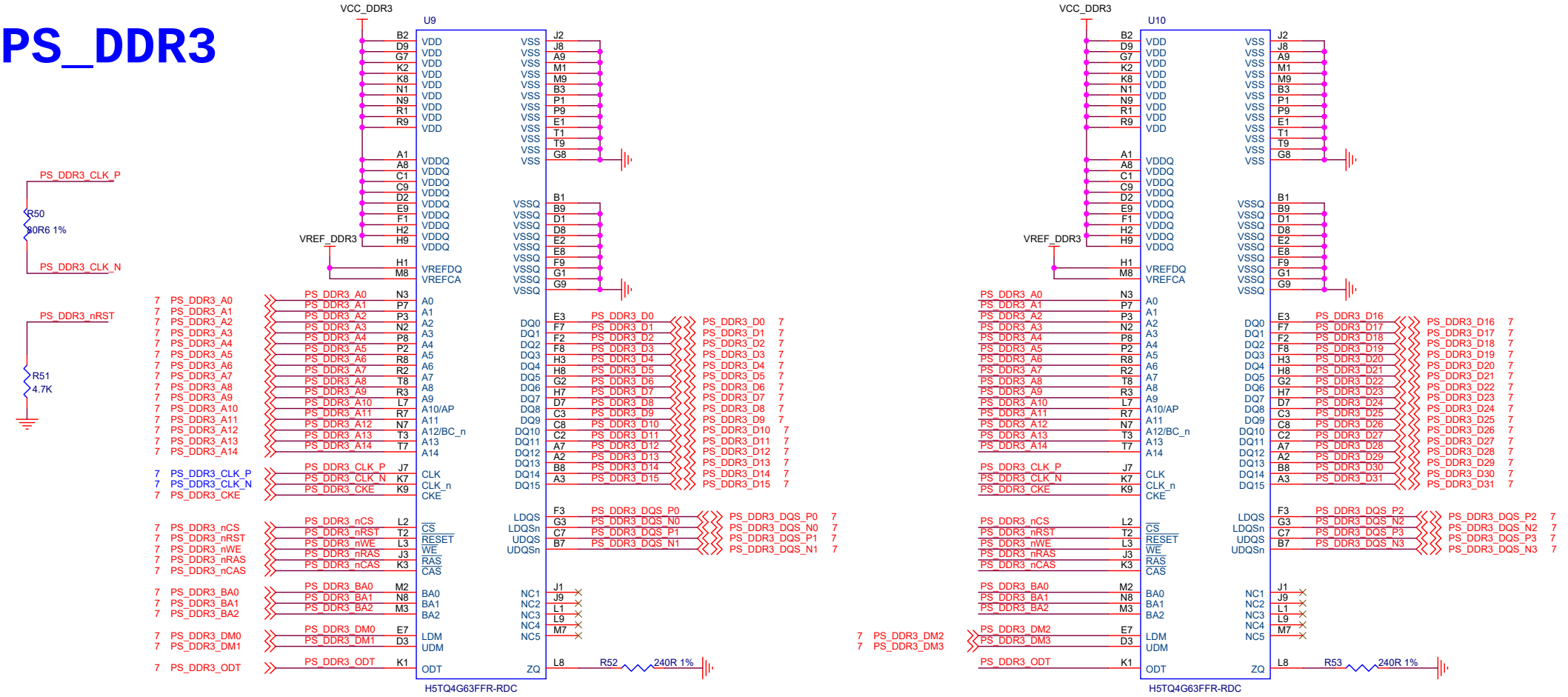
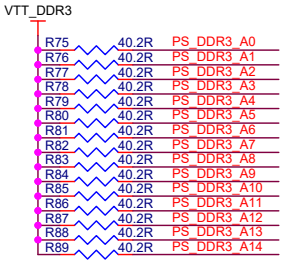
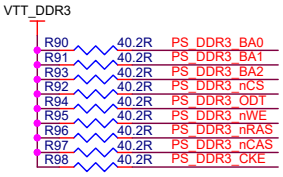
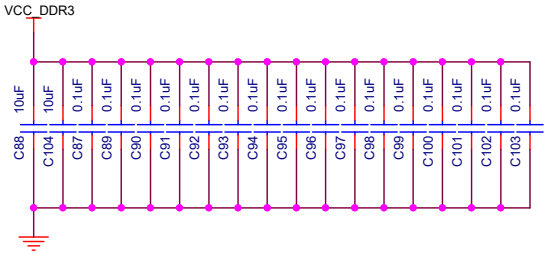
PS_DDR3

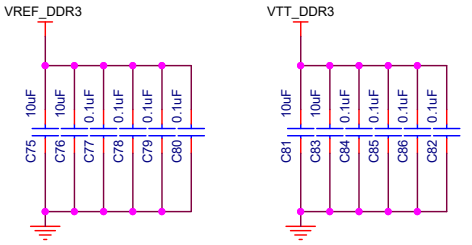


Check DDR3 Resistor









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Title	DDR RAM	
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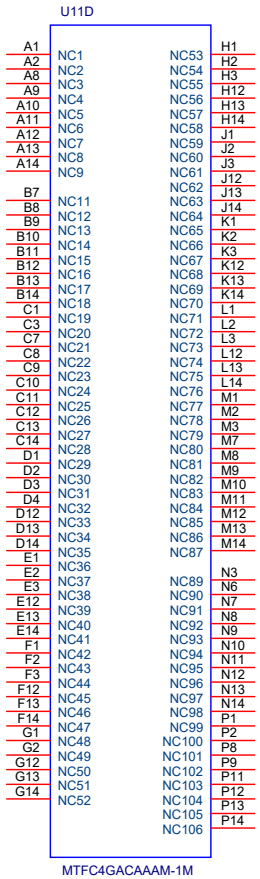

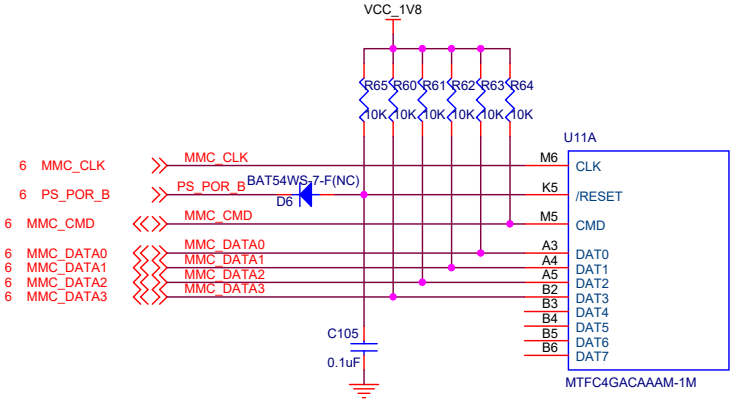

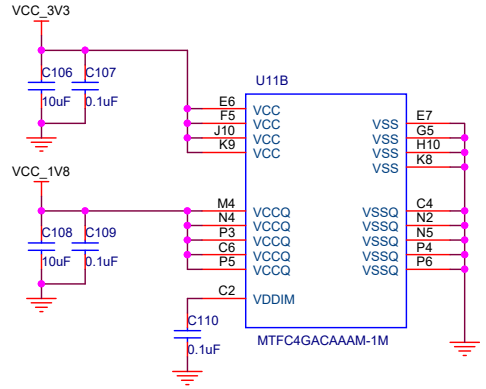

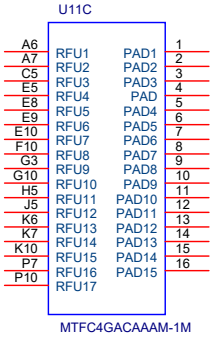

mmc_nrst should be warm reset

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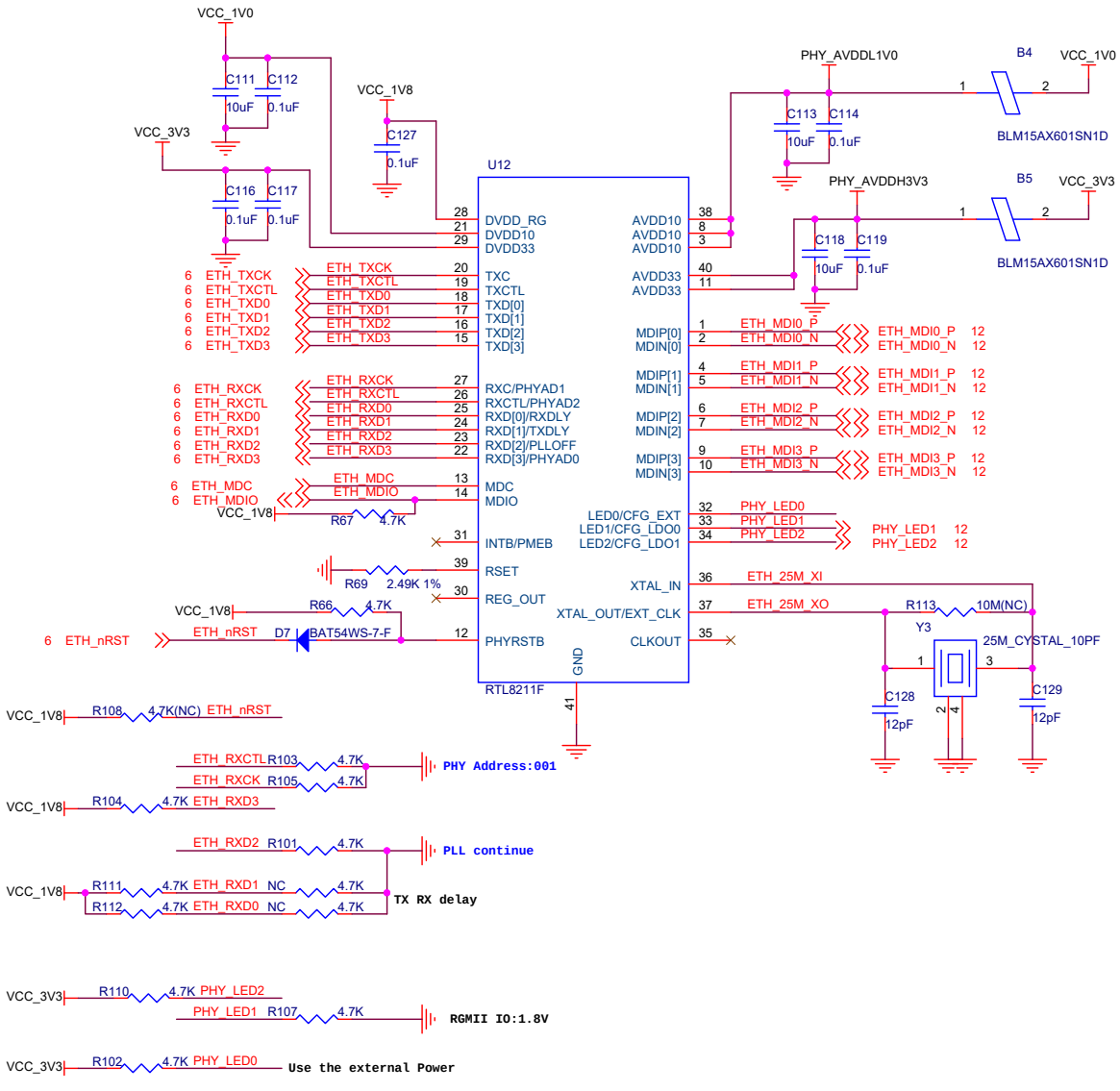

MicroPhase	MicroPhase Inc. www.microphase.cn
Title	GPHY
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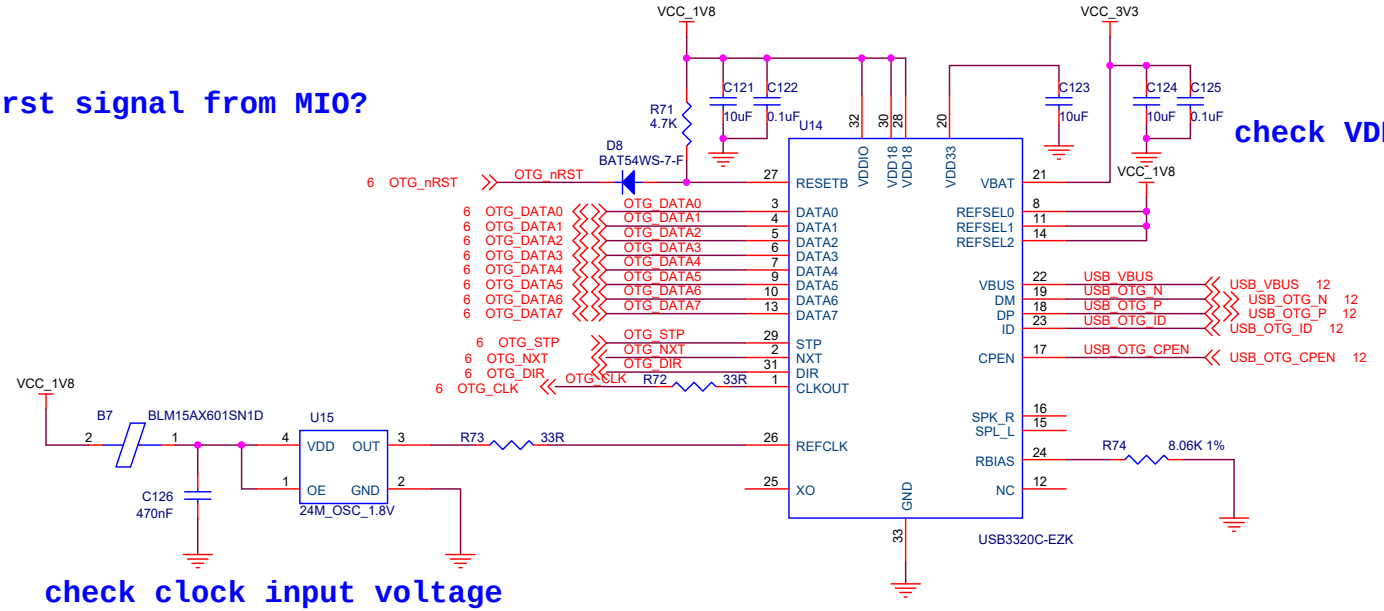
check rst signal from MIO?

check VDD33 output or input



check clock input voltage

MicroPhase	MicroPhase Inc. www.microphase.cn	
Title	USB OTG	
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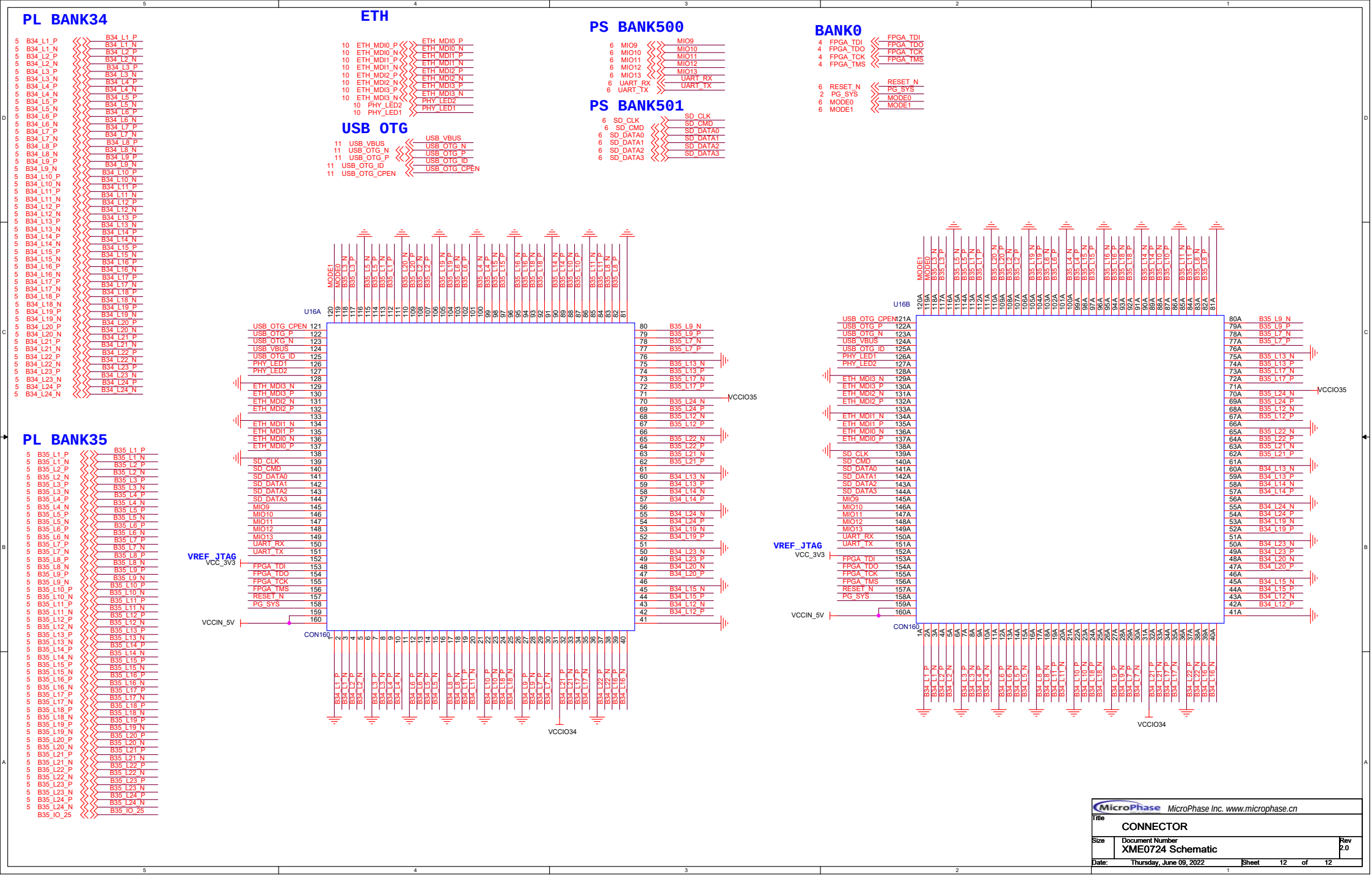
PL BANK34
B34_L1_P
B34_L1_N
B34_L2_P
B34_L2_N
B34_L3_P
B34_L3_N
B34_L4_P
B34_L4_N
B34_L5_P
B34_L5_N
B34_L6_P
B34_L6_N
B34_L7_P
B34_L7_N
B34_L8_P
B34_L8_N
B34_L9_P
B34_L9_N
B34_L10_P
B34_L10_N
B34_L11_P
B34_L11_N
B34_L12_P
B34_L12_N
B34_L13_P
B34_L13_N
B34_L14_P
B34_L14_N
B34_L15_P
B34_L15_N
B34_L16_P
B34_L16_N
B34_L17_P
B34_L17_N
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B34_L20_N
B34_L21_P
B34_L21_N
B34_L22_P
B34_L22_N
B34_L23_P
B34_L23_N
B34_L24_P
B34_L24_N
PL BANK35
B35_L1_P
B35_L1_N
B35_L2_P
B35_L2_N
B35_L3_P
B35_L3_N
B35_L4_P
B35_L4_N
B35_L5_P
B35_L5_N
B35_L6_P
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B35_L24_N
B35_IO_25
ETH
ETH_MDI0_P
ETH_MDI0_N
ETH_MDI1_P
ETH_MDI1_N
ETH_MDI2_P
ETH_MDI2_N
ETH_MDI3_P
ETH_MDI3_N
PHY_LED2
PHY_LED1
USB OTG
USB_VBUS
USB_OTG_N
USB_OTG_P
USB_OTG_ID
USB_OTG_CPEN
PS BANK500
MIO9
MIO10
MIO11
MIO12
MIO13
UART_RX
UART_TX
PS BANK501
SD_CLK
SD_CMD
SD_DATA0
SD_DATA1
SD_DATA2
SD_DATA3
BANK0
FPGA_TDI
FPGA_TDO
FPGA_TCK
FPGA_TMS
RESET_N
PG_SYS
MODE0
MODE1
U16A
CON160
VCCIO35
VCCIO34
VCCIN_5V
VCC_3V3
VREF_JTAG
U16B
CON160
VCCIO35
VCCIO34
VCCIN_5V
VCC_3V3
VREF_JTAG
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