MANGO DSP LTD.

MANGO PHOENIX PC/104-*PLUS* HARDWARE MANUAL

DSP VIDEO PROCESSING SOLUTION

CONFIDENTIAL

Authorized Customer Use

Legal Information

Copyright

Disclaimer

Mango DSP Ltd. reserves the right to make changes in specifications at any time without notice. The information furnished by Mango DSP in this material is believed to be accurate and reliable. However, Mango DSP assumes no responsibility for its use.

Trademarks

Mango DSP and Phoenix PC/104-*Plus* are trademarks and "Processing the Digital Vision" is a service mark of Mango DSP Ltd.

Windows, the Windows logo, Windows 98/2000/Millenium/XP, and Windows NT, are either registered trademarks or trademarks of Microsoft Corporation in the United States and/or other countries. Other product and company names mentioned herein may be the trademarks of their respective owners.

Linux is a registered trademark of Linus Torvalds.

Patents

Contact Information

Mango DSP Ltd., Israel

Postal: Har Hotzvim Industrial Park
P.O. Box 45116
Jerusalem, 91450 Israel

Tel: +972-2-532 8706
fax: +972-2-532 8705

Phoenix PC/104-*Plus* H/W User's Manual

Part Number 385-00020-001

Detailed Revision History

Rev.	Date	Author	Approved	Description
A0	13/11/03	I. Kravitz		Preliminary Release
A1	4/1/04	I. Kravitz		Updated A/V specs; inserted picture
A2	6/4/04	I. Kravitz		Updated Audio Connector pinout
A3	16/01/07	I. Kravitz		Updated Picture

Table of Contents

List of Figures

List of Tables

Abbreviation List

The following terms and abbreviations are used throughout the document.

A/D	Analog to Digital Converter
D/A	Digital to Analog Converter
DSP	Digital Signal Processor
EDMA	Enhanced Direct Memory Access
EMIF	External Memory Interface
FPGA	Field Programmable Gate Array
GPIO	General Purpose I/O
HPI	Host Port Interface
JTAG	Joint Test Action Group
L1P	Level-one Program Cache
L1D	Level-one Data Cache
McASP	Multi-channeled Audio Serial Port
McBSP	Multi-channeled Buffered Serial Port
PMC	PCI Mezzanine Card
SDRAM	Synchronous Dynamic RAM
SPI	Serial Peripheral Interface
TDM	Time Domain Multiplexed

Related Documentation

1. PCI Local Bus Specification Revision 2.2.
2. PC/104 Specification.
3. PC/104-*Plus* Specification.
4. TMS320DM642 Data Manual SPRS200B
5. TMS320DM642 Technical Overview SPRU615 Application Report
6. TMS320C6000 Peripherals Reference Guide.
7. PLX PCI 6152 PCI to PCI Bridge Data Sheet.
8. Micron SDRAM MT48LC4M32B2 Datasheet.
9. Philips Semiconductor SAA7115H datasheet.
10. AKM AK5384 A/D datasheet.

1. Introduction

This document describes the hardware implementation of the Phoenix PC/104-*Plus*™ board. The Mango Phoenix PC/104-*Plus* is a powerful platform that can fit onto any standard PC/104-*Plus* chassis. Designed with two TI DM642 Digital Media Processors, the Mango Phoenix PC/104-*Plus* constitutes a compelling video processing solution. Combining multiple video and audio inputs and DSP processing, the Phoenix PC/104-*Plus* offers a programmable solution for even the most demanding audio/video imaging applications. Ease of design is further enhanced with the ready for use Mango video libraries such as the JPEG Encoding libraries. These video libraries include a comprehensive set of video compression encoders and decoders as well as many imaging functions. This architecture allows for four video inputs and eight audio inputs to be multiplexed into two DSPs for audio/video capture.

This document defines the functional hardware specifications for the Mango Phoenix PC/104-*Plus* board. The Phoenix inputs four composite video channels through four SMC type RF connectors. The composite video channel is decoded by the Phillips Video A/D device and transmitted to one of the video ports of the DM642 DSP. Another composite video channel is decoded by another A/D and its output is transmitted to a second video port of the DSP. Another two composite video streams are decoded in the same manner to the second DSP on board. Thus, four independent and simultaneous channels of video are captured and processed on the Mango Phoenix PC/104-*Plus* board.

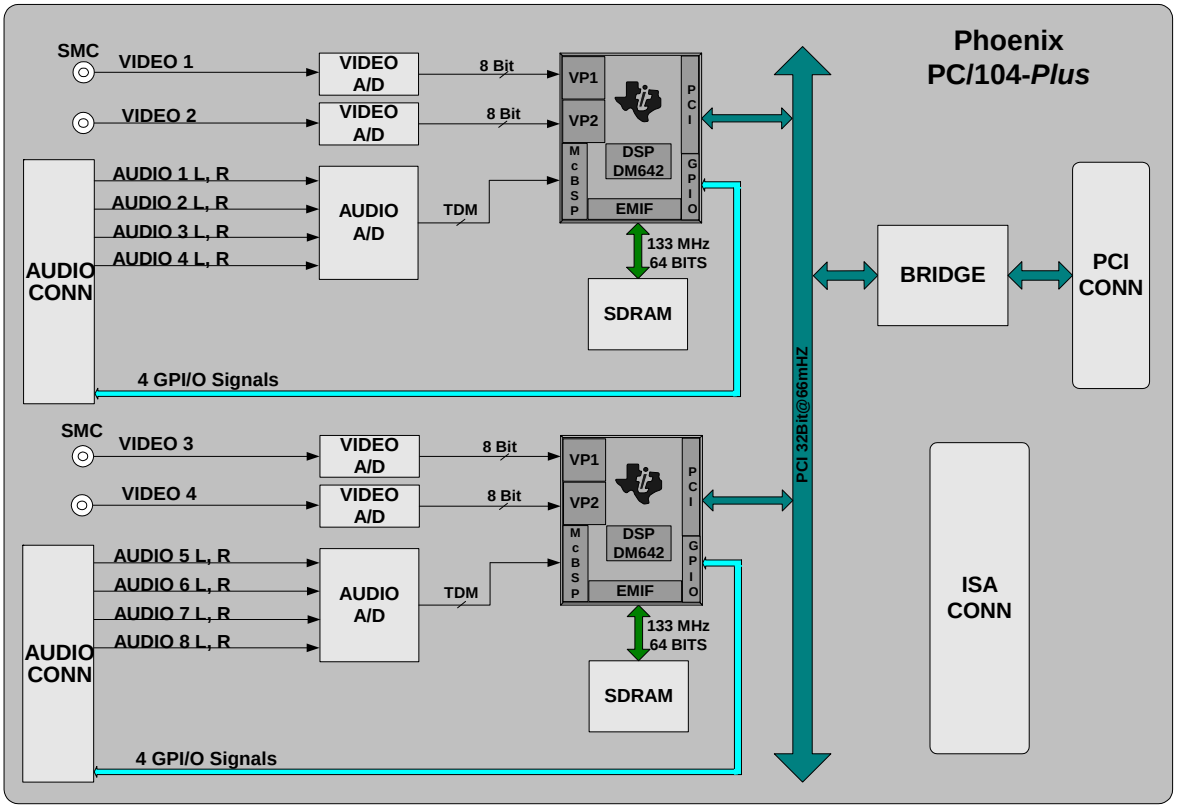
Eight audio stereo channels are input to the board via a forty pin connector header. The eight audio ports are transmitted to four 4-channel audio A/D devices. Each audio A/D handles two stereo audio inputs. The audio A/D converters, which are controlled by the DSP, samples all the inputs, and outputs a serial stream to the DSPs McBSP serial port for processing. The DSP handles the synchronization of the audio and video data.

The DSP has a 32-bit 66 MHz PCI bus that inputs data from the external PC/104-*Plus* PCI connector. The PC/104-*Plus* specification currently supports a PCI Bus of 32-bit and 33 MHz only. Each DSP has a 64-bit 133 MHz External Memory Interface (EMIF) bus that connects to 32 Mbytes of SDRAM. The 64-bit wide SDRAM bus allows for data transfer at over 1 gigabyte per second.

1.1. Block Diagram

Figure 1 is a block diagram of the Phoenix PC/104-*Plus* board.

Figure 1: Block Diagram of Phoenix PC/104-*Plus* Board



2. The Phoenix PC104- Plus Features

2.1. General Specifications

Table 1: Phoenix PC/104-*Plus* Specifications

Characteristics	Specifications
Board Form Factor	PC/104-*Plus*
PCI Compatibility	Rev. 2.2
PCI Bus	32 Bits 33 MHz
PCI Device	PLX PCI6152 Bridge
DSP	Two TI TMS320DM642
SDRAM	32 MByte per DSP
Video	4 Composite Video Inputs
Audio	8 Stereo Inputs
I/O	4 GPIO signals per DSP
ISA	Pass through only
Power requirements	+5VDC @ 1.5 Amp
Operating Temperature	0ºC - 70ºC
Storage Temperature	-40ºC to 85ºC
Relative Humidity	5% to 90% (non-condensing)
Dimensions: Length Width Height	 3.775 inches 3.55 inches per PC/104-*Plus* spec (15mm stacking)

2.2. Video Specifications

Table 2: Video Specification

Characteristics	Specifications
Video Signal Standard	EIA RS-170, NTSC, PAL, ITU-601.
Bandwidth	7 MHz at -3 dB
Horizontal Resolution	400 lines or more
Linearity	10 gray scale or better
Composite Input	1.0Vp-p, 75 ohm negative sync
Level Control	Automatic Gain Control (AGC)

2.3. Audio Specifications

Table 3: Audio Specification

Characteristics	Specifications
Number of Channels	Eight Stereo
Input Level	1 V RMS
Input Impedance	20K ohm
Output Level	1 V RMS (5K ohm load)
Bandwidth	30 Hz to 10 KHz
Signal-to-Noise Ratio	96 dB typical
Dynamic Range	72 dB
Total Harmonic Distortion	- 96 dB typical
Sampling Frequency	48 KHz

2.4. LED Indicators

Table 4: LED Indicators

Characteristics	Specifications
DS1	3.3 V LED
DS2	5 V LED
DS3	General Purpose LED on DSP1
DS4	General Purpose LED on DSP2

2.5. Switches and Jumpers

Table 5: Switches and Jumpers

Connector	Description
SW1	Power On Reset Switch
U76	Rotary Switch For PC/104-*Plus* Add In Modules
JP1	Boundary Scan Selector
JP2	PCI Bus frequency 33/66 MHz

2.6. Connectors

Table 6: Phoenix PC/104-*Plus* Connectors

Connector	Description	Manufacturer	Part #
U45	Video 1	Rosenberger	39S201-400E3
U46	Not Used		
U49	Video 2	Rosenberger	39S201-400E3
U50	Not Used		
U53	Video 3	Rosenberger	39S201-400E3
U54	Not Used		
U57	Video 4	Rosenberger	39S201-400E3
U58	Not Used		
J4	40-Pin SMT Audio Connector	Molex	53505-4090
J1, J3	ISA Connectors	CommConn	1185CPF-G104
J2	PCI Connector	CommConn	1242PF-120G
J5	DSP JTAG Connector	Samtec	TSM-107-01-T-DV

3. Connector Pinouts

3.1. ISA Bus Connector

Table 7: ISA J1, J3 Connector Pin out

PIN	ROW A	ROW B
0	GND	GND
1	MEMCS16	SBHE
2	IOCS16	LA23
3	IRQ10	LA22
4	IRQ11	LA21
5	IRQ12	LA20
6	IRQ15	LA19
7	IRQ14	LA18
8	DACK0	LA17
9	DRQ0	MEMR
10	DACK5	MEMW
11	DRQ5	SD8
12	DACK6	SD9
13	DRQ6	SD10
14	DACK7	SD11
15	DRQ7	SD12
16	+5V	SD13
17	MASTER	SD14
18	GND	SD15
19	GND	KEY

PIN	ROW A	ROW B
1	IOCHCHK	GND
2	SD7	RESETDRV
3	SD6	+5V
4	SD5	IRQ9
5	SD4	-5V
6	SD3	DRQ2
7	SD2	V12-
8	SD1	ENDXFR
9	SD0	+12V
10	IOCHRDY	KEY
11	AEN	SMEMW
12	SA19	SMEMR
13	SA18	IOW
14	SA17	IOR
15	SA16	DACK3
16	SA15	DRQ3
17	SA14	DACK1
18	SA13	DRQ1
19	SA12	REFRESH
20	SA11	SYSCLK
21	SA10	IRQ7
22	SA9	IRQ6
23	SA8	IRQ5
24	SA7	IRQ4
25	SA6	IRQ3
26	SA5	DACK2
27	SA4	TC
28	SA3	BALE
29	SA2	+5V
30	SA1	OSC
31	SA0	GND
32	GND	GND

3.2. PCI Bus Connector

Table 8: PCI J2 Connector Pin out

PIN	ROW A	ROW B	ROW C	ROW D
1	G/5V/KEY	RSVD	+5V	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1	AD15	+3.3V
9	SERR	GND	AB0	PAR
10	GND	PERR	+3.3V	SDONE
11	STOP	+3.3V	LOCK	GND
12	+3.3V	TRDY	GND	DEVSEL
13	FRAME	GND	IRDY	+3.3V
14	GND	AD16	+3.3V	C/BE2
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0	GND	REQ1	VI/O
24	GND	REQ2	+5V	GNT0
25	GNT1	VI/O	GNT2	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD	+5V	RST
29	+12V	INTA	INTB	INTC
30	-12V	RSVD	RSVD	G/3V/KEY

3.3. Audio Connector

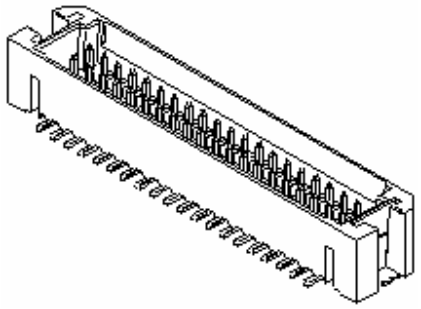


Table 9: J4 Audio Connector

J4	Name	Dir
1	AUDIO_R8	I
2	GND	
3	GND	
4	AUDIO_L8	I
5	AUDIO_R7	I
6	GND	
7	GND	
8	AUDIO_L7	I
9	AUDIO_R6	I
10	GND	
11	GND	
12	AUDIO_L6	I
13	AUDIO_R5	I
14	GND	
15	GND	
16	AUDIO_L5	I
17	AUDIO_R4	I
18	GND	
19	GND	
20	AUDIO_L4	I

J4	Name	Dir
21	AUDIO_R3	I
22	GND	
23	GND	
24	AUDIO_L3	I
25	AUDIO_R2	I
26	GND	
27	GND	
28	AUDIO_L2	I
29	AUDIO_R1	I
30	GND	
31	GND	
32	AUDIO_L1	I
33	GPIO5_DSP1	I/O
34	GPIO2_DSP1	I/O
35	GPIO1_DSP1	I/O
36	GPIO0_DSP1	I/O
37	GPIO5_DSP2	I/O
38	GPIO2_DSP2	I/O
39	GPIO1_DSP2	I/O
40	GPIO0_DSP2	I/O

3.4. SMC Video Connector

Table 10: SMC Video Connectors

Connector	Description
U45	Video 1
U46	Not Used
U49	Video 2
U50	Not Used
U53	Video 3
U54	Not Used
U57	Video 4
U58	Not Used

3.5. JTAG: DSP J5

Table 11: J5 JTAG DSP Connector Pin outs

Pin #	Name	Dir.
1	TMS	I
2	TRST	I
3	TDI	I
4	GND	
5	P3_3V	

Pin #	Name	Dir.
6	GND	
7	TDO	O
8	GND	
9	TCK_RTN	
10	GND	

Pin #	Name	Dir.
11	TCK	I
12	GND	
13	EMU1	I
14	EMU0	I

4 . Description of PC/104-Plus Board

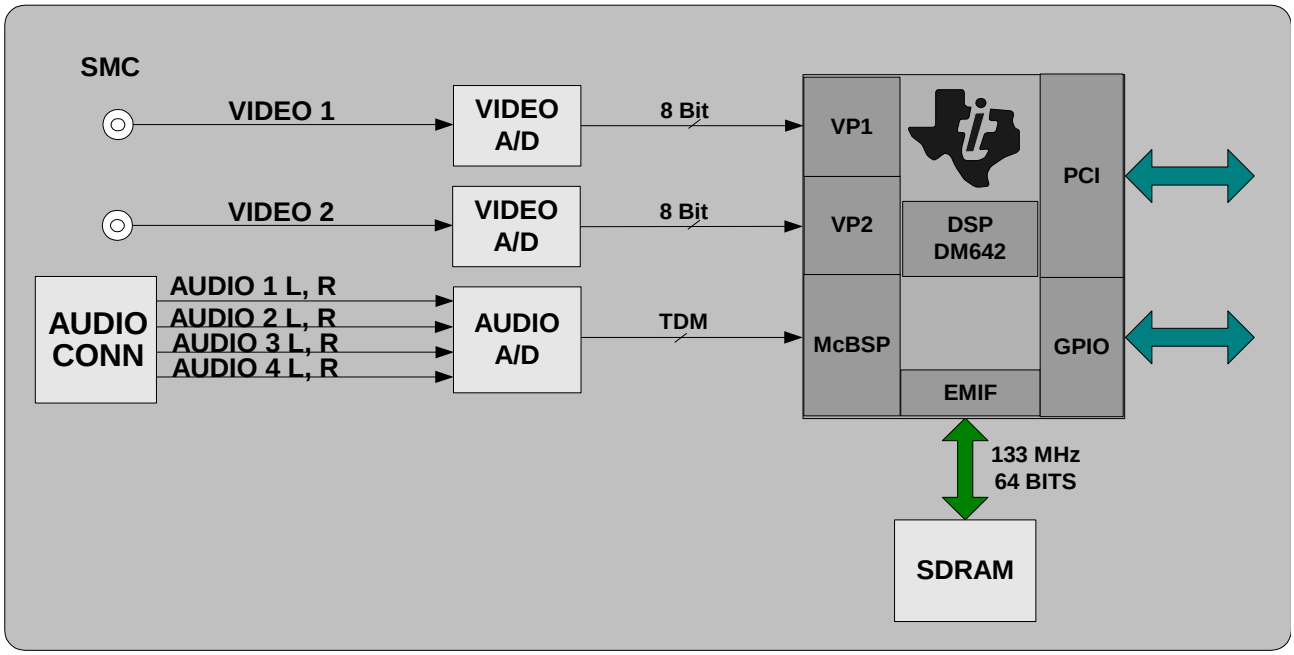
4.1. The DSP: TMS320DM642

The Phoenix PC/104-*Plus* board contains two Texas Instruments TM320DM642 DSP devices. Each DSP receives two video streams at two of its video ports. These two video streams are the two composite video inputs.

Each DSP receives four stereo audio streams at the McBSP serial port. The audio A/D device receives the four stereo inputs from the audio connector and outputs the serial data to the DSP in the TDM format. The DSP synchronizes the audio and video data.

Figure 2 is a diagram of one DSP on the board. The second DSP is identical to the first.

Figure 2: DSP interconnections



The TMS320DM642 fixed-point DSP has the following features:

- High Performance Digital Media Processor
  - 2-, 1.67 ns Instruction Cycle Time
  - 500-, 600 MHz Clock Rate
  - Eight 32-Bit Instructions/Cycle
  - 4000, 4800 MIPS
- VelociTI.2 Advanced Very Long Instruction Word C64x DSP Core
  - Six ALUs (32-/40 Bit) supporting single 32-bit, dual 16-bit, quad 8-bit Arithmetic per Clock Cycle
  - Two Multipliers Support; Four 16 X 16-Bit Multiplies or Eight 8 X 8-Bit Multiplies per Clock Cycle
  - 64 32-Bit General Purpose Registers
- Instruction Set Features
  - Byte Addressable (8-/16-/32-/64-Bit Data)
  - 8-Bit Overflow Protection
  - Bit-Field Extract, Set, Clear
- L1/L2 Memory Architecture
  - 128K-Bit L1P Program Cache
  - 128K-Bit L1D Data cache
  - 2M-Bit L2 Unified Mapped RAM/Cache
- External Memory Interface
  - 64-Bit EMIF
  - Glueless Interface to SRAM and SDRAM
  - 1024M-Byte Total Addressable External Memory Space
- Enhanced DMA (EDMA) Controller (64 Independent Channels)
- 10/100 Mb/sec Ethernet MAC

- Management Data Input/Output (MDIO)
- Three Configurable Video Ports
  - Glueless interface to common Video Decoder and Encoder Devices
  - Supports Video Standards CCIR601, ITU-BT.656, BT.1120, SMPTE 125M, 260M,274M, and 296M
  - Supports Raw Video I/O
  - Transport Stream Interface Mode
- VCXO Interpolated Control Port (VIC)
  - Supports Audio/Video Synchronization
- Host Port Interface
  - User Configurable Bus Width (32-/16-Bit)
- 32-Bit 66 MHz 3.3V PCI Interface (PCI Specification 2.2)
- Multichannel Audio Serial Port (McASP)
  - Eight serial Data Pins
  - Inter-IC Sound (I2S) Bit Stream Format
  - Integrated Digital Studio I/F Transmitter supports S/PDIF, IEC60958-1, AES-3, CP-430 Formats
- Two Multichannel Buffered Serial Ports
- I2C Bus
- Three 32-Bit General Purpose Timers
- Sixteen General Purpose I/O Pins
- Flexible PLL Clock Generator
- IEEE-1149.1 JTAG Boundary Scan Compatible
- 3.3V I/O, 1.4V Internal

The two DSPs on the Phoenix PC/104-*Plus* Board each have their own local SDRAM. The 64-bit EMIF Bus on each DSP is connected to the SDRAM. The DSPs communicate with each other on the 32-bit 33 MHz PCI Bus.

4.1.1. DSP Memory

The TMS320DM642 has a cache-based architecture with two-level memory architecture for program (designated L1P) and data (designated L1D). The level one program cache controller interfaces the CPU to the L1P. A 256-bit wide path is provided from the CPU to allow a continuous stream of eight 32-bit instructions. The level-one data cache controller is the interface between the CPU and the L1D. The L1D allows simultaneous access by both sides of the CPU. Both the program and data memory share the second level memory designated L2. L2 is a 1024-Byte memory space that can be configured as all memory mapped SRAM, all cache, or a combination of the two.

4.1.1.1. L1P Description

The L1P on the DM642 is a 16 KByte direct-mapped cache with a 32-byte line size and 512 sets. A 32-bit CPU program address is divided into three pieces to determine the physical L1P location where the data can reside. The L1P address location register is shown below.

31 ... 14	13 ... 5	4 ... 0
TAG	SET INDEX	OFFSET

The five least significant bits indicate the byte offset of the program fetch packet. The next nine bits of the program address are used to indicate in which set the data can reside. The data of each address can only reside in one of 512 sets. The upper 18 bits are used as a unique tag to label what data is currently residing in that cache line.

The L1P operation is controlled by the CPU control status register, the L1P flush base address register, the L1P flush word count register, and the cache configuration register.

4.1.1.2. L1D Description

The L1D is a 16 KByte cache with a 64-bit wide write bus from L1D to the L2 memory. It is a two-way set associative cache with a 64-byte line size and 128 sets. A physical address from the CPU is divided into four regions to select the cache set to allocate the data in and to select the correct word from that set. The L1P address location register is shown below.

31 ... 13	12 ... 6	5 ... 2	1 ... 0
TAG	SET INDEX	WORD	OFFSET

The lower two address bits are a word offset into the address. The next four bits selects the word that contains the requested data. The next seven bits identify the set to search for the requested data. The upper 19 bits are the tag value for the address.

The L1D operation is controlled by the CPU control status register, the L1D flush base address register, the L1D flush word count register, and the cache configuration register.

4.1.2. Memory Map

The DM642 has one memory map which is shown in the table below. Internal memory is always located at address 0 but can be used as both program and data memory. The external memory address ranges begin at 0x8000 0000 for the EMIF.

Table 12: DSP Memory Map Summary

Address Range	*Size (Bytes)*	*Description*
0x0000 0000 – 0x0003 FFFF	256K	Internal RAM (L2)
0x0004 0000 – 0x000F FFFF	768K	Reserved
0x0010 0000 – 0x017F FFFF	23M	Reserved
0x0180 0000 – 0x0183 FFFF	256K	EMIF Registers
0x0184 0000 – 0x0187 FFFF	256K	L2 Registers
0x0188 0000 – 0x018B FFFF	256K	HPI Registers
0x018C 0000 – 0x018F FFFF	256K	McBSP0 Registers
0x0190 0000 – 0x0193 FFFF	256K	McBSP1 Registers
0x0194 0000 – 0x0197 FFFF	256K	Timer 0 Registers
0x0198 0000 – 0x019B FFFF	256K	Timer 1 Registers
0x019C 0000 – 0x019F FFFF	256K	Interrupt Selector Registers
0x01A0 0000 – 0x01A3 FFFF	256K	EDMA RAM and EDMA Registers
0x01A4 0000 – 0x01AB FFFF	512K	Reserved
0x01AC 0000 – 0x01AF FFFF	256K	Timer 2 Registers
0x01B0 0000 – 0x01B3 EFFF	256K - 4K	GPIO Registers
0x01B3 F000 – 0x01B3 FFFF	4K	Device Configuration Registers
0x01B4 0000 – 0x01B4 3FFF	16K	I2CO Data and Control Registers
0x01B4 4000 – 0x01B4 BFFF	32K	Reserved
0x01B5 0000 – 0x01B7 FFFF	192K	Reserved
0x01B8 0000 – 0x01BB FFFF	256K	Reserved
0x01BC 0000 – 0x01BF FFFF	256K	Emulation

Address Range	*Size (Bytes)*	*Description*
0x01C0 0000 – 0x01C3 FFFF	512K	PCI Registers
0x01C4 0000 – 0x01C4 3FFF	16K	VP0 Control
0x01C5 0000 – 0x01C4 7FFF	16K	VP1 Control
0x01C4 8000 – 0x01C4 BFFF	16K	VP2 Control
0x01C0 0000 – 0x01C3 FFFF	512K	PCI Registers
0x01C4 0000 – 0x01C4 3FFF	16K	VP0 Control
0x01C4 C000 – 0x01C4 FFFF	16K	VIC Control
0x01C5 0000 – 0x01C7 FFFF	192K	Reserved
0x01C8 0000 – 0x01C8 0FFF	4K	EMAC Control
0x01C8 1000 – 0x01C8 2FFF	8K	EMAC Wrapper
0x01C8 3000 – 0x01C8 37FF	2K	EWRAP Registers
0x01C8 3800 – 0x01C8 3FFF	2K	MDIO Control Registers
0x01C8 4000 – 0x01FF FFFF	3.5M	Reserved
0x0200 0000 – 0x0200 0033	52	QDMA Registers
0x0200 0034 – 0x02FF FFFF	938M – 52	Reserved
0x3000 0000 – 0x33FF FFFF	64M	McBSP0 Data
0x3400 0000 – 0x37FF FFFF	64M	McBSP1 Data
0x3800 0000 – 0x3BFF FFFF	64M	Reserved
0x3C00 0000 – 0x3C0F FFFF	1M	McASP0 Data
0x3C10 0000 – 0x3FFF FFFF	64M – 1M	Reserved
0x4000 0000 – 0x73FF FFFF	832M	Reserved
0x7400 0000 – 0x75FF FFFF	32M	VP0 Channel A Data
0x7600 0000 – 0x77FF FFFF	32M	VP0 Channel B Data
0x7800 0000 – 0x79FF FFFF	32M	VP1 Channel A Data
0x7A00 0000 – 0x7BFF FFFF	32M	VP1 Channel B Data
0x7C00 0000 – 0x7DFF FFFF	32M	VP2 Channel A Data
0x7E00 0000 – 0x7FFF FFFF	32M	VP2 Channel B Data
0x8000 0000 – 0x8FFF FFFF	256M	EMIF CEO
0x9000 0000 – 0x9FFF FFFF	256M	EMIF CE1
0xA000 0000 – 0xAFFF FFFF	256M	EMIF CE2
0xB000 0000 – 0xBFFF FFFF	256M	EMIF CE3
0xC000 0000 – 0xFFFF FFFF	1G	Reserved

4.1.3. External memory Interface

The DM642 EMIF Bus is 64-bits wide for direct connection to high speed synchronous memory. It has a maximum bus rate of 133 MHz. It has a memory controller than can interface to SDRAM, SRAM and FIFO. The EMIF signals are described in the table below.

Table 13: EMIF Signal Description

PIN	I/O/Z	DESCRIPTION
ECLKIN	I	EMIF A/B clock input.
ECLKOUT1,2	O/Z	EMIF A/B output clock at EMIF input clock frequency.
ED[63:0]	I/O/Z	EMIF 64 bit data bus I/O.
EA[22:3]	O/Z	EMIF external address output.
CEO[0:3}	O/Z	Active low chip select for memory space 0 to 3.
BEA[7:0]	O/Z	EMIF active low byte enables.
ARDY	I	Active high asynchronous ready input to insert wait states.
AOE/SDRAS/SOE	O/Z	Multiplexed active low: output enable (asynchronous)/ RAS signal/output enable (synchronous).
ARE/SDCAS/SADS/ SRE	O/Z	Multiplexed active low: read strobe (asynchronous)/ CAS strobe/memory address strobe (synchronous) or read enable.
AWE/SDWE/SWE	O/Z	Multiplexed active low: write strobe (asynchronous)/ SDRAM write enable/write enable (synchronous).
SDCKE	O/Z	EMIFA SDRAM clock enable.
SOE3	O/Z	EMIF A/B synchronous memory output enable for CE3.
HOLD	I	Active low external bus hold.
HOLDA	O	Active low external bus hold acknowledge.
BUSREQ	O	Active high bus request signal.
PDT	O/Z	Peripheral device transfer data.

The 64-bit EMIF bus is connected directly to the 32 MByte SDRAM. The DSP controls the operation of the SDRAM through the control signals in the table above. The DSP provides the RAS, CAS, WE, and clock to the SDRAM.

4.1.4. Boot Modes And Configuration

The DM642 boot mode selection and certain peripheral selections are determined at device reset. There are also some device configurations and peripheral selections that can be software configurable via the PERCFG peripheral configuration register after device reset. While the reset signal is low the DM642 is held in reset and is initialized to the configured reset state. The rising edge of reset starts the processor running with the boot configuration it is set for. The DM642 has three types of boot modes:

- Host Boot: If host boot is selected the CPU is stalled while the remainder of the device is released. During this period, an external host can initialize the CPU's memory space. The Phoenix PC/104-*Plus* defaults to this mode by setting the PCI_EN pin to logic 1 and booting from the host computer on the PCI Bus.
- EMIF Boot: If EMIF boot is selected the DM642 boots from an external EPROM. The 1 KByte ROM code located at CE1 is copied to address 0 by the EDMA using the default ROM timings, while the CPU is internally stalled. After the code is transferred the CPU is released and begins to execute the program from address 0.
- No Boot: With no boot the CPU begins direct execution from the memory located at address 0.

4.2. TMS320DM642 Boot and Device Configuration

The following configurations are latched during device reset:

Input Clock Mode: The on chip PLL frequency multiplier is configured through the CLKMODE input pins. The Phoenix PC/104-*Plus* is configured by resistor options for an X 12 operation. A 50 MHz external oscillator is provided for an internal operational frequency of 600 MHz.

Boot Configuration: The pull up and pull down resistors on the EMIF address bus pins AEA[22:21], determine the boot configuration. These two pins of each DSP have resistor pairs for selecting the Boot mode. They are set for the value 01 which selects Host Boot mode (based on the state of the PCI_EN bit).

Device Configuration: The DM642 device configurations are determined by the TOUT1/LENDIAN, GP0(3)/PCIEEAI, and the HD5 pins, and the pull up and pull down resistors on the EMIF address bus AEA[20:19] all of which are latched at device reset.

The table below describes these DM642 device configuration pins.

Table 14: DM642 Device Configuration Pins

Configuration Pin	Pin Number	Functional Description
TOUT1/LENDIAN	B5	Device Endian mode (LEND) 0: Big Endian mode 1: Little Endian mode
AEA[22:21]	[U23,V24]	Boot mode [1:0] 00 – No Boot 01 – HPI/PCI Boot 10 – Reserved 11 – EMIF Boot
AEA[20:19]	[V25,V26]	EMIFA input clock select AECLKIN_SEL = 00b: EMIF runs at AECLKIN rate AECLKIN_SEL = 01b: EMIF runs at 1/4 CPU clock rate AECLKIN_SEL = 10b: EMIF runs at 1/6 CPU clock rate AECLKIN_SEL = 11b: Reserved
GPO[3]/PCIEEAI	L5	PCI EEPROM Auto-Initialization (PCIEEAI) 0 – PCI auto-initialization through EEPROM disabled. 1 – PCI auto-initialization through EEPROM enabled. (PCI_EN must be = to 1).
HD5/AD5	Y1	HPI peripheral bus width (HPI_WIDTH) 0 – HPI operates at HPI16. (HPI bus is 16-bits wide. HD[15:0] are used, HD[31:16] in Hi-Z state) 1 – HPI operates as HPI32. (HPI bus is 32 bits wide. HP[31:0] are used).
PCI_EN; TOUT0/MAC_EN	[E2,C5]	Peripheral selection 00 – HPI (default mode) 01 – EMAC and MDIO 10 – PCI 11 – Reserved

4.2.1. Peripheral Selection At Device Reset

Some DM642 peripherals share the same pins (are internally muxed) and are mutually exclusive (HPI, GPIO [15:9], PCI and EEPROM, EMAC, MDIO and VIC). Other peripherals are always available (Timers, I2C0, GPIO[7:0]).

The following table shows which of the multiplexed peripherals are selected based on the state of PCI_EN and MAC_EN at reset.

Table 15: DM642 HPI, PCI, EMAC, MDIO and GPIO Selection

Peripheral Selection				Peripherals Selected					
PCI_EN Pin E2	PCI_EEAI Pin L5	HD5 PinY1	MAC_EN Pin C5	HPI Data Lower	HPI Upper	32-Bit PCI	EEPROM	EMAC MDIO	GPIO [15:9]
0	0	0	0	√	Hi-Z	Disabled	Disabled	Disabled	√
0	0	0	1	√	Hi-Z	Disabled	Disabled	√	√
0	0	1	0	√	√	Disabled	Disabled	Disabled	√
0	0	1	1	Disabled		Disabled	Disabled	√	√
1	1	X	X	Disabled		√	√	Disabled	Disabled

On the Phoenix PC/104-*Plus* the PCI_EN and the PCI_EEAI pins are pulled up high to select the 32-bit PCI mode, and GPIO pins 0 to 8 only. The HPI peripheral is disabled as well as GPIO bits [15:9].

4.2.2. Peripheral Selection After Device Reset

After device reset certain peripherals must be configured by writing to designated registers. They are the peripheral configuration register (PERCFG), the device status register (DEVSTAT), and the JTAG identification register (JTAGID).

The table below describes the Peripheral Configuration Register (PERCFG) Selection Bits.

Table 16: Peripheral Configuration Register Selection

BIT	NAME	DESCRIPTION
31:17:00	Reserved	Reserved. Read only, writes have no effect.
6	VP2EN	Video Port 2 (VP2) Enable bit. 0 = VP2 is disabled (default). 1 = VP2 is enabled.
5	VP1EN	Video Port 1 (VP1) Enable bit. 0 = VP1 is disabled (default). 1 = VP1 is enabled.
4	VP0EN	Video Port 0 (VP0) Enable bit. 0 = VP0 is disabled (default). 1 = VP0 is enabled.
3	I2COEN	Inter-IC 0 (I2C0) Enable bit. 0 = I2C0 is disabled (default). 1 = I2C0 is enabled.
2	McBSP1EN	Video Port 1(VP1) lower Data vs. McBSP1 Enable bit. 0 = VP1 lower data pins enabled (if VP1EN = 1), McBSP1 is disabled; VP1 upper data bits are dependent on McASP0EN and VP1EN bits. 1 = McBSP1 is enabled, VP1 lower data pins disabled.
1	McBSP0EN	Video Port 0 (VP0) lower Data vs. McBSP0 Enable bit. 0 = VP0 lower data pins enabled (if VP0EN = 1), McBSP0 is disabled; VP0 upper data bits are dependent on McASP0EN and VP0EN bits. 1 = McBSP0 is enabled, VP0 lower data pins disabled.
0	McASP0EN	McASP0 vs. VP0/VP1 upper data pins select bit. 0 = McASP0 is disabled; VP0 & VP1 upper data pins enabled. VP0 & VP1 lower data pins are dependent on McBSP0/1EN & VP0/1En bits. 1 = McASP0 is enabled. VP0 & VP1 upper data bits are disabled; VP0 & VP1 lower data bits are dependent on McBSP0/1EN & VP0/1EN bits.

4.2.3. Video Ports

The DM642 device has three configurable video port peripherals (VP0, VP1, and VP2). These video port peripherals provide a direct interface to common video decoders and encoders such as the Philips SAA7115H A/D on the Phoenix PC/104-*Plus* board. All three video ports have the capability to operate as a video capture port, a video display port, or a transport stream interface (TSI) capture port. The DM642 video port supports multiple resolutions and video standards (CCIR601, ITU-BT.656, BT.1120, SMPTE, 125M, 260M, 274M, and 296M).

4.2.3.1. Video Capture Mode

The video port provides the following functions when it is operating in the video capture mode.

- Capture Rate up to 80 MHz
- Two channels of 8/10-bit digital video input from a digital or analog (through a video A/D decoder) camera. Digital video input is in YCbCr 4:2:2 formats with 8 or 10 bit resolution multiplexed in ITU-R BT.656 format.
- One channel of Y/C 16/20-bit digital video in YCbCr 4:2:2 formats on separate Y and Cb/Cr inputs.
- YCbCr 4:2:2 to YCbCr 4:2:0 horizontal conversions and half scaling in 8-bit 4:2:2 modes.
- Direct interface for two channels of up to 10-bit or one channel of up to 20-bit raw video from A/D converters.

4.2.3.2. Video Display Mode

The video port provides the following functions when it is operating in the video display mode.

- Display rate up to 110 MHz
- One channel of continuous digital video output. Digital video output is YCbCr 4:2:2 with 8/10-bit resolution multiplexed in ITU-R BT.656 format.
- One channel Y/C 16/20-bit digital video output in YCbCr 4:2:2 formats on separate Y and Cb/Cr outputs.
- YCbCr 4:2:0 to 4:2:2 horizontal Conversions.
- Programmable clipping
- One channel of raw data output up to 20-bits. Two channel synchronized raw data output.
- Sync to external video controller

4.2.3.3. TSI Capture Mode

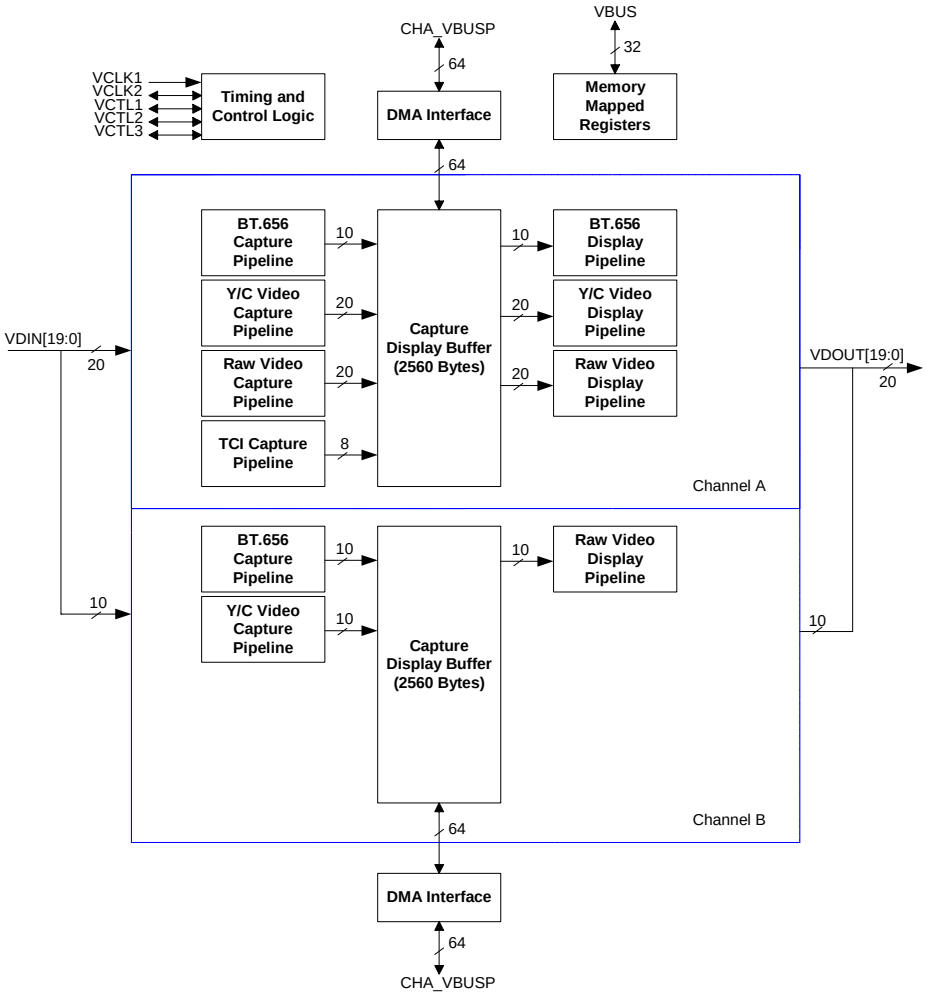
The video port provides the following functions when it is operating in the TSI Capture mode.

- Transport Stream Interface (TSI) from a front end device such as a demodulator or forward error correction device in 8-bit parallel format at up to 30 Mbytes per second

4.2.4. Video Port Architecture

A high level block diagram of the video port architecture is shown below.

Figure 3: Video Port Block Diagram



Each video port consists of two channels A and B with a 5120-byte capture or display buffer that can be split between the two channels. Both channels are always configured for either capture or display

only. Separate data pipelines control the formatting of capture or display data for each of the BT.656, Y/C, raw video and TSI modes.

For capture operation, the port may operate as two 8/10-bit channels of BT.656 or raw video capture, or as a single channel of 8/10-bit BT.656, 8/10-bit raw video, 16/20-bit Y/C video, 16/20-bit raw video, or 8-bit TSI.

For display operation, the port may operate as a single channel of 8/10-bit BT.656 display, or as a single channel of 8/10-bit BT.656, 8/10-bit raw video, 16/20-bit Y/C video, or 16/20-bit raw video display.

It may also operate in a two channel 8/10-bit raw mode in which the two channels are locked to the same timing.

Channel B is not used during single channel operation.

4.2.5. Phoenix PC/104-Plus Video Port Board Settings

The Phoenix board is designed such that four channels of video can be processed by the two DSPs. The design uses the fact that the DSP has three video ports of which two are used by the Phoenix PC/104-*Plus* design. One composite video channel is input into the video A/D SA7115H device. The video A/D decodes the composite video input and outputs the data to a Video Port 1 on the DSP. Video port 2 of each DSP likewise receives the output of another video A/D. The DSP can therefore process either one video channel at full D1 resolution, or two video channels at half D1 resolution.

Video port 0 of each DSP is configured as the McBSP. The McBSP of each DSP receives the audio stereo data from two A/D AKM AK5384 A/D devices which is driven as a serial TDM data stream.

4.2.6. General Purpose Input/Output (GPIO)

The GPIO peripheral provides sixteen dedicated general purpose pins that can be configured as either inputs or outputs. When configured as an output, the user can write to an internal register to control the state driven on the output pin. When configured as an input, the user detects the state of the input by reading the state of an internal register.

Most of the sixteen GPIO pins are multiplexed with other device pins. On the Phoenix PC/104-*Plus* which is configured for the PCI mode, GPIO bits 9:15 are used for PCI control signals and are not available as general purpose I/O.

GPIO bits 1 and 2 are multiplexed with CLKOUT4 and CLKOUT6 respectively. These pins are software configurable. To use these pins as GPIO pins the GPxEN bits in the GPIO Enable Register and the GPxDIR bits in the GPIO Direction Register must be properly configured. If GPxEN is set high then GPx pin is enabled. If GPxDIR is set high then the GPx pin is an output. If it is low then the GPx pin is an input.

GPIO bit 3 is multiplexed with the PCI EEPROM auto-initialization bit. Since the PCI enable bit (PCI_EN = 1) is set then this bit is not a general purpose bit. This bit establishes whether the PCI auto-initialization EEPROM is used. If the bit is set high the PCI auto-init is through the EEPROM. If the bit is clear then the PCI auto-init through the EEPROM is disabled. This is the default setting.

GPIO bits 4, 5, 6 and 7 are multiplexed with external interrupts EXT_INT4, 5, 6 and 7 respectively. When these pins function as external interrupts (by selecting the corresponding interrupt enable register bit IER[7:4]), they are edge driven interrupt inputs and the polarity can be independently selected via the interrupt polarity register bits EXTPOL[3:0].

GPIO bit 8 is multiplexed with PCI66. When PCI_EN is set high then this bit can select the operating frequency of the PCI bus. If the bit is set then the PCI bus operates at 66 MHz (default). If the bit is cleared then the PCI bus operates at 33 MHz. This bit is pulled up high on the board by jumper JP2 to ensure 33 MHz PCI bus operation.

Four GPIO bits from each DSP are connected to the 40-pin audio connector for general purpose I/O. Table 17 below shows which of the four GPIO bits from each DSP are connected to the audio connector.

Table 17: DSP GPIO Bits Connected To Audio Connector

Signal Name	DSP Name	J2 Pin #
GPIO5_DSP1	GPO5	33
GPIO2_DSP1	CLKOUT6_GPO2	34
GPIO1_DSP1	CLKOUT4_GPO1	35
GPIO0_DSP1	GPO0	36
GPIO5_DSP2	GPO5	37
GPIO2_DSP2	CLKOUT6_GPO2	38
GPIO1_DSP2	CLKOUT4_GPO1	39
GPIO0_DSP2	GPO0	40

4.2.7. Multichannel Buffered Serial Port (McBSP)

The multi-channel buffered serial port (McBSP) is based on the standard serial port interface. The McBSP provides the following functions:

- Full-duplex communication
- Double buffered data registers for a continuous data stream
- Independent framing and clocking for receive and transmit
- Direct interface to industry standard codecs, analog interface chips, and other serially connected A/D and D/A devices
- External shift clock or an internal programmable frequency shift clock for data transfer
- Auto-buffering capability through the 5-channel DMA controller.

The McBSP consists of a data path and a control path which connect to external devices. Data is communicated via a Receive clock (CLKR) and a transmit clock (CLKX). Control information (clocking and frame synchronization) is transmitted with four other pins: Received serial data (DR), Transmitted serial data (DX), Receive frame synchronization (FSR), and Transmit frame synchronization (FSX).

Data is sent to devices interfacing to the McBSP via the DX and DR pins. Control information is sent via the CLKX CLKR, FSX, and FSR pins. The DM642 DSP communicates to the McBSP via 32-bit wide control registers accessible via the internal peripheral bus. Either the CPU or the DMA/EDMA controller reads the received data fro the Data receive register (DRR) and writes the data to be transmitted to the Data Transmit Register (DXR). Data in the DXR is shifted out by the DX pin via the Transmit Shift Register (XSR). Data received on the DR pin is shifted into the RSR and copied into the Receive Buffer Register (RBR). RBR data is copied to the DRR which can be read by the CPU or the DMA/EDMA.

The Phoenix PC/104-*Plus* utilizes one of the two serial ports of the DSP (McBSP0) for the stereo audio inputs. McBSP0 is multiplexed with pins from the DSPs Video Port 0.

Two Audio A/D devices are cascaded together to convert four stereo audio channels into a TDM serial data format TDM256 mode. The Serial Time Domain Output (STDO1) pin of A/D number 2 outputs eight channels (four stereo left and right) of TDM data, four from each A/D into the DSP. The DSP must then process the serial data and time stamp each audio channel to the corresponding video channel.

4.2.8. Multichannel Audio Serial Port (McASP)

The Multichannel Audio Serial Port (McASP) operates as a general purpose audio serial port. The McASP consists of independent transmit and receive sections that have separate master clocks, bit clocks, and frame syncs with different transmit modes and bit stream formats. The transmit and receive sections may operate independently or synchronized. In addition, all the McASP pins can be configured as general purpose I/O (GPIO) pins.

The McASP is designed to connect to audio D/A converters, codecs, digital audio interface (DIR) receivers, and SPDIF transmit physical layer components.

4.3. SDRAM

The Phoenix PC/104-*Plus* provides 32 MBytes of SDRAM per DSP. The SDRAM Bus is unbuffered from the DM642 DSP and is composed of two 4M X 32-Bit SDRAM devices and configured as 4MBytes x 64-Bit words. The SDRAM consists of two 1 Meg X 4 banks X 32-Bit 133 MHz SDRAM chips, MT48LC4M32B2-FC-7, by Micron. The device has the following features:

- Fully Synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle.
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge, includes Concurrent Auto Precharge, and Auto Refresh Modes
- Self refresh Modes
- 64 ms, 4.096-cycle refresh (15.6 µs/row)
- Supports CAS Latency of 1, 2, and 3

4.4. Video

4.4.1. Input Connector

The Phoenix PC/104-*Plus* board inputs the four video channels on four high quality RF SMC connectors. The SMC is a screw on connector where the two connector parts are plugged together and secured by means of a screw on coupling. The connection is vibration proof and suited for mobile applications.

4.4.2. Video Input Ports

The Phoenix PC/104-*Plus* supports four video inputs which are transmitted to the board with a 75 ohm coax cable to a high quality RF SMC connector. The four SMC coax inputs support four composite video channels. Each of the four A/D devices receives one composite video channel and transmits the data to the DSP for further processing.

The DSP receives two video streams at two of its video ports. The DSP can either process one of the video streams at full D1 performance or it can process both video channels at a reduced half D1 performance.

4.4.3. Phillips SAA7115 Video Decoder

The PAL/NTSC/SECAM video decoder IC, Philips SA7115H is a video capture device which includes an adaptive PAL/NTSC comb filter, VBI-data slicer, anti-aliasing filter, 9-bit A/D converters, and Automatic Gain Control (AGC). The SA7115H accepts analog inputs CVBS or S-Video (Y/C) from a TV or VCR source and supports 8 or 16-bit wide output data with auxiliary reference data for interfacing to VGA controllers.

The device is programmed through the I2C bus with full write and read capability for all programming registers with a bit rate up to 400 Kbits per second.

4.5. Audio

4.5.1. Input Connector

The Phoenix PC/104-*Plus* board receives eight audio stereo channels and eight general purpose I/O signals on a Molex vertical dual row SMT 40-pin wire to board header. The mating connector houses individually crimped wires. This provides individual shielding for each audio left and right signal. *See section 3.3 for the correct pinout.*

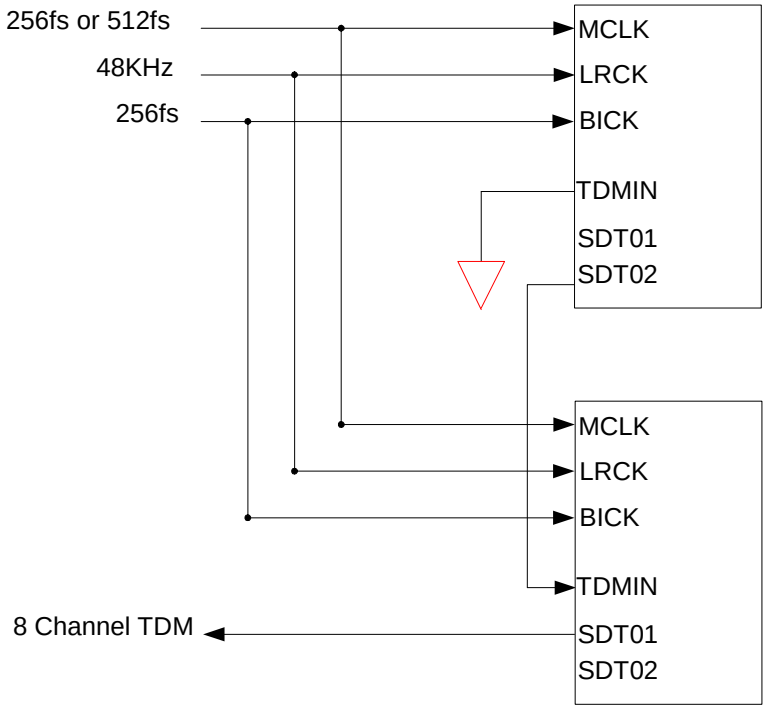
4.5.2. Audio Codec

The Phoenix PC/104-*Plus* board receives eight stereo audio channels at the Molex connector. Each audio input is transmitted to an AK5384 107 db 24-bit 96 KHz 4-channel A/D converter. The A/D has a wide sampling rate of 8 KHz to 96 KHz and is suitable for multi-channel audio systems. The AK5384 achieves high accuracy by using enhanced dual bit Sigma Delta techniques. The Phoenix PC/104-*Plus* board transmits two stereo channels to each A/D for processing.

The AK5384 is operated in the Cascade TDM mode. Two devices are cascaded together in a daisy chain configuration at TDM256 mode.

Figure 3 shows how the two AK5834 A/D devices are connected together.

Figure 4: Two AK5384 A/D devices connected in the Cascade TDM Mode



The serial data stream that is output from the second A/D contains all four stereo channels in a time domain multiplexed output format shown in Figure 4 below.

Figure 5: Cascade TDM Timing

L1	R1	L2	R2	L3	R3	L4	R4

The DSP shall process the serial audio data and combine the corresponding audio with its video data.

4.6. The Board – PC/104-Plus Form Factor

The Phoenix PC/104-*Plus* was designed in accordance with the PC/104-*Plus* standard form factor. The standard was sponsored by the PC/104 Embedded Consortium. The paper defines the mechanical and electrical specifications for a compact version of a PCI board. The PC/104 was originally designed for the ISA Bus. The specification is known as PC/104 because of the 104 signal contacts on the two bus connectors P1 and P2 of the ISA Bus. The PC/104-*Plus* specification adds support for the PCI Bus. The PC/104 boards are designed with a reduced form factor and have a self stacking bus to eliminate the need for back planes and card cages.

The PC/104 specification defines the module dimensions for a single board PC/104 which is 3.8 inches deep and 3.6 inches wide. It also defines the location space for the connectors and the height restrictions for the components on board and the pinout assignment for the ISA and PCI buses. Four PCI modules are allowed in a PC/104-*Plus* stack.

The Phoenix PC/104-*Plus* module implements only the PCI bus. The board shall provide the ISA connector for a pass through of the ISA Bus. There are no ISA devices on the board.

4.6.1. The PCI Bus

The Phoenix PC/104-*Plus* board implements the PCI Bus as written in the PCI Local Bus Specification Revision 2.2. The PCI Local Bus is a 32-bit or 64-bit bus with multiplexed address and data lines. The PCI Bus consists of 32 or 64 bits of data, plus control signals. The PCI signals are shown below in Table 18.

Table 18: PCI Bus Signal Description

Pin Name	#	Dir	Technology	Functional Description
PCI_CLK	1	I	PCI 3.3V	**PCI Clock**—Provides timing for all PCI transactions and is an input to all PCI devices. The rising edge of this clock defines all other timing parameters and most PCI signals are sampled on it (except: PCI_RST_N & PCI_INTA_N).
PCI_IDSEL	1	I	PCI 3.3V	**Initialization Device Select**—Used as a chip select during configuration read and write transactions.
PCI_AD	64	I/O	PCI 3.3V	**Address/Data Bus**—Address and Data are multiplexed on the same PCI pins. A bus transaction comprises an address phase followed by a one or more data phases. PCI supports both read and write bursts.
PCI_CBE_N	8	I/O	PCI 3.3V	**Bus Command and Byte Enable lines**—Active Low. These are multiplexed on the same PCI pins. Bus Command during the address phase; Byte Enables during the data phase.
PCI_PAR	1	I/O	PCI 3.3V	**Parity**—Parity is even across PCI_AD & PCI_CBE_N. Parity generation is required by all PCI agents.
PCI_FRAME_N	1	I/O	PCI 3.3V	**Cycle Frame**—Active Low. This is driven by the current master to indicate the beginning and duration of an access and rescinded at the end of the transaction.
PCI_TRDY_N	1	I/O	PCI 3.3V	**Target Ready**—Active Low. Indicates the target agent's (selected device's) ability to complete the current data phase of the transaction
PCI_IRDY_N	1	I/O	PCI 3.3V	**Initiator Ready**—Active Low. Indicates current bus master's ability to complete the current data phase of the transaction.
PCI_STOP_N	1	I/O	PCI 3.3V	**Stop**—Active Low. Indicates the current target is requesting the master to stop the current transaction.
PCI_DEVSEL_N	1	I/O	PCI 3.3V	**Device Select**—Active Low. Indicates the driving device has decoded its address as the target of the current access.
PCI_REQ_N	1	O	PCI 3.3V	**Request**—Active Low. Indicates to the arbiter that this agent desires use of the bus. This is a point-to-point signal.
PCI_GNT_N	1	I	PCI 3.3V	**Grant**—Active Low. Indicates to the agent that access to the bus has been granted.
PCI_PERR_N	1	I/O	PCI 3.3V	**Parity Error**—Active Low. Used only for the reporting of data parity errors during all PCI transactions except a Special Cycle.
PCI_SERR_N	1	OOD		**System Error** (Open Drain)—Active Low. Used for reporting address and data parity errors, on the Special Cycle command, or any other system error where the results will be catastrophic.
PCI_INTA_N	1	OOD		**Interrupt A** (Open Drain)—Active Low. Asynchronous to PCI_CLK. A device asserts this interrupt when requesting attention from its device driver.
PCI_RST_N	1	I	PCI 3.3V	**PCI Reset**—Active Low. Brings PCI-specific registers and signals to a consistent state

4.6.2. Signal Grouping

A means of selecting the appropriate signals has been established that allows installation and configuration of add-in Phoenix PC/104-*Plus* modules. Figure 6 shows the method:

Figure 6: PCI Signal Select

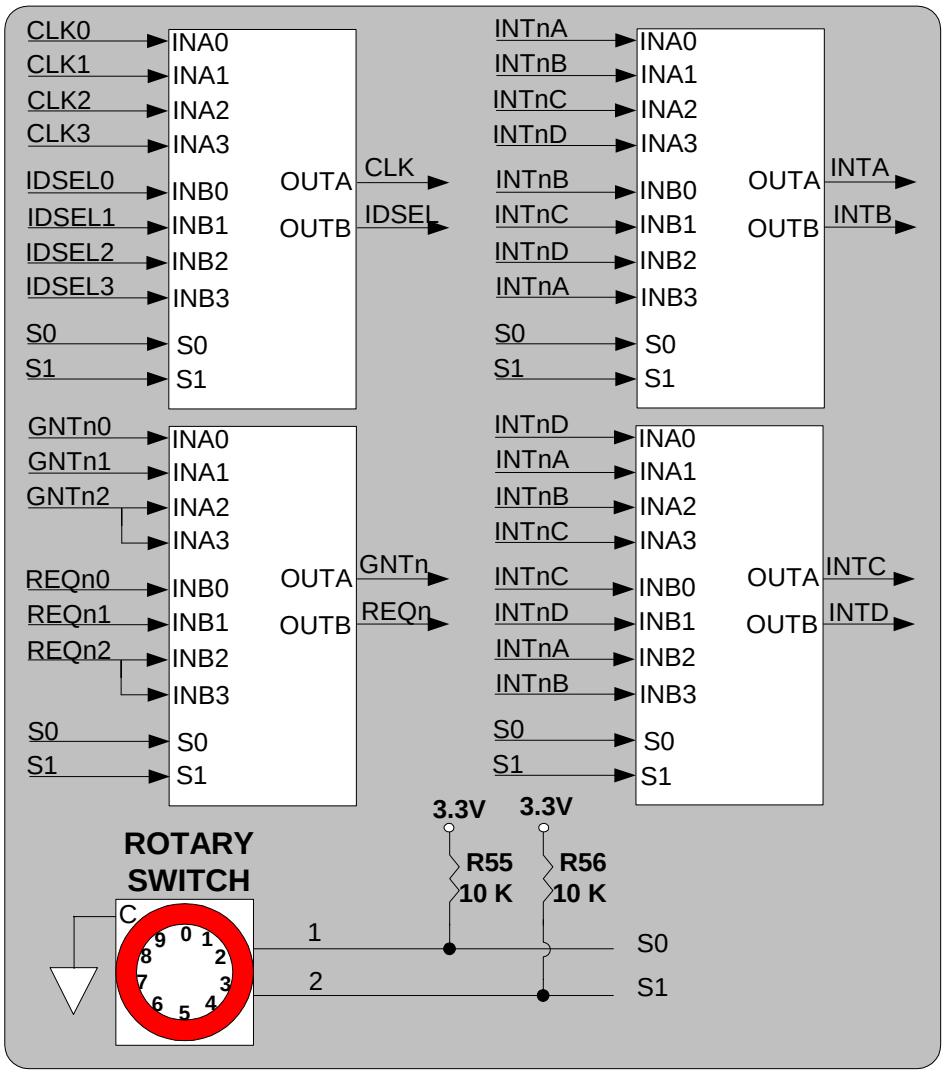


Figure 6 shows the multiplexer chips used to provide the signal select lines for add on Phoenix PC/104-*Plus* boards. The rotary switch controls the select lines to the multiplexer chips. Table 19 shows the rotary switch settings.

Table 19: Rotary Switch Settings

Switch Position	Module Slot	REQ	GNT	CLK	IDSEL	ID Address	INT0	INT1	INT2	INT3
3, 7	1	REQ0	GNT0	CLK0	IDSEL0	AD20	INTA	INTB	INTD	INTC
2, 6	2	REQ1	GNT1	CLK1	IDSEL1	AD21	INTB	INTC	INTA	INTD
1, 5, 9	3	REQ2	GNT2	CLK2	IDSEL2	AD22	INTC	INTD	INTB	INTA
0, 4, 8	4	REQ2	GNT2	CLK3	IDSEL3	AD23	INTD	INTA	INTC	INTB

4.6.3. PCI 66 MHz Support

The PC/104-*Plus* board can support a 66 MHz PCI Bus. Since the system at present does not support the 66 MHz speed a jumper JP2 has been installed which pulls up the PCI66 signal of the DSPs to a logic high when the jumper is installed. This causes the DSPs PCI bus to operate at 33 MHz. In the future if the system has been upgraded to support 66 MHz then the jumper shall be removed and the board will support 66 MHz.

4.7. PCI BRIDGE

The PLX PCI 6152 is designed for applications that require high performance 32-bit PCI expansion. It is compatible to the Intel 21152 PCI to PCI bridge but is available in a small BGA package and is lower in power.

The Phoenix PC/104-*Plus* board is connected in a PC/104 stack to a host board with the PCI signals connected to the 120-pin J3 connector. The primary PCI Bus connects between J3 to the primary side of the PCI 6152 PCI to PCI Bridge. The secondary side of the PCI 6152 bridge connects to the two DM642 DSPs.

The PCI 6152 PCI to PCI Bridge is a transparent bridge which provides arbitration support for up to four secondary PCI devices and is fully compliant with PCI Local Bus Specification Revision 2.1. The PCI 6152 provides full support for delayed transactions, enabling buffering of memory read, I/O, and configuration transactions. The PCI 6152 supports bi-directional buffering of simultaneous multiple posted write and delayed transactions.

The PCI bridge is a transparent device. With the Phoenix PC/104-*Plus* connected to the system the host (system BIOS) shall see an additional two PCI devices which are the DSP chips. The PCI bridge supports clock frequencies up to 33/66 MHz at 32-Bits.

The secondary VIO pin (S_VIO) is connected to the 3.3V supply.

4.8. Power Supplies

The Phoenix PC/104-*Plus* board receives its power from the ISA connector. The ISA connector provides a 5V supply to the card. The board uses DC to DC switching power supplies to create all the voltages on the board. The board uses 3.3V for most of the devices on board. In addition the DSP requires 1.4V for its core voltage.

4.8.1. Power-On Reset

A Maxim reset device MAX6412 is provided on the board to perform a power on reset function. The MAX6412 is a microprocessor voltage monitor with a manual reset pin. The supervisor chip asserts a reset signal whenever the supply voltage falls below its threshold voltage. The reset output timeout period is externally set by a capacitor.

There is a pushbutton reset switch, SW1, which when activated will assert reset.

The reset output is driven to the two DSPs

The reset signal is driven on the board by two FET drivers.

4.8.2. Switches

Switches on the board include:

- Power On Reset – momentary push-button switch [SW1]
- JP1 is a 4-pin header which is used to select the DSPs functional mode of operation. The board is shipped without any jumpers. This default mode is the Emulation/Normal Mode of the device. In order to run the JTAG Boundary Scan function on the DSP a jumper must be placed between pins 1 and 2 and between pins 3 and 4. Pin 4 is the DSPs EMU0 pin while pin 2 is EMU1. The jumpers pull down EMU0 and EMU1 placing the DSP in the Boundary Scan/Normal mode of operation.
- J6 is a 14-pin header for the DSPs JTAG.
- JP2 is the jumper which selects the PCI speed of operation. If the jumper is present the PCI bus operates at 33 MHz. If the jumper is removed, the bus operates at 66 MHz.
- U76 is a rotary switch which is the means of conveniently selecting the signals for the configuration of additional PC/104-*Plus* modules in the system.

4.9. Indicators

LED indicators on the board are included for software convenience and for a power on condition. The power on indicator DS1 is connected to the 3.3V supply, DS2 is connected to the 5V supply.

Each DSP has one LED indicator connected to the timer output signal TOUT1. The following table shows the LED corresponding to the DSP.

Table 20: DSP LEDs

DSP	TOUT1
1	DS3
2	DS4

4.10. Clocks

The Phoenix PC/104-*Plus* provides two oscillator devices on board for separate control of the speeds of EMIF and the system clock of the DSP.

The oscillator used for EMIF is a 133 MHz oscillator. The oscillator output is sent to an ICS9112-16 Low Skew Clock Buffer. The output of the clock buffer is driven to the clock input of the EMIF of each DSP.

The second oscillator is the 50 MHz system clock. This oscillator is also driven to an ICS9112-16 clock buffer and then driven to the two DSPs.

The 50 MHz clock is transmitted to the PLL CLKIN input of the DSP. The PLL multiplies the clock frequency to generate the internal CPU clock. The DSP is configured by pins CLKMODE0 and CLKMODE1 for a factory set value of 10. This mode sets the internal PLL multiply factor to be X 12 for an internal operational frequency of 600 MHz.

The following table shows the CLKMODE0 and CLKMODE1 PLL Multiply Factor options to set the DM642 device to one of the valid PLL multiply clock modes.

Table 21: PLL Multiply Factors

CLKMODE1	CLOCKMODE0	CLKMODE (PLL Multiply Factors)	CLK Range MHz.	CPU Clock MHz.
0	0	Bypass (x1)	30-75	30–75
0	1	x6	30-75	180–450
1	0	x12	30-50	360–600
1	1	Reserved		

The third oscillator is the 27 MHz video clock. This oscillator is also driven to an ICS9112-16 clock buffer and then driven to all four SA7115H video A/D devices.

4.11. JTAG Connectors

The Phoenix PC/104-*Plus* contains a JTAG Header for emulation of the two DSPs. DSP JTAG connector J5 is the JTAG header for the DSP emulator chain.

4.11.1. DSP JTAG: J5

The J6 connector is a Samtec part number TSM-107-01-T-DV which is the standard 14 pin header that mates with the emulator connector.

The TDI signal is driven to the first DSP in the chain—DSP1. The TDO output is driven by the DSP to the TDI of the second DSP. The TDO of the second DSP is driven to the J5 DSP JTAG header.

5. Appendix A—Board Layout

5.1. Layout

Figure 7: The Phoenix PC/104-*Plus* board—Connector Side

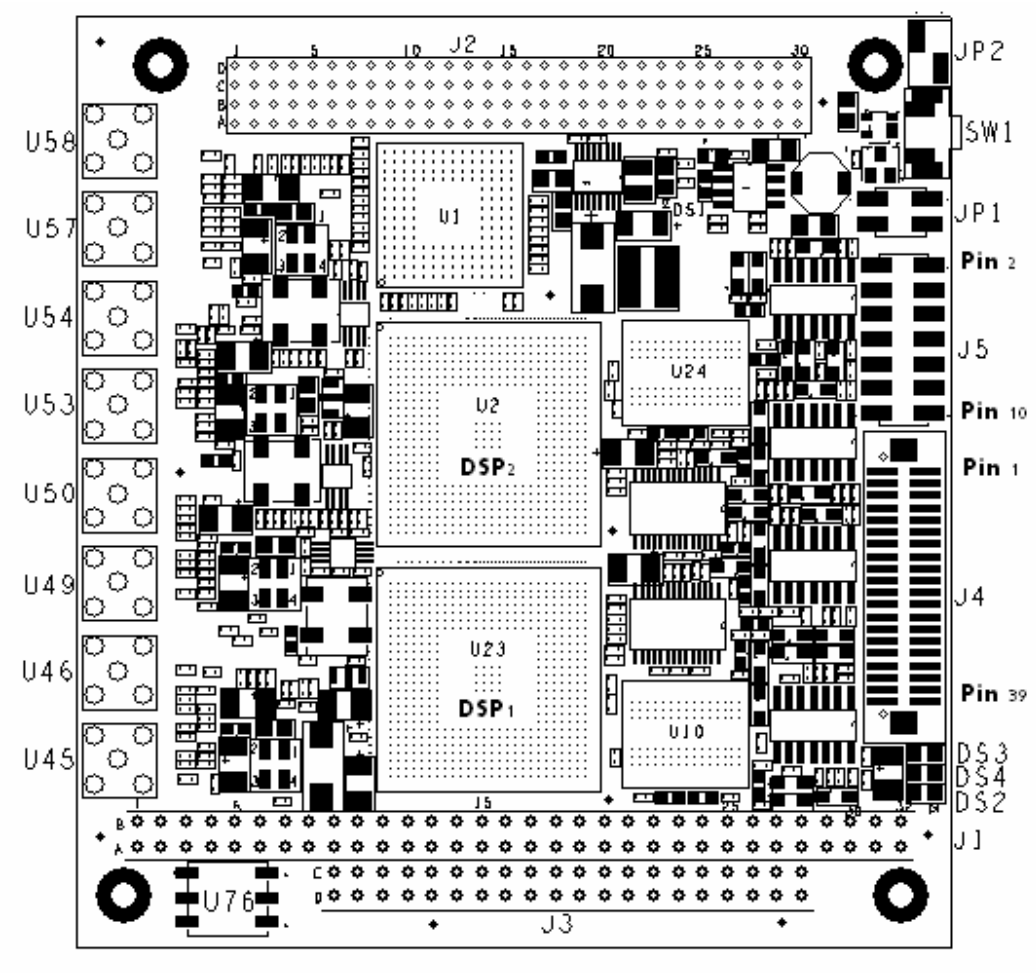


Figure 8: The Phoenix PC/104-*Plus* Board – Reverse Side