EE303 Digital System Prof. Y. Shin

Fall 2018

Final Exam

December 11, 2018

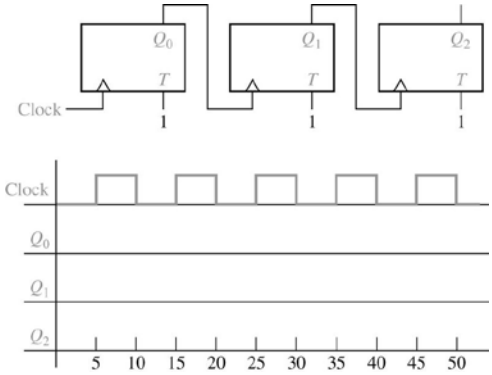
Name _____

Student ID _____

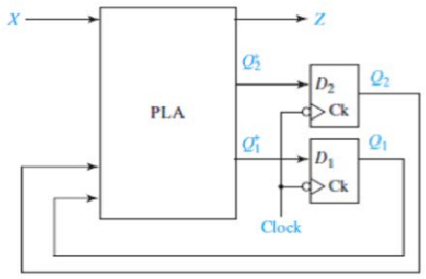
Problem	Max Points	Your Points
1	15	
2	10	
3	15	
4	10	
5	15	
6	10	
7	25	
8	20	
Total	120	

1. A reset-dominant flip-flop behaves like an S-R flip-flop, except that the input S = R = 1 is allowed, which causes the flip-flop to be reset.
   (a) Derive the characteristic equation. [5 pts]
   (b) Show how a reset-dominant flip-flop can be constructed by adding gates to an S-R flip-flop. [10 pts]

2. The following is a 3-bit ripple counter. Assume $Q_0 = Q_1 = Q_2 = 0$ at $t = 0$, and assume each flip-flop has a delay of 1 ns from the clock input to the Q output. Fill in Q_0, Q_1, and Q_2 of the timing diagram. [10 pts]



3. For the following sequential circuit, the table gives the contents of the PLA. (All PLA outputs are 0 for input combinations not listed in the table.)
   (a) Construct a state transition table and draw a state transition graph. [5 pts]
   (b) Complete the timing diagram below for the input sequence X = 10011. Assume that initially $Q_1 = Q_2 = 0$. [5 pts]
   (c) Identify any false outputs in the timing diagram. What is the correct output sequence for Z? [5 pts]



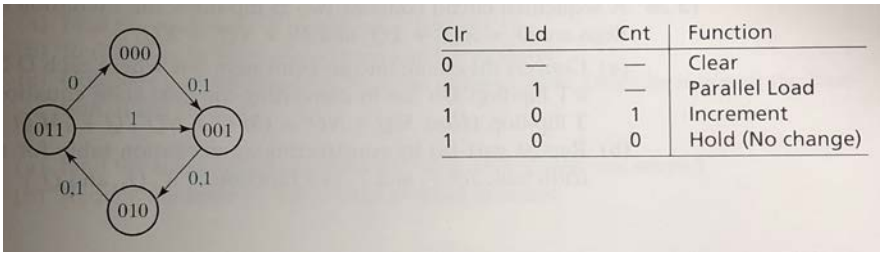
X	Q_1	Q_2	D_1	D_2	Z
0	1	–	1	0	0
1	0	1	1	0	0
0	0	1	0	1	1
1	0	0	0	1	1
1	1	0	0	0	1

4. A sequential circuit with one input and one output is used to stretch the first two bits of a 4-bit sequence as follows:

Input	Output
00XX	0000
01XX	0011
10XX	1100
11XX	1111

After every 4 bits, the circuit resets. Find a Mealy state transition graph (minimum number of states) and state table for the circuit. [10 pts]

5. A state graph for a single-input sequential circuit is given. Implement the circuit using a three-bit parallel loading counter that has the given operation table. Label the counter outputs Q_2, Q_1, Q_0, where Q_0 is the least significant bit and the parallel inputs P_2, P_1, P_0. [15 pts] <Hint: Derive the expressions for Clr, Ld, and Cnt>



Clr	Ld	Cnt	Function
0	—	—	Clear
1	1	—	Parallel Load
1	0	1	Increment
1	0	0	Hold (No change)

6. Consider the following two state assignments. The one on the right corresponds to the one on the left with A being complemented. Explain why the two state assignments can be considered equivalent. Assume D flip-flops. [10 pts]

PS (AB)	NS (A'B') X=0	NS (A'B') X=1	PO X=0	PO X=1
00 S_0	00 S_0	01 S_1	0	1
01 S_1	11 S_2	01 S_1	0	0
11 S_2	00 S_0	01 S_1	0	0

PS (AB)	NS (A'B') X=0	NS (A'B') X=1	PO X=0	PO X=1
10 S_0	10 S_0	11 S_1	0	1
11 S_1	01 S_2	11 S_1	0	0
01 S_2	10 S_0	11 S_1	0	0

7. Consider an iterative circuit. The output Z is 1 iff at least one of the (n-bit) X inputs is 1, and no group of two or more consecutive 1 inputs occurs.

   Example:

   0 0 1 0 1 0 0 0 1 0 0 gives an output $Z = 1$
   0 0 1 0 1 1 0 0 0 0 0 gives an output $Z = 0$

   (a) Derive a state table for a "cell". Use minimum number of states. [10 pts]
   (b) Derive the equations for the outputs of a cell & implement a cell using NOR gates and inverters. Derive the output circuit (for Z) as well. [10 pts]
   (c) Draw the sequential version of this iterative circuit. [5 pts]

8. Design a controller for an odd-parity generator. The circuit should transmit 7 bits from a shift register onto the output X. Then, on the next clock cycle, the eighth value of X should be chosen to make the number of 1's (in whole 8 bits) be odd. In other words, the last value of X should be 1 if there was an even number of 1's in the shift register, so that the 8-bit output word will have odd parity. The circuit is shown below. K will be 1 when the counter reaches 111.
   (a) Give the state graph for the controller (three states). [10 pts]
   (b) Implement the controller using D flip-flops and any necessary gates. Use a one-hot state assignment. [10 pts]