EE303A Digital System Design

Midterm

9:00 AM - **11:45** AM, April 21st, 2022

ID:

Name:

	Prob. 1	Prob. 2	Prob. 3	Prob. 4	Prob. 5	Total
Score	/80	/20	/30	/20	/30	/180

Read carefully before starting exam:

- You must stay until the exam is complete.
  - ✓ Write your answer **from 9:00 AM - 11:30 AM**. Do not touch your phone during this time.
  - ✓ Photograph and submit your answer **from 11:30 AM to 11:45 AM.** Do not write anything on your answer sheet during this time.
  - ✓ You must submit your answer to jmj0313@kaist.ac.kr **before 11:45 AM**.
- You can write your answers on any blank A4 sheet of paper.
  - ✓ Write your name/ID in each sheet
- If you have any questions, raise your hand.
- You must show all work.
  - ✓ Solutions without supportive work may not receive full credit.

Use complementary input or output variables (e.g. A', f') where necessary, unless otherwise specified.

Simplify the equations and logic diagrams for full credit, unless otherwise specified.

Use the minimum number of gates for full credit, unless otherwise specified.

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1. [Total 80 Pts.] Variants of the problems provided in the course materials.

   (a) [10 Pts.] Add 11 + (-31) in binary, using the 2's complements to represent negative numbers and a word length of 7 bits (including sign). Discuss whether the 7-bit result is correct.

   (b) [20 Pts.] Derive the most simplified expression in (i) sum-of-products and (ii) product-of-sums forms with the Karnaugh map below.

ab \ cd	00	01	11	10
00	0	1	0	0
01	0	1	0	0
11	1	1	1	1
10	1	1	0	1

   (c) [20 Pts.] Given: f(a,b,c,d) = $\sum m(0,1,2,4,5,9,11,13,15)$.

   Note: Do not use inverters. Use complementary input/output variables (e.g. a', f') where necessary.

   (i) Implement f using 2-input AND and 2-input OR gates.

   (ii) Convert the circuit in (i) to a circuit using only 2-input NOR gates.

   (d) [20 Pts.] Consider the block diagrams shown below.

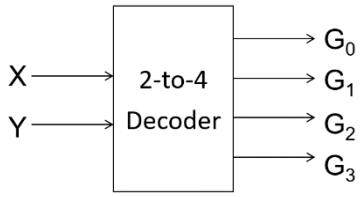


Fig. 1A.

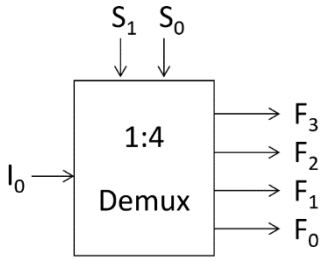


Fig. 1B

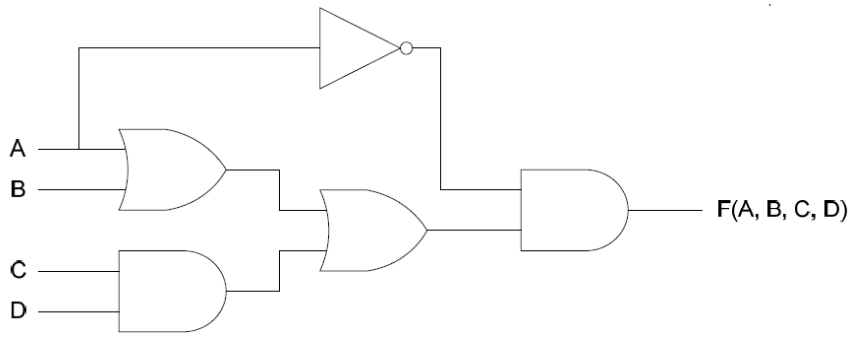
   (i) Implement the 2-to-4 decoder (Fig.1A) using 2-input AND gates and inverters. Give its truth table.

   (ii) Implement the 1-to-4 demultiplexer (demux; Fig.1B) using the block diagram for the decoder in Fig. 1A, 2-input AND gates, and new signals where necessary. Give its truth table.

(e) [10 Pts.] Write the simplified Boolean equations of the circuit whose output (f_1 and f_2) are defined by the following truth table. Note that the output may be undefined for some of the input combinations. Simplify the equations for full credit.

a	*b*	*c*	f_1	f_2
0	0	0	1	1
0	0	1	0	1
0	1	0	1	0
0	1	1	1	1
1	0	0	1	0
1	0	1	0	1
1	1	1	1	0

2. [Total 20 Pts.] Convert the circuit shown below to a similar one using only 2-input NAND gates. Do not use inverters. Do not use complementary inputs or outputs.



3. [Total 30 Pts.] Consider the function F(x,y,z,w) = Σm(1,4,7,9,14) with don't care conditions d(x,y,z,w) = Σd(0,3,5,6,12). Justify your answers by using Karnaugh maps.
(a) Find all prime implicants.

(b) Find all essential prime implicants.

(c) Give the minimal sum of products expression for F.

4. [Total 20 Pts.] Using the Boolean Postulates and Theorems, show that
(c'+abd+b'd+a'b)(c+ab+bd) = d(b+c)+ b(a+c)(a'+c').

Note: Show each step.

5. [Total 30 Pts.] Students have only one 8-bit adder (Fig. 2A) that takes two 8-bit operands, A(=$a_7a_6a_5a_4a_3a_2a_1a_0$) and B(=$b_7b_6b_5b_4b_3b_2b_1b_0$), and produces one 8-bit output, S(=$s_7s_6s_5s_4s_3s_2s_1s_0$) = A + B. You can ignore carry out of A + B.

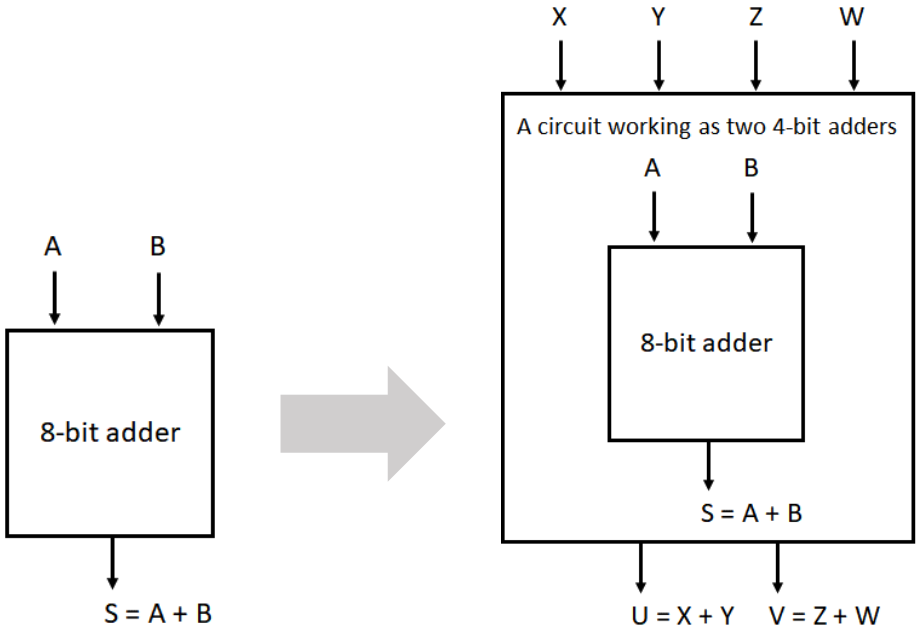


Fig. 2A. 8-bit adder

Fig. 2B. Your design

Using the 8-bit adder and other logic gates (e.g. XOR), students need to design a digital circuit that has the same functionality as two 4-bit adders (Fig. 2B). Your design will receive four 4-bit operands, X(=$x_3x_2x_1x_0$), Y(=$y_3y_2y_1y_0$), Z(=$z_3z_2z_1z_0$), and W(=$w_3w_2w_1w_0$), and must produce two 4-bit outputs, U(=$u_3u_2u_1u_0$) = X + Y and V(=$v_3v_2v_1v_0$) = Z + W. You can ignore carry out of X + Y and Z + W.

Design the circuit by defining Boolean expressions of each bit of A, B, U, and V in terms of X, Y, Z, W, S, and logic 0 or 1 level (e.g. $v_2 = s_2$. $a_3 = 0$).

Note: There may be many different solutions. Use one 8-bit adder and other logic gates. Keep your design simple for full credit.