



EE203B Digital System
Spring 2008

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Midterm Exam
April 4, 2008

Name _____

Student ID _____

Notes:

- Turn-off your cell phone.
- Do not use calculator or any other electronic devices.
- Max point assigned to each problem is roughly proportional to amount of time I predict you (unless you are too bad) to spend.
- Up to 3-hours (10 am ~ 1 pm) are allocated for this exam, but you are allowed to hand in your solution sheet early and leave the room (at your own risk) when you think you are done.
- Write down (clearly) on this sheet.
- HAVE FUN !!

Question	Max Points	Score
1	20	
2	15	
3	20	
4	25	
5	10	
6	30	
Total	120	

1 Answer the followings:

(a) Prove (in algebraic way) that functions f and g are equal ($f = g$) if $A \text{ XNOR } B = 0$.

$$f(A, B, C, D) = AC'D' + A'B'CE + A'BCE + ABC + DE' + BCD + AB'D'E$$

$$g(A, B, C, D) = BC'D' + A'B'CDE + A'CE + ABCE + AB'DE' + ACDE$$

[10 pts]

(b) Prove (in algebraic way) that $ab + c'(a' + d') = ab + bd + b'd' + a'c'd$, if $a'b + cd' = 0$. [10 pts]

2 Imagine that we just invented (for fun) a new gate, called T-gate (do not spend time to think about why it is T!). It has 4 inputs and 1 output. Its function is described by following minterm expansion:

$$T(A, B, C, D) = \Sigma m(7, 13, 14, 15)$$

Implement the function $f(A, B, C, D) = \Sigma m(0, 1, 3, 5, 6, 7, 9, 10, 12, 14, 15)$ using only T-gates and OR gates. Assume that both variables and their complements (A' , B' , C' , D') are available. Show the connection of gates. [15 pts]

3 Answer the followings:

(a) Simplify following functions using Q-M method. [15 pts]

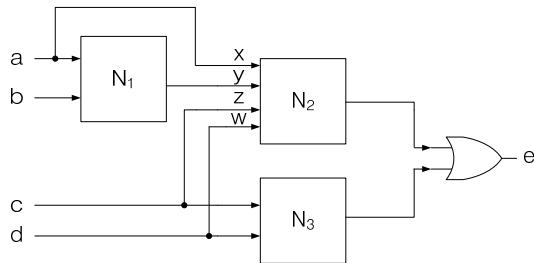
$$F1(A, B, C) = \Sigma m(1, 4, 6) + \Sigma d(2, 5)$$

$$F2(A, B, C) = \Sigma m(0, 6) + \Sigma d(7)$$

$$F3(A, B, C) = \Sigma m(1, 4, 7) + \Sigma d(5)$$

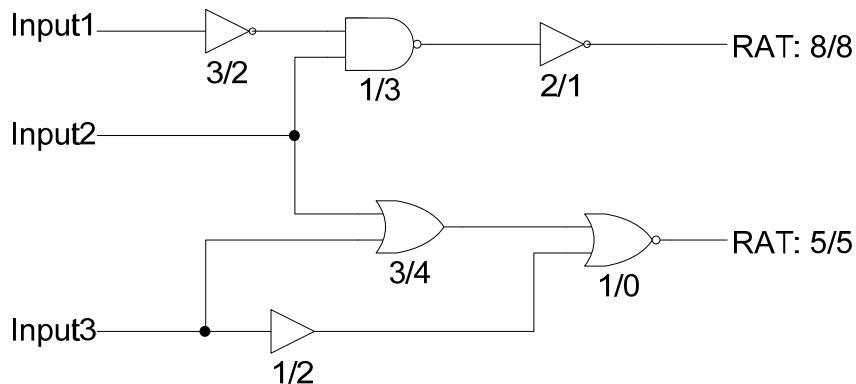
(b) Realize the same functions with a minimum two-level NAND-NAND circuit. [5 pts]

- 4 In the following circuit, illustrated by a connection of blocks, we try to design block N_2 .



- (a) N_2 is given by $\Sigma m(1, 5, 7, 10, 13)$. Derive simplified POS. [5 pts]
- (b) Assume that N_1 is an OR gate. Using this fact, realize N_2 using only 2-input NAND and INV. [10 pts]
- (c) Assume that N_3 is an AND gate. Using the knowledge of N_1 from (b) and N_3 , derive the simplified expression for N_2 . Draw the connection of gates for whole circuit (minimize the number of gates). [10 pts]

- 5 For the following circuit, we want to assign "signal arrival times" at all three inputs so that the slacks at two outputs become 0 (i.e. our circuit becomes very tight in terms of delay). Derive arrival times at three inputs. A pair of numbers of each gate indicates its delay for rising and falling input, respectively; those at the outputs are "required arrival times" for rising and falling signals. [10 pts]



- 6 Answer the followings:

- (a) K-map and Q-M method guarantee exact solution, i.e. minimum number of terms and minimum number of literals for SOP. However, in practice, we do not necessarily need exact solution, which is why heuristic minimizer such as ESPRESSO is good enough. Explain why. [5 pts]
- (b) We have a ROM, whose size is 16K, and which stores 8-bit word. How many bits of address do we need to access this ROM? [5 pts]

- (c) When we minimize two-level multi-output Boolean functions, we minimize the functions "together" in a sense that the essential prime implicants we try to find have to be "essential" over multiple functions. On the other hand, when we minimize multi-level multi-output Boolean functions, we initially minimize in two-level each function independently (i.e. we find essentials of each function "separately"). Explain why? [5 pts]
- (d) Is static hazard a problem? Explain. Can we remove a static hazard due to multiple-bit change? If yes, how; if no, why? [5 pts]
- (e) What are the differences between combinational and sequential circuits? [5 pts]
- (f) Explain the steps of logic minimization for 1-function in 2-level, multi-function in 2-level, 1-function in multi-level, and multi-function in multi-level. [5 pts]