EE303 Digital System   Prof. Youngsoo Shin

Fall 2014

Final Exam

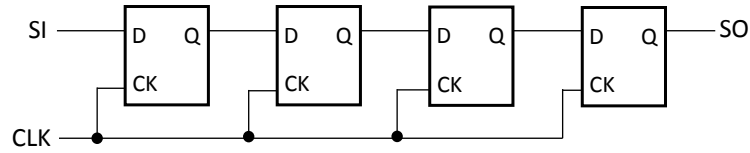December 16, 2014

Name _____

Student ID _____

Problem	Max Points	Your Points
1	10	
2	10	
3	10	
4	15	
5	10	
6	10	
7	10	
8	15	
9	10	
Total	100	

1. In one's complement addition, an end-around carry is added back to the sum. Is it possible that this generates another end-around carry? Explain. [10 pts]

2. Perform a multiplication of two biased numbers, $x + b$ and $y + b$, where b is a bias.
   a. Develop a direct multiplication method, i.e. multiply $x + b$ and $y + b$, and manipulate the expression to get $xy + b$. Explain the method step by step, and address which operation is needed in each step. The method should be as simple as possible to minimize hardware. [5 pts]

   b. Devise another multiplication method, which is simpler than (a), i.e. simpler in terms of hardware needed. [5 pts]
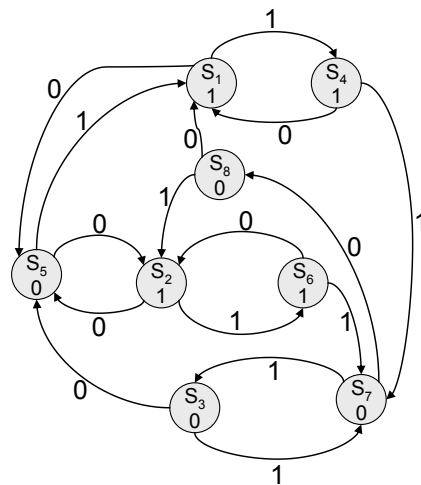
3. Consider a shift register below, which is made of 4 D flip-flops. The value applied at SI input will appear at SO output after 4 clock edges (or 4 clock cycles). Suppose that each flip-flop is now replaced by gated D latch. What is the requirement of latch (in terms of its timing parameters), so that the value applied at SI can still be observed at SO after 4 clock cycles? [10 pts]

4. Design a D flip-flop with asynchronous clear and preset (either active high or active low). Use latches and some extra logic gates. [15 pts]
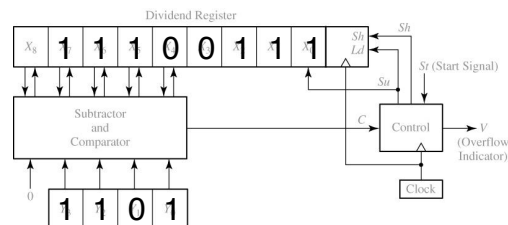
5. Design a J-K flip-flop using one D flip-flop and some extra logic gates. [10 pts]

6. Which states are equivalent in the following state graph? Draw a new simplified graph? Use the concept of k-equivalence. [10 pts]

7. Given $F(A, B, C, D) = \prod M(0, 1, 3, 5, 7, 8, 9, 13, 15)$. Implement it (i.e. derive a minimal form of expression for F) in a hazard-free manner. [10 pts]

8. In a parallel divider shown below, if the initial upper 4-bit of dividend (e.g. 1110) is larger than divisor (1101), overflow is assumed. Can you handle this case (i.e. continue division without overflow) by loading the result of subtraction into the dividend register, shift it to the left, and then write the quotient in its LSB position? If yes, show the state graph. If no, can you modify the circuit and state graph (dividend register is still 9 bit) to make this possible? [15 pts]

9. Answer the followings:
    a. A sequential circuit is implemented using a ROM and flip-flops. It consists of 3 primary inputs, 4 primary outputs, and 5 flip-flops. What is the size of ROM that is needed? [5 pts]

    b. Design a 3-bit Gray code counter, which counts in sequence of 000, 001, 011, 010, 110, 111, 101, 100, and then back to 000. Use J-K FFs. [5 pts]