EE303 Digital System Prof. Y. Shin

Spring 2015

Final Exam

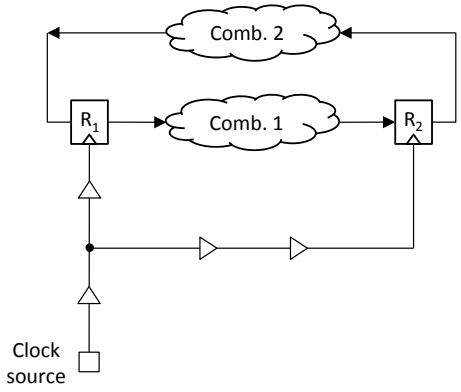
June 9, 2015

Name _____

Student ID _____

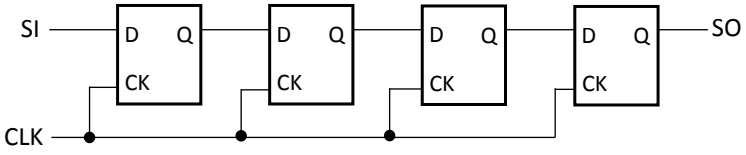
Problem	Max Points	Your Points
1	10	
2	10	
3	15	
4	15	
5	15	
6	10	
7	10	
8	15	
Total	100	

1. Consider a circuit shown below. The clock source generates a clock with period of 10. Delay of combinational logic 1 (Comb. 1) is from 2 to 7 (minimum delay is 2 and maximum delay is 7); that of Comb. 2 is 1~8. All clock buffers have a delay of 2. Suppose that registers R1 and R2 are positive edge-triggered flip-flops. Their clock-to-q delay is 1 and hold time is 2. In which flip-flops do you observe hold time violations and why?

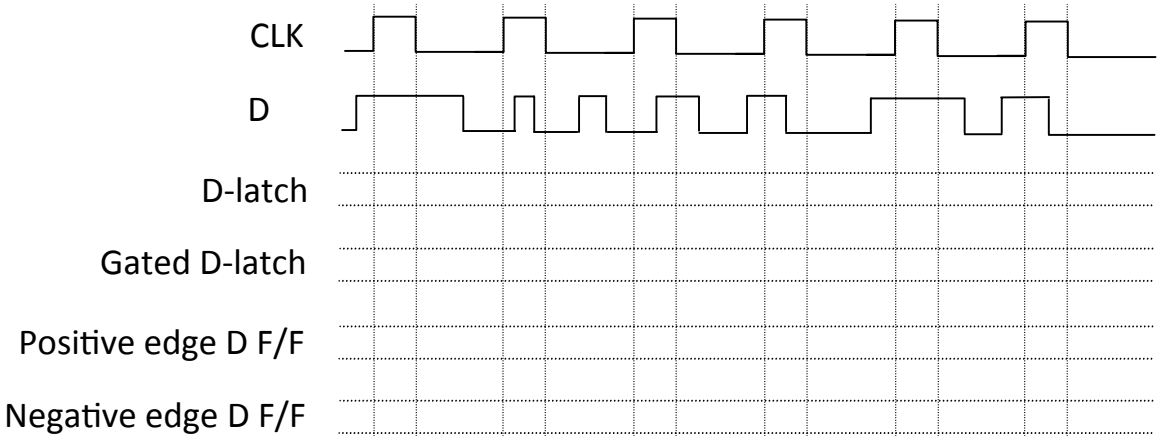


[10 pts]

2. Consider a shift register below, which is made of 4 D flip-flops. The value applied at SI input will appear at SO output after 4 clock edges (or 4 clock cycles). Each flip-flop is now replaced by gated D latch. What is the requirement of latch (in terms of its timing parameters), so that the value applied at SI can still be observed at SO after 4 clock cycles? [10 pts]



3. Draw the output waveform for the following four devices: [3+4+4+4 pts]
    a. D-latch (D wired to S-input and D' wired to R-input of S-R latch)
    b. Gated D-latch (G input connected to CLK)
    c. Positive edge-triggered D F/F
    d. Negative edge-triggered D F/F



4. Consider an S-R latch.
    a. Draw a STG with four states (QQ'=00, 01, 10, 11). Consider all possible input combinations (SR=00, 01, 10, 11). [10 pts]
    b. When do you observe the oscillation between states? [5 pts]

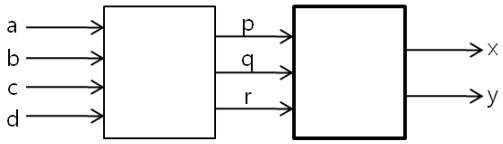
5. Consider a “universal shift register”. It can shift to the left, shift to the right, and load a new value; it also can be cleared at clock edge (i.e. synchronous clear). Design 1-bit cell. Its function is shown below. Use a D FF and some additional gates. [15 pts]

Clear	S0	S1	$Q[n]^+$
1	-	-	0
0	0	0	Q[n]
0	0	1	Q[n+1]
0	1	0	Q[n-1]
0	1	1	In[n]

6. Minimize the following state transition table. [10 pts]

P.S.	N.S.				P.O.
	xy=00	01	10	11	
S0	S0	S1	S2	S3	1
S1	S0	S3	S1	S4	0
S2	S1	S3	S2	S4	1
S3	S1	S0	S4	S5	0
S4	S0	S1	S2	S5	1
S5	S1	S4	S0	S5	0

7. In the following circuit, p(a, b, c, d) = ∑m(1, 5, 11, 13), q(a, b, c, d) = ∑m(3, 4, 7, 8, 10, 14, 15), and r(a, b, c, d) = ∑m(2, 4, 7, 8, 9, 14). Derive a minimum two-level multi-output NAND-NAND network to realize x(p, q, r) = ∑m(1, 4, 5) and y(p, q, r) = ∑m(1, 2). [10 pts]



8. Answer the followings:
   a. How many different state assignments are there if 8 states are given 3 bits? [5 pts]

   b. Derive Q+ as a function of J, K, and Q (in J-K flip-flop) [5 pts]

   c. Design a gated D latch using only NAND gates and inverters. [5 pts]