EE303 Digital System Prof. Y. Shin

Fall 2017

Final Exam

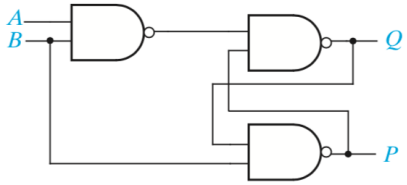
December 12, 2017

Name _____

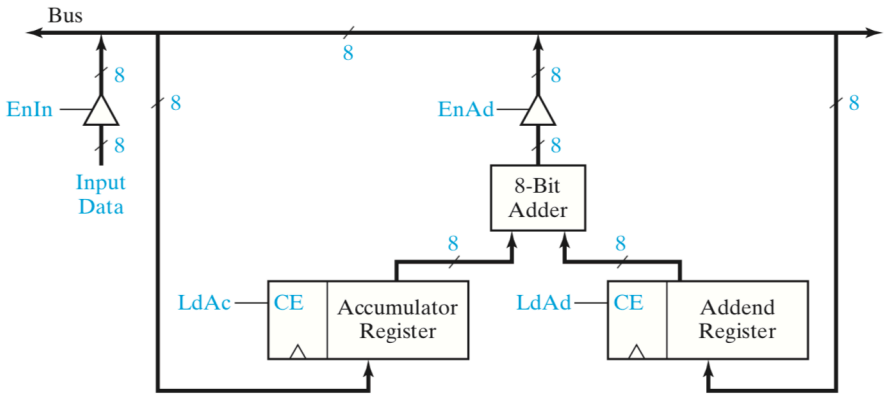
Student ID _____

Problem	Max Points	Your Points
1	20	
2	15	
3	20	
4	15	
5	25	
6	30	
7	25	
Total	150	

1. Analyze the latch circuit below.
    a. Derive the next-state equation Q^+. [5 pts]
    b. Construct the state table. Which states are stable and which states are not? Is the output P usable as Q'? [10 pts]
    c. Are there any restrictions on the allowable input combinations on A and B? [5 pts]

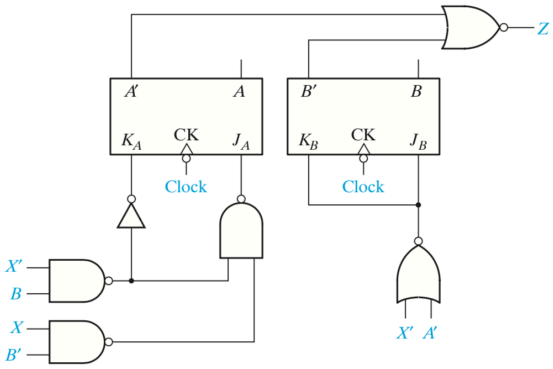


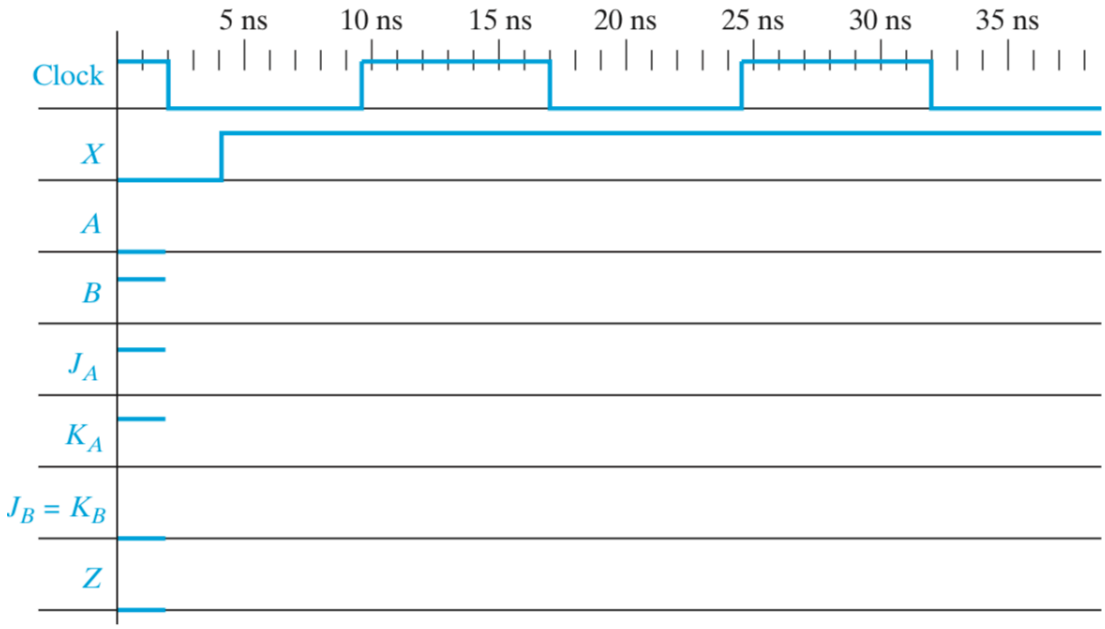
2. For the control signals and the input data in the following table, give the value of the accumulator register, the addend register, and the bus at the end of each clock cycle (i.e. immediately before the active clock edge). Express the register and bus values in decimal. [15 pts]



Clock Cycle	Input Data	EnIn	EnAd	LdAc	LdAd	Accumulator Register	Addend Register	Bus
0	18	1	0	1	0	0	0	18
1	13	1	0	0	1			
2	15	0	1	1	0			
3	93	1	0	0	1			
4	47	0	1	1	0			
5	22	1	0	0	1			
6	0	0	1	0	0			

3. For the circuit below, assume the delays of the NAND gates and NOR gates are 3 ns and the delay of the inverter is 2 ns. Assume the propagation delays and setup times for the J-K flip-flops are 4 ns and 2 ns, respectively.
    a. Fill in the given timing diagram. The clock period is 15 ns. Does the circuit operate properly with these timing parameters? [10 pts]
    b. What is the minimum clock period for this circuit, if X is changed early enough? How late may X change with this clock period without causing improper operation of the circuit? [10 pts]





4. A sequential circuit has one input and one output. The output becomes 1 and remains at 1 thereafter when at least one 1 and three 0's have occurred as inputs, regardless of the order of occurrence. Draw a state graph (Moore type) for the circuit. Use eight states. State graph should be drawn with no crossed lines. [15 pts]

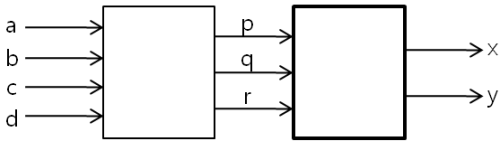
5. Consider the following state table.
    a. Reduce the state table to a minimum number of states. [10 pts]
    b. Use 3 guidelines to determine a state assignment for the reduced state table. You should satisfy all but one guideline. [5 pts]
    c. Assume J-K flip-flops. Derive flip-flop input equations and output equation [10 pts]

	$X = 0$	1	Z
A	A	B	1
B	C	E	0
C	F	G	1
D	C	A	0
E	I	G	1
F	H	I	1
G	C	F	0
H	F	B	1
I	C	E	0

6. Design a binary divider which divides a 7-bit dividend by a 2-bit divisor to give a 5-bit quotient. The system has an input *St* that starts the division process.
    a. Draw a block diagram for the subtracter-comparator. Comparator output is *C*. You may use full subtracters. [10 pts]
    b. Draw a block diagram for the rest of the system (assuming subtracter-comparator block). [10 pts]
    c. Draw the state graph for the control circuit. [5 pts]
    d. Give the contents of the dividend register and the value of *C* at each time step if initially the dividend is 01010011 and the divisor is 11. [5 pts]

7. Answer the followings.
    a. Multiplexer can be used to implement Boolean expression, in addition to its original function of data selection. Implement F = AB + BC + AC using a single 4:1 MUX. Implement G = (ABC + A'B')(C + D) using a single 8:1 MUX. [5 pts]

    b. In the following circuit, p(a, b, c, d) = Σ m(1, 5, 11, 13), q(a, b, c, d) = Σ m(3, 4, 7, 8, 10, 14, 15), and r(a, b, c, d) = Σ m(2, 4, 7, 8, 9, 14). Derive a minimum two-level multi-output NAND-NAND network to realize x(p, q, r) = Σ m(1, 4, 5) and y(p, q, r) = Σ m(1, 2). [10 pts]



    c. Design a J-K flip-flop using one D flip-flop and some extra logic gates. [10 pts]