1

CD \ AB	00	01	11	10
00	0	1	1	1
01	1	0	1	1
11	1	1	0	1
10	1	1	1	0

In min. SOP, f = AC′ + BD′ + A′C + B′D

In min. POS, f = (A+B+C+D)(A+B′+C+D′)(A′+B+C′+D)(A′+B′+C′+D′)

Partial score: X

2

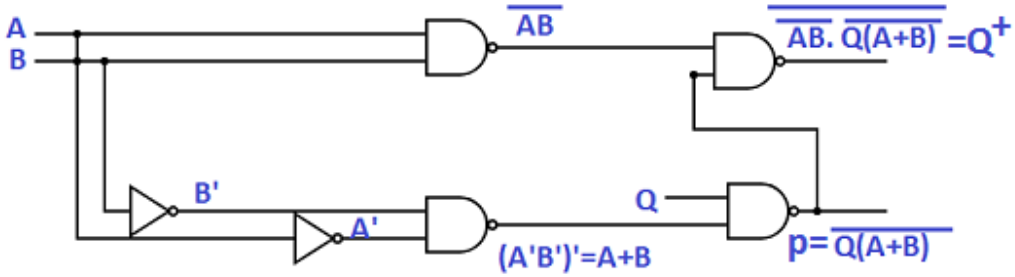
a. +5pts

A	B	Q	Q+
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Q+ = AB + QA + QB

Partial score: correct state table (+2pts), correct characteristic equation (+3pts)

b. +10pts



Partial score: correct functionality, but wrong component (-2pt for each component)

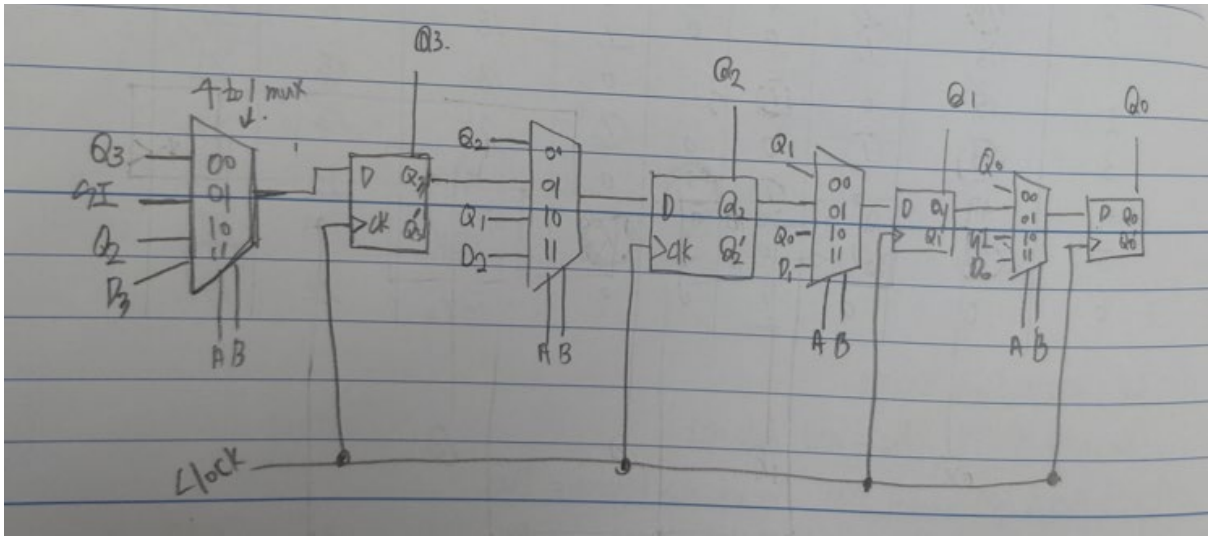
3.

Clock cycle	Input Data	En/n	EnAd	LdAc	LdAd	Accumulator Register	Addend Register	Bus
0	18	1	0	1	0	0	0	18
1	13	1	0	0	1	18	0	13
2	15	0	1	1	0	18	13	31
3	93	1	0	0	1	31	13	93
4	47	0	1	1	0	31	93	124
5	22	1	0	0	1	124	93	22
6	0	0	1	0	0	124	22	146

정답시 10점

정답이 아닐 경우: 칸 18개중 1개 맞을 때 마다 0.5점

4.



정답시 15점

정답이 아닐 경우:

정답 회로에서 SI 표기를 안하면 -5점

Load 기능 구현시: +4점

Right shift 구현시: +4점

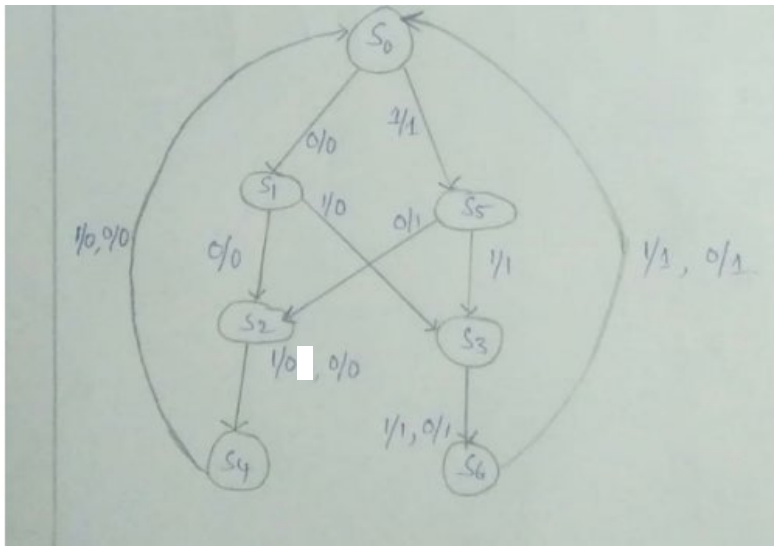
Left shift 구현시: +4점

5. A sequential circuit with one input and one output is used to stretch the first two bits of a 4-bit sequence as follows:

Input	Output
00XX	0000
01XX	0011
10XX	1100
11XX	1111

After every 4 bits, the circuit resets. Find a Mealy state transition graph (minimum number of states) and state table for the circuit. [10 pts]

Sol)



→ 5 pts

State Table

State	Next State		yz	
	X = 0	X = 1	X = 0	X = 1
S_0	S_1	S_5	0	1
S_1	S_2	S_3	0	0
S_2	S_4	S_4	0	0
S_3	S_6	S_6	1	1
S_4	S_0	S_0	0	0
S_5	S_2	S_3	1	1
S_6	S_6	S_0	1	1

→ 5 pts

Minimum #states 로 구현하지 않았지만 기능이 맞은 경우 → 2 pts

6. A sequential circuit contains two D flip-flops; their input expressions are D1 = XQ1 + XQ2 and D2 = XQ1 + XQ2', where X is a circuit input. Convert the circuit into an equivalent one where each D flip-flop is replaced by a T flip-flop. Derive new flip-flop input expressions.

DFF to TFF transfer: T = DQ' + D'Q

D	Q_n	Q_{n+1}	T
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

➔ $T_1 = D_1Q_1' + D_1'Q_1 = (XQ_1 + XQ_2)Q_1' + (XQ_1 + XQ_2)'Q_1 =$ **$XQ_1'Q_2 + X'Q_1$** [5pts]
➔ $T_2 = D_2Q_2' + D_2'Q_2 = (XQ_1 + XQ_2')Q_2' + (XQ_1 + XQ_2')'Q_2 =$ **$XQ_2' + X'Q_2 + Q_1'Q_2$** [5pts]

Boolean expression expanding mistake -2pts

7. The following are possible state assignments for a six-state sequential circuits.

	(i)	(ii)	(iii)	(iv)	(v)
S_0	000	010	100	110	001
S_1	001	111	101	010	111
S_2	010	001	000	111	101
S_3	011	110	001	011	011
S_4	100	000	111	000	000
S_5	101	100	110	100	010

a. Which two state assignments are equivalent?

Complement of (iv) and swap first and last column → (iii)
(iii) and (iv) are equivalent [5pts]

b. For each assignment (except (i)), give an equivalent assignment for which state S0 is assigned to 000.

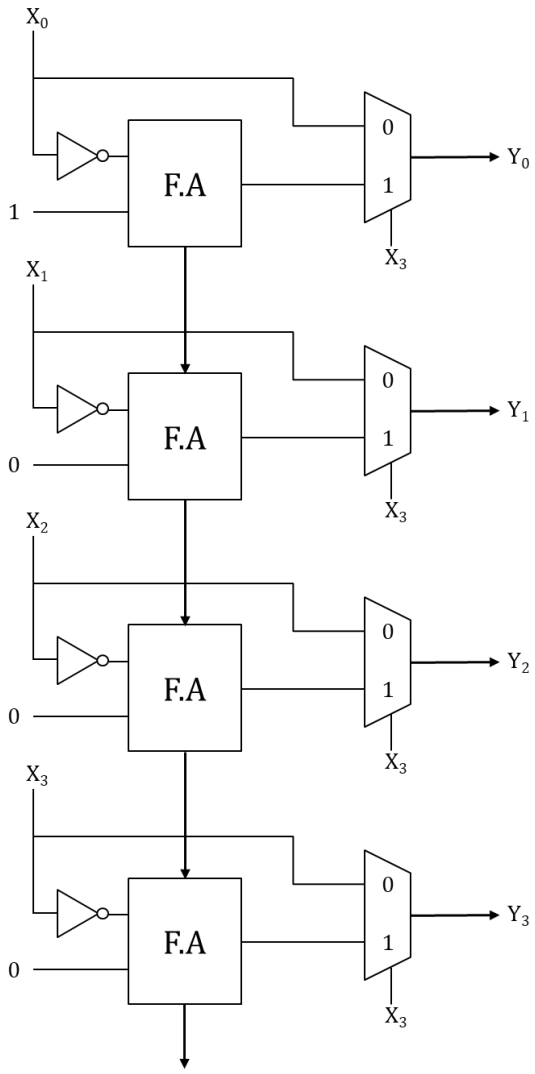
	(ii)	(iii)	(iv)	(v)
S_0	000	000	000	000
S_1	101	001	100	110
S_2	011	100	001	100
S_3	100	101	101	010
S_4	010	011	110	001
S_5	110	010	010	011

[10 pts] each assignment 2.5pts
If (iv) and (iii) represent the same, it is also answer

8. Make a circuit which gives the absolute value of a 4-bit 2's complement number. Use full adders, multiplexers, and inverters.

For 4-bit binary number X = $X_3X_2X_1X_0$
If X > 0: |X| = X
If X < 0: |X| = -X
2's complement is calculated like below
2's complement of $X_3X_2X_1X_0$ = $X_3'X_2'X_1'X_0'$ + 0001

Output Y = $Y_3Y_2Y_1Y_0$ which is |X|
So if X is positive number (X_3 = 0), Y = $X_3X_2X_1X_0$,
If X is negative number (X_3 = 1), Y = 2's complement of $X_3X_2X_1X_0$



If circuit is functionally well, answer is correct [15 pts]
Only functional for 1 condition (positive/negative) [5pts]