1. [Total 80 Pts.]

(a) [10 Pts.]

Sol)

$(11)_{10} = (0001011)_2$

$(-31)_{10} = -(0011111)_2 = (1100001)_2$

→ $(0001011)_2 + (1100001)_2 = (1101100)_2$

→ $11 + (-31) = (1101100)_2 = -(0010100)_2 = -20$

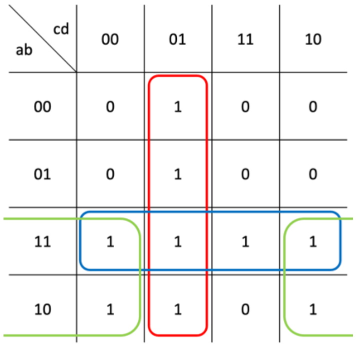
Grading criteria

(+10pts) with right answer using the 2’s complement and proper discussion.

(b) [20 Pts.]

Sol)

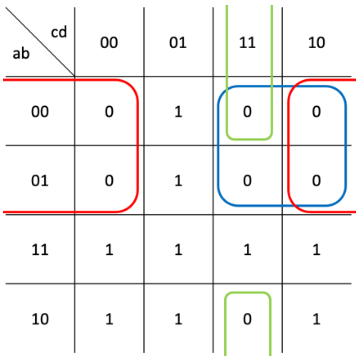
(i) sum-of-products



ab \ cd	00	01	11	10
00	0	1	0	0
01	0	1	0	0
11	1	1	1	1
10	1	1	0	1

→ $f = c'd + ab + ad'$

(ii) product-of-sums



ab \ cd	00	01	11	10
00	0	1	0	0
01	0	1	0	0
11	1	1	1	1
10	1	1	0	1

→ $f = (a'd' + a'c + b'cd)' = (a + d)(a + c')(b + c' + d')$

Grading criteria

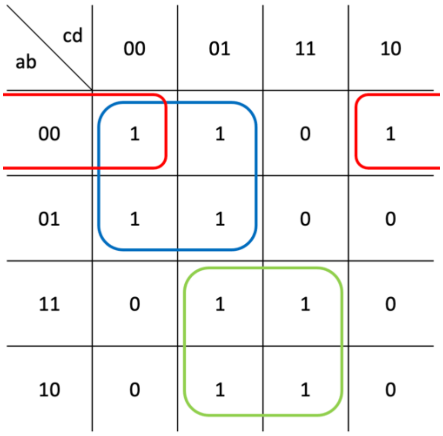
문제에서 제시한 표현방식으로 답안을 작성하지 않은 경우 (POS, SOP), 최종 답안이 맞아도 2점의 감점이 있습니다

If the answer is not expressed according to the given condition (POS, SOP), 2 points will be deducted even if the answer is correct.

(c) [20 Pts.]

Sol)

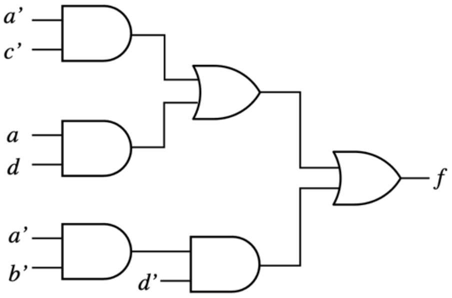
(i)



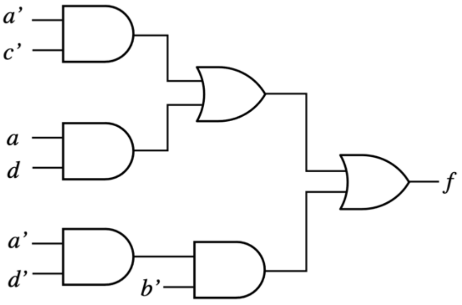
ab \ cd	00	01	11	10
00	1	1	0	1
01	1	1	0	0
11	0	1	1	0
10	0	1	1	0

→ *f = a’c’ + ad + a’b’d’*

* Total 9 combinations of diagrams are possible



→

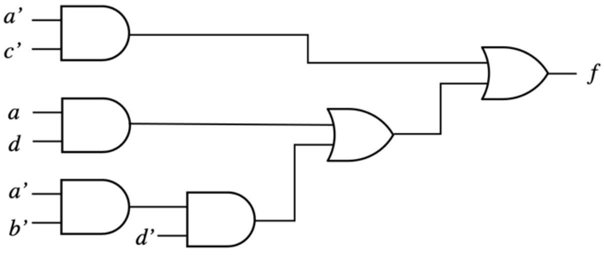


Bottom AND gate combinations (3 types)

(a’b’)d’ / (a’d’)b’ / a’(b’d’)

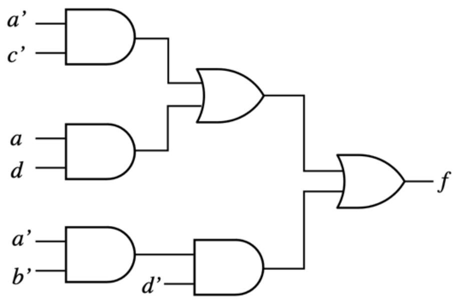
↓ *OR gate combinations (3 types)*

(a’c’ + ad) + a’b’d’ / (a’c’ + a’b’d’) + ad / a’c’ + (ad + a’b’d’)

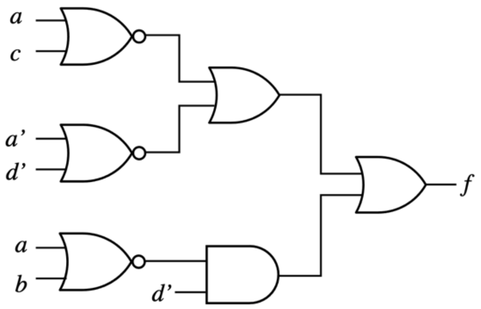


→ 3*3 = 9 types

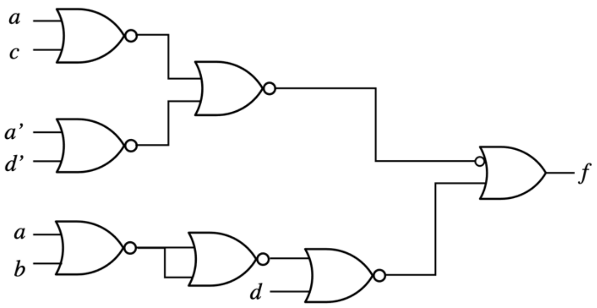
(ii)



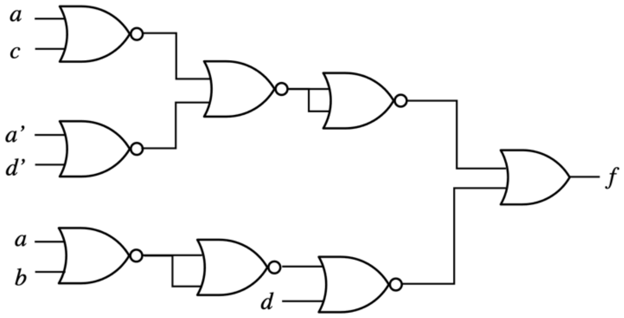
→



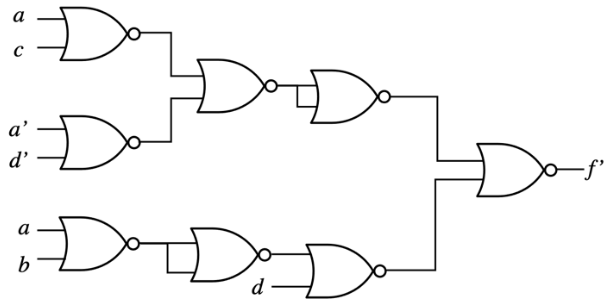
→



→



→



* Total 9 combinations of diagrams are possible (same reason as (i))

Grading criteria

(i)

정확한 f (또는 f’) 수식을 구한 경우 5점

정확한 circuit diagram을 그린 경우 5점

Circuit을 그릴 때 변수명을 잘못 표기한 경우 (ex. a를 a’으로 잘못 표기) 2점 감점

Correct formula for f (or f’) → 5 points
Correct implementation with AND, OR gate → 5 points
Incorrect variable in circuit (ex. a → a’) → -2 points penalty

(ii)

(i)에서 구한 circuit에서 bubbling 방식을 사용한 답이나, NOR 연산만으로 구현 가능하도록 f (또는 f’)의 수식을 변경하여 새로 circuit을 그린 답이나 모두 정답 (10 points)

Circuit을 그릴 때 변수명을 잘못 표기한 경우 (ex. a를 a’으로 잘못 표기) 2점 감점

NOR 만으로 circuit을 구현하지 않은 경우, 부분점수 없음

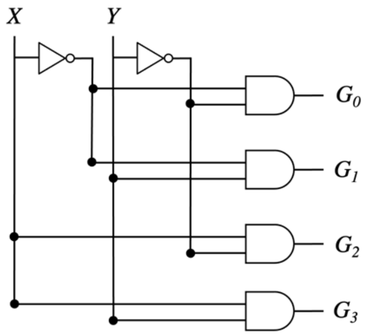
Any methods to draw circuit only with NOR gate are correct : Converting circuit using bubbling from answer of (i) or drawing new circuit from modified formula for f
Incorrect variable in circuit (a → a’) → -2 points penalty
If not using NOR gate, no additional credit

(d) [20 Pts.]

Sol)

(i)

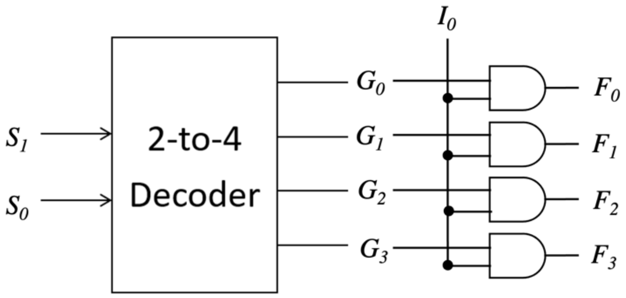
X	Y	G_0	G_1	G_2	G_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1



$G_0 = X'Y'$, $G_1 = X'Y$, $G_2 = XY'$, $G_3 = XY$

(ii)

S_1	S_0	I_0	F_3	F_2	F_1	F_0
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	0	0
0	1	1	0	0	1	0
1	0	0	0	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	0	0
1	1	1	1	0	0	0



Grading criteria

(i)

(+5pts) for right truth table.

(+5pts) for right circuit implementation.

(-2pts) for using another gate (e.g. XNOR, OR) except AND gate and INV.

(ii)

(+5pts) for right truth table.

(+5pts) for right circuit implementation.

(-2pts) for using another gate (e.g. XNOR, OR) except AND gate and INV.

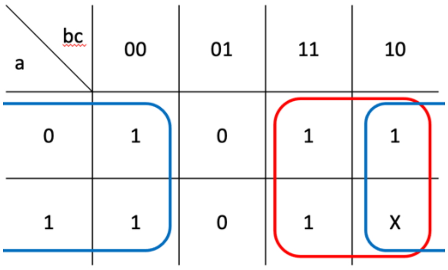
(-1pt) without 2-to-4 Decoder.

(-1pt) for using 3-input AND gate (not only 2-input AND gate).

(e) [10 Pts.]

Sol)

f_1:



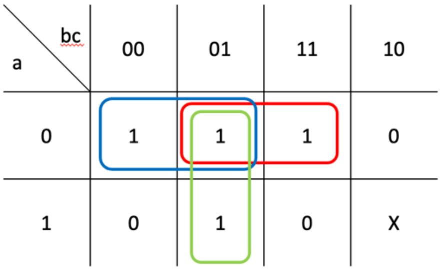
a \ bc	00	01	11	10
0	1	0	1	1
1	1	0	1	X

$f_1 = b + c'$

Grading criteria

- Not correct function: -5 pts
- Not simplified: -3pts

f_2:



a \ bc	00	01	11	10
0	1	1	1	0
1	0	1	0	X

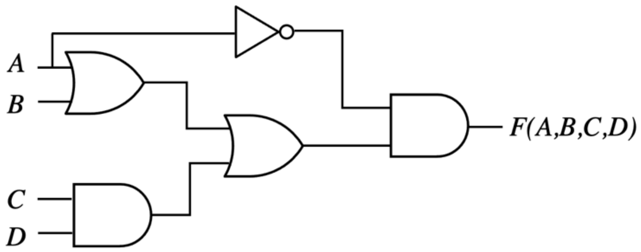
$f_2 = a'b' + a'c + b'c$

Grading criteria

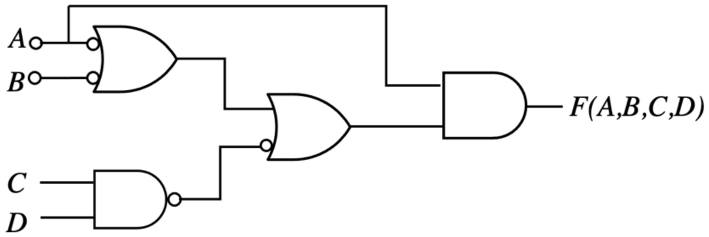
- Not correct function: -5 pts
- Not simplified: -3pts

2. [Total 20 Pts.]

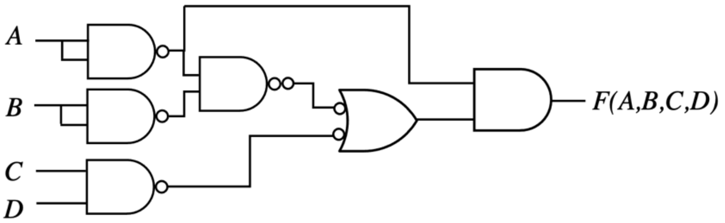
Sol)



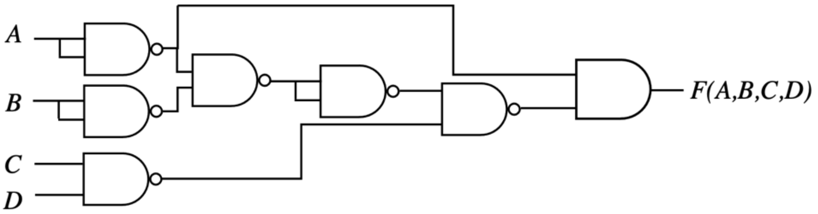
→



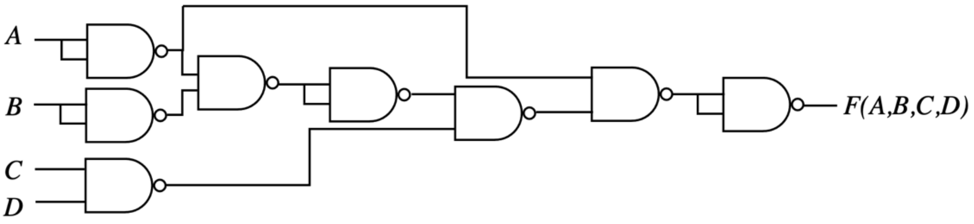
→



→



→



Grading criteria

(+20pts) for right circuit implementation.

(-2pts) for using another gate (e.g. 3-input NAND gate, INV) except 2-input NAND gate.

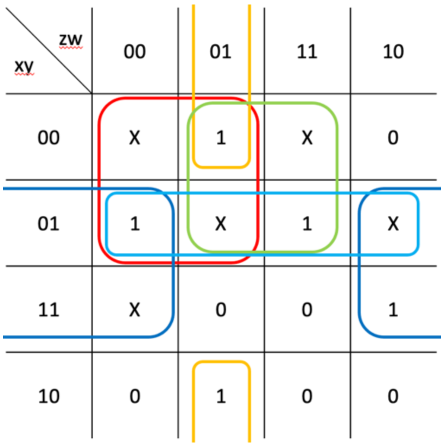
(-2pts) for minor error (e.g. a single NAND gate is more or less needed).

(-2pts) for using complementary input or output.

3. [Total 30 Pts.]

Sol)

(a)



xy \ zw	00	01	11	10
00	X	1	X	0
01	1	X	1	X
11	X	0	0	1
10	0	1	0	0

→ Prime implicants: $x'z'$ (red), $x'w$ (green), yw' (blue), $x'y$ (skyblue), $y'z'w$ (yellow)

Grading criteria

- Not correct element: -2pts per implicant
- Absence of each prime implicant: -2pts

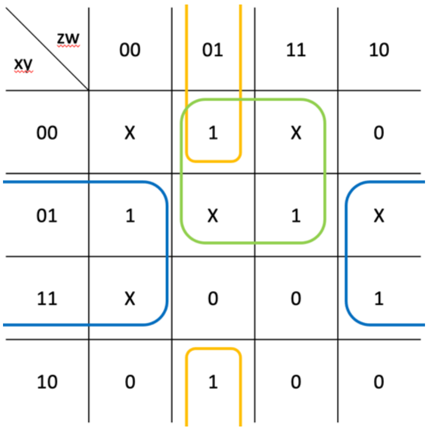
(b)

Essential prime implicants: yw' (blue), $y'z'w$ (yellow)

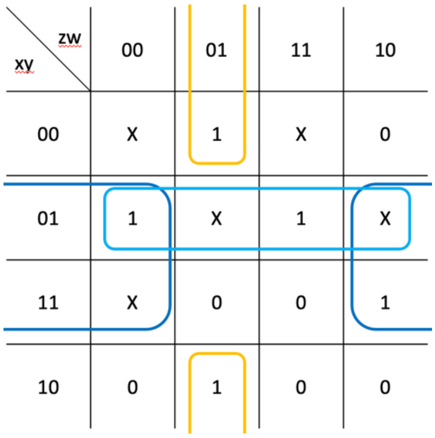
Grading criteria

- Incorrect essential prime implicants: -10pts

(c)



xy \ zw	00	01	11	10
00	X	1	X	0
01	1	X	1	X
11	X	0	0	1
10	0	1	0	0



xy \ zw	00	01	11	10
00	X	1	X	0
01	1	X	1	X
11	X	0	0	1
10	0	1	0	0

$F = x'w + yw' + y'z'w$ or $F = x'y + yw' + y'z'w$

Grading criteria

- Not minimum or incorrect: -10pts

4. [Total 20 Pts.]

Sol)

$(c'+abd+b'd+a'b)(c+ab+bd) = c'(ab+bd)+c(abd+b'd+a'b)$

$= abc'+bc'd+abcd+b'cd+a'bc = abc'+abcd+bc'd+a'bc+b'cd$

$= ab(c'+cd)+bc'd+a'bc+b'cd = ab(c'+d)+bc'd+a'bc+b'cd$

$= ab(c'+d)+bc'd+a'bc+a'bd+b'cd = abc'+abd+bc'd+a'bc+a'bd+b'cd$

$= (abd+a'bd)+abc'+bc'd+a'bc+b'cd = bd(a+a')+abc'+bc'd+a'bc+b'cd$

$= bd(1)+abc'+bc'd+a'bc+b'cd = bd+abc'+bc'd+abc'+a'bc+b'cd$

$= bd+bc'd+abc'+a'bc+b'cd = bd+abc'+a'bc+b'cd = d(b+b'c)+abc'+a'bc$

$= d(b+c)+abc'+a'bc = d(b+c)+b(ac'+a'c) = d(b+c)+b(a+c)(a'+c')$

or

$(c' + abd + b'd + a'b)(c + ab + bd)$
$= \cancel{c'c} + abcd + b'cd + a'bc + abc' + abd + \cancel{abb'd} + \cancel{aa'b} + bc'd + abd + \cancel{bb'd} + a'bd$
$= d(abc + b'c + ab + bc' + ab + a'b) + a'bc + abc'$
$= d(b(ac + a + c' + a + a') + b'c) + b(a'c + ac')$
$= d(b + b'c) + b(a'c + ac' + aa' + cc')$
$= d(b(c + b' + b) + b'c) + b(a + c)(a' + c')$
$= d(bb + bb' + bc + b'c) + b(a + c)(a' + c')$
$= d(b + b')(b + c) + b(a + c)(a' + c')$
$= d(b + c) + b(a + c)(a' + c')$

Grading criteria

The provided answers are just one of way to prove the relation.
Any answer with proper derivation could be answer.
Therefore, if you derived the relation without omitting the step you get full points.
(+20pts) with right derivation with proper explanation
Here, -10pts deduction if you made minor mistakes or omitting step.

If you failed to prove the relation, there is no partial points.
(+0pts) with wrong derivation

5. [Total 30 Pts.]

[Solution] One of the easiest ways is dividing the 8-bit adder into upper 4 bits and lower 4 bits. The upper 4 bits of the adder can perform as an independent 4-bit adder as long as there is no carry-in from the lower bit. Therefore, we must make sure the lower 4 bits of the adder do not produce any carry out to the 5-th bit. To achieve this, we should tie the 4-th bit of A and B (a_3 and b_3) to 0. Therefore, among the lower 4 bits, we can utilize only the lowest 3 bits as an independent 3-bit adder.

To expand this 3-bit adder to another 4-bit adder, we need to implement a full adder outside of the 8-bit adder using logic gates.

$a_7 = x_3$, $a_6 = x_2$, $a_5 = x_1$, $a_4 = x_0$, $a_3 = 0$, $a_2 = z_2$, $a_1 = z_1$, $a_0 = z_0$,
$b_7 = y_3$, $b_6 = y_2$, $b_5 = y_1$, $b_4 = y_0$, $b_3 = 0$, $b_2 = w_2$, $b_1 = w_1$, $b_0 = w_0$,
$u_3 = s_7$, $u_2 = s_6$, $u_1 = s_5$, $u_0 = s_4$,
$v_3 = z_3 \oplus w_3 \oplus s_3$, $v_2 = s_2$, $v_1 = s_1$, $v_0 = s_0$

Note that the 4-th sum bit, s_3 is considered as a carry-in input of the full adder outside the 8-bit adder.

Grading Criteria

You DON'T need to draw a circuit. Drawing a block diagram doesn't give you extra credit.

1) 5pts : Having the concept of dividing the 8-bit adder into upper 4 bits and lower 4 bits

2) A) 25pts : successfully defining Boolean expressions for A, B, U, V using X, Y, Z, W and S (deduction for minor calculation mistakes)

B) If your design leads to the right answer U and V, but you used so many gates(including NOT gates, all the gates considered 2-input instead of NOT), there would be deduction:

3~10 gates : 18pts

11~20 gates : 12pts

21~30 gates : 7pts

31~40 gates : 4pts

41 or more gates : 0pts (Since 8-bit adder itself is made up under 40 gates)

Ideas to ignore carry such as making one of a_7~ a_0 or b_7~ b_0 0, would get +3 points

-3 deduction if some of A, B, U ,V are not in boolean expression

C) 2pts for simple answers like

$a_7 = x_3$, $a_6 = x_2$, $a_5 = x_1$, $a_4 = x_0$, $a_3 = z_3$, $a_2 = z_2$, $a_1 = z_1$, $a_0 = z_0$,

$b_7 = y_3$, $b_6 = y_2$, $b_5 = y_1$, $b_4 = y_0$, $b_3 = w_3$, $b_2 = w_2$, $b_1 = w_1$, $b_0 = w_0$,

$u_3 = s_7$, $u_2 = s_6$, $u_1 = s_5$, $u_0 = s_4$, $v_3 = s_3$, $v_2 = s_2$, $v_1 = s_1$, $v_0 = s_0$

C) 2pts if you misunderstood the problem that every bit has no carry, and got the proper solution in this situation

D) 0pts : if no Boolean expression for each bit/if you didn’t use 8-bit adder/if you used 2 or more 8-bit adders

E) Any other answers would be given partial credits based on your solution