**EE201 Circuit Theory (Spring 2017)**
**Final Exam.**

**(Total: 240 Points / 10 Problems)**

**Student ID Number:**

**Name:**

**1. (20 points)** Find $i_1(t)$ and $i_2(t)$ for $t \geq 0$ for the circuit shown in Fig. 1.

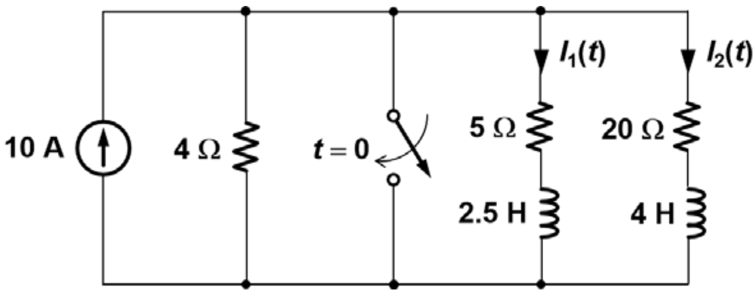
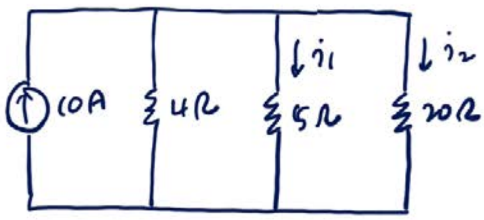



**Fig. 1**

At $t=0^-$, the circuit has reached the steady state and the inductors act like short circuits as shown below.

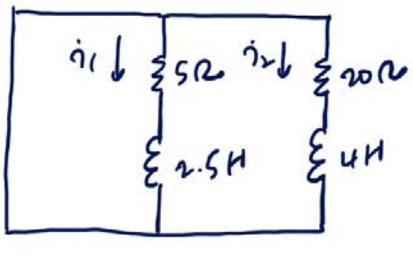



$$i_1(0^-) + i_2(0^-) = 10 \times \frac{4}{4 + 5\|20} = 5A.$$

$$i_1(0^-) = i_1(0^+) = 5 \times \frac{20}{5+20} = 4A.$$

$$i_2(0^-) = i_2(0^+) = 5 - 4 = 1A.$$

For $t>0$, the switch is closed and the energies stored in $L_1$ and $L_2$ flow through the closed switch and become dissipated in $5\Omega$ and $20\Omega$ resistors, respectively, as shown below.




$$i_1(t) = i_1(0^+) e^{-t/\tau_1} \text{ where } \tau_1 = \frac{2.5}{5} = \frac{1}{2}.$$

$$\therefore i_1(t) = 4e^{-2t} \text{ A for } t>0.$$

$$i_2(t) = i_2(0) e^{-t/\tau_2} \text{ where } \tau_2 = \frac{4}{20} = \frac{1}{5}$$

$$\therefore i_2(t) = 1e^{-5t} \text{ A for } t>0.$$

**2.** Consider the circuit in Fig. 2(a), where a DC power supply is modeled as a DC voltage source in series with a resistor $R_S$. The two voltage sources and the single-pole double-throw switch model the disturbance in the power supply voltage, sketched in Fig. 2(a). Let's assume that the load draws a constant current $I_L$ and is modeled as a current source.

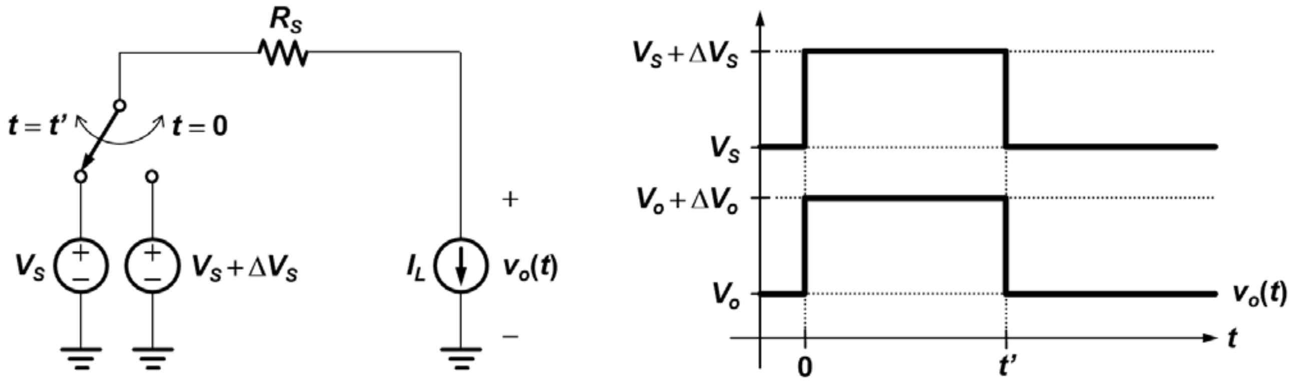



**Fig. 2(a)**

We wish to design the simplest possible circuit that will isolate the load from disturbances in the power supply voltage. A standard solution to this problem involves the use of a capacitor $C_D$, as shown in Fig. 2(b). The $C_D$ is called a decoupling capacitor since it decouples disturbances in the input supply voltage from the output voltage applied to the load.

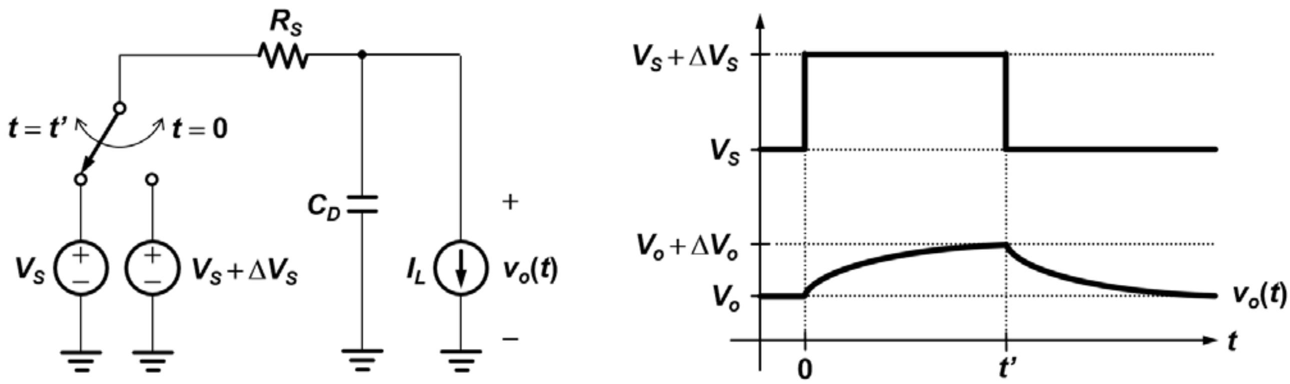


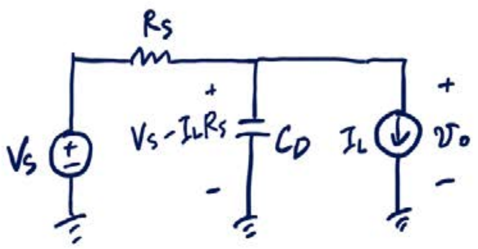

**Fig. 2(b)**

**(a)** **(10 points)** Determine $v_o(t)$ for $0 \le t \le t'$ in terms of $V_S$, $\Delta V_S$, $I_L$, $R_S$ and $C_D$, when the decoupling capacitor is employed for the supply disturbance isolation.

The voltage across $C_D$ can be expressed in the following form:

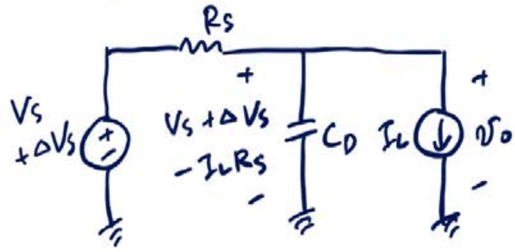
$v_o(t) = K_1 + K_2 e^{-t/\tau}$ for $0 \le t \le t'$.

At $t = 0^-$, the circuit is configured as shown below.




$v_o(0^-) = v_o(0^+) = K_1 + K_2 = V_S - I_L R_S$

If the switch position were not changed at $t = t'$, the circuit becomes as shown below at $t = \infty$.




$v_o(\infty) = K_1 = V_S + \Delta V_S - I_L R_S$

Since $\tau = R_S C_D$, $v_o(t) = V_S + \Delta V_S - I_L R_S - \Delta V_S e^{-t/R_S C_D}$ for $0 \le t \le t'$.

**(b) (10 points)** Find $\Delta V_o$, when the decoupling capacitor is used.

At $t = t'$, $v_o(t') = V_o + \Delta V_o = V_S + \Delta V_S - I_L R_S - \Delta V_S e^{-t'/R_S C_D}$.

Since $V_o = v_o(0) = V_S - I_L R_S$, $\Delta V_o = \Delta V_S \left[1 - e^{-t'/R_S C_D}\right]$.

**(c) (10 points)** From the result of (b), explain how the isolation performance changes for different values of the decoupling capacitance. Consider the case in which $V_S$ is 5 V, $R_S$ is 20 Ω, and the input disturbance is characterized by $\Delta V_S = 1$ V and $t' = 0.5$ ms. If the output changes are to be limited to only 0.2 V, what is the required capacitance value of $C_D$?

From the expression, $\Delta V_o = \Delta V_S \left(1 - e^{-t'/R_S C_D}\right)$ ①, it can be said that the larger is the $C_D$, the smaller becomes the $\Delta V_o$.
In other words, the isolation performance improves as the decoupling capacitance increases.

Rewriting ① to solve for $C_D$,

$$C_D = \frac{t'}{R_S \ln\left(\frac{\Delta V_S}{\Delta V_S - \Delta V_o}\right)} = \frac{0.5m}{20 \times \ln\left(\frac{1}{1-0.2}\right)} = 112\ \mu F$$

**3.** The network in Fig. 3 models an automobile ignition system. The voltage source represents the standard 12-V battery. The inductor is the ignition coil, which is magnetically coupled to the starter (not shown). The inductor's internal resistance is modeled by the resistor, and the switch is the keyed ignition switch. Initially, the switch connects the ignition circuitry to the battery, and thus the capacitor is charged to 12 V. To start the engine, we close the switch, thereby discharging the capacitor through the inductor.

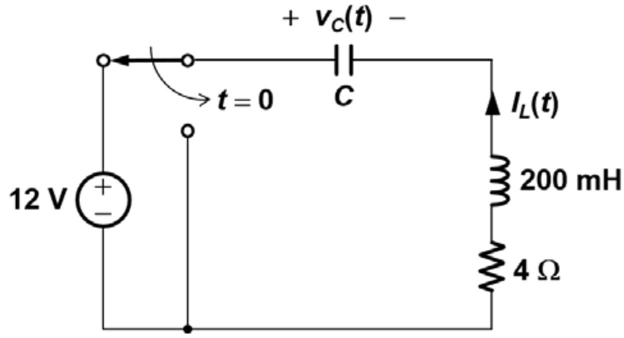



**Fig. 3**

**(a) (30 points)** Assuming that optimum starter operation requires an overdamped response for $i_L(t)$ that reaches 1 A within 100 ms after switching and remains above 1 A for longer than 1 s, find a value for the capacitor that will produce such a current waveform.

**(b) (20 points)** Determine the expression and draw a rough sketch of $i_L(t)$ for $t \geq 0$ when the capacitor value found in (a) is used.

Before the switch is moved at $t=0$, the capacitor behaves like an open circuit, and the inductor behaves like a short circuit.

Therefore, $i_L(0^-) = i_L(0^+) = 0\,A$ and $v_c(0^-) = v_c(0^+) = 12\,V$.

After switching at $t=0$, the circuit is a unforced series RLC network described by the following characteristic equation:

$s^2 + \frac{R}{L}s + \frac{1}{LC} = (s+s_1)(s+s_2) = 0$, which has roots at $s = -s_1$ and $-s_2$.

We can write $s_1 + s_2 = \frac{R}{L} = \frac{4}{200m} = 20$ and $s_1 s_2 = \frac{1}{LC}$.

Since the network must be overdamped, the inductor current is of the form, $i_L(t) = K_1 e^{-s_1 t} + K_2 e^{-s_2 t}$.

As we know $i_L(0^+) = K_1 + K_2 = 0$, $K_2 = -K_1$.

Also at $t=0^+$, the sum of the inductor voltage and the capacitor voltage should be zero, because $i_L = 0$ and thus $i_L R = 0$.

Therefore, we can write

$v_L(0^+) = -L\frac{di_L(0^+)}{dt} = -L \times (-s_1 K_1 + s_2 K_1) = -v_C(0^+) = -12$

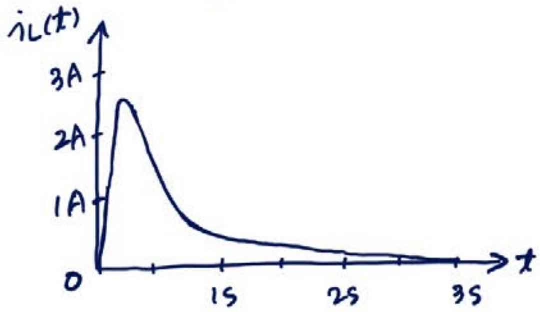
$$\therefore K_1 = \frac{12}{L(S_2-S_1)} = \frac{60}{S_2-S_1}$$

Let us arbitrarily choose $S_1=3$ and $S_2=17$, which satisfies the condition $S_1+S_2=20$.

Then $K_1 = \frac{60}{17-3} = 4.29$ and $C = \frac{1}{LS_1S_2} = \frac{1}{200m \times 3 \times 17} = 98\ mF$

$\therefore i_L(t) = 4.29\,(e^{-3t} - e^{-17t})$

The following figure shows a plot of $i_L(t)$.




At $t=100ms$, $i_L$ reaches 2.39, which meets the initial magnitude specifications.
However, 1s later, at $t=1.1s$, $i_L$ falls to 0.16 A, which is well below the magnitude-over-time requirement.
Simply put, $i_L$ falls too quickly.

To make an informed estimate for $S_1$ and $S_2$, let us investigate the effect that the roots exhibit on the current waveform when $S_2>S_1$.
Since $S_2>S_1$, the exponential associated with $S_2$ will decay toward zero faster than that associated $S_1$.

This causes $i_L(t)$ to rise in the beginning - the larger the value of $S_2$, the faster the rise.

After $5\times(1/S_2)$ seconds have elapsed, the exponential associated with $S_2$ is almost zero and $i_L(t)$ decreases exponentially with a time constant of $\tau = 1/S_1$.

Thus, to slow the fall of $i_L(t)$, we shoud reduce $S_1$.

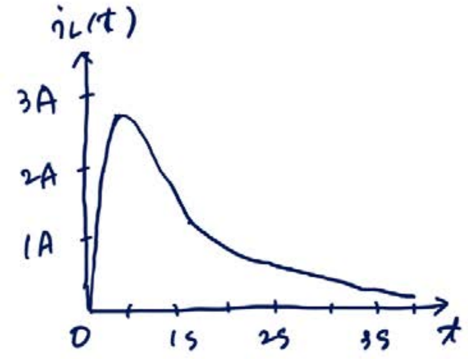
Hence, let us choose $S_1=1$.

Since $S_1+S_2=20$, $S_2=19$.

Under this condition, $C = \frac{1}{LS_1S_2} = \frac{1}{200m \times 1 \times 19} = 263\ mF$ and

$$K_1 = \frac{60}{S_2-S_1} = \frac{60}{19-1} = 3.33$$

Thus, $i_L(t) = 3.33\,(e^{-t} - e^{-19t})$ A, which can be plotted as follows.




At $t = 100ms$, $i_L$ reaches $2.52A$.

At $t = 1.1s$, $i_L$ is $1.11A > 1A$.

Therefore, the choice of $C = 263mF$ meets all the requirements.

**4.** **(20 points)** Given the network in Fig. 4, find the Thévenin's equivalent circuit of the network at terminals *A*–*B*.

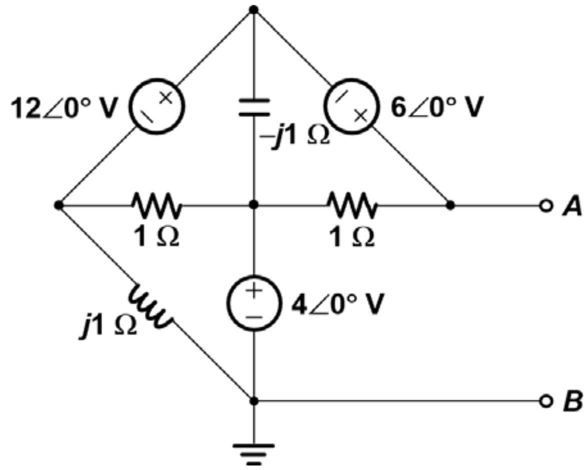
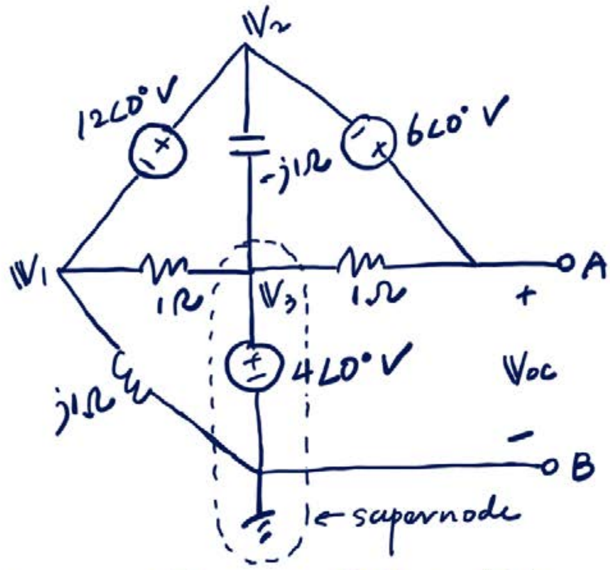



**Fig. 4**




Applying KCL at the supernode,

$$\frac{V_1-V_3}{1}+\frac{V_2-V_3}{-j1}+\frac{V_1}{j1}+\frac{V_{oc}-V_3}{1}=0$$

$$(1+j1)V_1 - V_2 + (1-j2)V_3 + V_{oc}\times j1 = 0 \quad ①$$

$$V_3 = 4\angle 0° \quad ②$$

$$V_2 - V_1 = 12\angle 0° \rightarrow V_2 = V_1 + 12\angle 0° \quad ③$$

$$V_{oc} - V_2 = 6\angle 0°$$

$$\rightarrow V_{oc} = V_2 + 6\angle 0° = V_1 + 18\angle 0° \quad ④$$

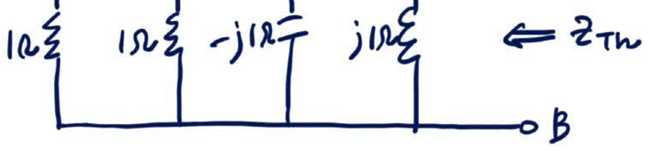
Rewriting ① using ②, ③ and ④,

$$(1+j1)V_1 - V_1 - 12\angle 0° + (1-j2)\times 4\angle 0° + j1(V_1 + 18\angle 0°) = 0$$

$$\rightarrow j2\times V_1 = 12\angle 0° - (1-j2)\times 4\angle 0° - j1\times 18\angle 0°. \quad \therefore V_1 = -5-j4$$

From ④, $V_{oc} = V_1 + 18\angle 0° = 13-j4 = 13.6\angle -17.1°$

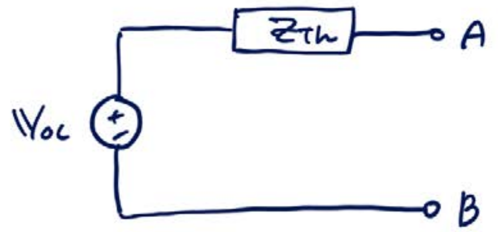
Setting all the independent voltage sources to 0V, the circuit becomes as shown below.




$$\frac{1}{Z_{Th}} = 1 + 1 + \frac{1}{-j1} + \frac{1}{j1} = 2$$

$$\therefore Z_{Th} = 0.5\,\Omega$$

Therefore, the Thévenin's equivalent circuit can be drawn as follows.




$V_{oc} = 13.6 \angle -17.1°$

$Z_{Th} = 0.5\,\Omega$ //

**5.** A sinusoidal signal, $v_1(t) = 2.5 \cos \omega t$, when added to a DC level of $V_2 = 2.5$ V, provides a 0- to 5-V clock signal used for a microprocessor. If the oscillation frequency of the signal is to be 1 GHz, let us design the appropriate circuit.

Consider the circuit in Fig. 5 where inputs $v_1(t)$ and $V_2$ are connected to yield the output $v_o(t)$. The component *A* should block any DC component in $v_1(t)$ from reaching the output but permit the 1-GHz signal to pass right through. Thus, the impedance of component *A* should be infinite at DC but very low at 1 GHz. Similarly, the component *B* should pass the DC component of $V_2$ while blocking any high-frequency signal. Therefore, the impedance of component *B* should be zero at DC but very high at high frequency.

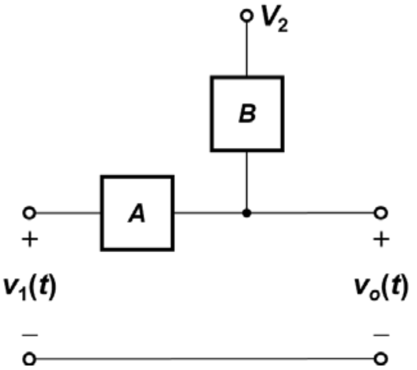
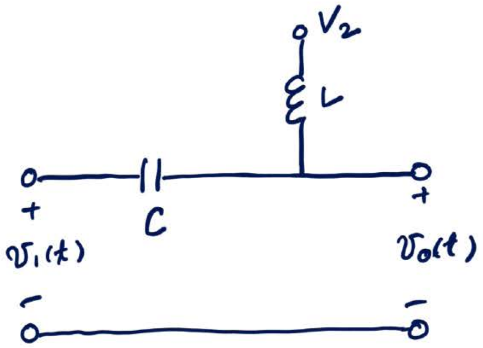



**Fig. 5**

**(a) (10 points)** Draw the simplest possible circuit network which is implemented using actual circuit elements by replacing the components *A* and *B* with circuit elements.




**(b) (10 points)** Determine the values of the used circuit elements so that the impedance of component *A* becomes 1 Ω and at 1 GHz and the impedance of component *B* becomes 10 kΩ at 1 GHz.

The impedance of A is $\frac{1}{j\omega C}$ and the impedance of B is $j\omega L$.

$\therefore \frac{1}{2\pi \times 1G \times C} = 1$ and $2\pi \times 1G \times L = 10k$

$\Rightarrow C = 159$ pF and $L = 1.59\ \mu H$.

**6.** **(20 points)** The op-amp circuit shown in Fig. 6 is called inductance simulator. Derive the input impedance $Z_{in}$ (= $V_{in}$ / $I_{in}$) of the given circuit.

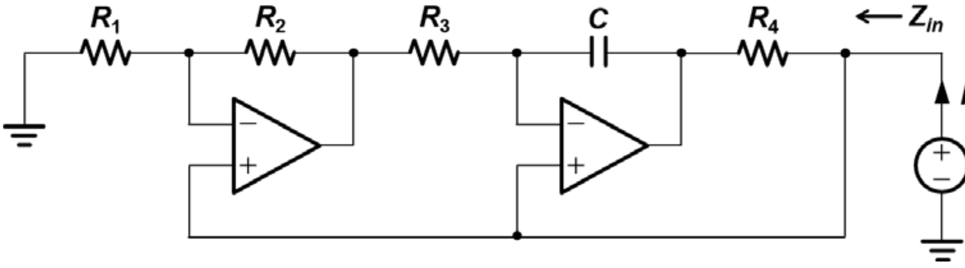
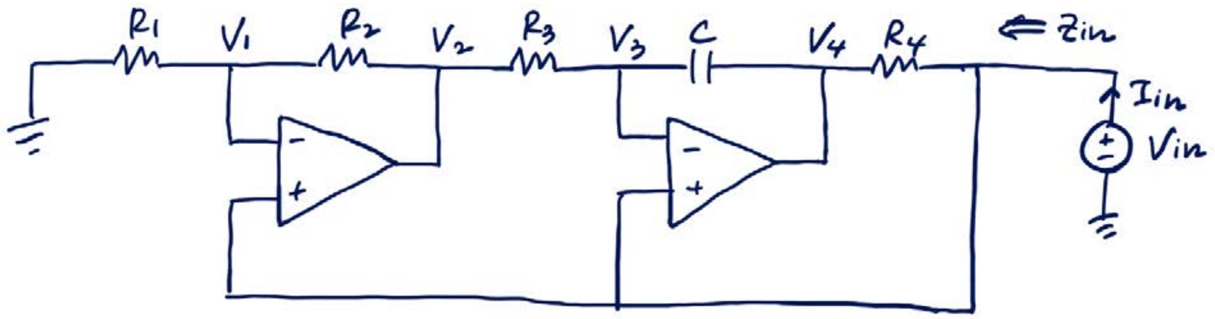



**Fig. 6**




Knowing that $V_1 = V_{in}$, we can write a nodal equation at the node of $V_1$ as follows.

$$\frac{V_{in}}{R_1} + \frac{V_{in} - V_2}{R_2} = 0 \Rightarrow V_2 - V_{in} = \frac{R_2}{R_1} V_{in} \quad \text{①}$$

At the node of $V_3$, again knowing that $V_3 = V_{in}$,

$$\frac{V_{in} - V_2}{R_3} + \frac{V_{in} - V_4}{1/j\omega C} = 0 \Rightarrow V_{in} - V_4 = \frac{V_2 - V_{in}}{j\omega C R_3} \quad \text{②}$$

Substituting ① into ②,

$$V_{in} - V_4 = \frac{R_2}{j\omega C R_1 R_3} V_{in}.$$

$$\therefore I_{in} = \frac{V_{in} - V_4}{R_4} = \frac{R_2}{j\omega C R_1 R_3 R_4} V_{in}$$

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{j\omega C R_1 R_3 R_4}{R_2}$$

**7. (20 points)** Determine the impedance $Z_L$ for maximum average power transfer and the value of the maximum average power transferred to $Z_L$ for the circuit in Fig. 7.

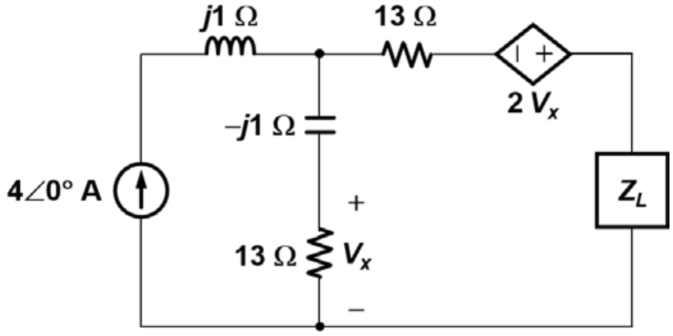
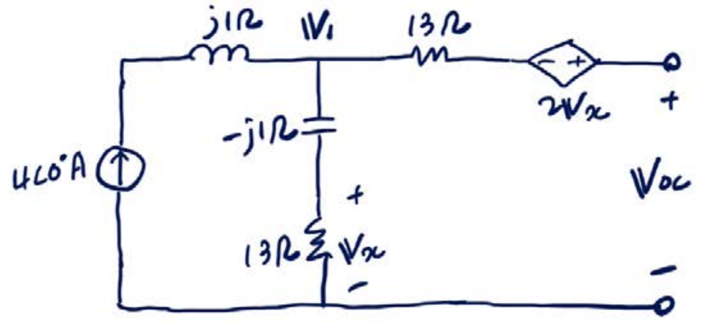



**Fig. 7**



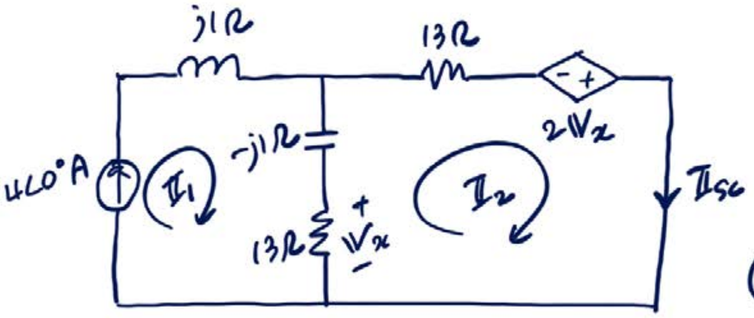

$V_1 = 4\angle 0^\circ \times (-j1 + 13)$

$= 52 - j4$

$V_x = 4\angle 0^\circ \times 13 = 52$

$V_{oc} = V_1 + 2V_x$

$= 52 - j4 + (2 \times 52) = 156 - j4$




$I_1 = 4\angle 0^\circ$ ①  $I_2 = I_{sc}$ ②

$V_x = 13(I_1 - I_2) = 52 - 13 I_2$ ③

$13 I_2 - 2V_x - V_x - j1(I_2 - I_1) = 0$

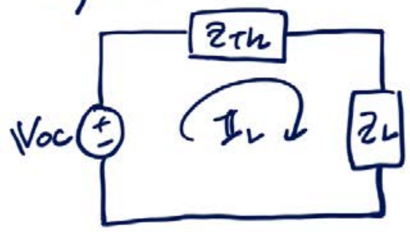
$j1 \times I_1 + (13 - j1) I_2 - 3V_x = 0$ ④

Solving ①, ②, ③ and ④ simultaneously,

$I_{sc} = 3 - j0.019$ A

$\therefore Z_{Th} = \dfrac{V_{oc}}{I_{sc}} = 52 - j1\ \Omega$

Therefore, we can redraw the given network using the Thévenin's equivalent circuit.




For maximum power transfer,

$Z_L = Z_{Th}^* = 52 + j1\ \Omega$

$I_L = \dfrac{V_{oc}}{Z_{Th} + Z_L} = \dfrac{156 - j4}{104} = 1.5\angle -1.47^\circ$ A

$\therefore$ The maximum average power transferred to $Z_L$ is

$$P_{L,max} = \frac{1}{2}|I_L|^2 \times R_L = \frac{1}{2} \times 1.5^2 \times 52 = 58.5\,W.$$

**8.** **(20 points)** Given the network in Fig. 8, find the input source voltage and the input power factor.

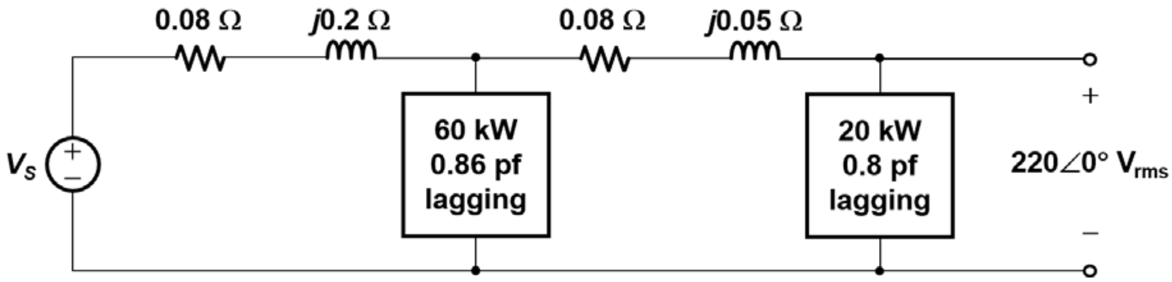
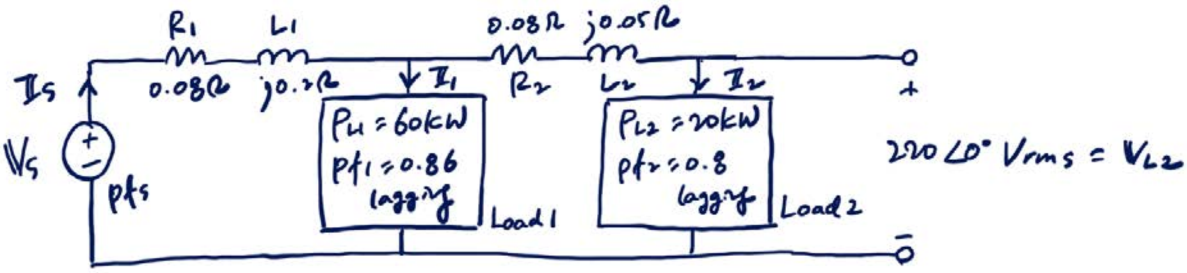



**Fig. 8**




At load 2, $|\mathbb{I}_2| = \dfrac{P_{L2}}{|\mathbb{V}_{L2}| \times pf_2} = \dfrac{20k}{220 \times 0.8} = 113.64$ Arms

$\theta_{I_2} = \theta_{V_{L2}} - \cos^{-1}(pf_2) = -36.87°$ $\quad \therefore \mathbb{I}_2 = 113.64\angle{-36.87°}$ Arms

At load 1, $|\mathbb{I}_1| = \dfrac{P_{L1}}{|\mathbb{V}_{L1}| \times pf_1}$ where $\mathbb{V}_{L1} = \mathbb{V}_{L2} + \mathbb{I}_2 \times (0.08 + j0.05)$

$= 220\angle 0° + 113.64\angle{-36.87°} \times (0.08 + j0.05)$

$= 230.68\angle{-0.23°}$ Vrms

$\therefore |\mathbb{I}_1| = \dfrac{60k}{230.68 \times 0.86} = 302.44$ Arms, $\theta_{I_1} = \theta_{V_1} - \cos^{-1}(pf_1) = -0.23 - \cos^{-1}(0.86)$

$= -30.91°$

Thus, $\mathbb{I}_1 = 302.44\angle{-30.91°}$ Arms

At the source side, $\mathbb{I}_S = \mathbb{I}_1 + \mathbb{I}_2 = 302.44\angle{-30.91°} + 113.64\angle{-36.87°}$

$= 415.63\angle{-32.54°}$ Arms

$\mathbb{V}_S = \mathbb{V}_{L1} + \mathbb{I}_S \times (0.08 + j0.2) = 230.68\angle{-0.23°} + 415.63\angle{-32.54°} \times (0.08 + j0.2)$

$= 307.72\angle 9.59°$ Vrms

$pf_S = \cos(\theta_{V_S} - \theta_{I_S}) = \cos(9.59° + 32.54°) = 0.74$ lagging

**9.** Consider the circuit in Fig. 9. Assume that the frequency *f* is 60 Hz.

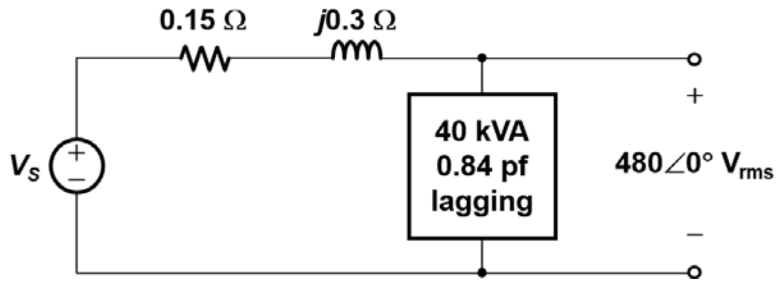



**Fig. 9**

**(a) (10 points)** Determine the value of capacitance that must be connected in parallel with the load so that the power factor of the combined load and capacitor is unity.

The complex power before the power factor correction is given by

$S_{old} = 40\angle\cos^{-1}(0.84) = 40\angle 32.86° = 33.6 + j21.7$ kVA.

After power factor correction, the new complex power for the combined load and capactor should be $S_{new} = 33.6 + j0$ kVA.

Therefore, we can write $S_{cap} = S_{new} - S_{old} = -j21.7$ kVA.

$Q_{cap} = \frac{V_L^2}{X_C} \rightarrow X_C = \frac{V_L^2}{Q_{cap}} = \frac{(480)^2}{21.7k} = 10.62\Omega$

Since $X_C = \frac{1}{\omega C}$, $C = \frac{1}{\omega X_C} = \frac{1}{2\pi \times 60 \times 10.62} = 249.77\ \mu F$.

**(b) (10 points)** Calculate the complex power supplied by the source after the power factor has been corrected to unity.

The current supplied by the source can be calculated as

$I_S = \frac{P_L}{|V_L| \times pf} = \frac{33.6k}{480} = 70$ Arms.

The complex power for the line parasitics is given by

$S_{line} = 70^2 \times (0.15 + j0.3) = 735 + j1470$ VA

$\therefore S_{source} = S_{line} + S_{new} = (0.735 + j1.47) + 33.6$

$= 34.335 + j1.47$ kVA

$= 34.37\angle 2.45°$ kVA.

10. **(20 points)** A student has discovered that her tape player has the limited high-frequency response shown in Fig. 10a. She decides to insert a "treble boost" circuit between the tape deck and the main amplifier that has the transfer function shown in Fig. 10b. Passing the tape audio through the boost should produce a "flat" response out to about 20 kHz. The circuit in Fig. 10c is her design. Show that the circuit's transfer function has the correct form, and select the component values for $R_1$ and $R_2$ for proper operation.

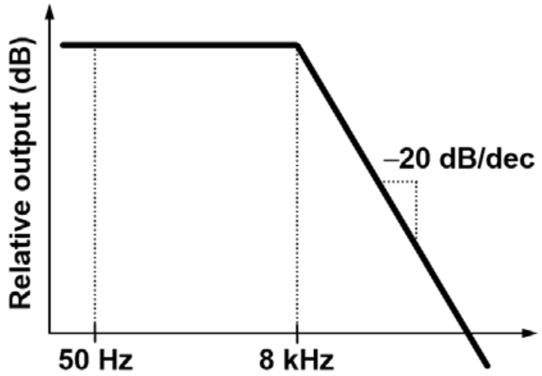



Fig. 10a

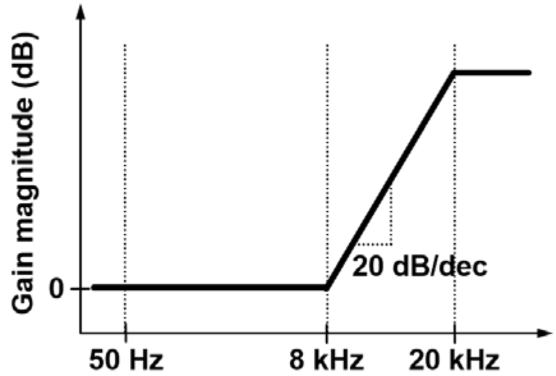



Fig. 10b

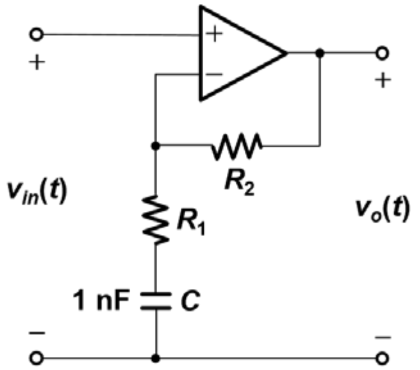
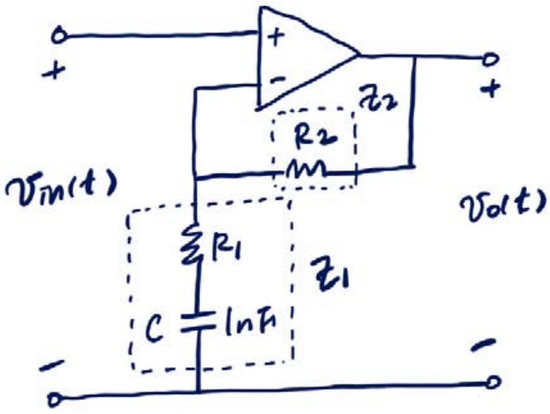



Fig. 10c




$$\frac{V_o}{V_{in}} = 1 + \frac{Z_2}{Z_1}$$

$$= 1 + \frac{R_2}{R_1 + 1/j\omega C_1} = \frac{1 + j\omega C(R_1+R_2)}{1 + j\omega C R_1}.$$

Hence, we get the transfer function having one pole at $f_p = \frac{1}{2\pi C R_1}$ and one zero at $f_z = \frac{1}{2\pi C(R_1+R_2)}$.

In addition, we can find that $f_z$ is lower than $f_p$, which is required condition to implement the transfer function shown in Fig. 10b

Hence, the circuit's transfer function has the correct form..

Since the pole frequency should be 20 kHz,

$$f_p = 20k = \frac{1}{2\pi C R_1} \longrightarrow R_1 = \frac{1}{2\pi C f_p} = \frac{1}{2\pi \times 1n \times 20k} = 7.96\,k\Omega$$

The zero frequency should be 8 kHz, and thus

$$f_z = 8k = \frac{1}{2\pi C(R_1+R_2)} \longrightarrow R_2 = \frac{1}{2\pi C f_z} - R_1 = \frac{1}{2\pi \times 1n \times 8k} - 7.96k$$

$$= 11.93\,k\Omega$$