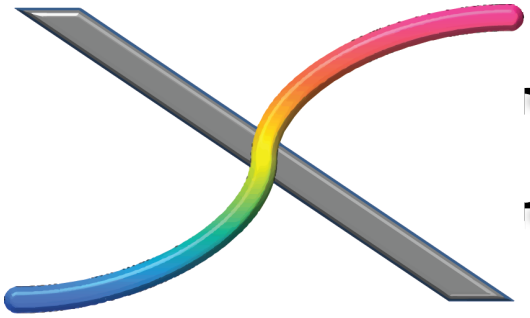
SEVENTH FRAMEWORK PROGRAMME
THEME ICT-2013.3.4
Advanced Computing, Embedded and Control Systems



EXCESS

Execution Models for Energy-Efficient Computing Systems
611183

V 1.0
Evaluation of Cluster Power Tools

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Executive Summary

This document presents the EXCESS execution environment and its power measurement system. The analysis of its accuracy and usability is also a part of the this document.

Contents

1 Power Cluster Environment

The EXCESS cluster is used as an experimental platform for the development in the field of energy-aware high performance computing. Users of the cluster are enabled to perform technical implementations and evaluations, which are not feasible or at least currently limited on conventional HPC platforms. Furthermore, the cluster includes additional components to monitor of cluster's hardware in order to support applications at runtime to determine the optimal configuration (or resource allocation, respectively) through a correlation analysis. This section briefly describes the latest cluster built with a special focus on the installed power measurement system.

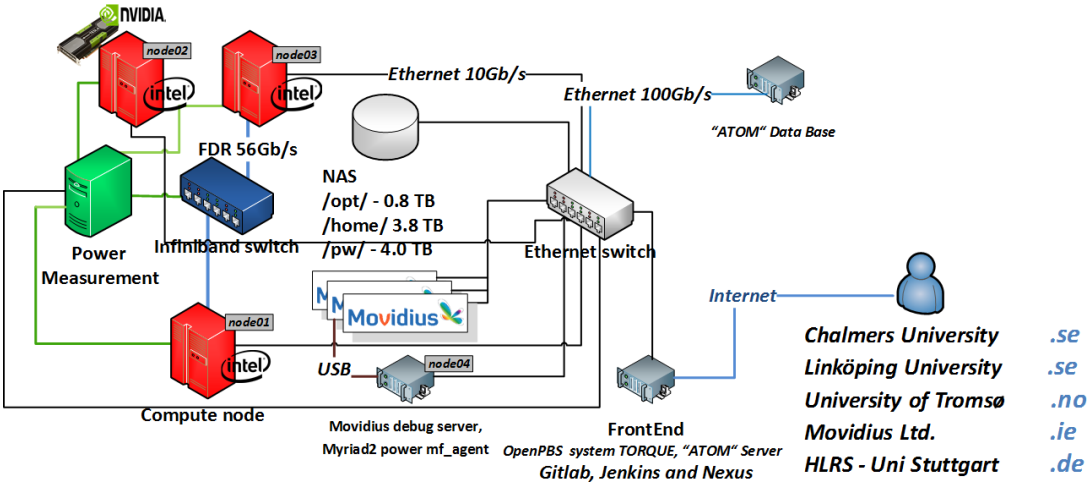

Figure 1: The EXCESS cluster

1.1 EXCESS Cluster

The cluster consists of three compute nodes, and other essential infrastructure components such as a NAS server, a front end node, a power measurement system, and network

switches (see Figure 1). The interested reader can find a detailed overview of these components in Deliverables D5.2 and D3.4 [12, 11].

Table 1: Configuration of compute nodes `node01` and `node02`

Amount	Hardware Component
1 x	Intel Server Chassis P4308XXMHGC;
1 x	Intel Server Board S2600COE
2 x	Intel Xeon CPU: E5-2690 v2 - 10 cores 25MB L3 smart cache 4 mem. ch. DDR3 1866 MHz = 59.7 GB/s[2]
2 x	Intel Heat sink AUPSRCB
8 x	HP Memory 4 GB DDR3 MFG 708633-B21 - 1866 MHz PC3-14900 CL13 - ungepuffert - Dual Rank - ECC[3]
1 x	GPU im node01: Tesla K40c - GPU Clock: 745 MHz; Shading Units: 2880 GDDR5 12288 MB; 288 GB/s; PCIe3.0 8GT/s x16[5]
1 x	Connect-IB HCA, Mellanox MCB193A-FCAT; single-port QSFP FDR IB (56Gb/s); PCIe3.0 8GT/s x16[4]
1 x	Hard disk: 500GB WD5003AZEX Black
1 x	SSD: 128GB Vertex450
1 x	Schaltnetzteil: node01: *DPS-750XB A REV02F* node02: *EartWatts EA-650*

Table 2: Configuration of compute node `node03`

Amount	Hardware Component
1x	Chenbro 4U 17.5” Compact Industrial Server Chassis RM42300
1x	Gigabyte Server Board - MD70-HB0 (Rev. 1,2)
2x	Intel Xeon CPU: E5-2680 v3 (Haswell) - 12 cores 30MB L3 Smart Cache 4 Mem. Ch. DDR4 2133 MHz = 68 GB/s [1]
2x	Enermax Heat sink ETS-T40-W
8x	SAMSUNG DRAM 16GB Samsung DDR4-M393A2G40DB0-CPB- 2133 MHz CL15 - Registered DIMM - Dual Rank - ECC [6]
1x	Intel Ethernet Server Adapter I350-T2 - PCI Express 2.1 x4 Low Profile - 1000Base-Tx2
1x	Hard disk: 500GB WD5003AZEX Black
1x	SSD: 240GB Vertex460A
1x	Power supply: `EartWatts EA-750`

1.2 Power Measurement

As mentioned above, the various cluster components such as entire nodes, processors, PCIe interfaces and so on, are monitored by the external power measurement system. In contrast to the power measurement of the Movidius hardware, where the measurement shunts and A/D converters are part of the system implemented as a daughter card (see

[14]), we use four PCIe cards APCIE-3021-16 [7]. Each PCIe card includes eight analogue input channels and a single A/D converter. These cards are installed in the power measurement system based on the *x_86* server with Linux OS (Kernel 2.6.32). Its services provide wide functionalities covering the dynamic configuration, execution, filtering and analysis of the measurements, which all compose the EXCESS cluster's power tools.

We described the power tools and their usage in Deliverable D5.7 in the section "EXCESS Cluster Power Tools" [10]. Customized drivers, services and a technical description of the power measurement system, based on PCIe-A/D converters, are available in the EXCESS repository at:

`https://github.com/excess-project/cluster-power-tools`

1.3 Results

Firstly, we defined the set of benchmarks for obtaining information about the efficiency of the hardware and software. The benchmarks and their results serve as examples for both the use of the cluster environment and the analysis of the performance- and energy efficiency of the installed hardware and software. You can find the source code by following the link: https://github.com/excess-project/benchmarks

The measurement system supports the electric power profiling of the hardware components with high accuracy and high frequency with up to 50 kHz (by measurement both valtoge and electic current of a hardware component). The electrical power of all processors (including the DRAM modules) are measured with a relative error of — $\varepsilon_{rel} = 100 \times \frac{P_{real}-P_{meas}}{P_{real}}$— less than ± 0.1%, where P_{meas} is the measured and P_{real} real power consumption. One can decrease the error to ± 0.01% by applying implemented filters. The latter can be implemented at the cost of reducing the time resolution. The service PTP[1] synchronizes the clocks between the power measurement system and the compute nodes, which hold the drift between the distributed clocks by less than 20 µs (experimentally established). We reserved a dedicated Ethernet interface on each of the nodes for this service (not shown on Figure 1).

1.3.1 Power Measurement Accuracy Analysis

Each compute node of the EXCESS cluster receives electrical power from the provided power supply. The integrated VRMs[2] provide the chips with an appropriate supply voltage. Both of the steps involve the work of semiconductor switches such as *MOSFET*s[3]. These are the interference sources, referred to as ripple noise voltage, which limits the accuracy of the power profiling. To test this hypothesis, we compared three different power sources:

- *Server Power Supply* Intel DPS-750XB A REV02F
- *Desktop Power Supply* Antec EartWatts EA-650

[1]The Precision Time Protocol (PTP) is a protocol used to synchronize clocks throughout a computer network.

[2]Voltage Regulator Module

[3]metaloxidesemiconductor field-effect transistor

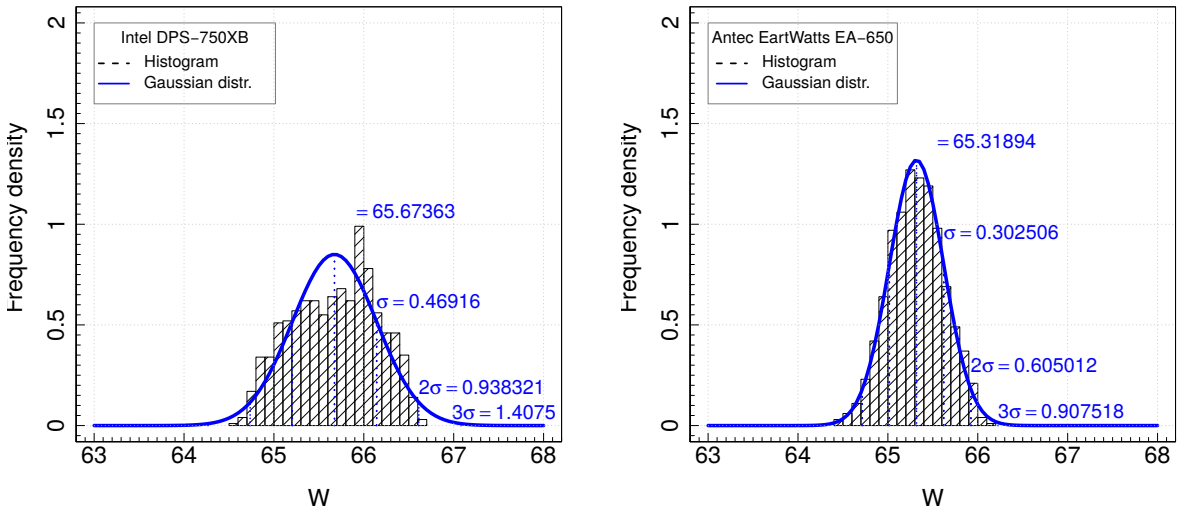

Figure 2: The histograms and density functions of the normal distribution are shown for the electric power of the circuit equipped with RB50-2R2-J 2.2Ω *and power supply Intel DPS-750XB A (on the left side) or Antec EartWatts EA-650 (on the right side). The sample contains a total of* 1000 *measurements of the voltage and electric current over the time. The measuring frequency was* 50.0 kHz.

- *Lithium polymer battery* LiPo 11.1 V

We connected a power resistor *RB50-2R2-J* 2.2 Ω to the above listed power sources as if it were a conventional processor, although with the difference that the resistor is a passive load. For each of the sources under load, we recorded the voltage and current profiles. The histograms of the calculated power, as product of applied voltage and the electric current for two power supplies, are illustrated in Figure 2. Each of the samples contains a total of 1.000 measurements for voltage and current, which were sampled at a frequency of 50 kHz. Additionally, the normal (or Gaussian) distribution with the adequate parameters is shown. To yield the distribution, the standard deviation σ and mean value μ were calculated for the measured values. As it can be seen from Figure 2, the generated sample for *EartWatts EA-650* comes very close to the normal distribution. In contrast, the *Intel DPS-750XB* generates samples that do not follow a Gaussian distribution.

A possible cause for this could be the modulation technique used for pulse-width modulation (PWM) within the power supplies[4]. This modulation is done through the synchronized switching of the *MOSFET* transistors. The number of transistors and the frequency of the switching, along with other features, affects the cleanness of the recorded signal. Figure 3 shows two oscilloscope profiles of the voltage signal for both of the power supplies under passive load (*RB50-2R2-J*). The amplitude of the *Intel DPS-750XB* signal is about 0.2% of the voltage level, and is four times higher than one of *Antec EartWatts EA-650*. The frequencies are 116 kHz for *Intel DPS-750XB* and 70 kHz for *EartWatts EA-650*. The interested reader can find an extensive study about *Antec*

[4]PWM controls the amount of power delivered to the hardware components.

EartWatts EA-650's features in [15]. Unfortunately, we could not find any detailed information about *Intel DPS-750XB*'s architecture. A book written by Valter Quercioli on "Width Modulated (PWM) Power Supplies" [18] contains detailed information about the functioning of *PWM*s, though.

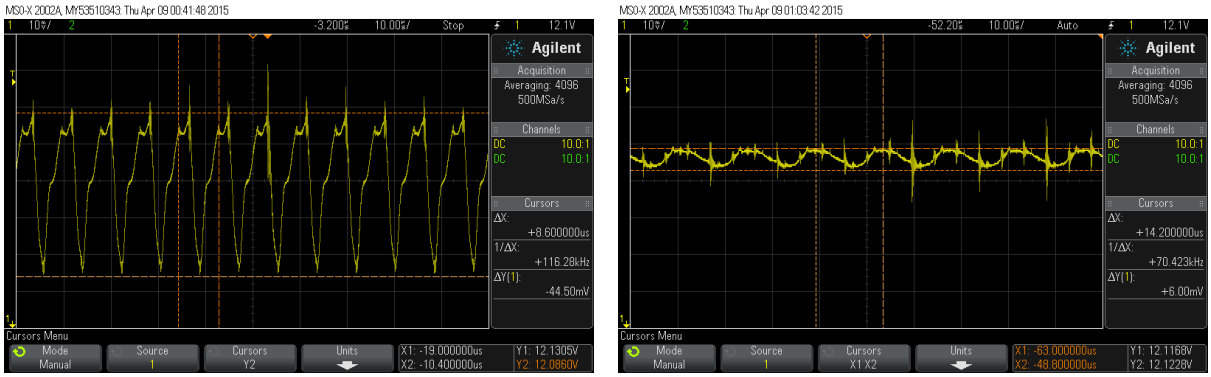

Figure 3: The figures show the oscillograms taken in mode "Average over 4096 samples" at 500 *MSa/s. The change in the voltage over time was measured in parallel to the resistor* RB50-2R2-J 2.2Ω*, which was connected to the +12 VCD output of the power supply Intel DPS-750XB A (on the left side) or Antec EartWatts EA-650 (on the right side).*

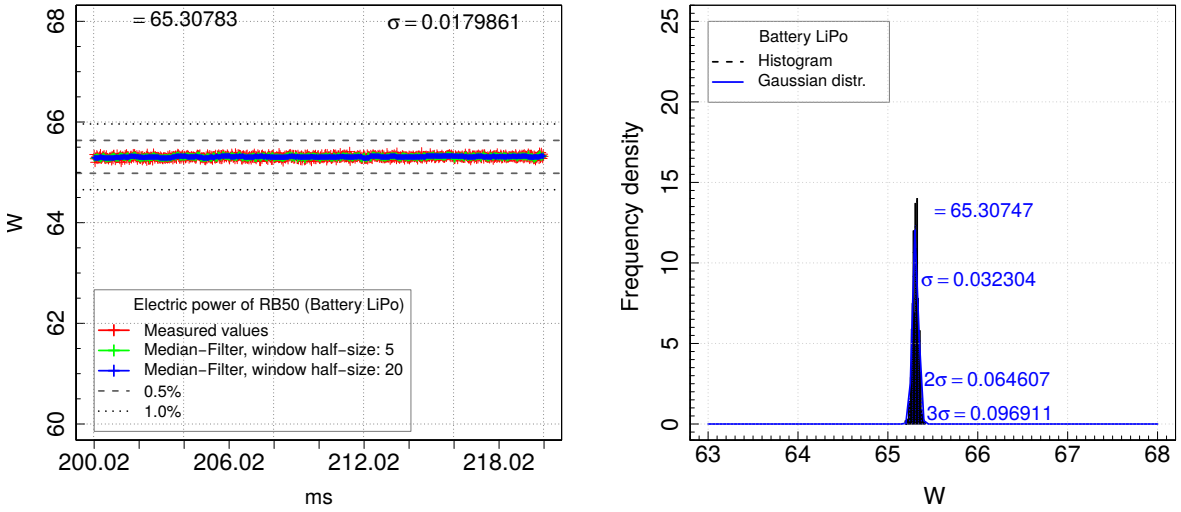

Figure 4: The measured power consumption ($P = V \cdot A$) over time (on the left side) and the histogram and density functions of the normal distribution are shown for the circuit with the resistor RB50-2R2-J 2.2 Ω *and lithium polymer battery* LiPo 11.1 V*. The measuring frequency was* 50.0 kHz*.*

Figure 4 shows the power measurements when the lithium polymer battery *LiPo 11.1 V* is connected to the power resistor. Additionally, the figure illustrates the recorded power profile. In contrast to a power supply, the battery does not produce a ripple noise voltage. This is clearly visible through the small value of σ, and the thin line of the power profile; the profile contains the measured and filtered values (cf. legend on the diagram).

As mentioned earlier, the power measurement system records both the voltage and electrical current profiles. In the second step, we measured the power consumption of the processor *Intel E5-2690v2* (*Ivy Bridge*) during the idle state—meaning that no computational job was executed on the compute node. The histogram for 500 voltage measurement for the power supply *Antec EartWatts EA-650* is shown on the left-hand diagram in Figure 6. When the lithium battery is connected to the processor, the standard deviation σ for the measured values is noticeably reduced.

Figure 5 depicts the corresponding histograms for the measured electric current. The results show that the battery, as a power source, affects much less the measurement of the power supply. Opposite to this, the measurement of the processor *E5-2680v3* (Haswell) shows no noticeable differences between the operation with *Antec* and *LiPo 11.1 V*. The histograms showing the latter case are depicted in Figure 7.

In contrast to *Ivy Bridge*, *Haswell* is able to switch to the power management state C6, which powers down the cores, ring and uncore components [9]. However, during the idle state, the operation system services are still active and activate these components at regular intervals (every $\sim$ 1 ms on the EXCESS cluster). This leads to a sharp increase or decrease in the electrical current (cf. Figure 8). Similarly to the voltage measurement, the choice of the power source has no noticeable effect on the measurements. A plausible reason for this may be that the *Haswell* processor includes a fully integrated voltage regulator additionally to the main-board regulator [8]. Both regulators cause additional noise in measurements, which is comparable with the power supply noise. The similarity between the normal distribution and the distribution of the measured values enables us to increase the measurement accuracy by applying the median-filter included in the EXCESS power tools. This works particularly well for the *Haswell* processor and voltage measurements. Further details on the power measurement for various hardware components of the EXCESS compute nodes in idle state are available in the Deliverable D5.4 [13].

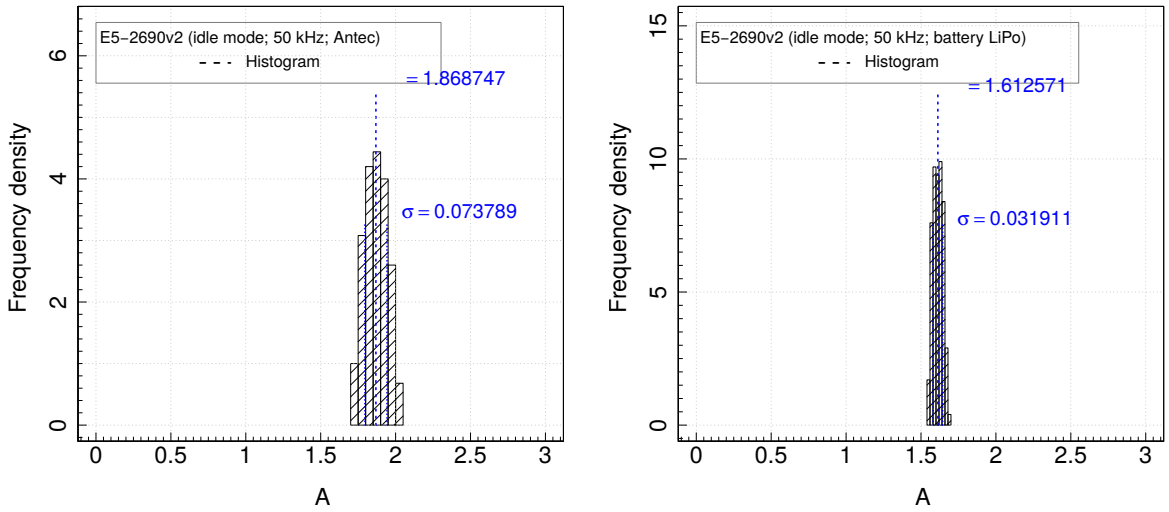

Figure 5: The histograms show the dispersion of 500 electric current measurements in the circuit of the first processor Intel E5-2690v2 *(*Ivy Bridge*) and the power supply Antec EartWatts or Intel DPS-750XB A. During the measurement, there was no computational jobs on the compute node. The measuring frequency is set to* 50.0 kHz.

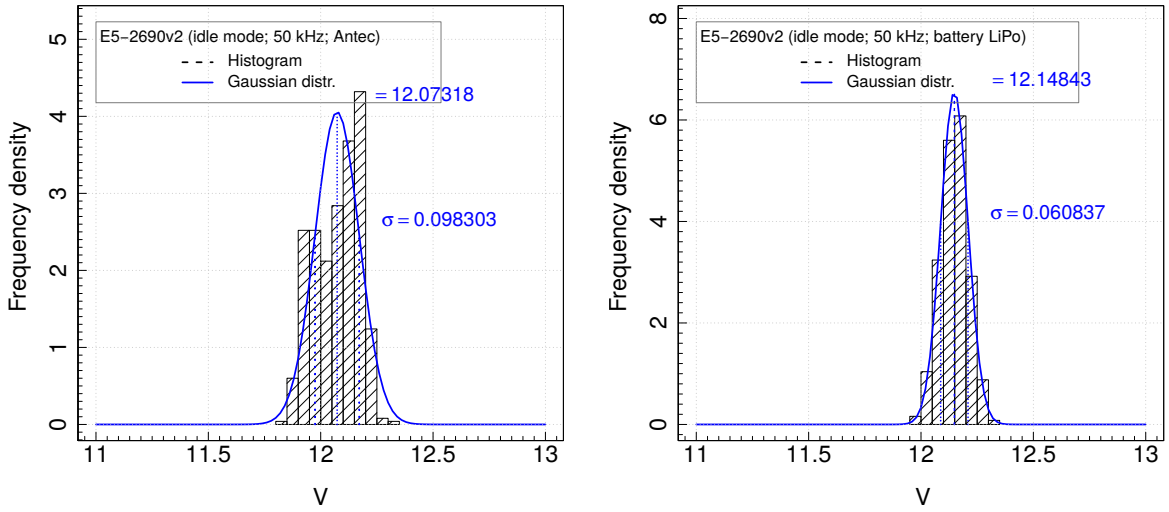

Figure 6: The histograms show the dispersion of 500 voltage measurements in the circuit of the first processor Intel E5-2690v2 *(*Ivy Bridge*) and the power supply Antec EartWatts or Intel DPS-750XB A. During the measurement, no computational jobs where running on the compute node. The measuring frequency is set to* 50.0 kHz.

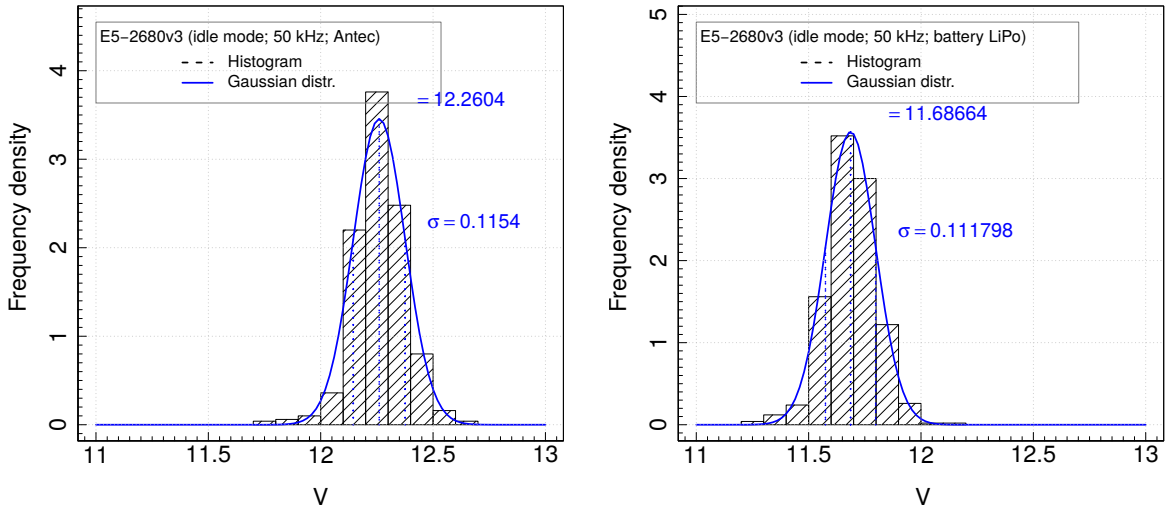

Figure 7: The histograms show the dispersion of 500 voltage measurements in the circuit of the first processor Intel E5-2680v3 *(*Haswell*) of a compute node and the power supply Antec EartWatts or Intel DPS-750XB A. During the measurement, there was no computational jobs on the compute node. The measuring frequency was* 50.0 kHz.

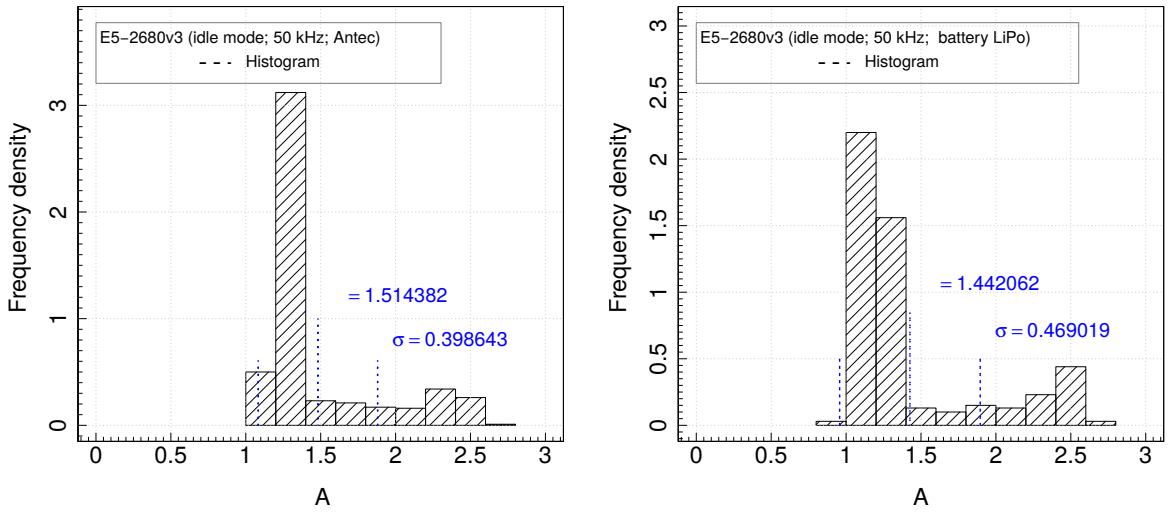

Figure 8: The histograms show the dispersion of 500 electric current measurements in the circuit of the first processor Intel E5-2680v3 *(*Haswell*) of a compute node and the power supply Antec EartWatts or lithium polymer battery* LiPo 11.1 V*. During the measurement, no computational jobs were executed on the compute node. The measuring frequency was set to* 50.0 kHz

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1.3.2 Clock Synchronization Analysis

Figure 9 shows the power profile of the first processor *E5-2680v3* (Haswell) on node03 during the execution of the kernel operation *ADD*, $a[i] = b[i] + c[i]; 0 < i < 57664$, on each of the 12 cores. The double-precision floating-point arrays fit into the L3-cache. The loop was repeated 30 times. The test is scheduled as follows:

1. Start 12 OpenMP Threads
2. Refill the cache with the arrays
3. Start the PAPI counters (e.g. RAPL, UNHALTED_CORE_CYCLES)
4. Read the timestamp
5. Read the TSC register[5]
6. Compute the kernel *ADD* 30 times
7. Read the TSC register
8. Read the timestamp
9. Save metrics and go to the next test

Two determined timestamps are shown in Figure 9 with two vertical dotted lines. The difference between these two timestamps is 2.122 ms. The duration time, which was measured with TSC, equals to 2.029 ms. This results in a time-synchronization error, and instrumentation overhead of 0.093 ms. The median-filter was applied to the measured values. The result of the filtering step, the standard deviation σ, and the mean value μ are also depicted in the figure. At the beginning of the computation, the power increases within 0.2 ms and then stays stable until the end of the execution.

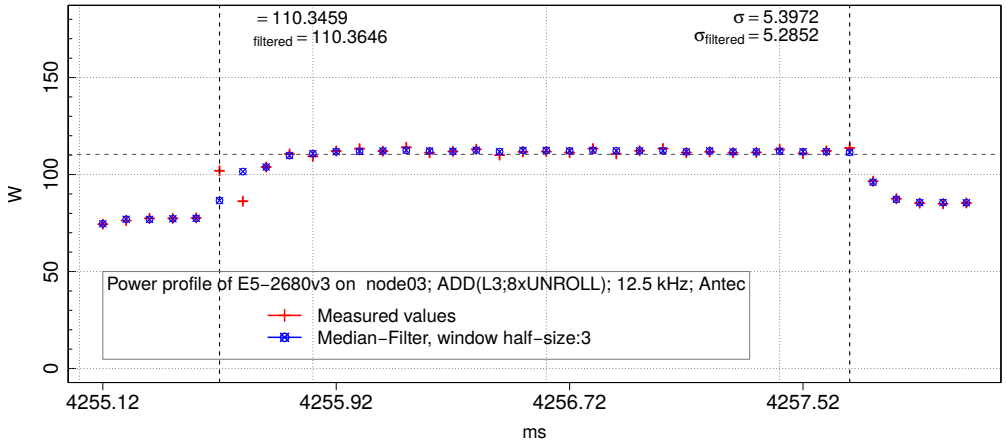

Figure 9: The diagram shows the power profile of the first processor E5-2680v3 *(Haswell) on node03 during the execution of a kernel operation* ADD $a[i] = b[i] + c[i]; 0 < i < 57664$ *on each of 12 cores.*

[5]The Time Stamp Counter (TSC) register counts the number of cycles since reset. It provides a high-resolution, low-overhead way to measure the time.

1.3.3 Comparison between RAPL and A/D Converters

The power stream benchmark contains various kernel operations including the previously mentioned kernel *ADD*. During the benchmark, the kernel is started with various configurations, which include all combinations of the possible CPU frequencies and the number of active cores (see Deliverable D3.4 [11] for further details).

The results of the power measurement system were compared with the results of the RAPL counters for all configurations. The RAPL counters of the Ivy Bridge and Haswell processors show less power consumption than the measurements with the A/D converters. This difference grows with the increase of the measured power, and can be approximated with $K(P_{rapl}) = \alpha_0 + \alpha_1 P_{rapl}$, where P_{rapl} is the obtained RAPL value.

Hence, the results—obtained through the power measurement system $P_{a/d}$—can be approximated with the equation $P_{a/d} = P_{a/d} + K(P_{rapl}) + \epsilon_{P_{rapl+K}}$, where $\epsilon_{P_{rapl+K}}$ is the error of the approximation. The comparison for the kernel *ADD*, if the data fits RAM: $a[i] = b[i] + c[i]; 0 < i < 42949664$ on each of cores, is plotted on Figure 10. Additionally, the upper limits of the error $\epsilon_{P_{rapl}} = P_{a/d} - P_{rapl}$ are specified.

Table 3 contains the approximation of the difference between the measurements done with RAPL counters and A/D converters for various configurations of the kernel operation *ADD*.

We have also compared the RAPL measurements with other kernels. The observed differences were within the limits that were calculated for the kernel *ADD*. It should be noted that the RAPL counters do not consider the power consumption of the board's *VRM*. Another property is that the differences between the RAPL and A/D converter measurements are approximately linear for the same kernel both as a function of the CPU frequency while the number of active cores is fixed, and as a function of the number of

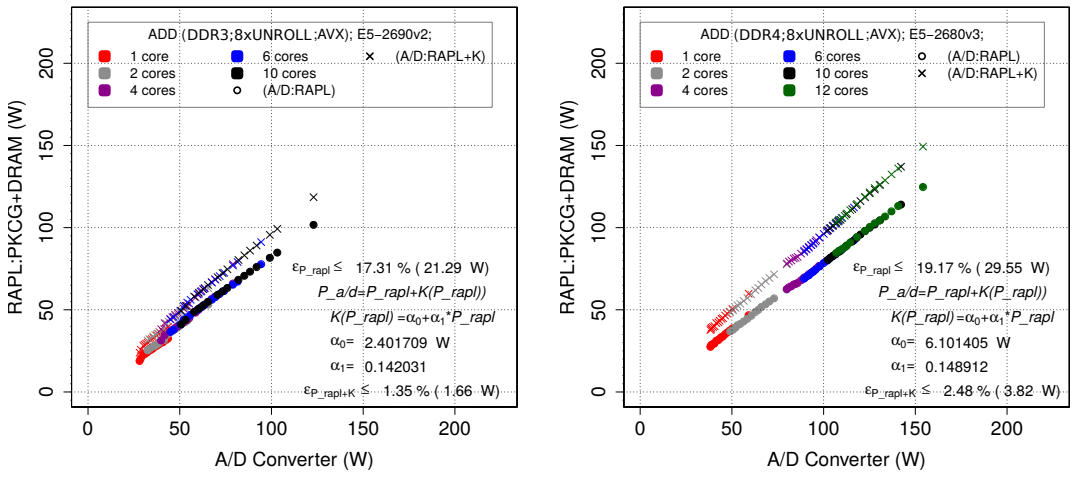

Figure 10: Comparison between RAPL counters and the EXCESS power monitoring system based on A/D converters. The values on the diagrams are obtained by the power measurements with the RAPL counters and A/D converters for all combinations of the number of threads and CPU frequencies during the execution of the kernel operation ADD*, if the data fits into the RAM:* $a[i] = b[i] + c[i]; 0 < i < 42949664$ *on each core.*

active cores while the CPU frequency is constant.

1.4 Integration of Power Measurement System

The cluster environment provides two methods for the power profiling, which can be divided in two main groups:

High-Resolution Mode All measured values are stored on a local hard disk on the power measurement system. The values for each metric (voltage V and electric current A) are stored in chains, which contain the measurements for 1 second; the interval is configurable. Each of the individual chains is stored in an unformatted file, which hides the single precision floating point numbers. The timestamp of the first measurement in the chain is also stored in a dedicated file. After the measurement is stopped, all data is archived and copied to a shared folder owned by a user. The power measurement tools were specially designed to handle and analyse such data.

Runtime Mode The power measurement system, parallel to the measurements, calculates the average power consumption of the hardware components, and sends the consumption to the database of the EXCESS monitoring framework. The transaction will be initiated when new incoming chains with the measurements for the voltage and electric current are ready. The time interval for the average values is also configurable. Currently, the system sends values averaged over 100 ms.

The *High-resolution* and *Runtime* modes can be used together in any combination. The power measurement of the compute nodes is switched on automatically at the beginning of a job. At the end of a job, the power measurement will be finished. Alternatively, the measurement can be started and finished manually.

1.5 Conclusion

The EXCESS cluster provides an execution environment together with the EXCESS power monitoring tools. The tools are implemented with respect to usability, accuracy and scalability. The current configuration of the system supports the simultaneous operation of a maximum of 32 measurement channels running at 12.5 kHz. It should be

Table 3: Differences between the measurements done with RAPL counters and A/D converters for various configurations of the kernel operation ADD.

CPU	Kernel	$K(P_{rapl})$	$\epsilon_{P_{rapl+K}}$	$\epsilon_{P_{rapl}}$
E5-2690v2 (Ivy Bridge)	ADD;L1	$1.460\,56 + 0.212\,115 \cdot P_{rapl}$	$< 2.22\%(2.72\text{W})$	$\leq 24.5\%(29.98\text{W})$
E5-2690v2 (Ivy Bridge)	ADD;L2	$5.137\,535 + 0.002\,18 \cdot P_{rapl}$	$< 0.76\%(0.91\text{W})$	$\leq 5.11\%(6.17\text{W})$
E5-2690v2 (Ivy Bridge)	ADD;L3	$3.414\,631 + 0.112\,679 \cdot P_{rapl}$	$< 0.73\%(0.97\text{W})$	$\leq 14.81\%(19.63\text{W})$
E5-2690v2 (Ivy Bridge)	ADD;DDR3	$2.401\,709 + 0.142\,031 \cdot P_{rapl}$	$< 1.35\%(1.66\text{W})$	$\leq 17.31\%(21.29\text{W})$
E5-2680v3 (Haswell)	ADD;L1	$3.407\,782 + 0.144\,827 \cdot P_{rapl}$	$< 1.02\%(1.19\text{W})$	$\leq 17.49\%(20.34\text{W})$
E5-2680v3 (Haswell)	ADD;L2	$4.302\,786 + 0.125\,509 \cdot P_{rapl}$	$\leq 0.84\%(0.9\text{W})$	$\leq 17.32\%(18.68\text{W})$
E5-2680v3 (Haswell)	ADD;L3	$3.291\,371 + 0.143\,92 \cdot P_{rapl}$	$\leq 1.7\%(2.31\text{W})$	$\leq 17.37\%(23.67\text{W})$
E5-2680v3 (Haswell)	ADD;DDR4	$6.101\,405 + 0.148\,912 \cdot P_{rapl}$	$\leq 2.48\%(3.82\text{W})$	$\leq 19.17\%(29.55\text{W})$

noted that the number of the measurement channels can be at least doubled. However, there are two disadvantages of such a system, which can be probably eliminated.

The first disadvantage is the measurement of the processors together with the memory modules. The reason for this is that the same power connector is used for both the processor and memory. Probably the most reliable method to distinguish the CPU power from the power of the RAM is using so-called *DDR Riser Cards*: the measurement shunts, which are integrated in these cards, can be connected to the measurement channels of the system. However, these cards could affect the memory frequency in a negative way.

The second disadvantage comes from the fact that the power measurement and the progress of the program execution are synchronized with the help of timestamps. Currently, a user has to add manually additional instructions to store the timestamps of the various phases of the program. These timestamps and measurement values can then be used as input data for the power tools to create a detailed analysis of the program. In this context, we aim to write a plug-in for the visualization performance tool *Vampir* [16]. *Vampir* provides various visualization techniques to show the collected performance and power data. Then, the user can use automatic instrumentation provided by several trace tools including *Score-P trace* [17] or *Vampir trace* [16].

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2 Glossary

Term	Description
API	Application Programming Interface
ATOM	Monitoring framework for the conventional HPC and Movidius platforms
AVX	Advanced Vector Extensions
BSD	Berkeley Software Distribution (BSD) is a Unix operating system derivative
Chalmers	Chalmers University of Technology
FMA	Fused Multiply-Add instruction
CG	Conjugate Gradient method
CT	Computed tomography
CRS	Compressed sparse row storage format represents a sparse matrix.
EXCESS	Execution Models for Energy-Efficient Computing Systems
GPGPU	General Purpose Computation on Graphics Processing Unit
HLRS	High Performance Computing Center Stuttgart
HPC	High Performance Computing
I/O	Input/Output
JTAG	Joint Test Action Group specifies the use of a dedicated debug port
LiU	Linköping University
MPI	Message Parsing Interface
PBS	Portable Batch System
PTP	Precision Time Protocol
PCIe	PCI Express (Peripheral Component Interconnect Express)
RISC	Reduced instruction set computing
RTEMS	Real-Time Executive for Multiprocessor Systems
SHAVE	Movidius SHAVE processor is a hybrid stream processor architecture combining the various features of GPUs, DSPs and RISC
TCP/IP	Transmission Control Protocol / Internet Protocol (TCP/IP)
UiT	University of Tromsø
USB	Universal Serial Bus
USTUTT	Stuttgart University
x_86	x86 is a family of instruction set for architectures based on the Intel CPUs.