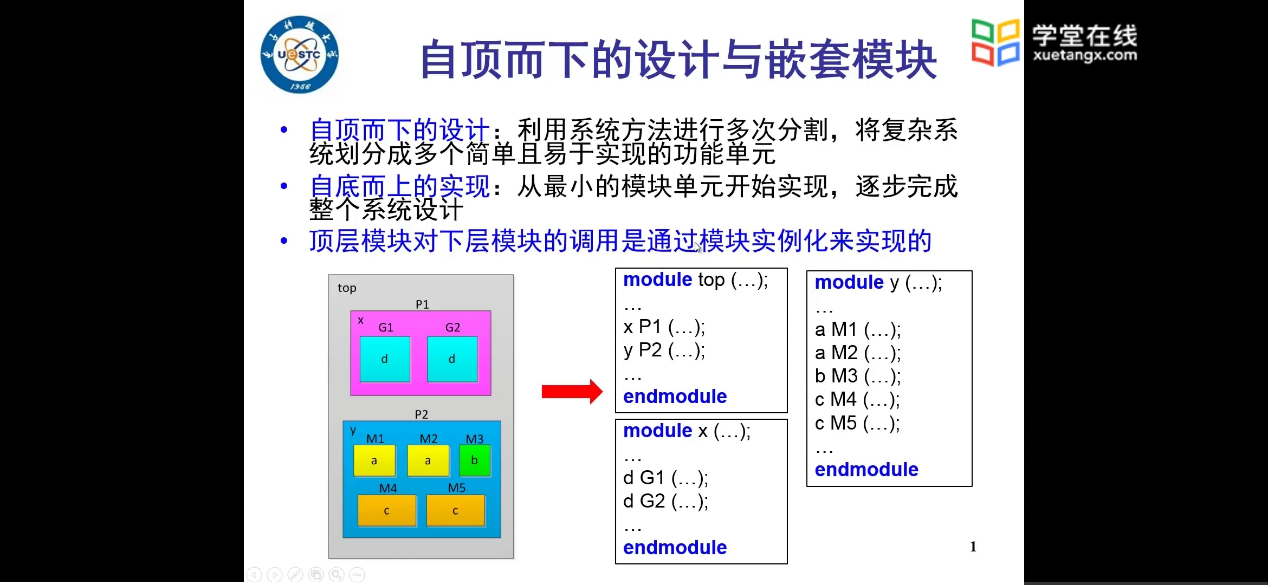
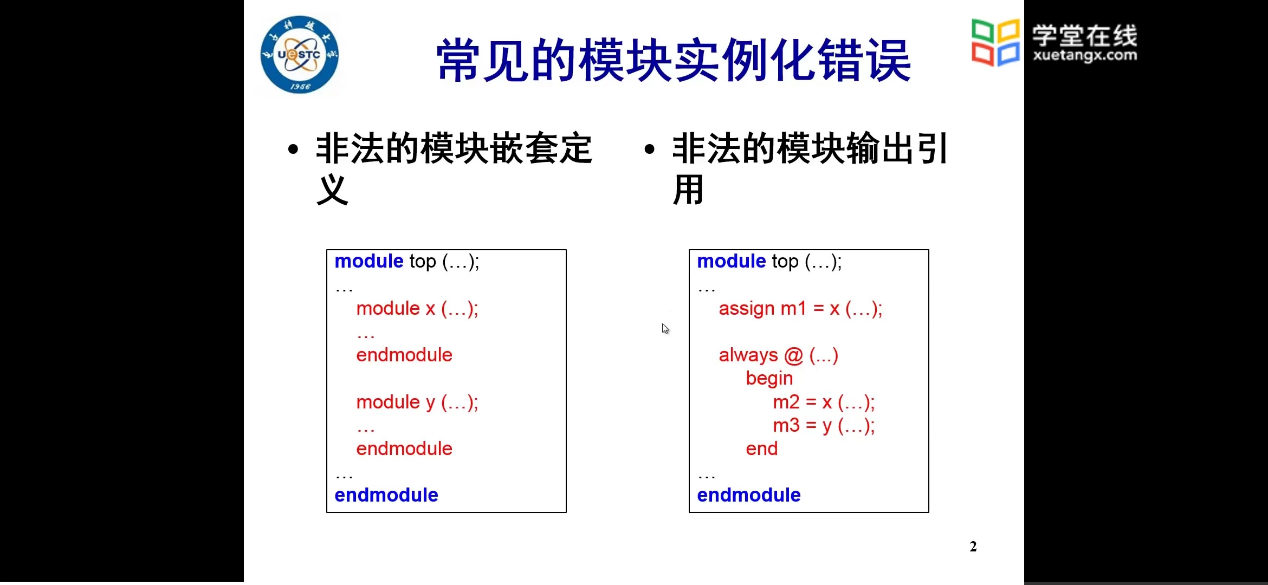
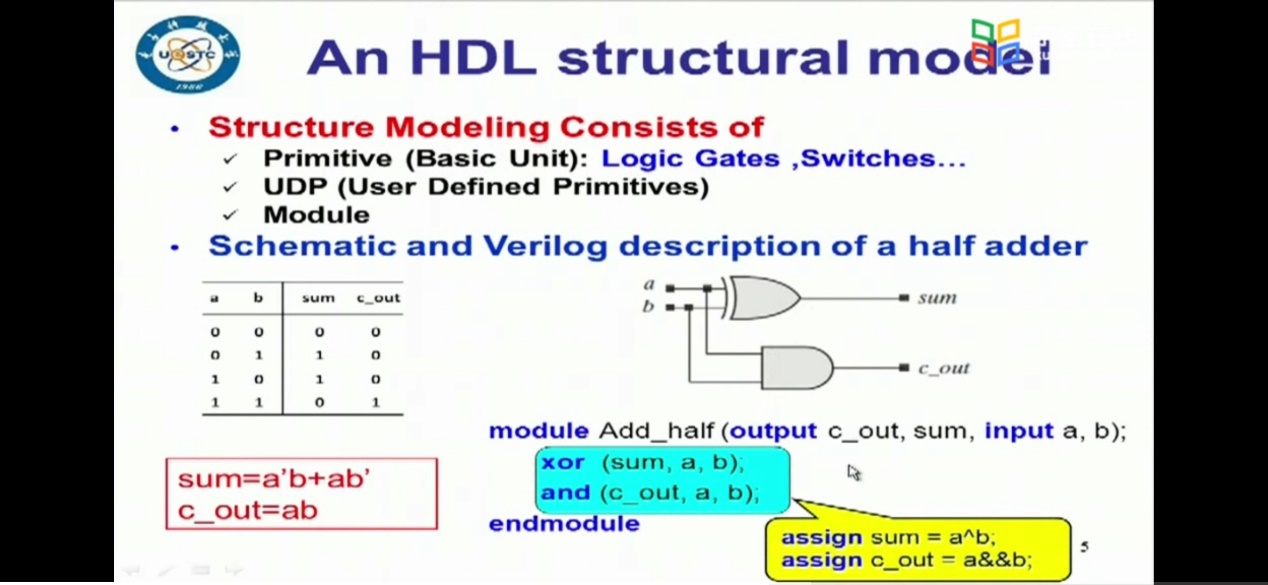


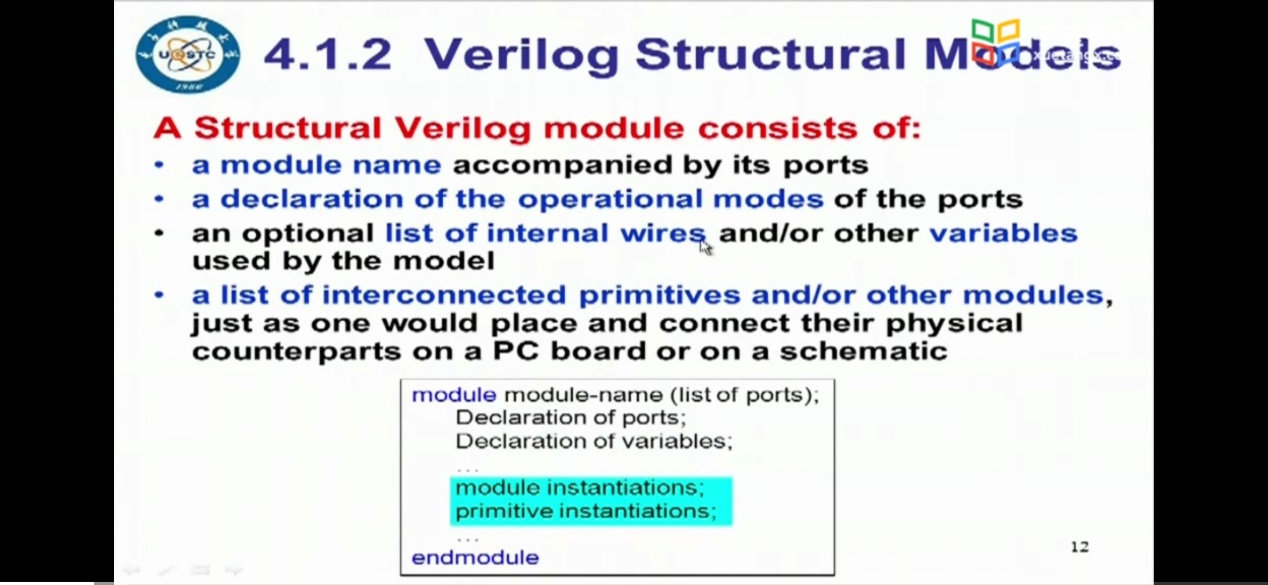
上面的方式为主。

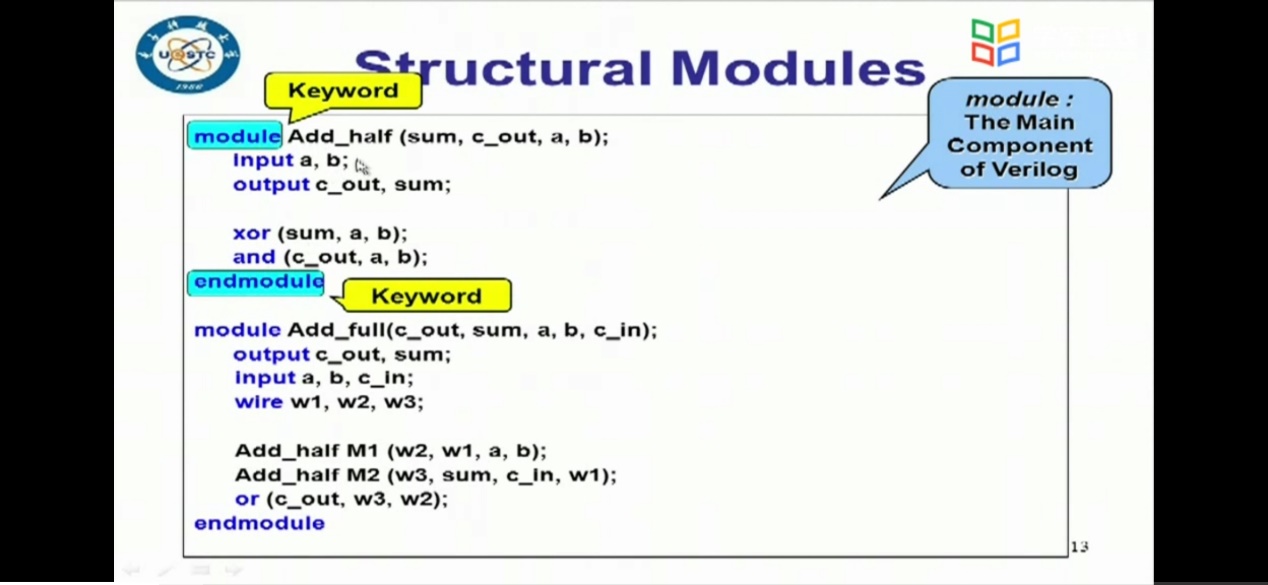


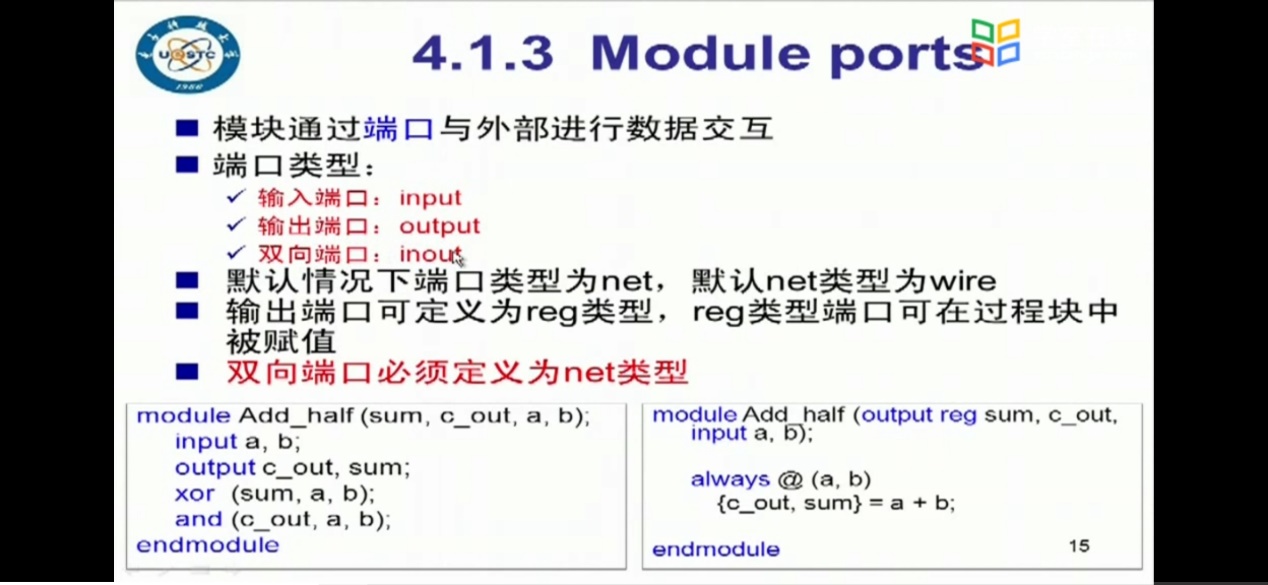
注意模块名和实例名区别

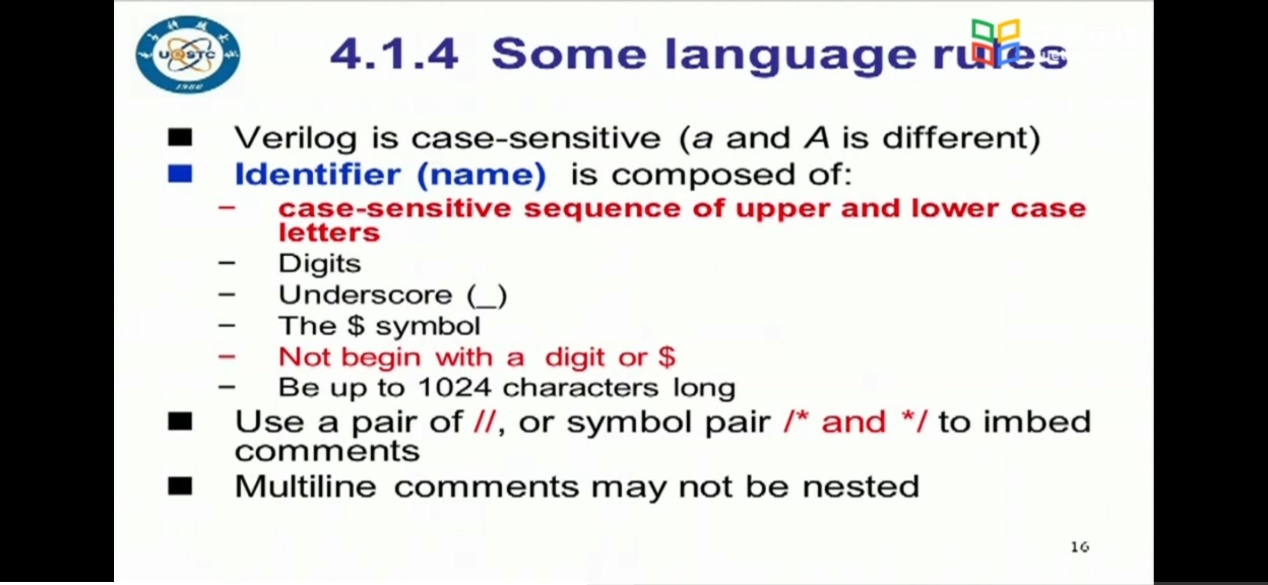




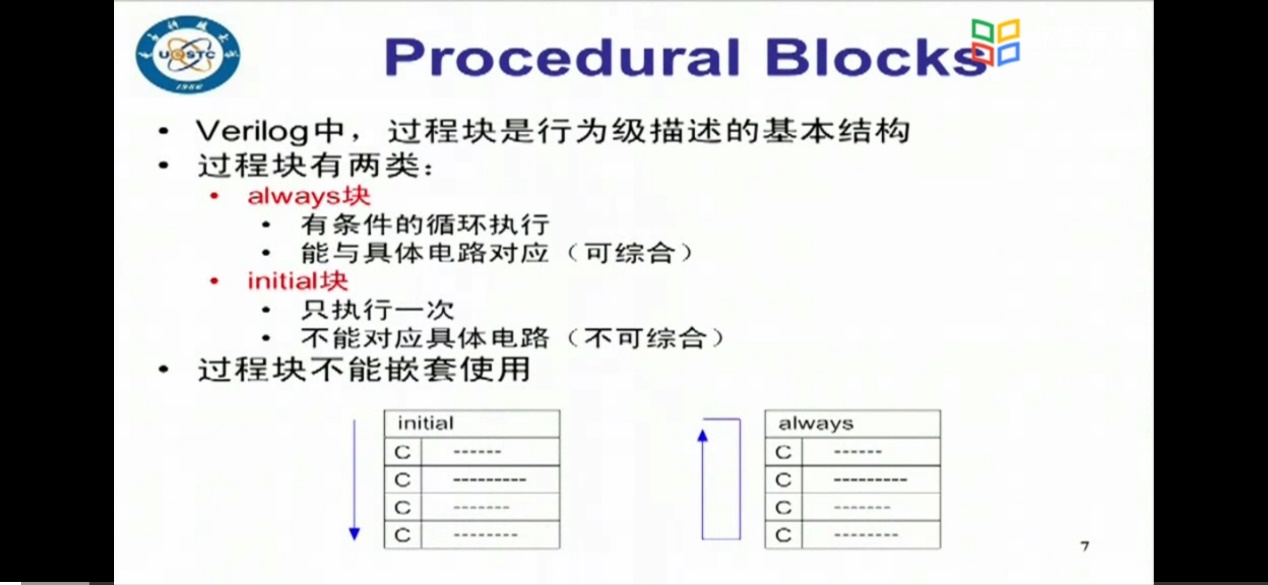


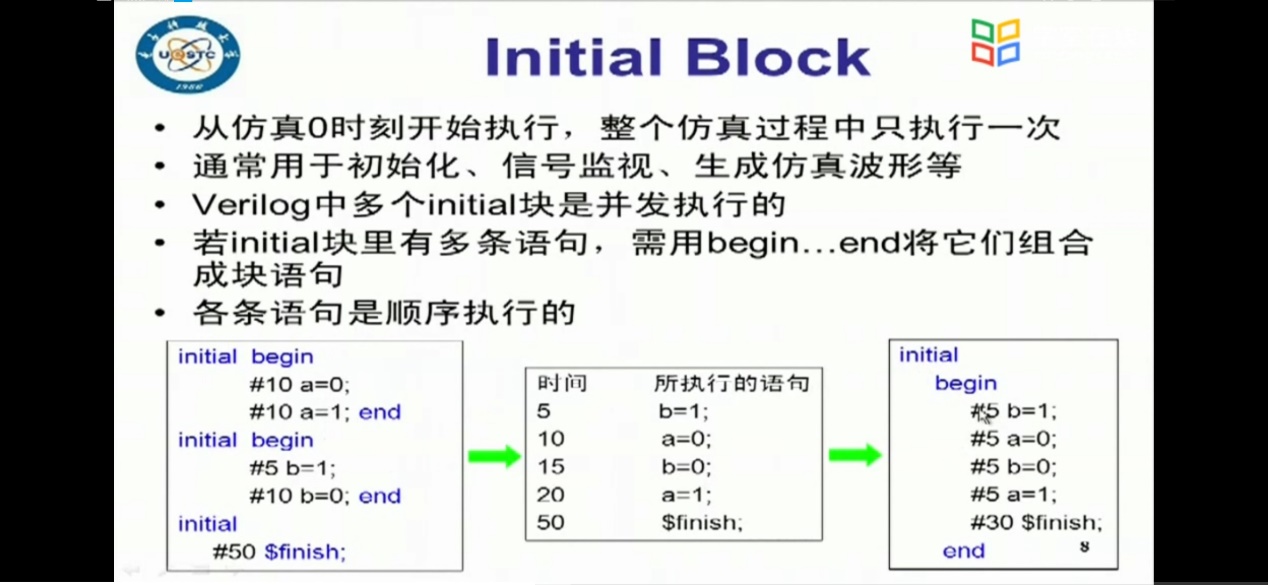


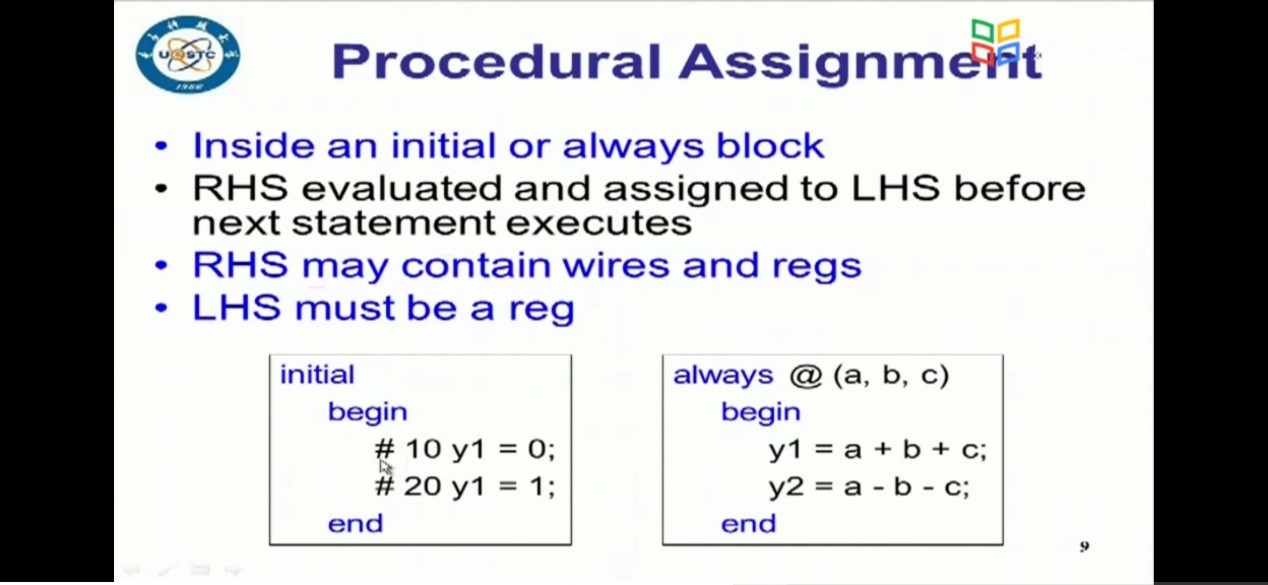










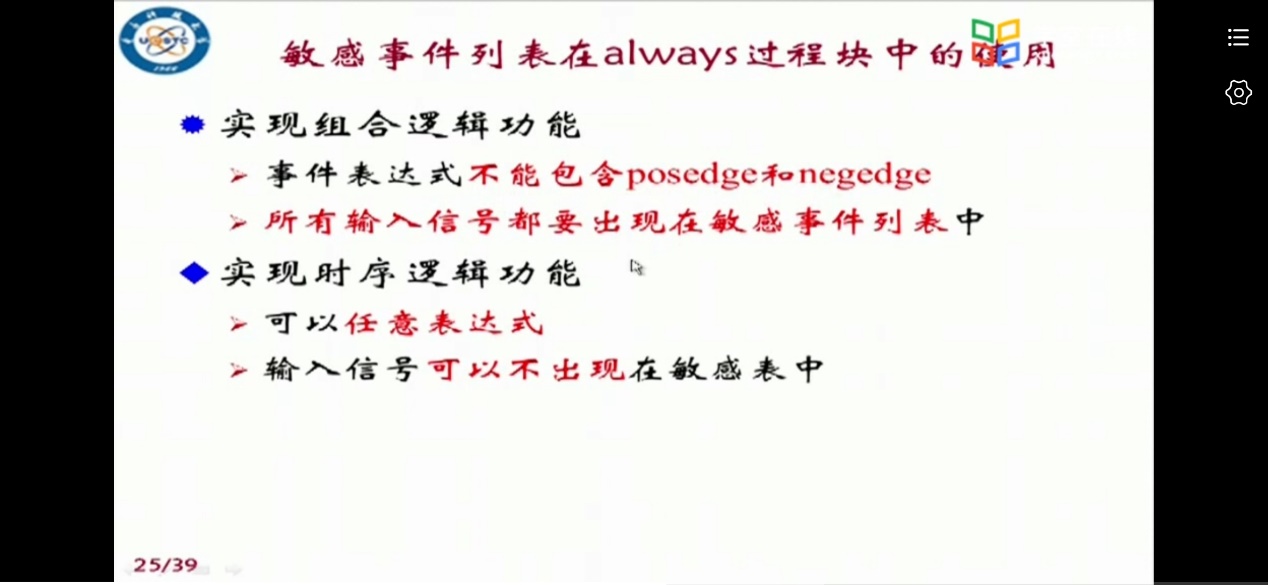




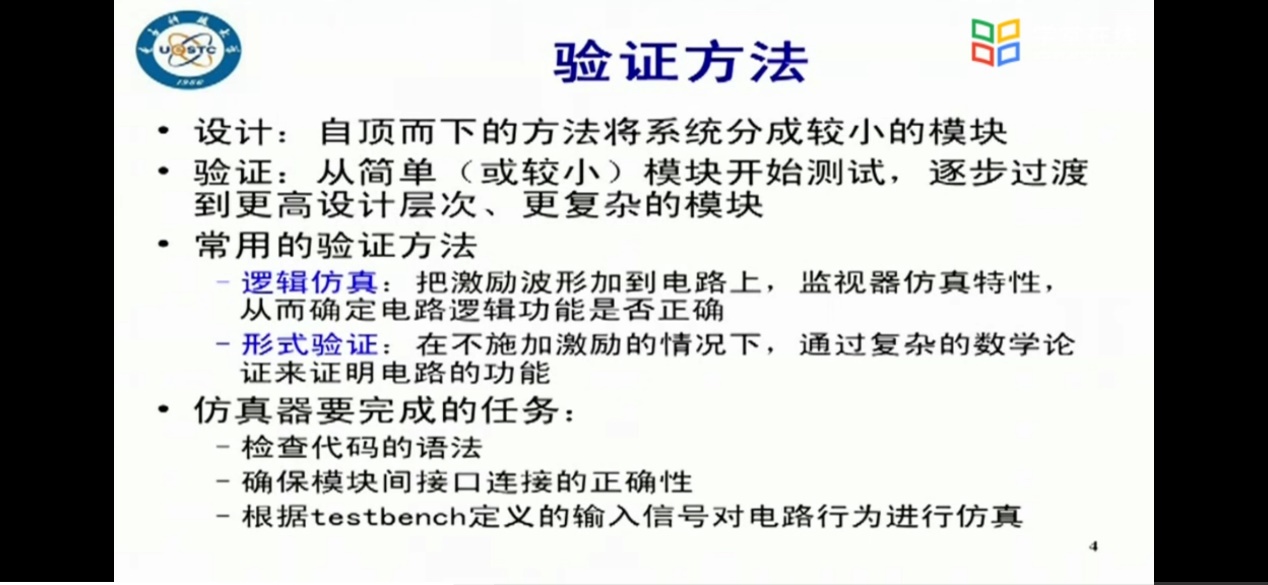


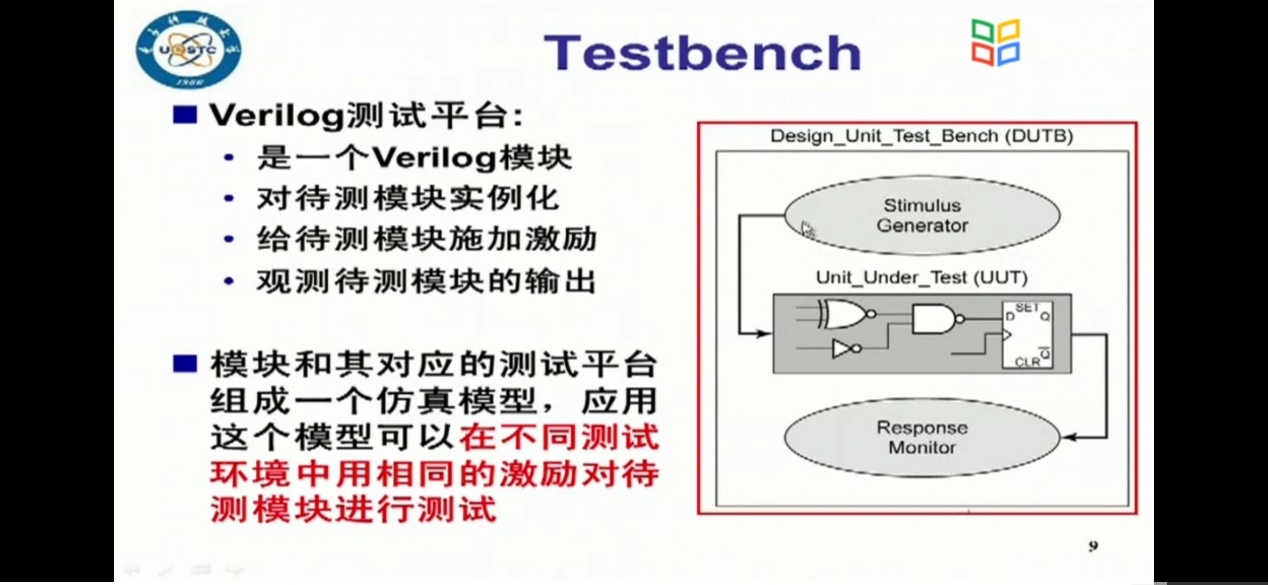


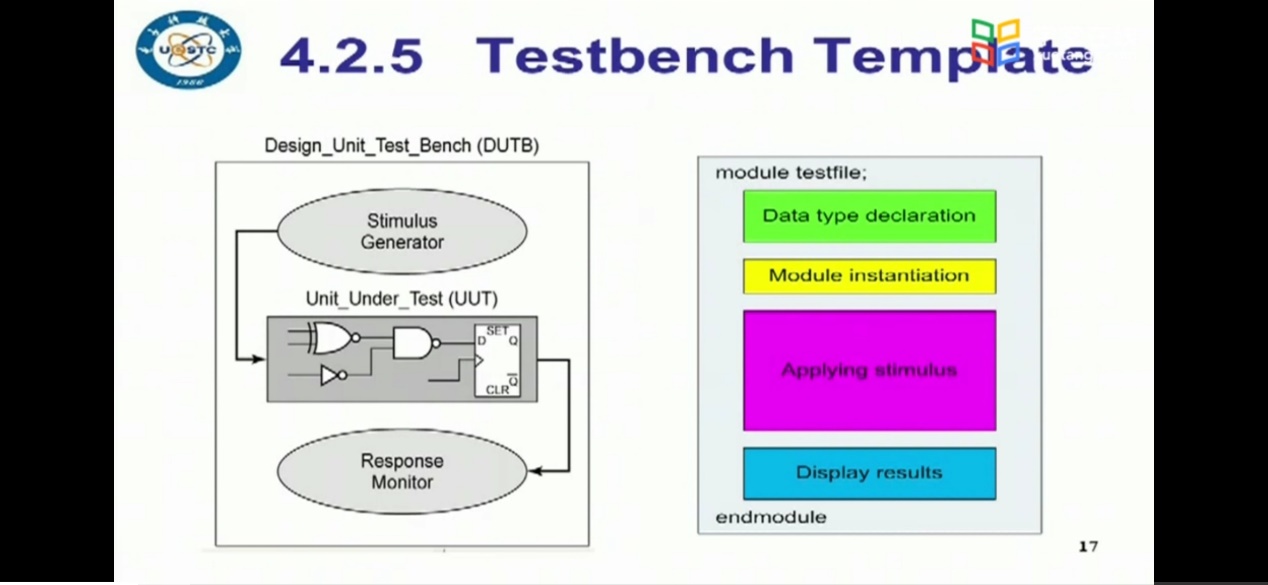




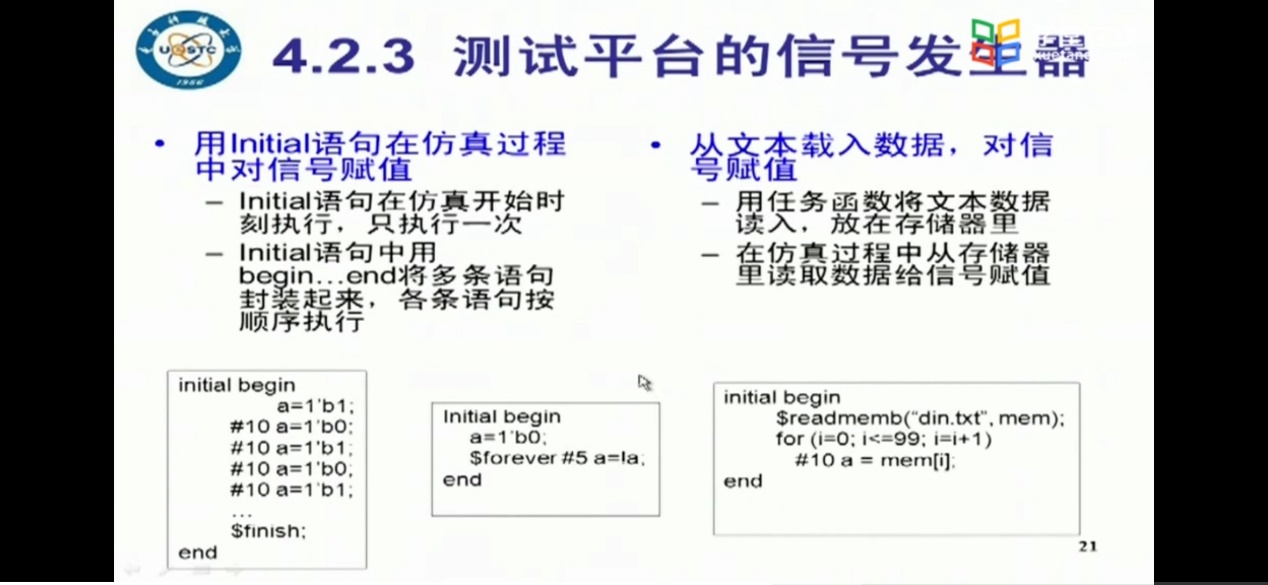
if-else都有的话是组合逻辑，如果只有个if那是时序逻辑。

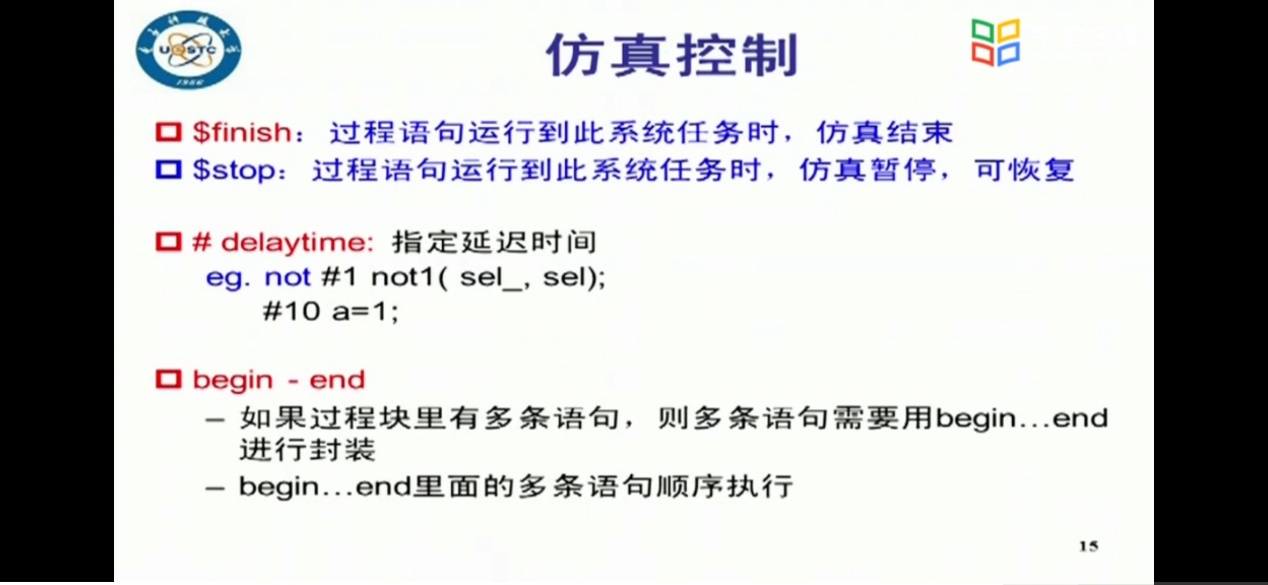


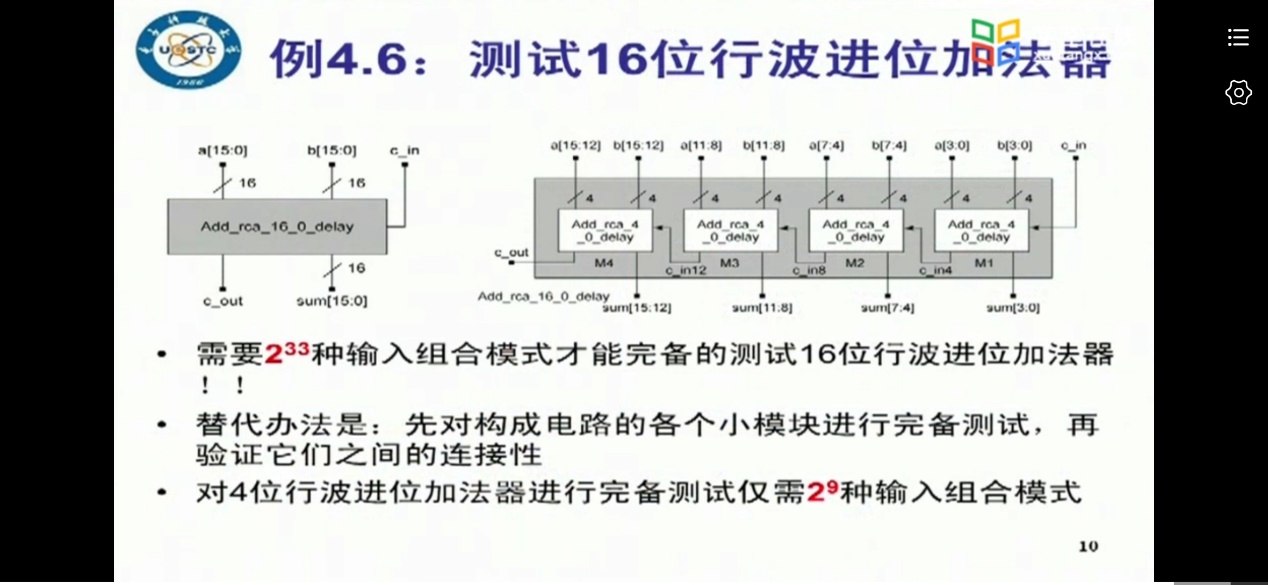


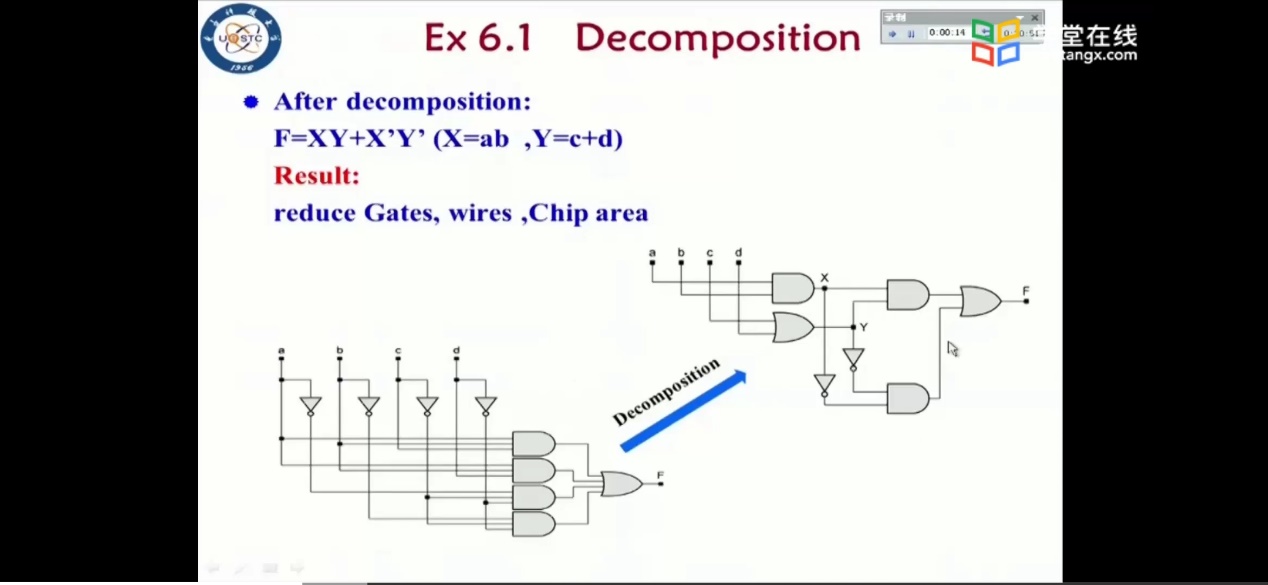


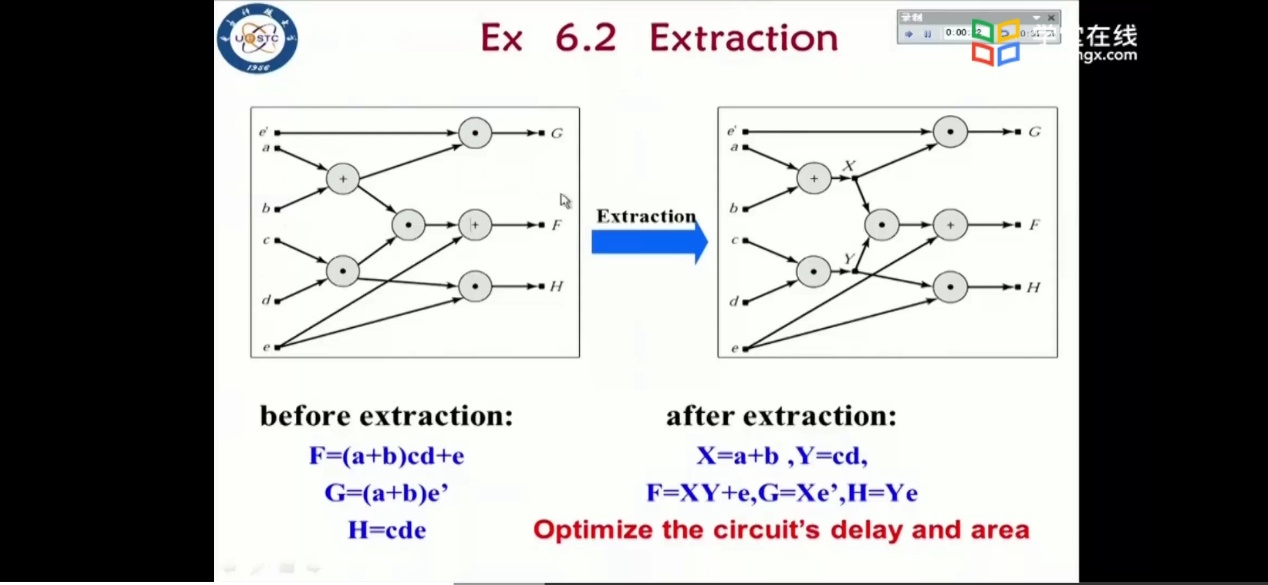


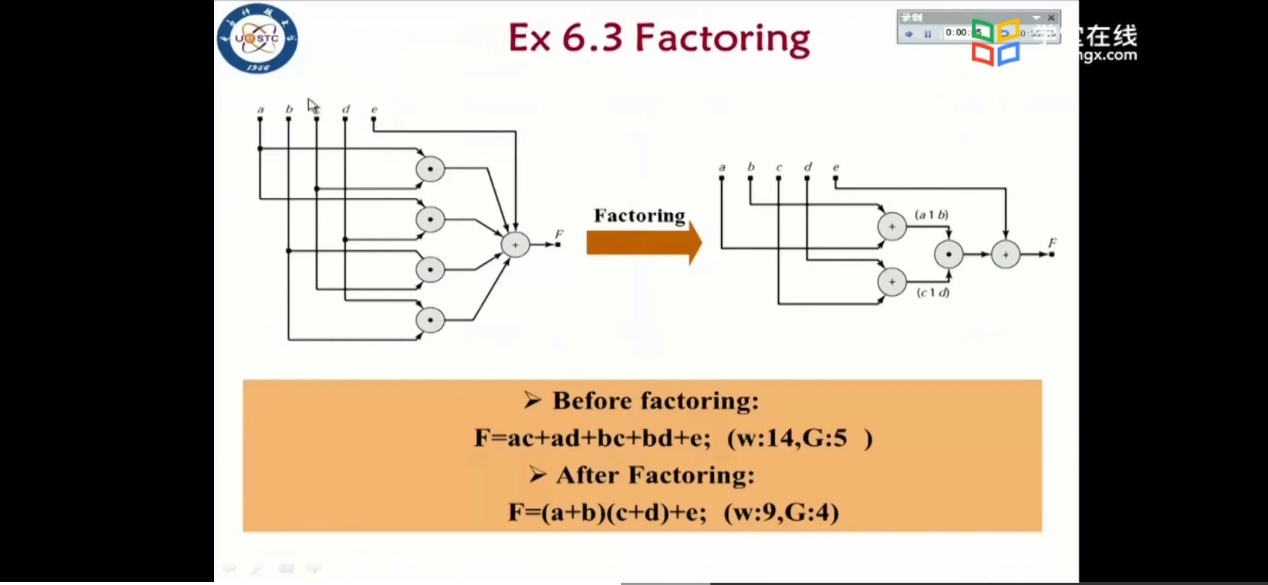


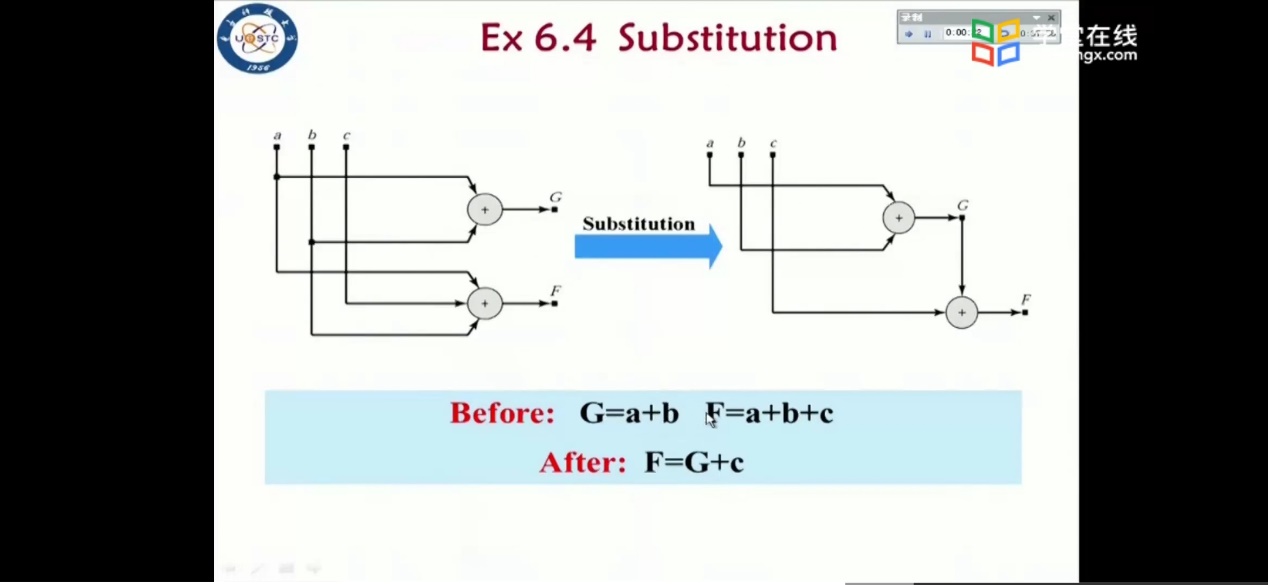


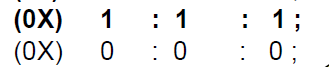
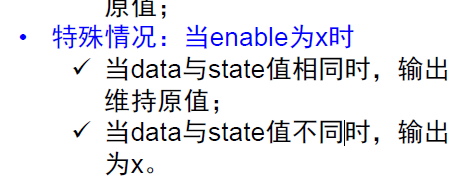
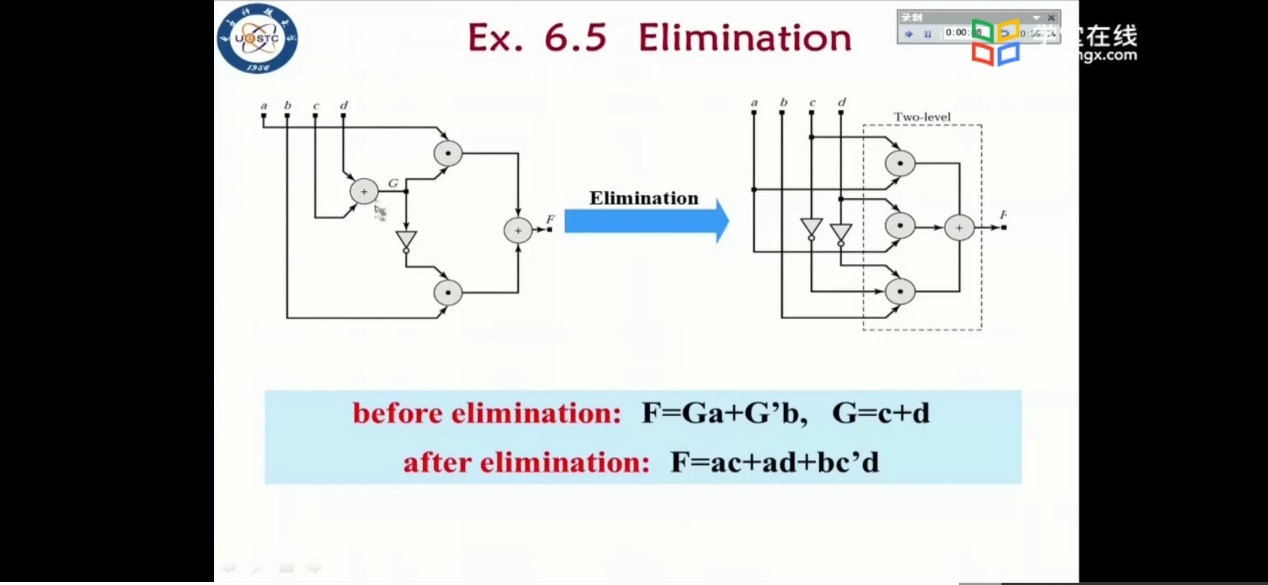




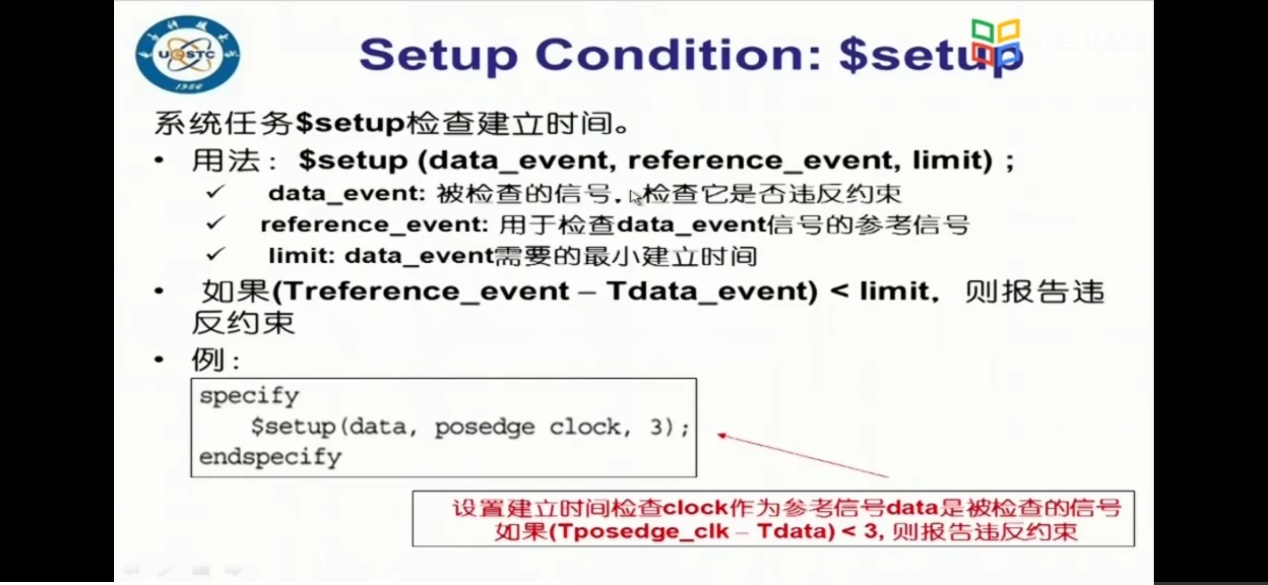


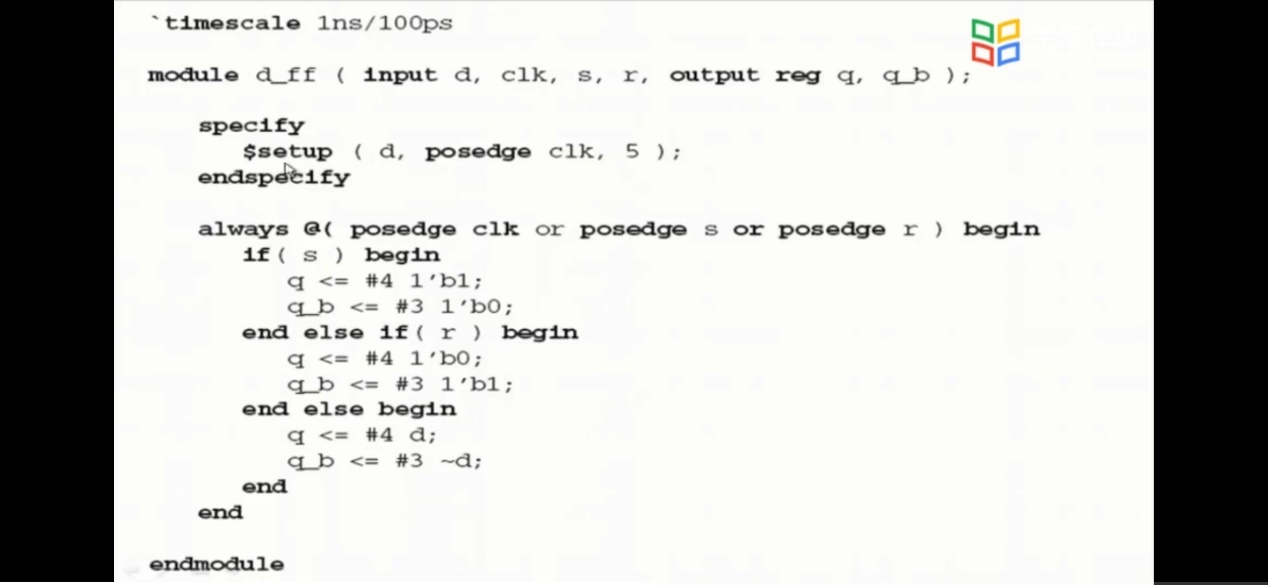


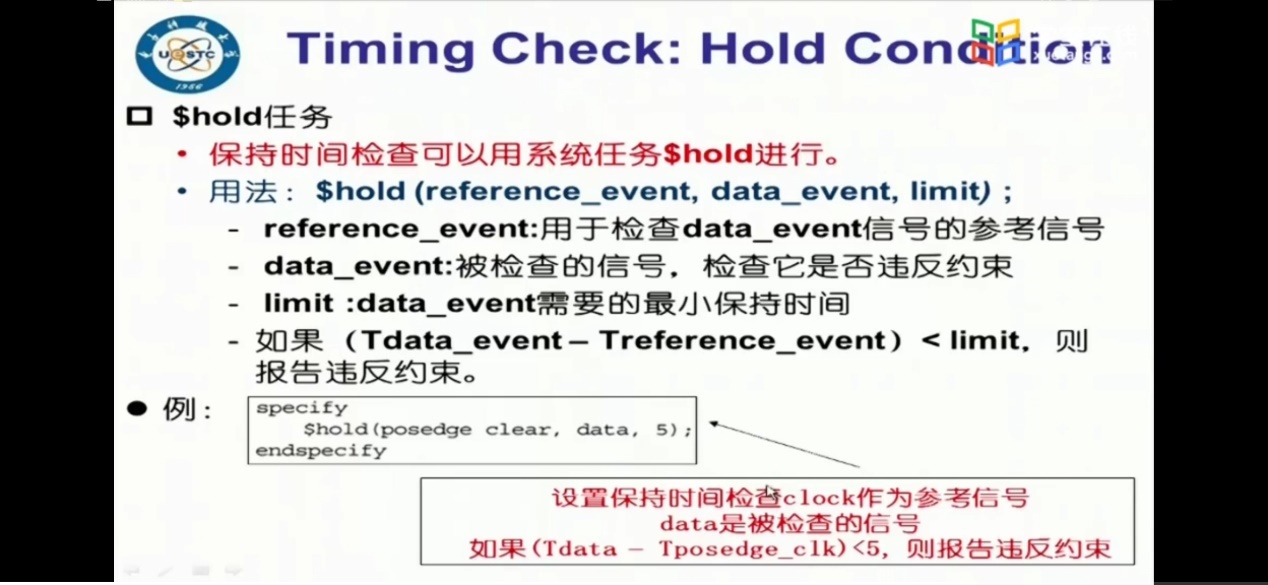


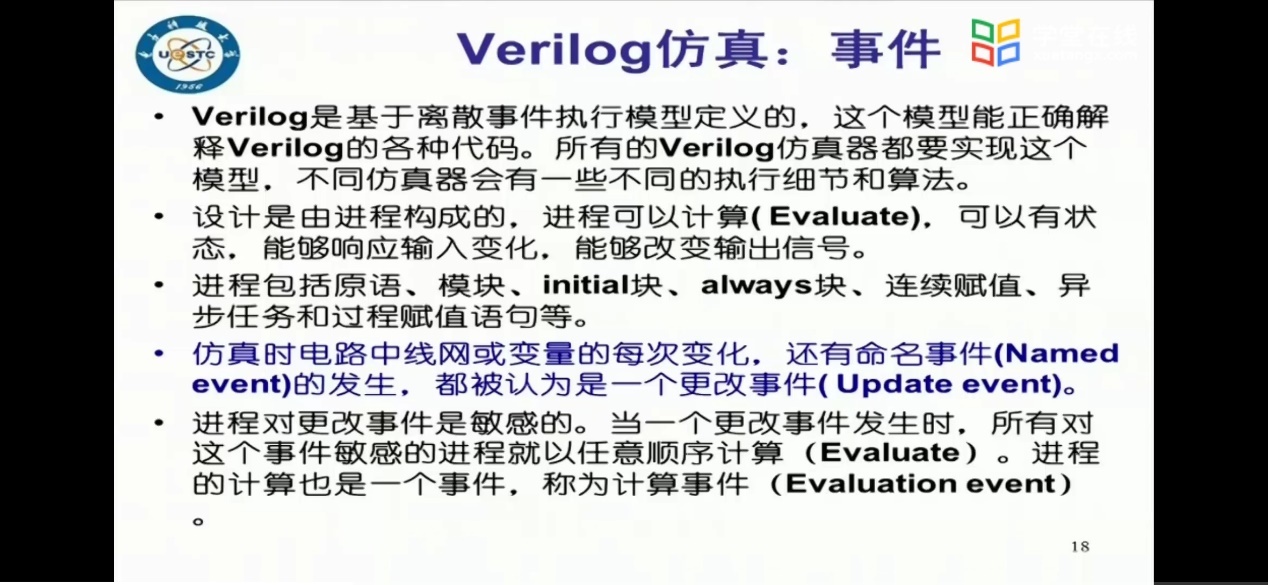


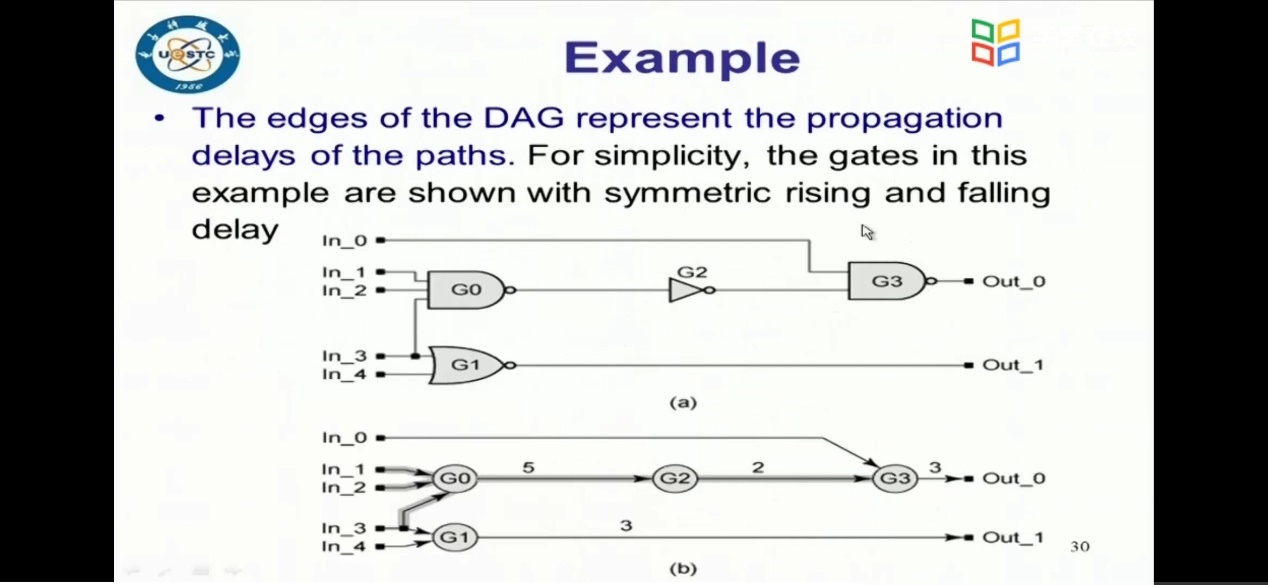
STA：不管功能；DTA：管功能，需要测试向量。

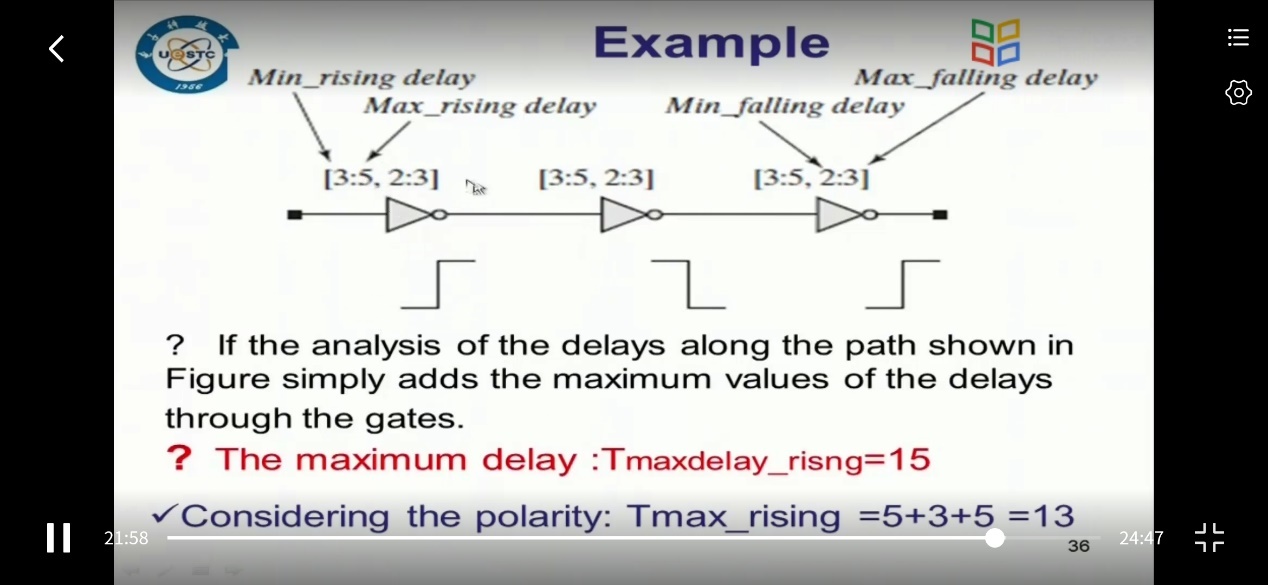












积分器：数字领域等于累加器，因为积分等于面积和。

微分器：通过当前时刻的信号值与上个时刻的信号值的差值。（数字系统）

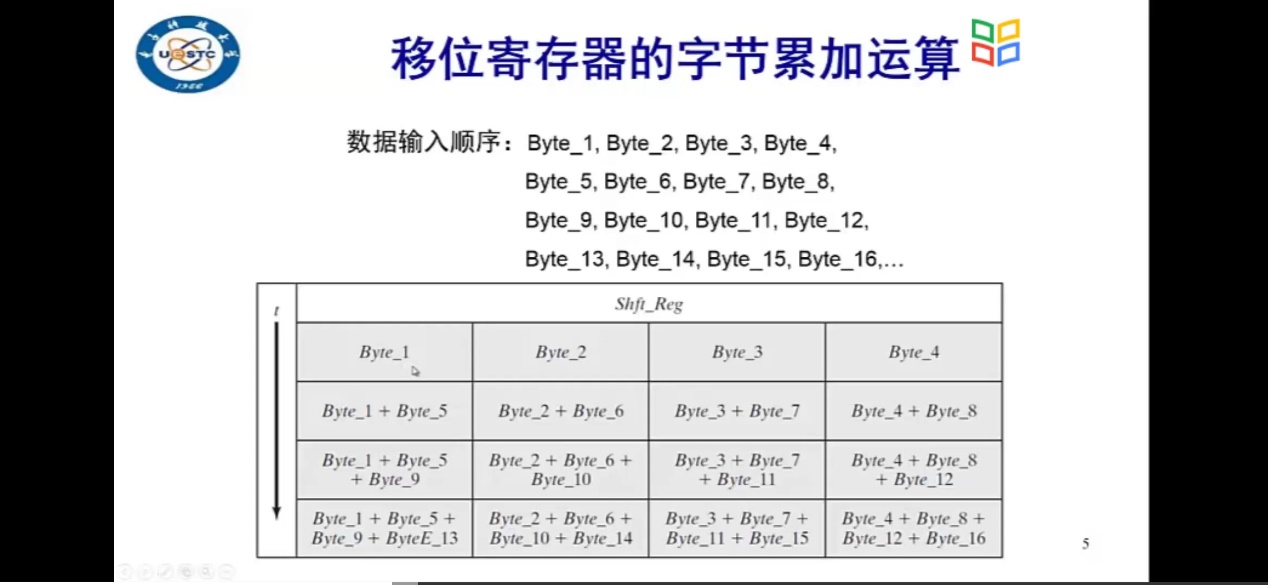
FIR滤波器：

检验FIR滤波器系数，让输入持续为零，只有一个周期为一，看输出就是系数。

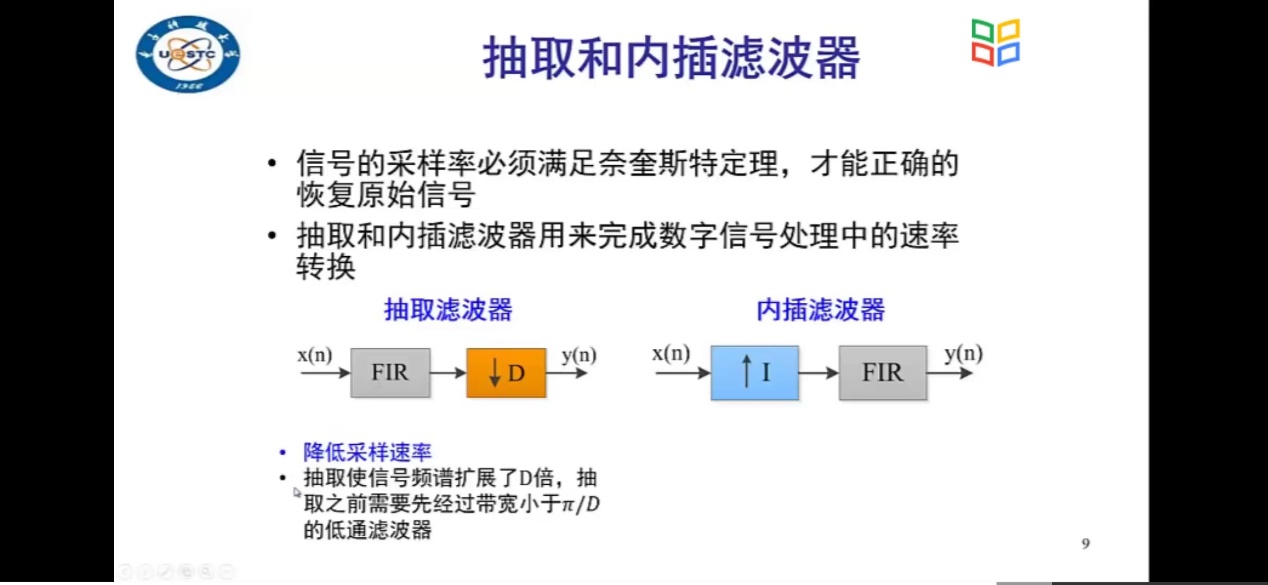
调用IP核生成FIR滤波器的步骤：

1. MATLAB生成满足要求的FIR滤波器的系数；
2. 导入quartus的IP核生成Verilog模型
3. 评估Verilog模型的性能，与MATLAB模型结果比较

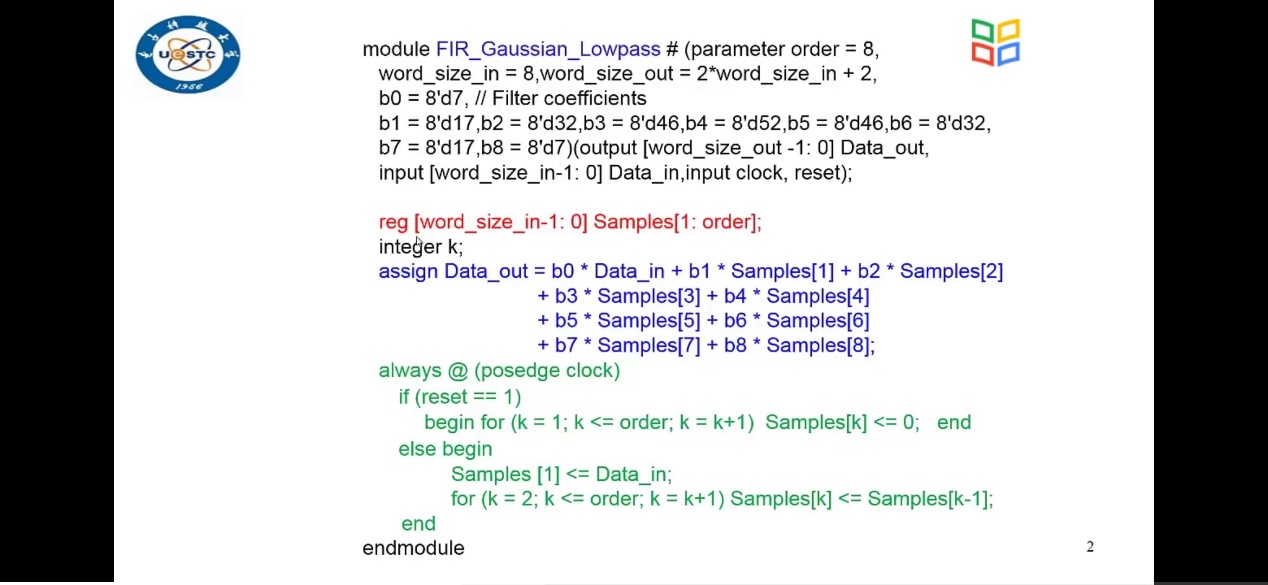
环形缓冲器：用指针代替数据的移动。

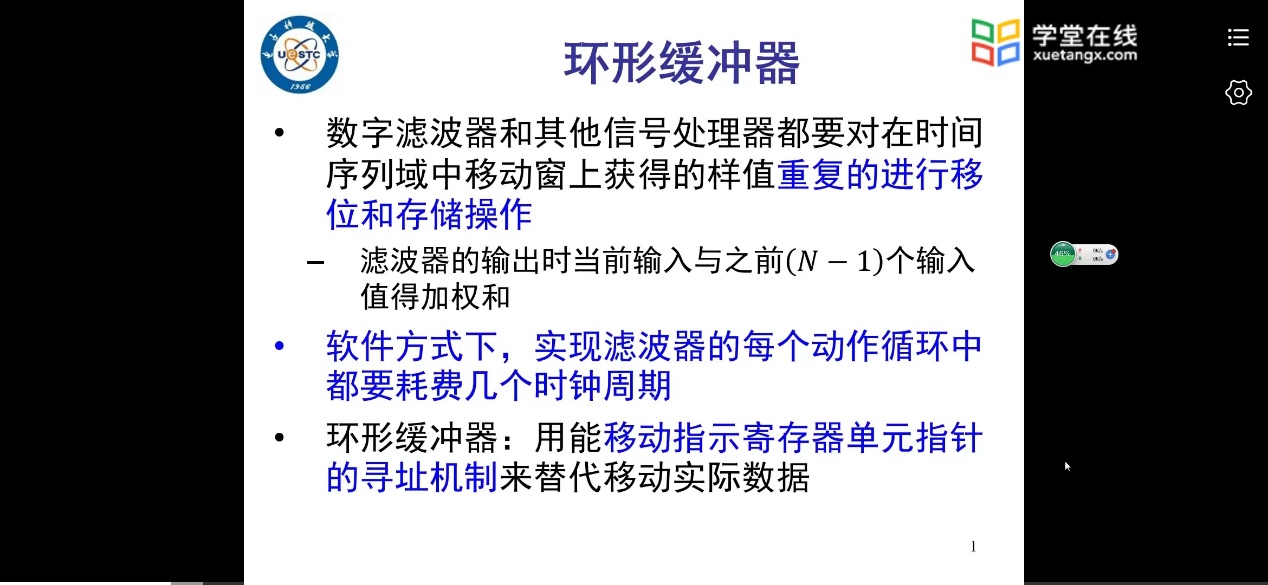


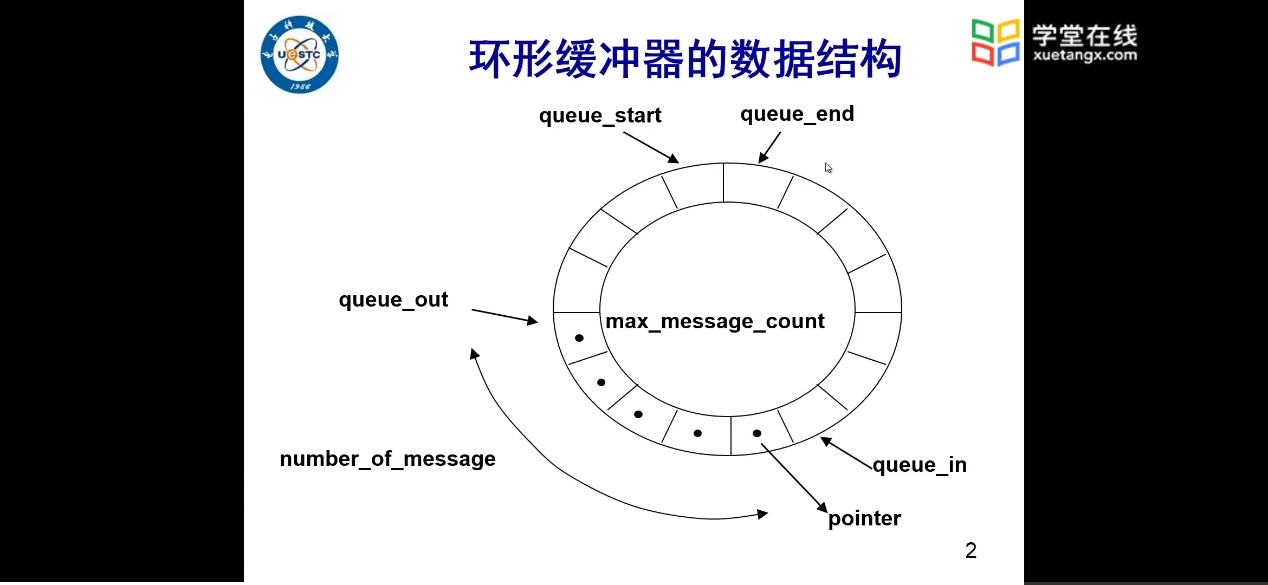


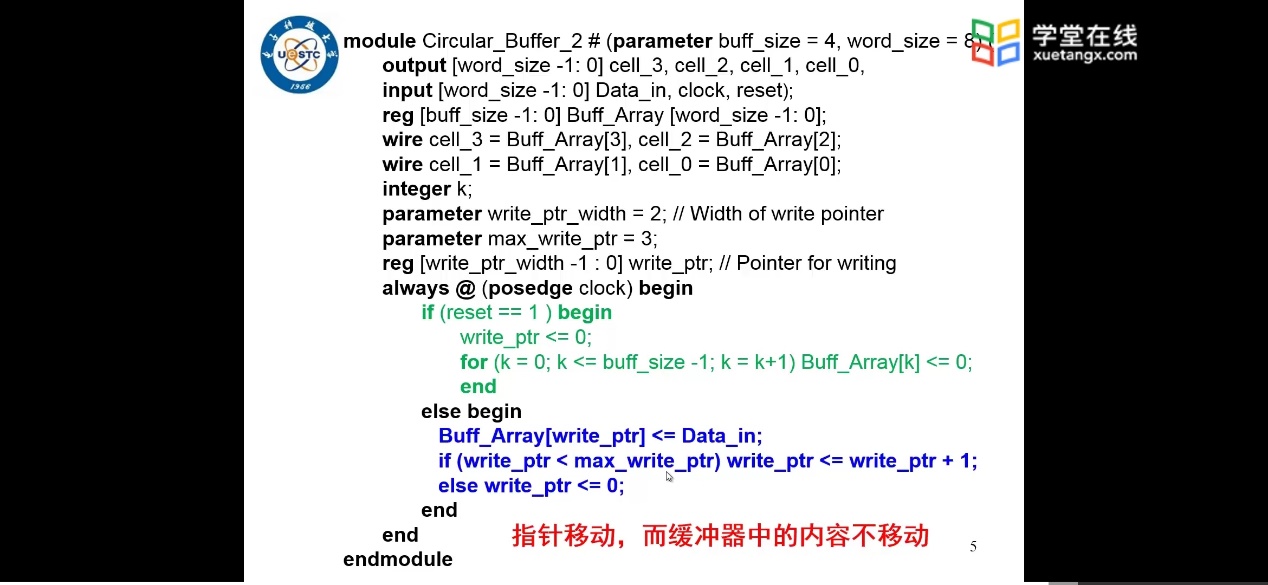
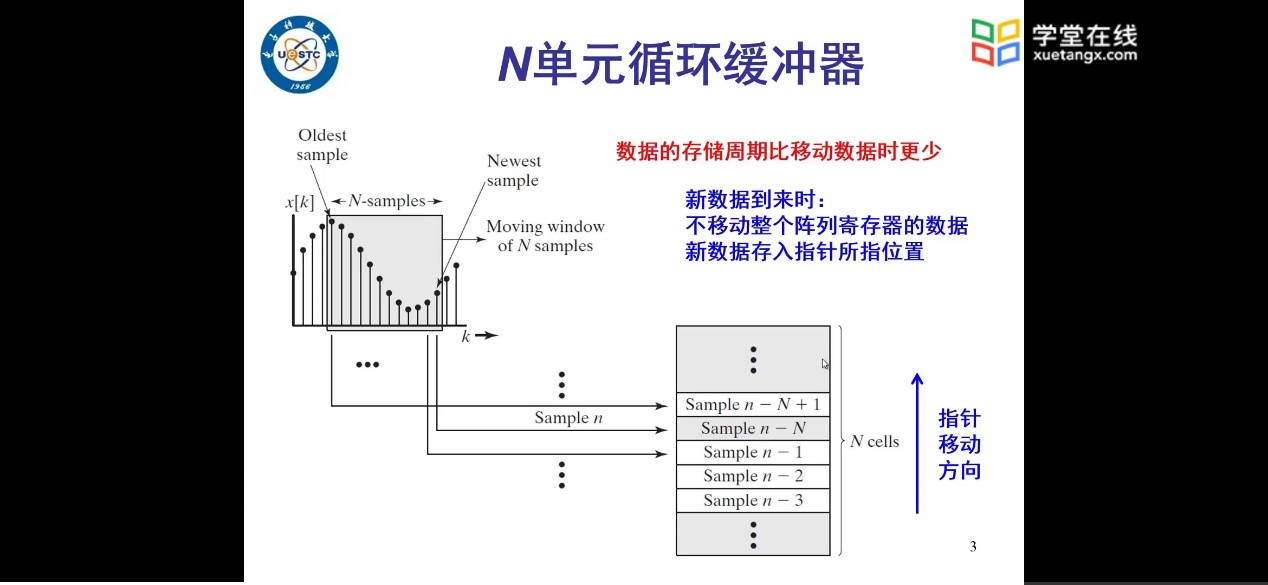


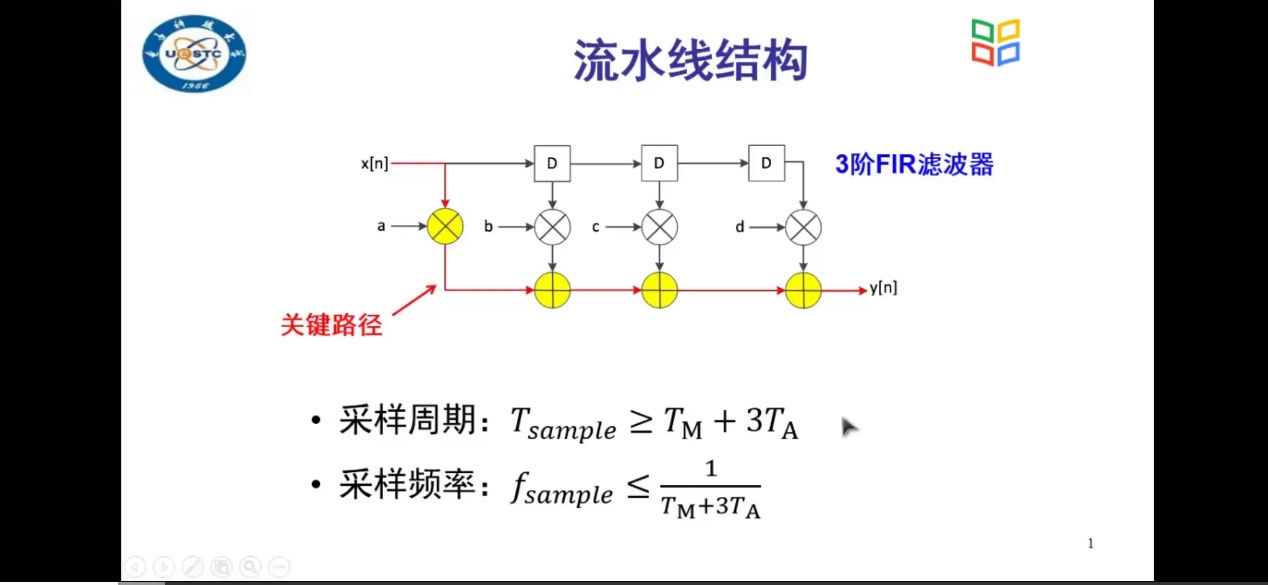


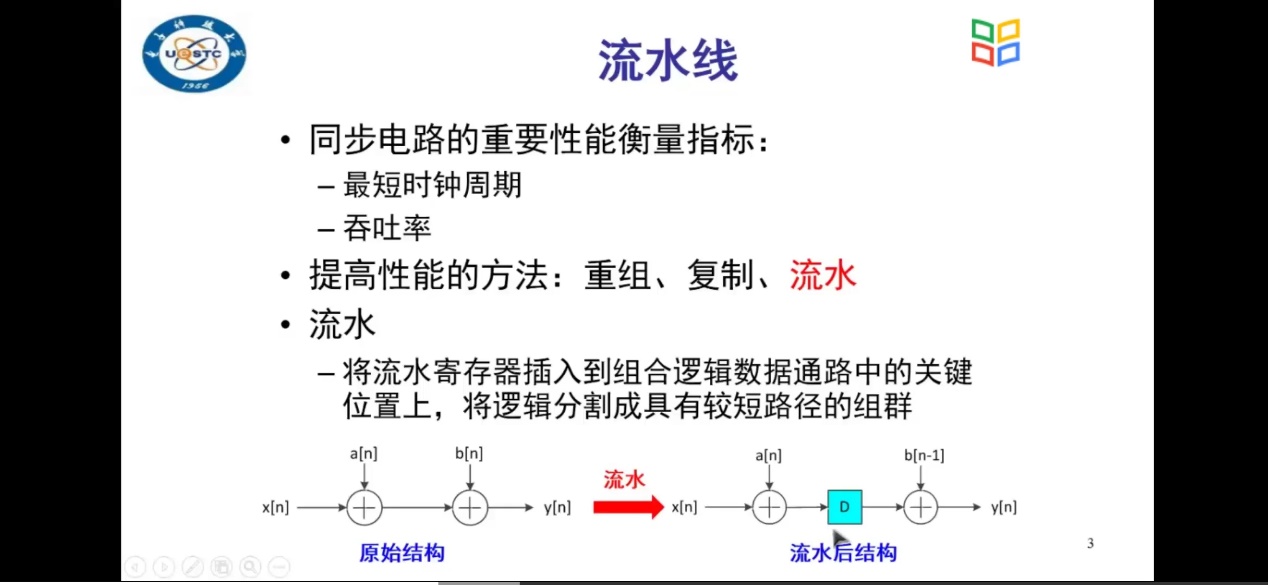




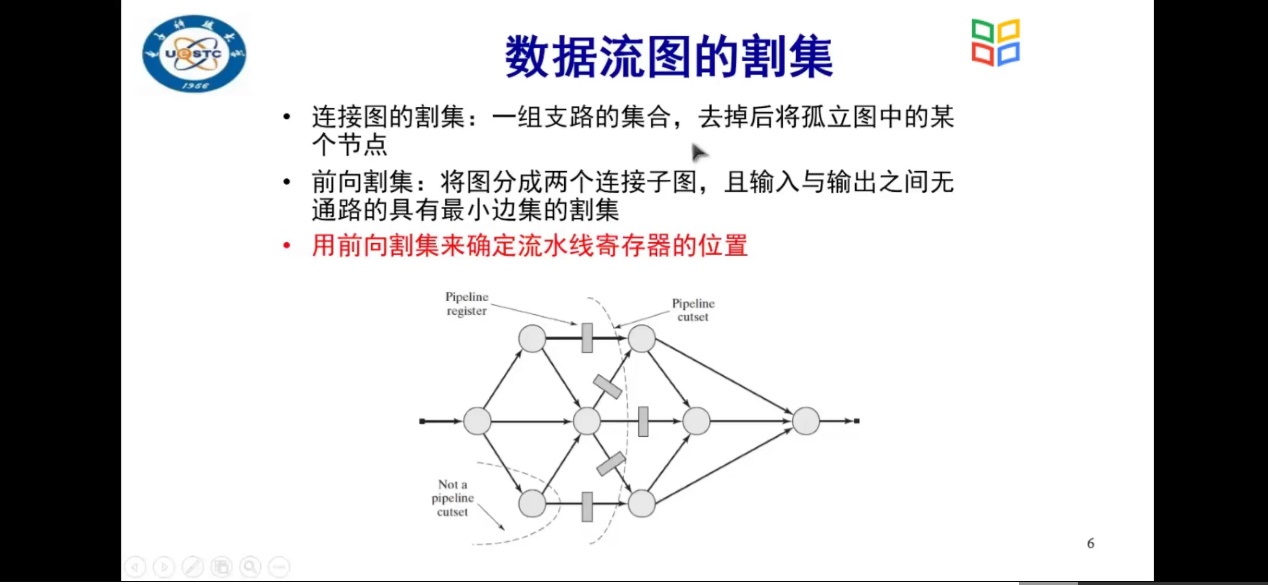












输入输出之间最小边集：少割一条边就会使输入和输出连起来。

MAC：乘（✖）累加（∑）操作。

