

AN14244

i.MX 8ULP Processor Estimated Power-on Hours

Rev. 1 — 8 March 2024

Application note

Document information

Information	Content
Keywords	AN14244, i.MX 8ULP, power-on hours, PoH, effective junction temperature
Abstract	This document describes the estimated power-on hours (PoH) for the i.MX 8ULP applications processor (<i>device</i>) based on the criteria used in the qualification process.



1 Introduction

This document describes the estimated power-on hours (PoH) for the i.MX 8ULP applications processor (device) based on the criteria used in the qualification process. The device PoH described here are estimates and do not represent a guaranteed lifetime for a device.

This document is intended to provide guidance on how to interpret different device qualification levels in terms of the following factors:

- The target operating voltage
- The maximum supported junction temperature (T_j)

The document also describes how these factors relate to the PoH of the device.

The data presented in this document is provided for your convenience. It does not represent all potential failing mechanisms. Also, it may not accurately represent the behavior for all mission profiles or applications. The data demonstrates how temperature can impact the PoH of the device, and it is based on:

- The activation energy using the Arrhenius equation for temperature acceleration
- The voltage acceleration parameter using the power-law for voltage acceleration
- The data collected during high-temperature operating life (HTOL)

2 Device qualification levels and available PoH

The i.MX 8ULP processor supports the following qualification levels:

- Industrial qualification
- Commercial qualification

Each qualification level defines the power-on hours (PoH) available to the device under a given set of conditions, such as:

- Target core voltage (VDD_SOC) for the application
- Junction temperature of the device (T_j)

Note: While the device (SoC) can operate at the maximum T_j listed in its data sheet, operating the device at this temperature for an extended period reduces its operating PoH.

Note: Always ensure that the device is thermally managed and the maximum junction temperature is not exceeded.

Note: For the device voltage and temperature limits, refer to the respective device data sheet available on nxp.com.

The junction temperature (T_j) of the device is the temperature of the transistors in the device. It is a different measurement than the case and the ambient temperature. Most applications do not have a constant T_j during operation.

The charts in this document show the relationship between the T_j and PoH. The percentage of on-time at different temperatures is part of what defines each mission profile.

If the junction temperature is not constant during an application, you can calculate the effective junction temperature (T_{j-eff}) using weighting with the Arrhenius factor. For more details, see [Section 3](#).

Note: The data provided in this document are estimates for the PoH, based on the qualification test data and experience with this device. These estimates must not be viewed as a limit on an individual device lifetime. Also, they must not be construed as a guarantee by NXP to the actual lifetime of the device. Sales and warranty terms and conditions still apply.

2.1 Industrial qualification

Figure 1 provides the PoH for the use conditions of the industrial device. The PoH value assumes that the device is powered on and is active for 100% of the time (100% duty cycle). The PoH can be read directly from the curves shown in Figure 1 to determine the impact of junction temperature at the listed conditions.

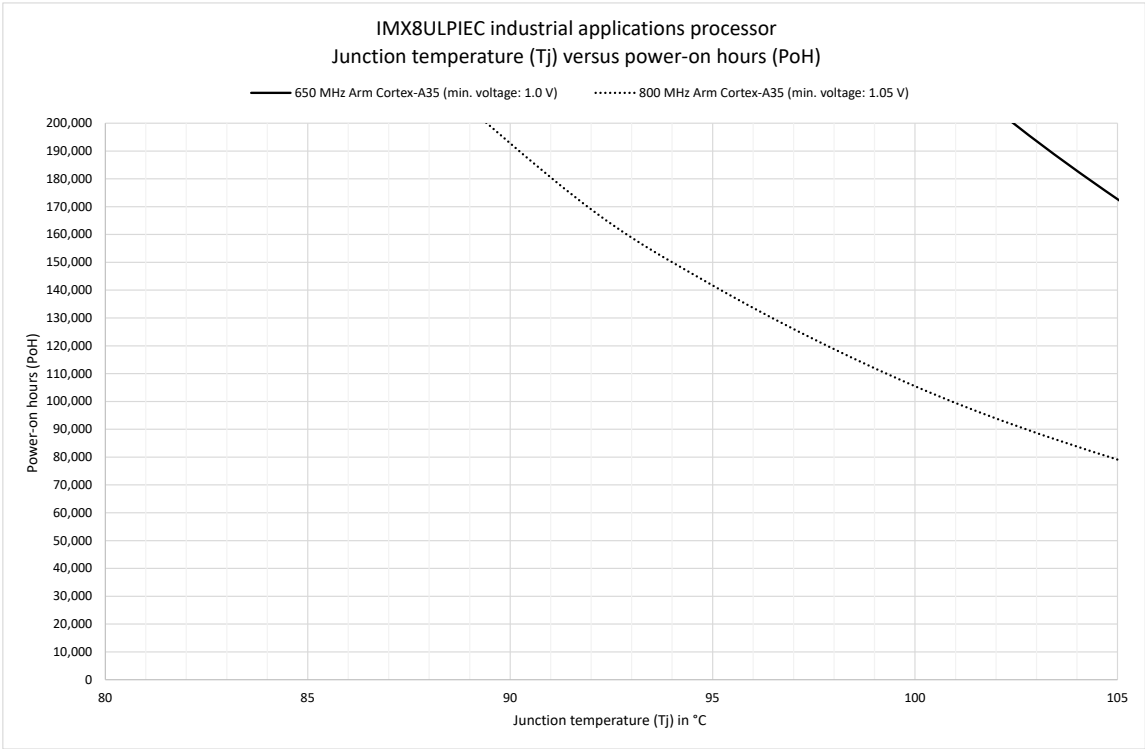


Figure 1. i.MX 8ULP industrial PoH estimates

2.2 Commercial qualification

Figure 2 provides the number of PoH for the use conditions of the commercial device. The PoH can be read directly from the curves shown in Figure 2 to determine the impact of junction temperature at the listed conditions.

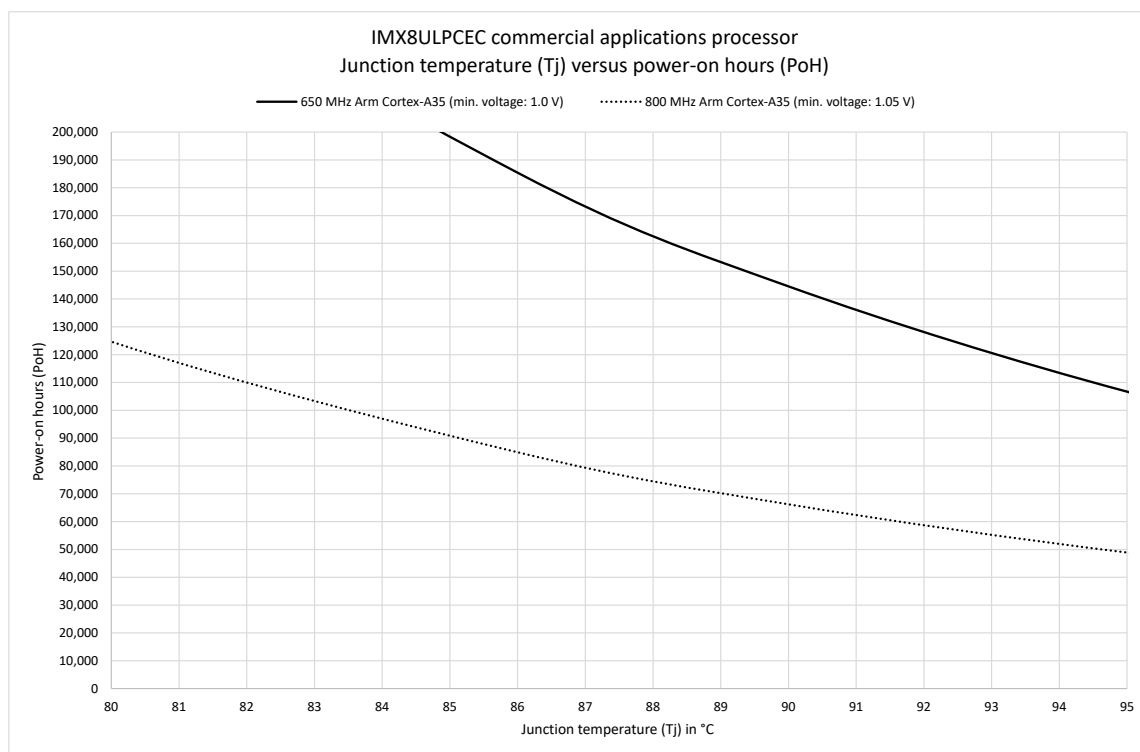


Figure 2. i.MX 8ULP commercial PoH estimates

3 Effective junction temperature

The junction temperature (T_j) of the device is the temperature of the transistors in the device. It is a different measurement than the case and the ambient temperature. Most applications do not have a constant T_j during operation.

The charts in this document show the relationship between the T_j and PoH. The percentage of on-time at different temperatures is part of what defines each mission profile. The effective junction temperature (T_{j-eff}) is the single T_j that represents the mission profile. It can be used to extrapolate the PoH in the charts shown in [Figure 1](#) and [Figure 2](#):

- T_{j-eff} depends only on the temperatures during the on-time duty cycles of a mission profile. Temperatures when the device is powered off do not affect T_{j-eff} .
- T_{j-eff} is not a simple average of temperatures, as the on-time at higher temperatures consumes more operating life than on-time at lower temperatures.
- If the junction temperature is not constant during an application, you can calculate T_{j-eff} using weighting with the Arrhenius factor.

3.1 Calculating T_{j-eff}

Assuming that the temperature dependence follows Arrhenius behavior, you can calculate the T_{j-eff} using the following method:

1. Determine the percentage of time (t_n) that the application is powered on at a small set of discrete temperatures (T_n).
2. Calculate the average failure rate using the Arrhenius method:

$$FR_{AV} = \left[t_1 \cdot e^{\left(\frac{-E_A}{kT_1}\right)} + t_2 \cdot e^{\left(\frac{-E_A}{kT_2}\right)} + \dots + t_n \cdot e^{\left(\frac{-E_A}{kT_n}\right)} \right] \quad (1)$$

3. Then, calculate the effective temperature:

$$T_{j-eff} = \frac{-E_A}{k \ln(FR_{AV})} \quad (2)$$

Here are some notes on the variables and constants used in the formulas above:

- E_A : Activation energy. A typical value for E_A is 0.7 eV, which is used to generate the charts in this document.
- k : Boltzmann constant. Its value is 8.62×10^{-5} .
- T_n : Temperature in Kelvin. The resulting T_{j-eff} must also be in Kelvin.
- t_n : The percentage of time at a given temperature. t_n must be noted in decimal, for example, 50% becomes 0.50.

The following is a simple example explaining how to calculate T_{j-eff} of an application that has two constant temperature values for a given period.

Assume that the T_j of the device is at:

- 100 °C for 50% of the time
- 50 °C for the other 50% of the time the device is powered on

In this case, the average temperature is 75 °C.

Now, using [Equation 1](#), the average failure rate can be calculated as follows:

$$FR_{AV} = \left[0.5 \cdot e^{\left(\frac{-0.7}{k373.15}\right)} + 0.5 \cdot e^{\left(\frac{-0.7}{k323.15}\right)} \right] = 1.83 \times 10^{-10} \quad (3)$$

Then, using [Equation 2](#), the effective temperature can be calculated as follows:

$$T_{j-eff} = \frac{-0.7}{k \ln(FR_{AV})} = 362.18 \text{ K} = 89.03^\circ\text{C} \quad (4)$$

You can notice that T_{j-eff} of 89 °C is higher than the average temperature of 75 °C. It indicates that higher temperatures have a bigger impact on the life of the device.

4 Conclusion

Selecting the optimal operating performance point and thermal envelope is crucial to meet the target application power-on hours (PoH). Trade-offs between the target operating voltage/frequency of the device and the operating junction temperature (T_j) of the device can greatly improve the PoH of the device.

Lowering the operating junction temperature during an application (without impacting device performance) is the most effective way to increase the PoH of a device. It can be achieved by increasing the thermal dissipation capacity in the application. For optimal thermal management, refer to the device hardware developer's guide.

In cases where the thermal properties cannot be altered, a lower operating voltage can be used to increase the PoH of the device. However, lowering the voltage reduces device performance. To match the voltage specified in the data sheet, you may need to reduce the operating frequency.

You can use the data and examples provided in this application note as a reference during your application development. For additional recommendations on power optimization, refer to power optimization related application notes available on [nxp.com](https://www.nxp.com).

5 Revision history

[Table 1](#) summarizes the revisions to this document.

Table 1. Revision history

Document ID	Release date	Description
AN14244 v.1	8 March 2024	Initial public release

Legal information

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <https://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

AMBA, Arm, Arm7, Arm7TDMI, Arm9, Arm11, Artisan, big.LITTLE, Cordio, CoreLink, CoreSight, Cortex, DesignStart, DynamIQ, Jazelle, Keil, Mali, Mbed, Mbed Enabled, NEON, POP, RealView, SecurCore, Socrates, Thumb, TrustZone, ULINK, ULINK2, ULINK-ME, ULINK-PLUS, ULINKpro, μ Vision, Versatile — are trademarks and/or registered trademarks of Arm Limited (or its subsidiaries or affiliates) in the US and/or elsewhere. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved.

Contents

1 Introduction 2

2 Device qualification levels and available PoH 2

2.1 Industrial qualification 3

2.2 Commercial qualification 3

3 Effective junction temperature 4

3.1 Calculating Tj-eff 5

4 Conclusion 5

5 Revision history 6

Legal information 7

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.