PL25SL128C Secure EEPROM Datasheet

Features

- Dual Power Supply Operation
  - VCC1 Voltage Range: 2.7V to 3.6V
  - VCC2 Voltage Range : 4.5V to 5.5V
- SPI-compatible serial bus interface
- 64Kb Standard Serial EEPROM Memory
- Clock frequency
  - 133 MHz (MAX) for all protocols in STR
  - 90 MHz (MAX) for all protocols in DTR
- Execute-in-place (XIP)
- PROGRAM/ERASE SUSPEND operations
- Volatile and nonvolatile configuration settings
- Software reset
- Erase capability
  - Bulk erase
  - Sector erase 64KB uniform granularity
  - Subsector erase 4KB, 32KB granularity
- Low power consumption
  - 12 mA typical active current
  - 1 µA typical power down current
- Security and write/read protection
  - Volatile and nonvolatile locking and software write/read protection for each 64KB sector
  - Nonvolatile configuration locking
  - Hardware write protection: nonvolatile bits (BP[3:0] and TB) define protected area size
  - Program/erase protection during power-up
  - CRC detects accidental changes to raw data
- Certifications
  - RoHS Compliant, ISO 9001 Certified Manufacturing
- Environmental
  - Shock and Vibration Tested, Moisture Sensitivity Level (MSL) 1

Figure.1 CONNECTION DIAGRAMS

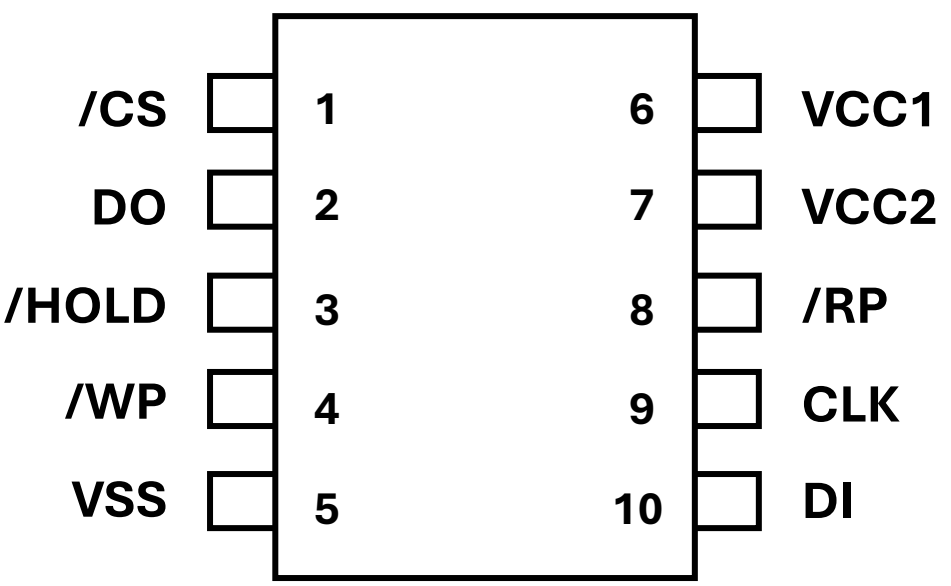

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Table 1. Pin Names

Index	PIN NAME	FUNCTION	TYPE
1	/CS	Chip Select Input	I
2	DO	Data Output	O
3	/HOLD	Hold Input	I
4	/WP	Write Protect Input	I
5	VSS	Ground	P
6	VCC1	3.3V Power Supply	P
7	VCC2	5V Power Supply	P
8	/RP	Read Protect Input	I
9	CLK	Serial Clock Input	I
10	DI	Data Input	I

SIGNAL DESCRIPTION

Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations.

Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted.

Read Protect (/RP)

To enable data reading from the chip, the /RP pin must be set to 5V (High). If the /RP pin is set to 0V (Low), data reading is disabled.

- VIH : 4V to 5.5V to enable data reading.
- VIL : Below 4V to disable data reading.
- Precaution: Ensure the /RP pin is not subject to voltage fluctuations or noise to avoid unintended data reading issues. Additionally, use proper PCB design to consistently provide a stable voltage between 4V and 5.5V to the RP# pin.

Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Note that the activation and deactivation of the /WP pin are governed by the same voltage levels as the /RP pin. Thus, a stable voltage between 4V and 5V is required to reliably disable write protection.

Figure 2. SPI Modes

The PL25QL128C is accessed through a SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Both SPI bus operation Modes 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3, as shown in Figure 3, concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0 the CLK signal is normally low. For Mode 3 the CLK signal is normally high. In either case data input on the DI pin is sampled on the rising edge of the CLK. Data output on the DO pin is clocked out on the falling edge of CLK.

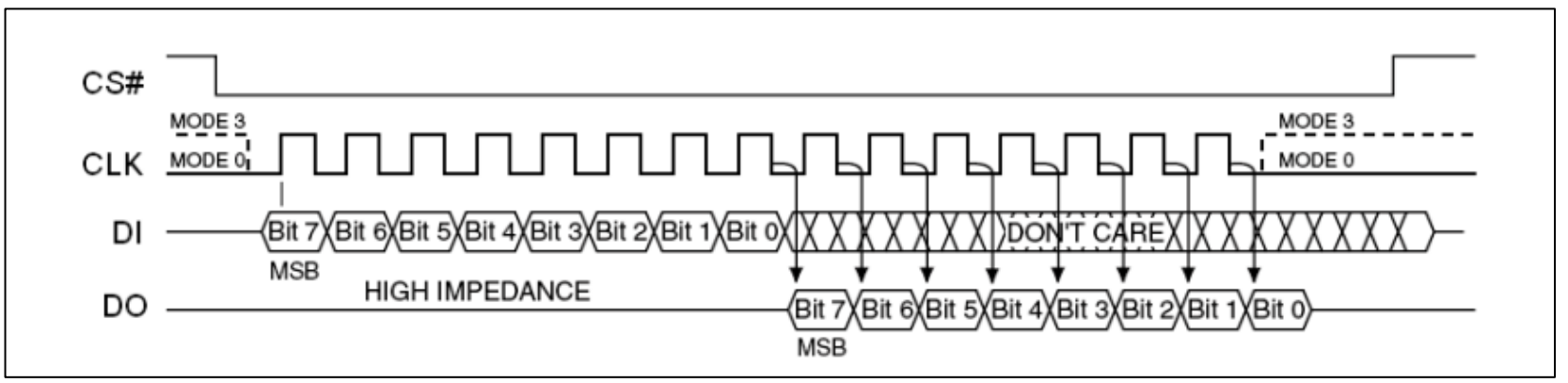

Table 2. Instruction Set

Instruction Name	Byte 1 Code	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	continuous
Read Identification	9Fh	(M7-M0)	(ID15-ID8)	(ID7-ID0)	(1)		
Manufacturer/Device ID	90h	dummy	dummy	00h	(M7-M0)	(ID7-ID0)	(2)
Deep Power-down	B9h						
Release from Deep Power-down, and Device ID	ABh	dummy	dummy	dummy	(ID7-ID0)		

1. (M7-M0) : Manufacturer, (ID15-ID8) : Memory Type, (ID7-ID0) : Memory Capacity
2. The Manufacturer ID and Device ID bytes will repeat continuously until CS# terminates the instruction.

Table 3. Manufacturer and Device Identification

OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			42h
90h	4Dh		42h
9Fh	4Dh	3015h	