Jaeseo Lee

Pohang, South Korea | jaeseolee96@gmail.com | linkedin.com/in/jaeseo-lee-04a96a110

Summary

Ph.D. candidate in the Department of Computer Science and Engineering at POSTECH. My primary research focuses are formal methods, model checking, POR (partial order reduction), and programming language semantics. Recently, I have been developing a unified semantic framework involving programming languages, physical dynamics, and inter-object communications. To make analyses with the unified semantics tractable, I have been working on state space reduction methods, including POR, in both theoretical and practical ways.

Education

Software Verification Lab. (POSTECH) — *Pohang, South Korea*
MS/Ph.D. in Computer Science and Engineering — *Feb 2017 - Present*

Pohang University of Science and Technology (POSTECH) — *Pohang, South Korea*
BS in Industrial and Management Engineering — *Mar 2011 - Feb 2017*

University of California, Berkeley — *Berkeley, California*
Concurrent Enrollment Program — *Jan 2015 – Dec 2015*

- Coursework: Operating Systems, Architecture, Machine Learning, Compiler, Security

Industry Collaboration Projects

Verification on PLC Programs, with *KSOE (HD Korea Shipbuilding & Offshore Engineering Co., Ltd.)* — *Jan 2020 – Dec 2020*

- Clarified the ambiguous semantics of PLC language described in natural languages
- Devise a bounded linear temporal logic (LTL) model checking method that checks conformity of PLC programs to specifications
- Created a language that can easily specify PLC programs' desired properties
- Developed STBMC [tool] that integrates the whole process of PLC program verification. This tool generates a counterexample if and only if one exists

Equivalence of LLVM IR Programs, with *GT One* — *June 2017 – Nov 2018*

- Proved equivalence of the left-hand side and right-hand side of security-enhancing code transformation rules
- Developed a lightweight tool with a translation validation approach

Publications

Formal Analysis of Networked PLC Controllers Interacting with Physical Environments (submitted) — *SAS, 2025*

Jaeseo Lee, Kyungmin Bae

Formal Semantics and Analysis of Multitask PLC ST Programs with Preemption — *FM, 2024*

Jaeseo Lee, Kyungmin Bae [paper]

Bounded Model Checking of PLC ST Programs using Rewriting Modulo SMT — *FTSCS, 2022*

Jaeseo Lee, Sangki Kim, Kyungmin Bae [paper]

Lightweight Equivalence Checking of Code Transformation for Code Pointer Integrity (in Korean) — *KCSE, 2019.12*

Jaeseo Lee, Tae-Hyoung Choi, Gyuho Lee, Jaegwan Yu, Kyungmin Bae [paper]

Teaching

CSED332: Software Design Methods (TA) *Fall, 2017*

CSED321: Programming Languages (TA) *Spring, 2019*

CSED332: Software Design Methods (TA) *Fall, 2019*

Scholarships

National Science & Technology Scholarship *Mar 2011 - Feb 2017*

Additional Work Experience

NSW Department of Education *Sydney, Australia*

Jan 2014 - Feb 2014

- Managed document workflows, including merging, splitting, and digitizing hard-copy materials for efficient electronic record-keeping
- Converted physical documents into electronic formats to support efficient access and archiving
- Collected and organized signed forms from staff across the department to support compliance with internal procedures
- Participated in departmental meetings to observe administrative and policy processes