HW2

T1

(a). The smallest positive normalized number is 2^{-126}.

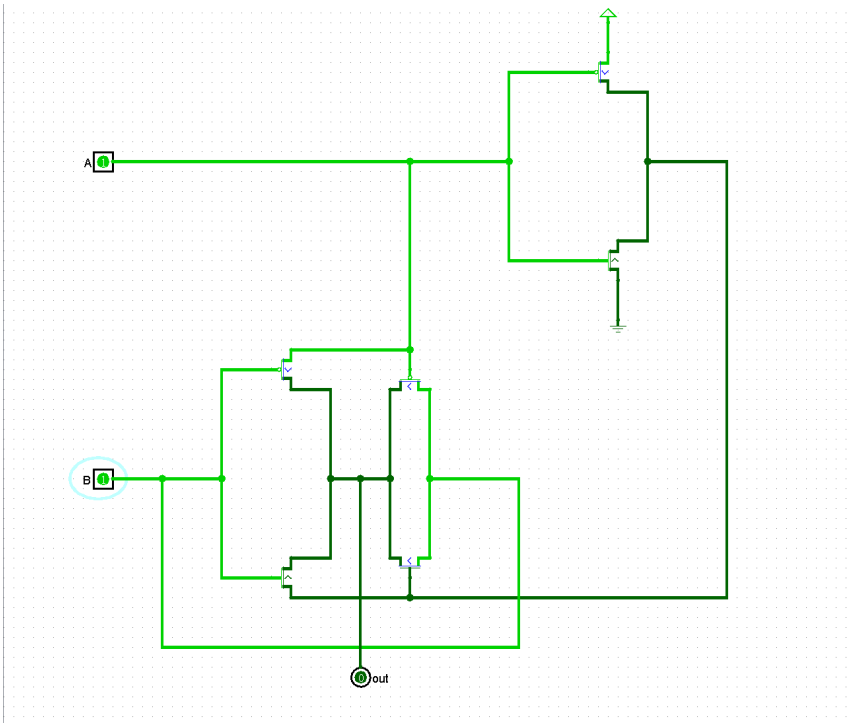
(b). The largest positive subnormal number is $0.FFFFFE * 2^{-126}$, where $0.FFFFFE$ is in hex.

T2

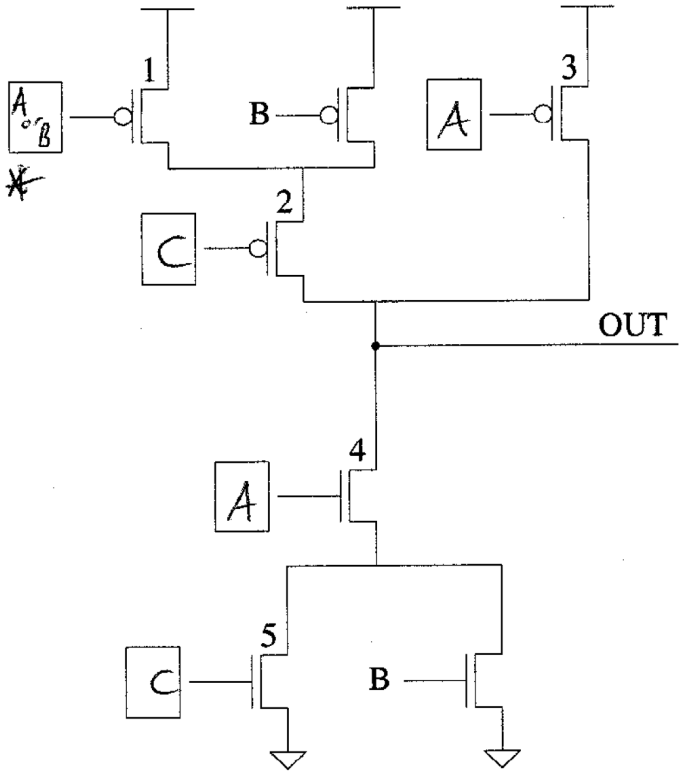
$01111111111111111111111111111111$, which equals $2147483648 = 2^{31}$.

T3

The is $A \cdot \overline{B} + \overline{A} \cdot B$. We can draw the transistor level circuit like this.



T4



A	B	C	OUT
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

T5

$$0\ OR\ X = X$$
$$0\ ORX = 1$$
$$0\ AND\ X = 0$$
$$1\ ANDX = 1$$
$$1\ XOR\ X = X$$

T6

Figure 3.39 is a simple combination circuit. The output value depends only on the input of the values. while the Figure 3.30 is a sequential logic.

T7

(a) $2^5 = 32$bit

(b) $1bit,\ 4bit$

T8

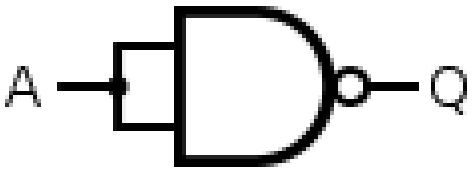
1. 3
2. Yes. The algebraic expressions is $Z = ((((A \cdot B) \cdot C) \cdot D) \cdot E)$. And it can simply

T9

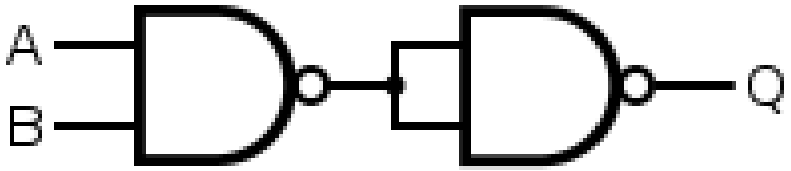
T10

A NAND gates is a universal gate, meaning that any other gate can be represented as a combination of NAND gate.

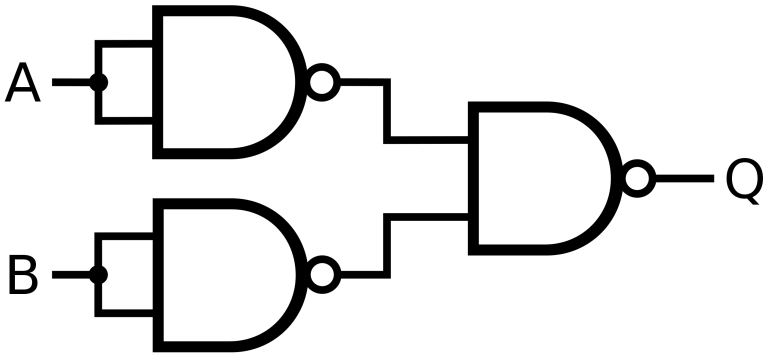
NOT



AND

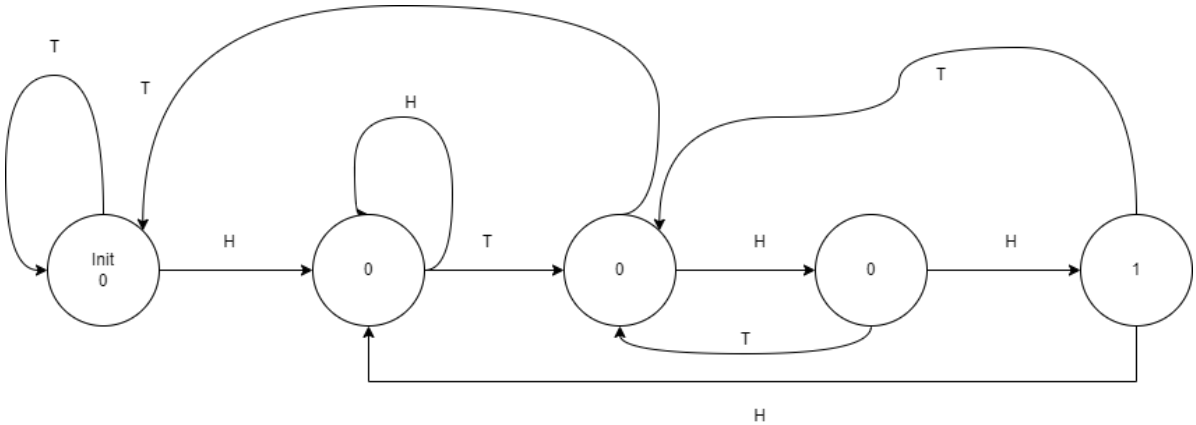


OR



T11

(a).



T12

T13

$2^8 \times 2^8 = 2^{16}$bytes.