**EDA234-LAB 1**

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In this assignment, we have created a VHDL design of a counter to count 0-58 seconds. The counter was designed and programmed to an FPGA board. The functionality of the counter was verified with the help of a seven-segment display on the FPGA board. The counter was implemented for a 100MHz clock. The counter was displayed on the seven-segment display by using a 200Hz switching frequency. The initial design of the counter was implemented with 69 registers as flip-flops. To reduce the number of registers, we have reduced the counter variables used in the design and could successfully implement the design with 42 registers as Flipflop. We created the design based on clock division logic. Collaborated with Shailesh Suresh Velloli to complete the lab handin1.