UCM-iMX8M-Plus

Reference Guide

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Table 1 Revision Notes

Date	Description
Mar 2021	• Initial release
September 2021	• Removed USB_ID signals from tables 17, 18, 44
November 2021	• Updated RGMII VIO information in section 4.5.2

Please check for a newer revision of this manual at the CompuLab website https://www.compulab.com. Compare the revision notes of the updated manual from the website with those of the printed or electronic version you have.

1 INTRODUCTION

1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate and program CompuLab UCM-iMX8M-Plus System-on-Module.

1.2 UCM-iMX8M-Plus Part Number Legend

Please refer to the CompuLab website 'Ordering information' section to decode the UCM-iMX8M-Plus part number: https://www.compulab.com/products/computer-on-modules/ucm-imx8m-plus-nxp-i-mx-8m-plus-som-system-on-module-computer/#ordering.

1.3 Related Documents

For additional information, refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
UCM-iMX8M-Plus Developer Resources	https://www.compulab.com/products/computer-on-modules/ucm-imx8m-plus-nxp-i-mx-8m-plus-som-system-on-module-computer/#devres
i.MX8M Plus Reference Manual	https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-8-processors/i-mx-8m-plus-arm-cortex-a53-machine-learning-vision-multimedia-and-industrial-iot:IMX8MPLUS?tab=Documentation_Tab
i.MX8M Plus Datasheet	

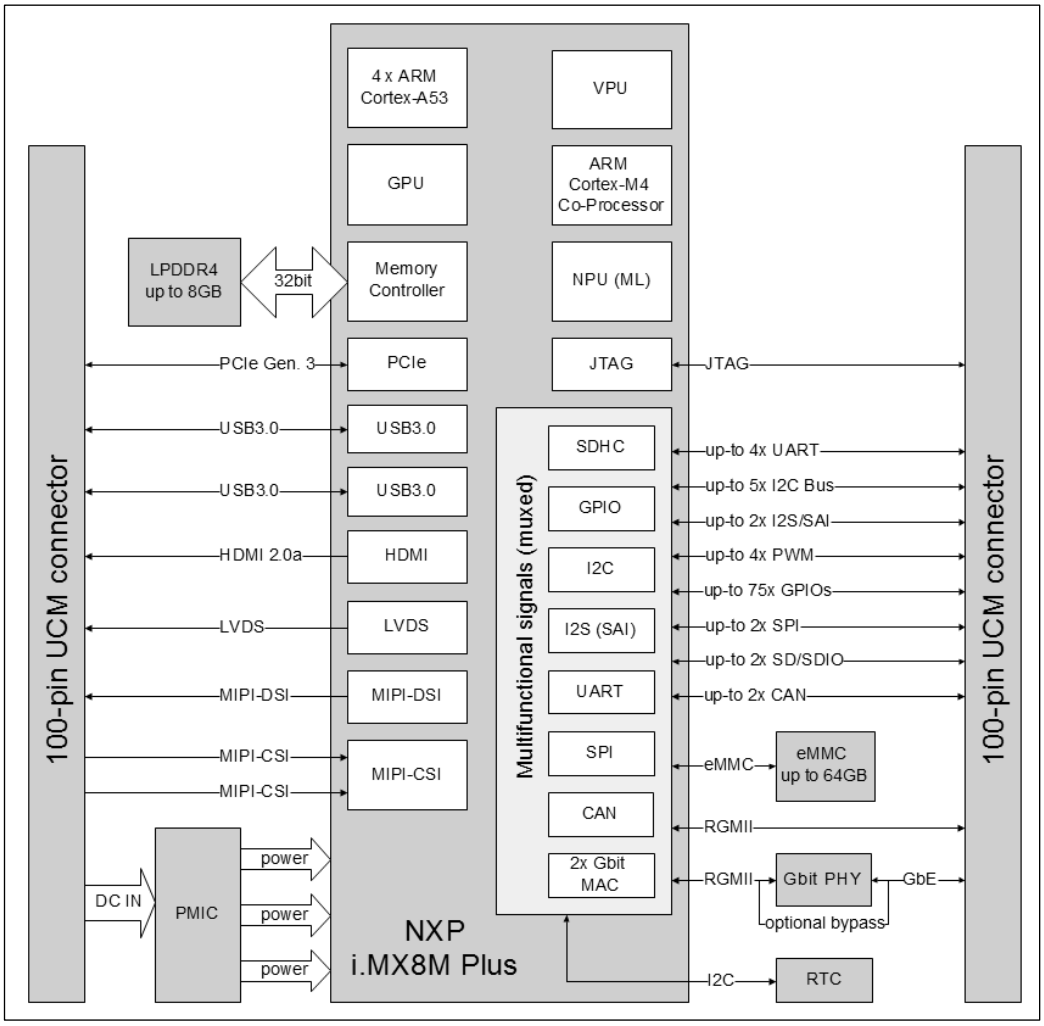
2 OVERVIEW

2.1 Highlights

- NXP i.MX8M Plus Processor, up-to 1.8GHz
- Up to 8GB LPDDR4 and 64GB eMMC
- 2D/3D GPU, 1080p VPU and audio DSP
- Integrated AI/ML Neural Processing Unit
- HDMI, LVDS, MIPI-DSI
- 2x MIPI-CSI camera inputs with dedicated ISP
- PCIe, GbE, RGMII, 2x USB3.0
- 2x CAN, 4x UART, 75x GPIO
- Tiny size and weight - 28 x 38 x 4 mm, 7 gram

2.2 Block Diagram

Figure 1 UCM-iMX8M-Plus Block Diagram



2.3 UCM-iMX8M-Plus Specifications

The "Option" column specifies the CoM/SoM configuration option required to have the particular feature. When a CoM/SoM configuration option is prefixed by “NOT”, the particular feature is only available when the option is not used. A feature is only available when a CoM/SoM configuration complies with all options denoted in the “Option” column.
"+" means that the feature is always available.

Table 3 Features and Configuration options

Feature	Description	Option
CPU Core and Graphics		
CPU	NXP i.MX8M Plus Quad, quad-core ARM Cortex-A53, 1.8GHz	C1800QM
	NXP i.MX8M Plus QuadLite, quad-core ARM Cortex-A53, 1.8GHz	C1800Q
Video Decode	1080p60 HEVC/H.265, AVC/H.264, VP9, VP8	C1800QM
Video Encode	1080p60 HEVC/H.265, AVC/H.264	C1800QM
GPU	GC7000UL (3D): OpenGL ES 3.1/3.0/2.0/1.1, OpenCL 1.1/1.2; GC520L (2D): DirectFB, GDI/DirectDraw	+
NPU	AI/ML Neural Processing Unit, up to 2.3 TOPS	C1800QM
Real-Time Co-processor	ARM Cortex-M7 @ 800 Mhz	+
DSP	Tensilica® HiFi 4 DSP	C1800QM
Memory and Storage		
RAM	1GB – 8GB, LPDDR4	D
Storage	eMMC flash, 16GB - 64GB	N
Display and Camera		
Display	HDMI 2.0a, up to 1080p60	+
	MIPI-DSI, 4 data lanes, up to 1080p60	+
	LVDS, 4 lanes, up to 1366x768 p60	+
Touchscreen	Capacitive touch-screen support through eSPI and I2C interfaces	+
Camera	2x MIPI-CSI, 4 data lanes	+
Network		
Ethernet	Gigabit Ethernet port (MAC+PHY)	+
RGMII	Primary RGMII	Not E
	Secondary RGMII	+
Audio		
Digital Audio	Up-to 2x I2S / SAI	+
	eARC	+
	S/PDIF input/output	+
I/O		
PCI Express	PCIe Gen. 3.0 x1	+
USB	2x USB3.0 (one host, one dual-role)	+
UART	Up to 4x UART	+
CAN bus	Up-to 2x CAN	+
MMC/SD/SDIO	Up to 2x SD/SDIO	+
SPI	Up to 2x SPI	+
I2C	Up to 5x I2C	+
PWM	Up to 4x general purpose PWM signals	+
GPIO	Up to 75x GPIO (multifunctional signals shared with other functions)	+
System Logic		
RTC	Real-time clock, powered by external battery	+
JTAG	JTAG debug interface	+

Table 4 Electrical, Mechanical and Environmental Specifications

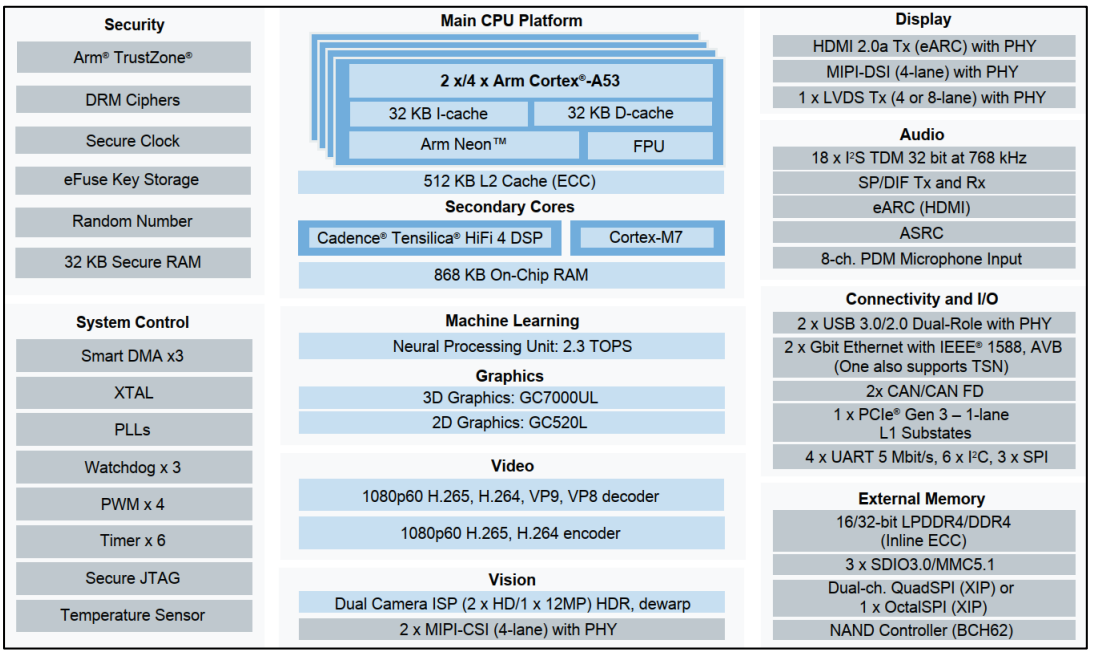
Electrical Specifications	
Supply Voltage	3.45V to 4.4V
Digital I/O voltage	3.3V
Mechanical Specifications	
Dimensions	28 x 38 x 4 mm
Weight	7 gram
Connectors	2 x 100 pin, 0.4mm pitch
Environmental and Reliability	
MTTF	> 200,000 hours
Operation temperature (case)	Commercial: 0° to 70° C
	Extended: -20° to 70° C
	Industrial: -40° to 85° C
Storage temperature	-40° to 85° C
Relative humidity	10% to 90% (operation)
	05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz

3 CORE SYSTEM COMPONENTS

3.1 i.MX8M Plus SoC

The i.MX8M Plus family of processors features advanced implementation of a quad ARM® Cortex®-A53 core, which operates at speeds of up to 1.8 GHz. A general purpose Cortex®-M7 core processor enables low-power processing.

Figure 2 i.MX8M Plus Block Diagram



3.2 Memory

3.2.1 DRAM

UCM-iMX8M-Plus is equipped with up to 8GB of onboard LPDDR4 memory. The LPDDR4 channel is 32-bits wide.

3.2.2 Bootloader and General Purpose Storage

UCM-iMX8M-Plus uses on-board non-volatile memory (eMMC) storage for storing the bootloader. The remaining eMMC space is intended to store the operating system (kernel & root filesystem) and general purpose (user) data.

4 PERIPHERAL INTERFACES

UCM-iMX8M-Plus implements a variety of peripheral interfaces through 2 x 100-pin (0.4mm pitch) carrier board connectors. The following notes apply to interfaces available through the carrier-board connectors:

- Some interfaces/signals are available only with/without certain configuration options of the UCM-iMX8M-Plus SoM. The availability restrictions of each signal are described in the "Signals description" table for each interface.
- Some of the UCM-iMX8M-Plus carrier board interface pins are multifunctional. Up to 4 functions (ALT modes) are accessible through each multifunctional pin. Multifunctional pins are denoted with an asterisk (*). For additional details, please refer to chapter 5.5.
- All of the UCM-iMX8M-Plus digital interfaces operate at 3.3V voltage levels unless noted otherwise.

The signals for each interface are described in the "Signal description" table for the interface in question. The following notes provide information on the "Signal description" tables:

- **"Signal name"** – The name of each signal with regards to the discussed interface. The signal name corresponds to the relevant function in cases where the carrier board pin in question is multifunctional.
- **"Pin#" –** The carrier board interface pin number where the discussed signal is available, multifunctional pins are denoted with an asterisk.
- **"Type" –** Signal type, see the definition of different signal types below
- **"Description" –** Signal description with regards to the interface in question.
- **"Availability" –** Depending on UCM-iMX8M-Plus configuration options, certain carrier board interface pins are physically disconnected (floating). The "Availability" column summarizes configuration requirements for each signal. All the listed requirements must be met (logical AND) for a signal to be "available" unless noted otherwise.

Each described signal can be one of the following types. Signal type is noted in the "Signal description" tables. Multifunctional pin direction, pull resistor, and open drain functionality is software controlled. The "Type" column header for multifunctional pins refers to the recommended pin configuration with regards to the discussed signal.

- **"AI"** – Analog Input
- **"AO"** – Analog Output
- **"AIO"** – Analog Input/Output
- **"AP"** – Analog Power Output
- **"I"** – Digital Input
- **"O"** – Digital Output
- **"IO"** – Digital Input/Output
- **"P"** – Power
- **"PD" -** Always pulled down onboard UCM-IMX8-Plus, followed by pull value.
- **"PU" -** Always pulled up onboard UCM-IMX8-Plus, followed by pull value.
- **"LVDS" -** Low-voltage differential signaling.

4.1 HDMI

The UCM-iMX8M-Plus HDMI interface is implemented with the HDMI interface of the i.MX8M Plus SoC. It supports the following main features:

- Compliant with HDMI 2.0a
- HDMI 2.1 eARC
- Supports display resolutions of up-to 1080p60

The following table summarizes the HDMI interface signals.

Table 5 HDMI Interface Signals

Signal Name	Pin #	Type	Description	Availability
HDMI_TXCN	P1-25	AO	Negative part of HDMI clock diff-pair	Always available
HDMI_TXCP	P1-23	AO	Positive part of HDMI clock diff-pair	Always available
HDMI_TX0N	P1-31	AO	Negative part of HDMI data diff-pair 0	Always available
HDMI_TX0P	P1-29	AO	Positive part of HDMI data diff-pair 0	Always available
HDMI_TX1N	P1-41	AO	Negative part of HDMI data diff-pair 1	Always available
HDMI_TX1P	P1-39	AO	Positive part of HDMI data diff-pair 1	Always available
HDMI_TX2N	P1-47	AO	Negative part of HDMI data diff-pair 2	Always available
HDMI_TX2P	P1-45	AO	Positive part of HDMI data diff-pair 2	Always available
HDMI_DDC_SCL	P1-70*	O	VESA Data Display Channel clock	Always available
HDMI_DDC_SDA	P1-63*	IO	VESA Data Display Channel data signal	Always available
HDMI_HPD	P1-92*	AO	Hot Plug Detect	Always available
HDMI_CEC	P1-85*	O	Consumer Electronics Control signal	Always available
EARC_N_HPD	P1-35	AO		Always available
EARC_P_UTIL	P1-37	AO		Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.2 MIPI-DSI Interface

The UCM-iMX8M-Plus MIPI-DSI interface is derived from the four-lane MIPI display interface available on the i.MX8M Plus SoC. The following main features are supported:

- Scalable data lane support, 1 to 4 data lanes
- Supports MIPI Standard for D-PHY
- Maximum resolution ranges up to FHD (1920 x 1080 @ 60 Hz)

The table below summarizes the MIPI-DSI interface signals

Table 6 MIPI-DSI Interface Signals

Signal Name	Pin #	Type	Description	Availability
DSI_CKN	P2-21	AO	Negative part of MIPI-DSI clock diff-pair	Always available
DSI_CKP	P2-23	AO	Positive part of MIPI-DSI clock diff-pair	Always available
DSI_DN0	P2-1	AO	Negative part of MIPI-DSI data diff-pair 0	Always available
DSI_DP0	P2-3	AO	Positive part of MIPI-DSI data diff-pair 0	Always available
DSI_DN1	P2-15	AO	Negative part of MIPI-DSI data diff-pair 1	Always available
DSI_DP1	P2-17	AO	Positive part of MIPI-DSI data diff-pair 1	Always available
DSI_DN2	P2-5	AO	Negative part of MIPI-DSI data diff-pair 2	Always available

Signal Name	Pin #	Type	Description	Availability
DSI_DP2	P2-7	AO	Positive part of MIPI-DSI data diff-pair 2	Always available
DSI_DN3	P2-11	AO	Negative part of MIPI-DSI data diff-pair 3	Always available
DSI_DP3	P2-13	AO	Positive part of MIPI-DSI data diff-pair 3	Always available

4.3 LVDS Interface

The UCM-iMX8M-Plus provides one LVDS interface derived from the i.MX8M Plus LVDS display bridge. It supports the following key features:

- Single channel (4 lanes) output at up to 80MHz pixel clock
- Resolutions of up to 1366x768p60

The table below summarizes the LVDS interface signals

Table 7 LVDS Interface Signals

Signal Name	Pin #	Type	Description	Availability
LVDS0_CLK_N	P1-82	AO	Negative part of LVDS clock diff-pair	Always available
LVDS0_CLK_P	P1-80	AO	Positive part of LVDS clock diff-pair	Always available
LVDS0_D0_N	P1-44	AO	Negative part of LVDS data diff-pair 0	Always available
LVDS0_D0_P	P1-42	AO	Positive part of LVDS data diff-pair 0	Always available
LVDS0_D1_N	P1-48	AO	Negative part of LVDS data diff-pair 1	Always available
LVDS0_D1_P	P1-46	AO	Positive part of LVDS data diff-pair 1	Always available
LVDS0_D2_N	P1-52	AO	Negative part of LVDS data diff-pair 2	Always available
LVDS0_D2_P	P1-50	AO	Positive part of LVDS data diff-pair 2	Always available
LVDS0_D3_N	P1-58	AO	Negative part of LVDS data diff-pair 3	Always available
LVDS0_D3_P	P1-56	AO	Positive part of LVDS data diff-pair 3	Always available

4.4 Camera Serial Interface

UCM-iMX8M-Plus provides two MIPI-CSI interfaces, both derived from the four-lane MIPI CSI host controller integrated into the i.MX8M Plus SoC with dedicated Image Signal Processor (ISP). The controller supports the following main features:

- Up-to four data lanes and one clock lane
- MIPI D-PHY specification V1.2
- Compliant to MIPI CSI2 Specification V1.3 except for C-PHY feature
- Supports primary and secondary image format:
  - YUV420, YUV420 (Legacy), YUV420 (CSPS), YUV422 of 8-bits and 10-bits
  - RGB565, RGB666, RGB888
  - RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
- Image Signal Processor (ISP):
  - Input formats: YCbCr420, YCbCr422, RAW8/10/12/14, RGB444/555/565/666/888
  - Image cropping, de-noising, LS and CA lens correction, AWB

Please refer to the i.MX8M Plus Reference manual for additional details. The following table summarizes MIPI-CSI signals.

Table 8 MIPI-CSI Interface Signals

Signal Name	Pin #	Type	Description	Availability
MIPI_CSI1 _CLK_N	P2-2	AI	Negative part of MIPI-CSI1 clock diff-pair	Always available
MIPI_CSI1 _CLK_P	P2-4	AI	Positive part of MIPI-CSI1 clock diff-pair	Always available
MIPI_CSI1_D0_N	P2-6	AI	Negative part of MIPI-CSI1 data diff-pair 0	Always available
MIPI_CSI1_D0_P	P2-8	AI	Positive part of MIPI-CSI1 data diff-pair 0	Always available
MIPI_CSI1_D1_N	P2-31	AI	Negative part of MIPI-CSI11 data diff-pair 1	Always available
MIPI_CSI1_D1_P	P2-33	AI	Positive part of MIPI-CSI1 data diff-pair 1	Always available
MIPI_CSI1_D2_N	P2-25	AI	Negative part of MIPI-CSI1 data diff-pair 2	Always available
MIPI_CSI1_D2_P	P2-27	AI	Positive part of MIPI-CSI1 data diff-pair 2	Always available
MIPI_CSI1_D3_N	P2-35	AI	Negative part of MIPI-CSI1 data diff-pair 3	Always available
MIPI_CSI1_D3_P	P2-37	AI	Positive part of MIPI-CSI1 data diff-pair 3	Always available
MIPI_CSI2 _CLK_N	P2-12	AI	Negative part of MIPI-CSI2 clock diff-pair	Always available
MIPI_CSI2 _CLK_P	P2-14	AI	Positive part of MIPI-CSI2 clock diff-pair	Always available
MIPI_CSI2_D0_N	P2-18	AI	Negative part of MIPI-CSI2 data diff-pair 0	Always available
MIPI_CSI2_D0_P	P2-20	AI	Positive part of MIPI-CSI2 data diff-pair 0	Always available
MIPI_CSI2_D1_N	P2-24	AI	Negative part of MIPI-CSI21 data diff-pair 1	Always available
MIPI_CSI2_D1_P	P2-26	AI	Positive part of MIPI-CSI2 data diff-pair 1	Always available
MIPI_CSI2_D2_N	P2-48	AI	Negative part of MIPI-CSI2 data diff-pair 2	Always available
MIPI_CSI2_D2_P	P2-50	AI	Positive part of MIPI-CSI2 data diff-pair 2	Always available
MIPI_CSI2_D3_N	P2-56	AI	Negative part of MIPI-CSI2 data diff-pair 3	Always available
MIPI_CSI2_D3_P	P2-58	AI	Positive part of MIPI-CSI2 data diff-pair 3	Always available

4.5 Ethernet

UCM-iMX8M-Plus incorporates an optional full-featured 10/100/1000 Ethernet interface, implemented with the i.MX8M Plus MAC coupled with an optional onboard Atheros AR8033 GbE PHY.

4.5.1 Gigabit Ethernet

UCM-iMX8M-Plus with onboard AR8033 PHY (“E” configuration option) supports the following main features:

- 10/100/1000 BASE-T IEEE 802.3 compliant.
- IEEE 802.3u compliant Auto-Negotiation.
- Supports all IEEE 1588 frames - inside the MAC.
- Automatic channel swap (ACS).
- Automatic MDI/MDIX crossover.
- Automatic polarity correction.
- Activity and speed indicator LED controls.

The table below summarizes the GbE interface signals.

Table 9 GbE Interface Signals

Signal Name	Pin #	Type	Description	Availability
AVDD33_ETH	P1-62	P	Center tap supply for Ethernet magnetics	Only with 'E' option
ETH0_LED_ACT	P2-83^	IO;PD8K2	Active High, activity LED driver. 2.5V signal, PHY strap	Only with 'E' option
ETH0_LINK-LED_10_100	P2-86	IO	Active High, 10/100Mbps link LED driver. 2.5V signal	Only with 'E' option
ETH0_LINK-LED_1000	P2-75^	IO; PD	Active High, 1Gbps link LED driver. 2.5V signal, PHY strap	Only with 'E' option
ETH0_MDI0N	P2-73	AIO	Negative part of 100ohm diff-pair 0	Only with 'E' option
ETH0_MDI0P	P2-74	AIO	Positive part of 100ohm diff-pair 0	Only with 'E' option

Signal Name	Pin #	Type	Description	Availability
ETH0_MDI1N	P2-80	AIO	Negative part of 100ohm diff-pair 1	Only with 'E' option
ETH0_MDI1P	P2-78	AIO	Positive part of 100ohm diff-pair 1	Only with 'E' option
ETH0_MDI2N	P2-81	AIO	Negative part of 100ohm diff-pair 2	Only with 'E' option
ETH0_MDI2P	P2-79	AIO	Positive part of 100ohm diff-pair 2	Only with 'E' option
ETH0_MDI3N	P2-85	AIO	Negative part of 100ohm diff-pair 3	Only with 'E' option
ETH0_MDI3P	P2-84	AIO	Positive part of 100ohm diff-pair 3	Only with 'E' option

NOTE: Pins denoted with "^" must not be pulled or driven by carrier board during SoM power-up or reset.

4.5.2 RGMII

UCM-iMX8M-Plus features up-to two RMGII interfaces.

Primary RGMII interface ENET0 is available only when UCM-iMX8M-Plus is assembled without the “E” configuration option.

Secondary RGMII interface ENET1 is available with all UCM-iMX8M-Plus configurations.

The tables below summarize the Ethernet RGMII interface signals.

Table 10 Primary RGMII ENET0 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ENET_MDC	P2-68*	O	Provides a timing reference to the PHY for data transfers on the MDIO signal	Always available
ENET_MDIO	P2-70*	IO	Transfers control information between the external PHY and the MAC. Data is synchronous to MDC. This signal is an input after reset	Always available Always available
ENET0_RD0	P2-86*	I	Ethernet input data from the PHY	Only w/o 'E' option
ENET0_RD1	P2-83*	I	Ethernet input data from the PHY	Only w/o 'E' option
ENET0_RD2	P2-84*	I	Ethernet input data from the PHY	Only w/o 'E' option
ENET0_RD3	P2-85*	I	Ethernet input data from the PHY	Only w/o 'E' option
ENET0_RX_CTL	P2-79*	I	Contains RX_EN on the rising edge of RGMII_RXC, and RX_EN XOR RX_ER on the falling edge of RGMII_RXC (RGMII mode)	Only w/o 'E' option
ENET0_RXC	P2-80*	I	Timing reference for RX_DATA[3:0] and RX_CTL in RGMII MODE	Only w/o 'E' option
ENET0_TD0	P2-75*	O	Ethernet output data to PHY	Only w/o 'E' option
ENET0_TD1	P2-78*	O	Ethernet output data to PHY	Only w/o 'E' option
ENET0_TD2	P2-77*	O	Ethernet output data to PHY	Only w/o 'E' option
ENET0_TD3	P2-73*	O	Ethernet output data to PHY	Only w/o 'E' option
ENET0_TXC	P2-81*	O	Timing reference for TX_DATA[3:0] and TX_CTL in RGMII MODE	Only w/o 'E' option
ENET0_TX_CTL	P2-74*	O	Contains TX_EN on the rising edge of RGMII_TXC, and TX_EN XOR TX_ER on the falling edge of RGMII_TXC (RGMII mode)	Only w/o 'E' option
RGMII0_VIO	P1-55	P	RGMII interface power supply input. This pin must be connected to 1.8V power rail	Only w/o 'E' option

NOTE: 1.8V power must be supplied via the RGMII_VIO pin if any of the RGMII ENET0 signals are used on the carrier-board

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

Table 11 Secondary RGMII ENET1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ENET_MDC	P2-68*	O	Provides a timing reference to the PHY for data transfers on the MDIO signal	Always available
ENET_MDIO	P2-70*	IO	Transfers control information between the external PHY and the MAC. Data is synchronous to MDC. This signal is an input after reset	Always available
ENET1_RD0	P2-41*	I	Ethernet input data from the PHY	Always available
ENET1_RD1	P2-43*	I	Ethernet input data from the PHY	Always available
ENET1_RD2	P2-45*	I	Ethernet input data from the PHY	Always available
ENET1_RD3	P2-47*	I	Ethernet input data from the PHY	Always available
ENET1_RX_CTL	P2-53*	I	Contains RX_EN on the rising edge of RGMII_RXC, and RX_EN XOR RX_ER on the falling edge of RGMII_RXC (RGMII mode)	Always available
ENET1_RXC	P2-55*	I	Timing reference for RX_DATA[3:0] and RX_CTL in RGMII MODE	Always available
ENET1_TD0	P2-60* P2-59*	O	Ethernet output data to PHY	Always available
ENET1_TD1	P2-61*	O	Ethernet output data to PHY	Always available
ENET1_TD2	P2-63*	O	Ethernet output data to PHY	Always available
ENET1_TD3	P2-65*	O	Ethernet output data to PHY	Always available
ENET1_TXC	P2-69*	O	Timing reference for TX_DATA[3:0] and TX_CTL in RGMII MODE	Always available
ENET1_TX_CTL	P2-67*	O	Contains TX_EN on the rising edge of RGMII_TXC, and TX_EN XOR TX_ER on the falling edge of RGMII_TXC (RGMII mode)	Always available

NOTE: RGMII ENET1 signals operate at 1.8V voltage level

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.6 PCI-Express

UCM-iMX8M-Plus provides one PCI Express port. The port requires an external PCIe reference clock to be supplied from the carrier-board.

Table 12 PCIE Interface Signals

Signal Name	Pin #	Type	Description	Availability
PCIE_REF_CLKN	P2-44	AI	100 MHz PCIe reference clock differential input negative	Always available
PCIE_REF_CLKP	P2-42	AI	100 MHz PCIe reference clock differential input positive	Always available
PCIE_RXN_N	P2-30	I	PCI Express receive data negative	Always available
PCIE_RXN_P	P2-32	I	PCI Express receive data positive	Always available
PCIE_TXN_N	P2-36	O	PCI Express transmit data negative	Always available
PCIE_TXN_P	P2-38	O	PCI Express transmit data positive	Always available
PCIE_CLKREQ_B	P2-90*	O	PCI Express Enable external clock generator	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.7 Sony/Philips Digital Interface (S/PDIF)

UCM-iMX8M-Plus provides one S/PDIF transmitter with one output and one S/PDIF receiver with one input.

Please refer to the i.MX8M Plus Reference manual for additional details. The table below summarizes the S/PDIF interface signals.

Table 13 S/PDIF Interface Signals

Signal Name	Pin #	Type	Description	Availability
SPDIF_EXT_CLK	P1-77*	I	External clock signal	Always available
SPDIF_RX	P1-79*	I	SPDIF input data line signal	Always available
SPDIF_TX	P1-81*	O	SPDIF output data line signal	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.8 Digital Audio (SAI)

UCM-iMX8M-Plus enables access to three of the i.MX8M Plus integrated synchronous audio interface (SAI) modules. The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces. The following main features are supported:

- One transmitter with independent bit clock and frame sync supporting 1 data line. One receiver with independent bit clock and frame sync supporting 1 data line.
- Maximum Frame Size of 32 words.
- Word size of between 8-bits and 32-bits. Separate word size configuration for the first word and remaining words in the frame.
- Asynchronous 32 × 32-bit FIFO for each transmit and receive channel

Please refer to the i.MX8M Plus Reference manual for additional details. The tables below summarize the SAI interface signals.

Table 14 SAI3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SAI3_MCLK	P1-49* P1-30*	IO	Audio master clock. An input when generated externally and an output when generated internally.	Always available
SAI3_RXD0	P1-28*	I	Receive data, sampled synchronously by the bit clock	Always available
SAI3_RXC	P1-32*	I	Receive bit clock. An input when generated externally and an output when generated internally.	Always available
SAI3_RXFS	P1-34*	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always available
SAI3_TXD0	P1-26*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
SAI3_TXC	P1-36*	O	Transmit bit clock. An input when generated externally and an output when generated internally.	Always available
SAI3_TXFS	P1-38*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always available

Table 15 SAI5 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SAI5_MCLK	P2-52* P1-96* P1-49*	IO	Audio master clock. An input when generated externally and an output when generated internally.	Always available
SAI5_RXD0	P1-100* P1-28*	I	Receive data 0, sampled synchronously by the bit clock	Always available
SAI5_RXD1	P1-38*	I	Receive data 1, sampled synchronously by the bit clock	Always available
SAI5_RXD2	P1-36*	I	Receive data 2, sampled synchronously by the bit clock	Always available
SAI5_RXD3	P1-26*	I	Receive data 3, sampled synchronously by the bit clock	Always available
SAI5_RXC	P1-89* P1-32*	I	Receive bit clock. An input when generated externally and an output when generated internally.	Always available
SAI5_RXFS	P1-87* P1-34*	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always available
SAI5_TXD0	P2-60*	O	Transmit data signal 0.Synchronous to bit clock.	Always available
SAI5_TXD1	P2-88* P2-76*	O	Transmit data signal 1.Synchronous to bit clock.	Always available
SAI5_TXD2	P2-63* P1-51*	O	Transmit data signal 2.Synchronous to bit clock.	Always available
SAI5_TXD3	P2-65* P1-33*	O	Transmit data signal 3.Synchronous to bit clock.	Always available
SAI5_TXC	P2-55* P1-53*	O	Transmit bit clock. An input when generated externally and an output when generated internally.	Always available
SAI5_TXFS	P2-53* P2-88*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always available

Table 16 SAI7 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SAI7_MCLK	P2-89*	IO	Audio master clock. An input when generated externally and an output when generated internally.	Always available
	P2-85			Only w/o 'E' option
SAI7_RXD0	P2-86	I	Receive data, sampled synchronously by the bit clock	Only w/o 'E' option
SAI7_RXC	P2-84*	I	Receive bit clock. An input when generated externally and an output when generated internally.	Only w/o 'E' option
SAI7_RXFS	P2-83*	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Only w/o 'E' option
SAI7_TXD0	P2-95*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
	P2-81*			Only w/o 'E' option
SAI7_TXC	P2-93*	O	Transmit bit clock. An input when generated externally and an output when generated internally.	Always available
	P2-80*			Only w/o 'E' option
SAI7_TXFS	P2-79	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Only w/o 'E' option

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.9 USB

i.MX8M Plus SoC is equipped with two dual-role USB3.0 controllers and PHYs. One port supports OTG functionality, while the second port is configured permanently for host mode.

Please refer to the i.MX8M Plus Reference manual for additional details.

The tables below summarize the USB3.0 interface signals.

Table 17 USB port #1 Signals

Signal Name	Pin #	Type	Description	Availability
USB1_DN	P1-14	IO	USB2.0 negative data	Always available
USB1_DP	P1-12	IO	USB2.0 positive data	Always available
USB1_VBUS_DET	P1-24	I	USB1 VBUS detect	Always available
USB1_TX_N	P1-18	AO	USB3.0 transmit negative lane	Always available
USB1_TX_P	P1-16	AO	USB3.0 transmit positive lane	Always available
USB1_RX_N	P1-8	AI	USB3.0 receive negative lane	Always available
USB1_RX_P	P1-6	AI	USB3.0 receive positive lane	Always available

Table 18 USB port #2 Signals

Signal Name	Pin #	Type	Description	Availability
USB2_DN	P1-5	IO	USB2.0 negative data	Always available
USB2_DP	P1-3	IO	USB2.0 positive data	Always available
USB2_VBUS_DET	P1-1	I	USB2 VBUS detect	Always available
USB1_TX_N	P1-15	AO	USB3.0 transmit negative lane	Always available
USB1_TX_P	P1-13	AO	USB3.0 transmit positive lane	Always available
USB2_RX_N	P1-9	AI	USB3.0 receive negative lane	Always available
USB2_RX_P	P1-7	AI	USB3.0 receive positive lane	Always available

4.10 MMC / SD /SDIO

UCM-iMX8M-Plus features two SD/SDIO ports. These ports are derived from the i.MX8M Plus SD/SDIO controllers uSDHC1 and uSDHC2. uSDHC IP supports the following main features:

- Fully compliant with MMC 5.1 command/response sets and physical layer
- Fully compliant with SD 3.01 command/response sets and physical layer

Please refer to the i.MX8M Plus Reference manual for additional details.

The table below summarizes the MMC/SD/SDIO interface signals.

Table 19 SD/SDIO port #1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SD1_CLK	P2-68*	O	Clock for MMC/SD/SDIO card	Always available
SD1_CMD	P2-70*	IO	CMD line connect to card	Always available
SD1_DATA0	P2-61*	IO	DATA0 line in all modes. Also used to detect busy state	Always available
SD1_DATA1	P2-59*	IO	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4- bit mode	Always available
SD1_DATA2	P2-41*	IO	DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode	Always available
SD1_DATA3	P2-43*	IO	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.	Always available
SD1_RESET_B	P2-62*	O	Card hardware reset signal, active LOW	Always available

NOTE: SD/SDIO port #1 is pre-configured to operate only at 3.3V voltage levels

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

Table 20 SD/SDIO port #2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SD2_nCD	P2-92*	I	Card detection pin	Always available
SD2_CLK	P2-96*	O	Clock for MMC/SD/SDIO card	Always available
SD2_CMD	P2-100*	IO	CMD line connect to card	Always available
SD2_DATA0	P2-97*	IO	DATA0 line in all modes. Also used to detect busy state	Always available
SD2_DATA1	P2-99*	IO	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4- bit mode	Always available
SD2_DATA2	P2-94*	IO	DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode	Always available
SD2_DATA3	P2-98*	IO	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.	Always available
SD2_RESET_B	P2-51*	O	Card hardware reset signal, active LOW	Always available
SD2_WP	P2-49*	I	Card write protect detection	Always available

NOTE: SD/SDIO port #2 can be configured to operate at 3.3V or 1.8V voltage levels. Voltage level is controlled by SoC pin GPIO1_IO04.

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.11 UART

UCM-iMX8M-Plus enables access to up-to four i.MX8M Plus universal asynchronous receiver/transmitter (UART) modules based on the UARTv2 IP. The i.MX8M Plus UARTv2 supports the following features:

- High-speed TIA/EIA-232-F compatible.
- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none).
- Programmable baud rates up to 4 Mbps.
- 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud.
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s).
- Hardware flow control support for a request to send and clear to send signals.
- RS-485 driver direction control.
- DCE/DTE capability.
- RX_DATA input and TX_DATA output can be inverted respectively in RS-232/RS-485 mode.
- Various asynchronous wake mechanisms with the capability to wake the processor from STOP mode through an on-chip interrupt.

NOTE: By default UART2 is assigned to be used as the main system console port.

NOTE: By default UART4 is assigned to be used as the M7 core debug port.

Please refer to the i.MX8M Plus Reference manual for additional details.

The tables below summarize the UART interface signals.

Table 21 UART1 Signals

Signal Name	Pin #	Type	Description	Availability
UART1_CTS_B	P1-21* P2-76*	O	UART-1 clear to send	Always available
UART1_RTS_B	P1-61* P2-61*	I	UART-1 request to send	Always available
UART1_RXD	P1-19* P1-53* P2-70*	I	UART-1 serial data receive	Always available
UART1_TXD	P1-72* P2-68* P2-88*	O	UART-1 serial data transmit	Always available

Table 22 UART2 Signals

Signal Name	Pin #	Type	Description	Availability
UART2_CTS_B	P1-32* P1-84*	O	UART-2 clear to send	Always available
UART2_RTS_B	P1-28* P1-86*	I	UART-2 request to send	Always available
UART2_RXD	P1-76* P1-38* P2-43* P2-97*	I	UART-2 serial data receive	Always available
UART2_TXD	P1-74* P1-36* P2-41 P2-99	O	UART-2 serial data transmit	Always available

Table 23 UART3 Signals

Signal Name	Pin #	Type	Description	Availability
UART3_RXD	P1-21*	I	UART-3 serial data receive	Always available
UART3_TXD	P1-61*	O	UART-3 serial data transmit	Always available

Table 24 UART4 Signals

Signal Name	Pin #	Type	Description	Availability
UART4_RXD	P1-84* P2-93* P2-96*	I	UART-4 serial data receive	Always available
UART4_TXD	P1-86* P2-95* P2-100*	O	UART-4 serial data transmit	Always available
UART4_CTS_B	P2-89*	O	UART-4 clear to send	Always available
UART4_RTS_B	P2-91*	I	UART-4 request to send	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.12 CAN Bus

UCM-iMX8M-Plus features up-to two CAN bus interfaces. These interfaces support the following key features:

- Full implementation of the CAN version 2.0B
- Compliant with the ISO 11898-1 standard

Please refer to the i.MX8M Plus Reference manual for additional details.

The tables below summarize the CAN interface signals.

Table 25 CAN1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
CAN1_TX	P1-53* P1-81* P1-70*	O	CAN transmit pin	Always available
CAN1_RX	P1-51* P1-79* P1-63*	I	CAN receive pin	Always available

Table 26 CAN2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
CAN2_TX	P1-21* P1-33* P1-85*	O	CAN transmit pin	Always available
CAN2_RX	P1-49* P1-61* P1-96* P1-92*	I	CAN receive pin	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.13 I2C

UCM-iMX8M-Plus features up-to five I2C bus interfaces. The following general features are supported by all I2C bus interfaces:

- Compliant with Philips I2C specification version 2.1
- Supports standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Multimaster operation
- Master or Slave operation mode

Please refer to the i.MX8M Plus Reference manual for additional details.

NOTE: I2C2 is the system I2C channel utilized for the following on-board functions: RTC, EEPROM.

The tables below summarize the I2C interface signals.

Table 27 I2C2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C2_SCL	P1-99	O	I2C serial clock line	Always available
I2C2_SDA	P1-97	IO	I2C serial data line	Always available

Table 28 I2C3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C3_SCL	P1-94* P2-93* P2-62*	O	I2C serial clock line	Always available
I2C3_SDA	P1-91* P2-95*	IO	Always available	Always available

Table 29 I2C4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C4_SCL	P2-90* P2-89* P2-41*	O	I2C serial clock line	Always available

Signal Name	Pin #	Type	Description	Availability
	P2-99*			
I2C4_SDA	P2-91* P2-43* P2-97*	IO	Always available	Always available

Table 30 I2C5 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C5_SCL	P1-70* P1-81* P1-100* P2-68*	O	I2C serial clock line	Always available
I2C5_SDA	P1-63* P1-79* P1-96* P2-70*	IO	Always available	Always available

Table 31 I2C6 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C6_SCL	P1-84* P1-85* P1-87* P2-61*	O	I2C serial clock line	Always available
I2C6_SDA	P1-86* P1-89* P1-92* P2-59*	IO	Always available	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.14 ECSPI

Up-to two SPI interfaces are accessible through the UCM-iMX8M-Plus carrier board interface. The SPI interfaces are derived from i.MX8M Plus integrated synchronous serial interface (eCSPI). Each instance of the eCSPI port can operate as either a master or as an SPI slave. The following features are supported:

- Data rate up to 52 Mbit/s.
- Full-duplex synchronous serial interface.
- Master/Slave configurable.
- Up-to four chip select signals to support multiple peripherals.
- Transfer continuation function allows unlimited length data transfers.
- 32-bit wide by 64-entry FIFO for both transmit and receive data.
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable.
- Direct Memory Access (DMA) support.

Please refer to the i.MX8M Plus Reference manual for additional details.

The tables below summarize the ECSPI interface signals.

Table 32 ECSPI2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ECSPI2_MISO	P2-89* P2-90* P2-98*	I	SPI-2 Master data in; slave data out	Always available
ECSPI2_MOSI	P1-91* P2-95*	O	SPI-2 Master data out; slave data in	Always available

Signal Name	Pin #	Type	Description	Availability
	P2-100*			
ECSPI2_SCLK	P1-94*	O	SPI-2 Master clock out; slave clock in	Always available
	P2-93*			
	P2-96*			
ECSPI2_SS0	P2-91*	O	SPI-2 Chip select 0	Always available
	P2-94*			

Table 33 ECSPI3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ECSPI3_MISO	P1-76*	I	SPI-3 Master data in; slave data out	Always available
ECSPI3_MOSI	P1-72*	O	SPI-3 Master data out; slave data in	Always available
ECSPI3_SCLK	P1-19*	O	SPI-3 Master clock out; slave clock in	Always available
ECSPI3_SS0	P1-74*	O	SPI-3 Chip select 0	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.15 PWM

UCM-iMX8M-Plus features up to four independent PWM output signals. The following key features are supported:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Interrupts at compare and rollover

Please refer to the i.MX8M Plus Reference manual for additional details.

The table below summarizes the PWM interface signals.

Table 34 PWM Interface Signals

Signal Name	Pin #	Type	Description	Availability
PWM1_OUT	P1-77*	O	PWM1 functional output	Always available
	P1-96*			
	P1-98*			
PWM2_OUT	P1-79*	O	PWM2 functional output	Always available
	P1-100*			
	P2-90*			
PWM3_OUT	P1-81*	O	PWM3 functional output	Always available
	P1-89*			
	P1-91*			
PWM4_OUT	P1-30*	O	PWM4 functional output	Always available
	P1-87*			
	P1-94*			

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.16 JTAG

UCM-iMX8M-Plus enables access to the i.MX8M Plus JTAG port through the carrier board interface.

Please refer to the i.MX8M Plus Reference manual for additional details.

The table below summarizes the JTAG interface signals.

Table 35 JTAG Interface Signals

Signal Name	Pin #	Type	Description	Availability
JTAG_MOD	P1-75	I	JTAG MODE	Always available
JTAG_nTRST	P1-63	I	Test Reset	Always available
JTAG_TCK	P1-73	I	Test Clock	Always available
JTAG_TDI	P1-71	I	Test Data In	Always available
JTAG_TDO	P1-67	O	Test Data Out	Always available
JTAG_TMS	P1-65	I	Test Mode Select	Always available

4.17 GPIO

Up-to 79 of the i.MX8M Plus general purpose input/output (GPIO) signals are available through the UCM-iMX8M-Plus carrier board interface. When configured as an output, it is possible to write to an i.MX8M Plus register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an i.MX8M Plus register. In addition, GPIO signals can produce interrupts.
Please refer to the i.MX8M Plus Reference manual for additional details.
The table below summarizes the GPIO interface signals.

Table 36 GPIO Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Always available
GPIO1_IO0	P1-59*	IO	GPIO	3.3V	Always available
GPIO1_IO1	P1-98*	IO	GPIO	3.3V	Always available
GPIO1_IO18	P2-73*	IO	GPIO	RGMII_VIO	Only w/o “E” option
GPIO1_IO19	P2-77*	IO	GPIO	RGMII_VIO	Only w/o “E” option
GPIO1_IO20	P2-78*	IO	GPIO	RGMII_VIO	Only w/o “E” option
GPIO1_IO21	P2-75*	IO	GPIO	RGMII_VIO	Only w/o “E” option
GPIO1_IO22	P2-74*	IO	GPIO	RGMII_VIO	Only w/o “E” option
GPIO1_IO23	P2-81*	IO	GPIO	RGMII_VIO	Only w/o “E” option
GPIO1_IO24	P2-79*	IO	GPIO	RGMII_VIO	Only w/o “E” option
GPIO1_IO25	P2-80*	IO	GPIO	RGMII_VIO	Only w/o “E” option
GPIO1_IO26	P2-86*	IO	GPIO	RGMII_VIO	Only w/o “E” option
GPIO1_IO27	P2-83*	IO	GPIO	RGMII_VIO	Only w/o “E” option
GPIO1_IO28	P2-84*	IO	GPIO	RGMII_VIO	Only w/o “E” option
GPIO1_IO29	P2-85*	IO	GPIO	RGMII_VIO	Only w/o “E” option
GPIO2_IO0	P2-68*	IO	GPIO	3.3V	Always available
GPIO2_IO1	P2-70*	IO	GPIO	3.3V	Always available
GPIO2_IO10	P2-62*	IO	GPIO	3.3V	Always available
GPIO2_IO12	P2-92*	O	GPIO	3.3V	Always available
GPIO2_IO13	P2-96*	O	GPIO	3.3V	Always available
GPIO2_IO14	P2-100*	IO	GPIO	3.3V	Always available
GPIO2_IO15	P2-97*	IO	GPIO	3.3V	Always available
GPIO2_IO16	P2-99*	IO	GPIO	3.3V	Always available
GPIO2_IO17	P2-94*	IO	GPIO	3.3V	Always available
GPIO2_IO18	P2-98*	IO	GPIO	3.3V	Always available
GPIO2_IO19	P2-51*	IO	GPIO	3.3V	Always available
GPIO2_IO2	P2-61*	IO	GPIO	3.3V	Always available
GPIO2_IO20	P2-49*	IO	GPIO	3.3V	Always available
GPIO2_IO3	P2-59*	IO	GPIO	3.3V	Always available
GPIO2_IO4	P2-41*	IO	GPIO	3.3V	Always available
GPIO2_IO5	P2-43*	IO	GPIO	3.3V	Always available
GPIO3_IO19	P1-87*	IO	GPIO	3.3V	Always available
GPIO3_IO20	P1-89*	IO	GPIO	3.3V	Always available
GPIO3_IO21	P1-100*	IO	GPIO	3.3V	Always available
GPIO3_IO25	P1-96*	IO	GPIO	3.3V	Always available
GPIO3_IO26	P1-70*	IO	GPIO	3.3V	Always available
GPIO3_IO27	P1-63*	IO	GPIO	3.3V	Always available
GPIO3_IO28	P1-85*	IO	GPIO	3.3V	Always available
GPIO3_IO29	P1-92*	IO	GPIO	3.3V	Always available
GPIO4_IO10	P2-53*	IO	GPIO	3.3V	Always available
GPIO4_IO11	P2-55*	IO	GPIO	3.3V	Always available
GPIO4_IO12	P2-60*	IO	GPIO	3.3V	Always available
GPIO4_IO14	P2-63*	IO	GPIO	3.3V	Always available
GPIO4_IO15	P2-65*	IO	GPIO	3.3V	Always available
GPIO4_IO16	P2-67*	IO	GPIO	3.3V	Always available
GPIO4_IO17	P1-69*	IO	GPIO	3.3V	Always available
GPIO4_IO19	P1-60*	IO	GPIO	3.3V	Always available
GPIO4_IO20	P2-52*	IO	GPIO	3.3V	Always available
GPIO4_IO21	P2-88*	IO	GPIO	3.3V	Always available
GPIO4_IO22	P1-53*	IO	GPIO	3.3V	Always available
GPIO4_IO24	P2-76*	IO	GPIO	3.3V	Always available
GPIO4_IO25	P1-51*	IO	GPIO	3.3V	Always available
GPIO4_IO26	P1-33*	IO	GPIO	3.3V	Always available
GPIO4_IO27	P1-49*	IO	GPIO	3.3V	Always available
GPIO4_IO28	P1-34*	IO	GPIO	3.3V	Always available
GPIO4_IO29	P1-32*	IO	GPIO	3.3V	Always available

Signal Name	Pin #	Type	Description	Voltage Domain	Always available
GPIO4_IO30	P1-28*	IO	GPIO	3.3V	Always available
GPIO4_IO31	P1-38*	IO	GPIO	3.3V	Always available
GPIO4_IO8	P2-45*	IO	GPIO	3.3V	Always available
GPIO4_IO9	P2-47*	IO	GPIO	3.3V	Always available
GPIO5_IO0	P1-36*	IO	GPIO	3.3V	Always available
GPIO5_IO1	P1-26*	IO	GPIO	3.3V	Always available
GPIO5_IO10	P2-93*	IO	GPIO	3.3V	Always available
GPIO5_IO11	P2-95*	IO	GPIO	3.3V	Always available
GPIO5_IO12	P2-89*	IO	GPIO	3.3V	Always available
GPIO5_IO13	P2-91*	IO	GPIO	3.3V	Always available
GPIO5_IO18	P1-94*	IO	GPIO	3.3V	Always available
GPIO5_IO19	P1-91*	IO	GPIO	3.3V	Always available
GPIO5_IO2	P1-30*	IO	GPIO	3.3V	Always available
GPIO5_IO20	P2-90*	IO	GPIO	3.3V	Always available
GPIO5_IO22	P1-19*	IO	GPIO	3.3V	Always available
GPIO5_IO23	P1-72*	IO	GPIO	3.3V	Always available
GPIO5_IO24	P1-76*	IO	GPIO	3.3V	Always available
GPIO5_IO25	P1-74*	IO	GPIO	3.3V	Always available
GPIO5_IO26	P1-21*	IO	GPIO	3.3V	Always available
GPIO5_IO27	P1-61*	IO	GPIO	3.3V	Always available
GPIO5_IO28	P1-84*	IO	GPIO	3.3V	Always available
GPIO5_IO29	P1-86*	IO	GPIO	3.3V	Always available
GPIO5_IO3	P1-81*	IO	GPIO	3.3V	Always available
GPIO5_IO4	P1-79*	IO	GPIO	3.3V	Always available
GPIO5_IO5	P1-77*	IO	GPIO	3.3V	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

NOTE: 2.5V or 3.3V power must be supplied via the RGMII_VIO pin if any of the RGMII_VIO domain signals are used on the carrier-board

5 SYSTEM LOGIC

5.1 Power Supply

Table 37 Power signals

Signal Name	Connector #	Pin#	Type	Description
V_SOM	P1	11, 27, 43, 57, 69, 83	P	Main power supply. Connect to a regulated DC supply or Li-Ion battery
	P2	9, 19, 29, 39, 57, 71, 87		
VCC_RTC	P1	93	P	RTC back-up battery power input. Connect to a 3V coin-cell lithium battery. If RTC back-up is not required, connect this pin to GND.
GND	P1	4, 10, 20, 40, 54, 64, 78, 88	P	Common ground
	P2	10, 16, 22, 28, 34, 40, 46, 54, 72, 82		
RGMII_VIO	P1	55	P	RGMII interface power supply input. This pin must be connected to 2.5V or 3.3V power rail depending on the PHY requirements

5.2 System and Miscellaneous Signals

5.2.1 External regulator control and power management

UCM-iMX8M-Plus supports carrier board power supply control by means of two dedicated output signals. Both signals are derived from the i.MX8M Plus SoC. The logic that controls both signals is supplied by the i.MX8M Plus SoC SNVS power rail.

The PMIC_STBY_REQ output can be used to signal the carrier board power supply that UCM-iMX8M-Plus is in ‘standby’ or ‘OFF’ mode. Utilizing the external regulator control signals enables carrier board power management functionality.

Please refer to the i.MX8M Plus Reference manual for additional details. The table below summarizes the external regulator control signals.

Table 38 External regulator control signals

Signal Name	Pin #	Type	Description	Availability
PMIC_STBY_REQ	P1-66	O	When the processor enters SUSPEND mode, it will assert this signal.	Always available
PMIC_ON_REQ	P1-68	O	Active high power-up request output from i.MX8M Plus SoC.	Always available
PWRBTN	P2-64	I	Pulled-Up Active low ON/OFF signal (designed for an ONOFF switch).	Always available

5.3 Reset

SYS_RST_PMIC signal is the main system reset input. Driving a valid logic zero invokes a global reset that affects every module on UCM-iMX8M-Plus. Please refer to the i.MX8M Plus Reference manual for additional details.

Table 39 Reset signals

Signal Name	Pin #	Type	Description	Availability
SYS_RST_PMIC	P1-2	I	Active Low cold reset input signal. Should be used as main system reset	Always available

5.4 Boot Sequence

UCM-iMX8M-Plus boot sequence defines which interface/media is used by UCM-iMX8M-Plus to load and execute the initial software (such as SPL or/and U-boot). UCM-iMX8M-Plus can load initial software from the following interfaces/media:

- The on-board primary boot device (eMMC with pre-flashed boot-loader)
- An external SD card using the SD/SDIO 2 interface

UCM-iMX8M-Plus will query boot devices/interfaces for initial software in the order defined by the active boot sequence. A total of two different boot sequences are supported by UCM-iMX8M-Plus:

- Standard sequence: designed for normal system operation with the on-board primary boot device as the boot media.
- Alternate sequence: designed to allow recovery from an external boot device in case of data corruption of the on-board primary boot device. Using the alternate sequence allows UCM-iMX8M-Plus to boot from an external SD card, effectively bypassing the onboard eMMC.

The initial logic value of ALT_BOOT signal defines which of the supported boot sequences is used by the system.

Table 40 Alternative Boot selection signal

Signal Name	Pin #	Type	Description	Availability
ALT_BOOT	P1-90	I	Active high alternate boot sequence select input. Leave floating or tie low for standard boot sequence	Always available

Table 41 UCM-iMX8M-Plus Boot sequences

Sequence	ALT_BOOT	First
Standard	Low or floating	Onboard eMMC (primary boot storage)
Alternate	High	SD card on SD/SDIO2 interface

5.5 Signal Multiplexing Characteristics

Up to 80 of the UCM-iMX8M-Plus carrier board interface pins are multifunctional. Multifunctional pins enable extensive functional flexibility of the UCM-iMX8M-Plus CoM/SoM by allowing usage of a single carrier board interface pin for one of several functions. Up-to 6 functions (MUX modes) are accessible through each multifunctional carrier board interface pin. The multifunctional capabilities of UCM-iMX8M-Plus pins are derived from the i.MX8M Plus SoC control module

NOTE: Pin function selection is controlled by software.

NOTE: Each pin can be used for a single function at a time.

NOTE: Only one pin can be used for each function (in case a function is available on more than one carrier board interface pin).

NOTE: An empty MUX mode is a "RESERVED" function and must not be used.

Table 42 Multifunctional Signals

Pin #	SoC Pin Name	GPIO	SAI	ENET1	SDIO	I2C	UART	SPI	PWM	CAN	SPDIF	Availability
P1-19	UART1_RXD	GPIO5_IO22					UART1_RX	ECSPI3_SCLK				Always
P1-21	UART3_RXD	GPIO5_IO26					UART3_RX UART1_CTS_B			CAN2_TX		Always
P1-26	SAI3_TXD	GPIO5_IO1	SAI3_TXD0 SAI5_RXD3								SPDIF1_EXT_CLK	Always
P1-28	SAI3_RXD	GPIO4_IO30	SAI3_RXD0 SAI5_RXD0				UART2_RTS_B					Always
P1-30	SAI3_MCLK	GPIO5_IO2	SAI3_MCLK SAI5_MCLK						PWM4_OUT		SPDIF1_OUT	Always
P1-32	SAI3_RXC	GPIO4_IO29	SAI3_RXC SAI5_RXC				UART2_CTS_B					Always
P1-33	SAI2_TXD0	GPIO4_IO26	SAI5_TXD3							CAN2_TX		Always
P1-34	SAI3_RXFS	GPIO4_IO28	SAI3_RXFS SAI3_RXD1								SPDIF1_IN	Always
P1-36	SAI3_TXC	GPIO5_IO0	SAI3_TXC SAI5_RXD2				UART2_TX					Always
P1-38	SAI3_TXFS	GPIO4_IO31	SAI3_TXFX SAI5_RXD1 SAI3_TXD1				UART2_RX					Always
P1-49	SAI2_MCLK	GPIO4_IO27	SAI5_MCLK SAI3_MCLK							CAN2_RX		Always

P1-51	SAI2_TXC	GPIO4_IO25	SAI5_TXD2							CAN1_RX		Always
P1-53	SAI2_RXC	GPIO4_IO22	SAI5_TXC				UART1_RXD			CAN1_TX		Always
P1-59	GPIO1_IO00	GPIO1_IO0										Always
P1-60	SAI1_TXD7	GPIO4_IO19										Always
P1-61	UART3_TXD	GPIO5_IO27					UART3_TXD UART1_RTS_B			CAN2_RX		Always
P1-63	HDMI_DDC_SDA	GPIO3_IO27				I2C5_SDA				CAN1_RX		Always
P1-70	HDMI_DDC_SCL	GPIO3_IO26				I2C5_SCL				CAN1_TX		Always
P1-72	UART1_TXD	GPIO5_IO23					UART1_TXD	ECSPI3_MOSI				Always
P1-74	UART2_TXD	GPIO5_IO25					UART2_TXD	ECSPI3_SS0				Always
P1-76	UART2_RXD	GPIO5_IO24					UART2_RXD	ECSPI3_MISO				Always
P1-77	SPDIF_EXT_CLK	GPIO5_IO5							PWM1_OUT		SPDIF1_EXT_CLK	Always
P1-79	SPDIF_RX	GPIO5_IO4				I2C5_SDA			PWM2_OUT	CAN1_RX	SPDIF1_IN	Always
P1-81	SPDIF_TX	GPIO5_IO3				I2C5_SCL			PWM3_OUT	CAN1_TX	SPDIF1_OUT	Always
P1-84	UART4_RXD	GPIO5_IO28				I2C6_SCL	UART4_RXD UART2_CTS_B					Always
P1-85	HDMI_CEC	GPIO3_IO28				I2C6_SCL				CAN2_TX		
P1-86	UART4_TXD	GPIO5_IO29				I2C6_SDA	UART4_TXD UART2_RTS_B					Always
P1-87	SAI5_RXFS	GPIO3_IO19	SAI5_RXFS			I2C6_SCL			PWM4_OUT			Always
P1-89	SAI5_RXC	GPIO3_IO20	SAI5_RXC			I2C6_SDA			PWM3_OUT			Always
P1-91	I2C3_SDA	GPIO5_IO19				I2C3_SDA		ECSPI2_MOSI	PWM3_OUT			Always
P1-92	HDMI_HPD	GPIO3_IO29				I2C6_SDA				CAN2_RX		Always
P1-94	I2C3_SCL	GPIO5_IO18				I2C3_SCL		ECSPI2_SCLK	PWM4_OUT			Always
P1-96	SAI5_MCLK	GPIO3_IO25	SAI5_MCLK			I2C5_SDA			PWM1_OUT	CAN2_RX		Always
P1-98	GPIO1_IO01	GPIO1_IO1							PWM1_OUT			Always
P1-100	SAI5_RXD0	GPIO3_IO21	SAI5_RXD0			I2C5_SCL			PWM2_OUT			Always
P2-41	SD1_DATA2	GPIO2_IO4		ENET1_RGMII_RD0	SD1_DATA2	I2C4_SCL	UART2_TXD					Always
P2-43	SD1_DATA3	GPIO2_IO5		ENET1_RGMII_RD1	SD1_DATA3	I2C4_SDA	UART2_RXD					Always
P2-45	SAI1_RXD6	GPIO4_IO8		ENET1_RGMII_RD2								Always
P2-47	SAI1_RXD7	GPIO4_IO9		ENET1_RGMII_RD3								Always
P2-49	SD2_WP	GPIO2_IO20			SD2_WP							Always
P2-51	SD2_RESET_B	GPIO2_IO19			SD2_RESET_B							Always
P2-52	SAI1_MCLK	GPIO4_IO20	SAI5_MCLK									Always
P2-53	SAI1_TXFS	GPIO4_IO10	SAI5_TXFS	ENET1_RGMII_RX_CTL								Always
P2-55	SAI1_TXC	GPIO4_IO11	SAI5_TXC	ENET1_RGMII_RXC								Always

P2-59	SD1_DATA1	GPIO2_IO3		ENET1_RGMII_TD0	SD1_DATA1	I2C6_SDA	UART1_CTS_B					Always
P2-60	SAI1_TXD0	GPIO4_IO12	SAI5_TXD0	ENET1_RGMII_TD0								Always
P2-61	SD1_DATA0	GPIO2_IO2		ENET1_RGMII_TD1	SD1_DATA0	I2C6_SCL	UART1_RTS_B					Always
P2-62	SD1_RESET_B	GPIO2_IO10			SD1_RESET_B	I2C3_SCL	UART3_RTS_B					Always
P2-63	SAI1_TXD2	GPIO4_IO14	SAI5_TXD2	ENET1_RGMII_TD2								Always
P2-65	SAI1_TXD3	GPIO4_IO15	SAI5_TXD3	ENET1_RGMII_TD3								Always
P2-67	SAI1_TXD4	GPIO4_IO16		ENET1_RGMII_TX_CTL								Always
P2-68	SD1_CLK	GPIO2_IO0		ENET1_MDC	SD1_CLK	I2C5_SCL	UART1_TXD					Always
P2-69	SAI1_TXD5	GPIO4_IO17		ENET1_RGMII_TXC								Always
P2-70	SD1_CMD	GPIO2_IO1		ENET1_MDIO	SD1_CMD	I2C5_SDA	UART1_RXD					Always
P2-73	ENET_TD3	GPIO1_IO18										NOT “E”
P2-74	ENET_TX_CTL	GPIO1_IO22									SPDIF1_OUT	NOT “E”
P2-75	ENET_TD0	GPIO1_IO21										NOT “E”
P2-76	SAI2_TXFS	GPIO4_IO24	SAI5_TXD1				UART1_CTS_B					Always
P2-77	ENET_TD2	GPIO1_IO19										NOT “E”
P2-78	ENET_TD1	GPIO1_IO20										NOT “E”
P2-79	ENET_RX_CTL	GPIO1_IO24	SAI7_TXFS									NOT “E”
P2-80	ENET_RXC	GPIO1_IO25	SAI7_TXC									NOT “E”
P2-81	ENET_TXC	GPIO1_IO23	SAI7_TXD0									NOT “E”
P2-83	ENET_RD1	GPIO1_IO27	SAI7_RXFS									NOT “E”
P2-84	ENET_RD2	GPIO1_IO28	SAI7_RXC									NOT “E”
P2-85	ENET_RD3	GPIO1_IO29	SAI7_MCLK								SPDIF1_IN	NOT “E”
P2-86	ENET_RD0	GPIO1_IO26	SAI7_RXD0									NOT “E”
P2-88	SAI2_RXFS	GPIO4_IO21	SAI5_TXFS				UART1_TX					Always
P2-89	ECSPI2_MISO	GPIO5_IO12	SAI7_MCLK			I2C4_SCL	UART4_CTS_B	ECSPI2_MISO				Always
P2-90	I2C4_SCL	GPIO5_IO20				I2C4_SCL		ECSPI2_MISO	PWM2_OUT			Always
P2-91	ECSPI2_SS0	GPIO5_IO13				I2C4_SDA	UART4_RTS_B	ECSPI2_SS0				Always
P2-92	SD2_CD_B	GPIO2_IO12			SD2_CD_B							Always
P2-93	ECSPI2_SCLK	GPIO5_IO10	SAI7_TXC			I2C3_SCL	UART4_RXD	ECSPI2_SCLK				Always
P2-94	SD2_DATA2	GPIO2_IO17			SD2_DATA2			ECSPI2_SS0			SPDIF1_OUT	Always
P2-95	ECSPI2_MOSI	GPIO5_IO11	SAI7_TXD0			I2C3_SDA	UART4_TXD	ECSPI2_MOSI				Always
P2-96	SD2_CLK	GPIO2_IO13			SD2_CLK		UART4_RXD	ECSPI2_SCLK				Always
P2-97	SD2_DATA0	GPIO2_IO15			SD2_DATA0	I2C4_SDA	UART2_RXD					Always
P2-98	SD2_DATA3	GPIO2_IO18			SD2_DATA3			ECSPI2_MISO			SPDIF1_IN	Always
P2-99	SD2_DATA1	GPIO2_IO16			SD2_DATA1	I2C4_SCL	UART2_TXD					Always
P2-100	SD2_CMD	GPIO2_IO14			SD2_CMD		UART4_TXD	ECSPI2_MOSI				Always

5.6 RTC

UCM-iMX8M-Plus features an on-board ultra-low-power AM1805 real time clock (RTC). The RTC is connected to the i.MX8M SoC using I2C2 interface at address 0xD2/D3.

Back-up power supply is required in order to keep the RTC running and maintain clock and time information when main supply is not present.

For more information about UCM-iMX8M-Plus RTC please refer to the AM1805 datasheet.

5.7 LED

UCM-iMX8M-Plus features a single general purpose green LED controlled by GPIO1_IO[12] signal of the i.MX8M Plus. The LED is ON when GPIO1_IO[12] is logic LOW.

5.8 Reserved Signals

The following UCM-iMX8M-Plus signals are reserved and must be left unconnected.

Table 43 Reserved Signals

Connector #	Pin#
P1	95
P2	66

6 CARRIER BOARD INTERFACE

The UCM-iMX8M-Plus CoM/SoM carrier board interface uses 2 x 100 Pin carrier board connectors. The SoM pinout is detailed in the table below.

6.1 Connectors Pinout

Table 44 Connector P1

Pin #	UCM-iMX8M-Plus Signal Name	Ref.		Pin #	UCM-iMX8M-Plus Signal Name	Ref.
2	SYS_RST_PMIC			1	USB2_VBUS	
4	GND			3	USB2_DP	
6	USB1_RX_P			5	USB2_DN	
8	USB1_RX_N			7	USB2_RX_P	
10	GND			9	USB2_RX_N	
12	USB1_DP			11	V_SOM	
14	USB1_DN			13	USB2_TX_P	
16	USB1_TX_P			15	USB2_TX_N	
18	USB1_TX_N			17	RESERVED	
20	GND			19	UART1_RXD ECSPI3_SCLK GPIO5_IO22	
22	RESERVED			21	UART3_RXD UART1_CTS_B CAN2_TX GPIO5_IO26	
24	USB1_VBUS			23	HDMI_TXCP	
26	SAI3_TXD0 SAI5_RXD3 GPIO5_IO1			25	HDMI_TXCN	
28	SAI3_RXD0 SAI5_RXD0 UART2_RTS_B UART2_RTS_B GPIO4_IO30			27	V_SOM	
30	SAI3_MCLK SAI5_MCLK PWM4_OUT GPIO5_IO2			29	HDMI_TX0P	
32	SAI3_RXC SAI5_RXC UART2_CTS_B GPIO4_IO29			31	HDMI_TX0N	
34	SAI3_RXFS SAI5_RXFX SAI3_RXD1 GPIO4_IO28			33	SAI5_TXD3 CAN2_TX GPIO4_IO26	
36	SAI3_TXC SAI5_RXD2 UART2_TXD GPIO5_IO0			35	EARC_N_HPD	
38	SAI3_TXFS SAI5_RXD1 SAI3_TXD1 UART2_RXD GPIO4_IO31			37	EARC_P_UTIL	
40	GND			39	HDMI_TX1P	
42	LVDS0_D0_P			41	HDMI_TX1N	
44	LVDS0_D0_N			43	V_SOM	
46	LVDS0_D1_P			45	HDMI_TX2P	
48	LVDS0_D1_N			47	HDMI_TX2N	
50	LVDS0_D2_P			49	SAI3_MCLK CAN2_RX GPIO4_IO27	
52	LVDS0_D2_N			51	SAI5_TXD2 CAN1_RX GPIO4_IO25	

54	GND			53	SAI5_TXC UART1_RXD CAN1_TX GPIO4_IO22	
56	LVDS0_D3_P			55	PHY_2P5	
58	LVDS0_D3_N			57	V_SOM	
60	GPIO4_IO19			59	GPIO1_IO00	
62	AVDD33_ETH			61	UART3_TXD UART1_RTS_B CAN2_RX GPIO5_IO27	
64	GND			63	HDMI_DDC_SDA I2C5_SDA CAN1_RX GPIO3_IO27	
66	PMIC_STBY_REQ			65	JTAG_TMS	
68	PMIC_ON_REQ			67	JTAG_TDO	
70	HDMI_DDC_SCL I2C5_SCL CAN1_TX GPIO3_IO26			69	V_SOM	
72	UART1_TXD ECSPI3_MOSI GPIO5_IO23			71	JTAG_TDI	
74	UART2_TXD ECSPI3_SS0 GPIO5_IO25			73	JTAG_TCK	
76	UART2_RXD ECSPI3_MISO GPIO5_IO24			75	JTAG_MOD	
78	GND			77	SPDIF_EXT_CLK PWM1_OUT GPIO5_IO5	
80	LVDS0_CLK_P			79	SPDIF_RX I2C5_SDA PWM2_OUT CAN1_RX GPIO5_IO4	
82	LVDS0_CLK_N			81	SPDIF_TX I2C5_SCL PWM3_OUT CAN1_TX GPIO5_IO3	
84	UART4_RXD I2C6_SCL UART2_CTS_B GPIO5_IO28			83	V_SOM	
86	UART4_TXD I2C6_SDA UART2_RTS_B GPIO5_IO29			85	HDMI_CEC I2C6_SCL CAN2_TX GPIO3_IO28	
88	GND			87	SAI5_RXFS I2C6_SCL PWM4_OUT GPIO3_IO19	
90	ALT_BOOT			89	SAI5_RXC I2C6_SDA PWM3_OUT GPIO3_IO20	
92	HDMI_HPD I2C6_SDA CAN2_RX GPIO3_IO29			91	I2C3_SDA ECSPI2_MOSI PWM3_OUT GPIO5_IO19	
94	I2C3_SCL ECSPI2_SCLK PWM4_OUT GPIO5_IO18			93	VCC_RTC	
96	SAI5_MCLK I2C5_SDA PWM1_OUT CAN2_RX GPIO3_IO25			95	QSPI_BOOT_EN_3P3	
98	PWM1_OUT GPIO1_IO1			97	SYS_I2C_SDA	

100	SAI5_RXD0 I2C5_SCL PWM2_OUT GPIO3_IO21			99	SYS_I2C_SCL	

Table 45 Connector P2

Pin #	UCM-iMX8M-Plus Signal Name	Ref.		Pin #	UCM-iMX8M-Plus Signal Name	Ref.
2	MIPI_CSI1_CLK_N			1	MIPI_DSI1_D0_N	
4	MIPI_CSI1_CLK_P			3	MIPI_DSI1_D0_P	
6	MIPI_CSI1_D0_N			5	MIPI_DSI1_D2_N	
8	MIPI_CSI1_D0_P			7	MIPI_DSI1_D2_P	
10	GND			9	V_SOM	
12	MIPI_CSI2_CLK_N			11	MIPI_DSI1_D3_N	
14	MIPI_CSI2_CLK_P			13	MIPI_DSI1_D3_P	
16	GND			15	MIPI_DSI1_D1_N	
18	MIPI_CSI2_D0_N			17	MIPI_DSI1_D1_P	
20	MIPI_CSI2_D0_P			19	V_SOM	
22	GND			21	MIPI_DSI1_CLK_N	
24	MIPI_CSI2_D1_N			23	MIPI_DSI1_CLK_P	
26	MIPI_CSI2_D1_P			25	MIPI_CSI1_D2_N	
28	GND			27	MIPI_CSI1_D2_P	
30	PCIE_RXN_N			29	V_SOM	
32	PCIE_RXN_P			31	MIPI_CSI1_D1_N	
34	GND			33	MIPI_CSI1_D1_P	
36	PCIE_TXN_N			35	MIPI_CSI1_D3_N	
38	PCIE_TXN_P			37	MIPI_CSI1_D3_P	
40	GND			39	V_SOM	
42	PCIE_REF_CLKP			41	SD1_DATA2 I2C4_SCL UART2_TXD ENET1_RGMII_RD0 GPIO2_IO4	
44	PCIE_REF_CLKN			43	SD1_DATA3 I2C4_SDA UART2_RXD ENET1_RGMII_RD1 GPIO2_IO5	
46	GND			45	ENET1_RGMII_RD2 GPIO4_IO8	
48	MIPI_CSI2_D2_N			47	ENET1_RGMII_RD3 GPIO4_IO9	
50	MIPI_CSI2_D2_P			49	SD2_WP GPIO2_IO20	
52	SAI5_MCLK GPIO4_IO20			51	SD2_RESET_B GPIO2_IO19	
54	GND			53	SAI5_TXFS ENET1_RGMII_RX_CTL GPIO4_IO10	
56	MIPI_CSI2_D3_N			55	SAI5_TXC ENET1_RGMII_RXC GPIO4_IO11	
58	MIPI_CSI2_D3_P			57	V_SOM	
60	SAI5_TXD0 ENET1_RGMII_TD0 GPIO4_IO12			59	SD1_DATA1 I2C6_SDA UART1_CTS_B ENET1_RGMII_TD0 GPIO2_IO3	
62	SD1_RESET_B I2C3_SCL UART3_RTS_B GPIO2_IO10			61	SD1_DATA0 I2C6_SCL UART1_RTS_B ENET1_RGMII_TD1 GPIO2_IO2	
64	PWRBTN			63	SAI5_TXD2 ENET1_RGMII_TD2 GPIO4_IO14	
66	POR_B_3P3			65	SAI5_TXD3 ENET1_RGMII_TD3 GPIO4_IO15	

68	SD1_CLK I2C5_SCL UART1_TXD ENET_MDC GPIO2_IO0			67	ENET1_RGMII_TX_CTL GPIO4_IO16	
70	SD1_CMD I2C5_SDA UART1_RXD ENET_MDIO GPIO2_IO1			69	ENET1_RGMII_TXC GPIO4_IO17	
72	GND			71	V_SOM	
74	ETH0_MDI0P ENET_TX_CTL GPIO1_IO22			73	ETH0_MDI0N ENET_TD3 GPIO1_IO18	
76	SAI5_TXD1 UART1_CTS_B GPIO4_IO24			75	ETH0_LINK-LED_1000 ENET_TD0 GPIO1_IO21	
78	ETH0_MDI1P ENET_TD1 GPIO1_IO20			77	ENET_TD2 GPIO1_IO19	
80	ETH0_MDI1N ENET_RXC SAI7_TXC GPIO1_IO25			79	ETH0_MDI2P ENET_RX_CTL SAI7_TX_SYNC GPIO1_IO24	
82	GND			81	ETH0_MDI2N ENET_TXC SAI7_TXD0 GPIO1_IO23	
84	ETH0_MDI3P ENET_RD2 SAI7_RXC GPIO1_IO28			83	ETH0_LED_ACT ENET_RD1 SAI7_RXFS GPIO1_IO27	
86	ETH0_LINK-LED_10_100 ENET_RD0 SAI7_RXD0 GPIO1_IO26			85	ETH0_MDI3N ENET_RD3 SAI7_MCLK GPIO1_IO29	
88	SAI5_TXFS SAI5_TXD1 UART1_TXD GPIO4_IO21			87	V_SOM	
90	I2C4_SCL ECSPI2_MISO PWM2_OUT PCIE_CLKREQ_B GPIO5_IO20			89	ECSPI2_MISO SAI7_MCLK I2C4_SCL UART4_CTS_B GPIO5_IO12	
92	SD2_CD_B GPIO2_IO12			91	ECSPI2_SS0 I2C4_SDA UART4_RTS_B GPIO5_IO13	
94	SD2_DATA2 ECSPI2_SS0 GPIO2_IO17			93	ECSPI2_SCLK SAI7_TXC I2C3_SCL UART4_RXD GPIO5_IO10	
96	SD2_CLK UART4_RXD ECSPI2_SCLK GPIO2_IO13			95	ECSPI2_MOSI SAI7_TXD0 I2C3_SDA UART4_TXD GPIO5_IO11	
98	SD2_DATA3 ECSPI2_MISO GPIO2_IO18			97	SD2_DATA0 I2C4_SDA UART2_RXD GPIO2_IO15	
100	SD2_CMD UART4_TXD ECSPI2_MOSI GPIO2_IO14			99	SD2_DATA1 I2C4_SCL UART2_TXD GPIO2_IO16	

6.2 Mating Connectors

Table 46 Connector type

UCM-iMX8M-Plus connector		Carrier board (mating) connector P/N	
Ref.	Implementation	Mfg.	P/N
P1, P2	Hirose DF40C-100DP-0.4V51	Hirose	DF40HC(3.0)-100DS-0.4V(51)

6.3 Mechanical Drawings

Figure 3 UCM-iMX8M-Plus top

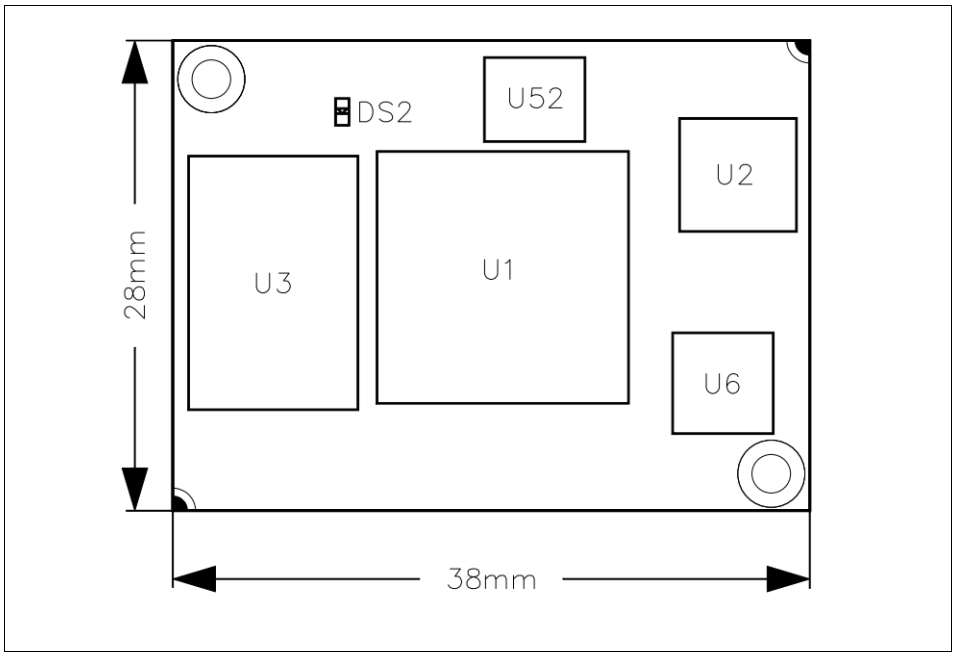
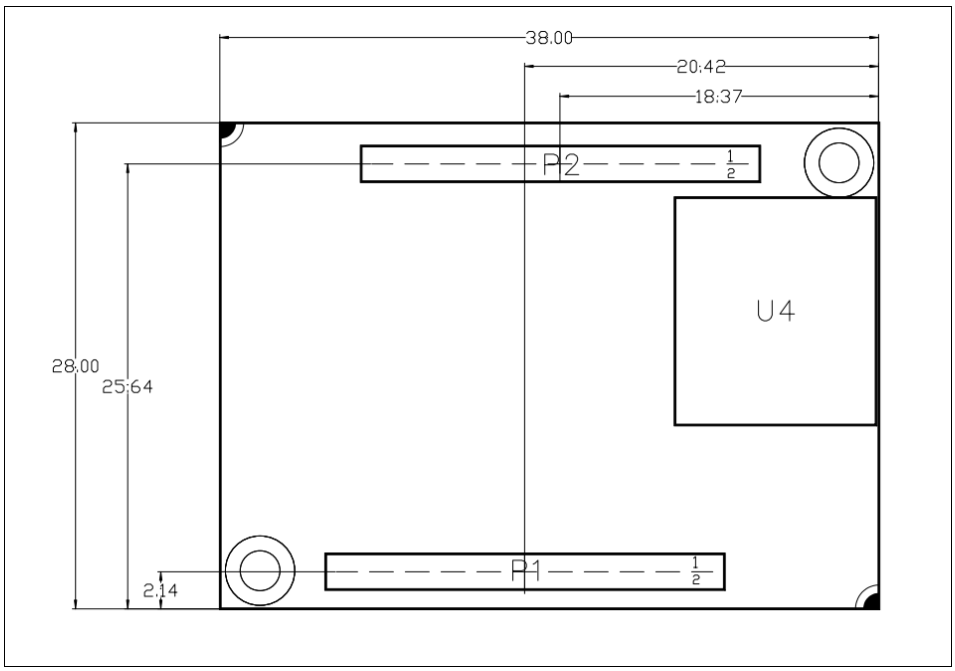


Figure 4 UCM-iMX8M-Plus bottom



1. All dimensions are in millimeters.
2. The height of all components is < 2.0mm.

3. Baseboard connectors provide 3 ± 0.15mm board-to-board clearance.
4. Board thickness is 1.6mm.
3D model and mechanical drawings in DXF format are available at
https://www.compulab.com/products/computer-on-modules/UCM-iMX8M-Plus-nxp-i-mx-8m-mini-som-system-on-module-computer/#devres

7 OPERATIONAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 47 Absolute Maximum ratings

Parameter	Min	Max	Unit
Main power supply voltage (V_SOM)	-0.3	4.8	V
Voltage on any non-power supply pin	-0.5	3.6	V
Backup battery supply voltage (VCC_RTC)	-0.3	3.8	V

NOTE: Exceeding the absolute maximum ratings may damage the device.

7.2 Recommended Operating Conditions

Table 48 Recommended Operating Conditions

Parameter	Min	Typ.	Max	Unit
Main power supply voltage (V_SOM)	3.45	3.7	4.4	V
Backup battery supply voltage (VCC_RTC)	1.5	3.0	3.6	V

7.3 Typical Power Consumption

Power consumption details will be added in a future version of this document.

Table 49 RTC timekeeping current

Use case	Use case description	I_{VCC_RTC}
RTC only	VCC_RTC (3.0V) is supplied from external coin-cell battery V_SOM is not present	70nA

7.4 ESD Performance

Table 50 ESD Performance

Interface	ESD Performance
i.MX8M Plus pins	2kV Human Body Model (HBM), 500V Charge Device Model (CDM)

8 APPLICATION NOTES

8.1 Carrier Board Design Guidelines

- Ensure that all V_SOM and GND power pins are connected.
- Major power rails - V_SOM and GND must be implemented by planes, rather than traces. Using at least two planes is essential to ensure the system signal quality because the planes provide a current return path for all interface signals.
- It is recommended to put several 10/100uF capacitors between V_SOM and GND near the mating connectors.
- Except for a power connection, no other connection is mandatory for UCM-iMX8M-Plus operation. All power-up circuitry and all required pullups/pulldowns are available onboard UCM-iMX8M-Plus.
- If for some reason you decide to place an external pullup or pulldown resistor on a certain signal (for example - on the GPIOs), first check the documentation of that signal provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation. For details please refer to section **Error! Reference source not found.**.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
  - PCIe, Ethernet, USB and more signals must be routed in differential pairs and by a controlled impedance trace.
  - Audio input must be decoupled from possible sources of carrier board noise.
- The following interfaces should meet the differential impedance requirements with manufacturer tolerance of 10%:
  - USB2.0: DP/DM signals require 90 ohm differential impedance.
  - All single-ended signals require 50 ohm impedance.
  - PCIe TX/RX data pairs and PCIe clocks require 85 ohm differential impedance.
  - Ethernet, MIPI-CSI and MIPI-DSI signals require 100 ohm differential impedance.
- The carrier board interface connectors provide 3mm mating height. Bear in mind that there are components on the bottom side of UCM-iMX8M-Plus. It is not recommended to place any components underneath the UCM-iMX8M-Plus module.
- Refer to the SB-UCMIMX8PLUS carrier board reference design schematics.
- It is recommended to send the schematics of the custom carrier board to Compulab support team for review.

8.2 Carrier Board Troubleshooting

- Using grease solvent and a soft brush, clean the contacts of the mating connectors of both the module and the carrier board. Remnants of soldering paste can prevent proper contact. Take care to let the connectors and the module dry entirely before re-applying power – otherwise, corrosion may occur.
- Using an oscilloscope, check the voltage levels and quality of the V_SOM power supply. It should be as specified in section 7.2. Check that there is no excessive ripple or glitches. First, perform the measurements without plugging in the module. Then plug in the module and measure again. Measurement should be performed on the pins of the mating connector.
- Using an oscilloscope, verify that the GND pins of the mating connector are indeed at zero voltage level and that there is no ground bouncing. The module must be plugged in during the test.

- Create a "minimum system" - only power, mating connectors, the module and a serial interface.
- Check if the system starts properly. In system larger than the minimum, possible sources of disturbance could be:
- Devices improperly driving the local bus
- External pullup/pulldown resistors overriding the module on-board values, or any other component creating the same "overriding" effect
- Faulty power supply
- In order to avoid possible sources of disturbance, it is strongly recommended to start with a minimal system and then to add/activate off-board devices one by one.
- Check for the existence of soldering shorts between pins of mating connectors. Even if the signals are not used on the carrier board, shorting them on the connectors can disable the module operation. An initial check can be performed using a microscope. However, if microscope inspection finds nothing, it is advisable to check using an X-ray, because often solder bridges are deep beneath the connector body. Note that solder shorts are the most probable factor to prevent a module from booting.
- Check possible signal short circuits due to errors in carrier board PCB design or assembly.
- Improper functioning of a customer carrier board can accidentally delete boot-up code from UCM-iMX8M-Plus, or even damage the module hardware permanently. Before every new attempt of activation, check that your module is still functional with CompuLab SB-UCMIMX8PLUS carrier board.
- It is recommended to assemble more than one carrier board for prototyping, in order to ease resolution of problems related to specific board assembly.