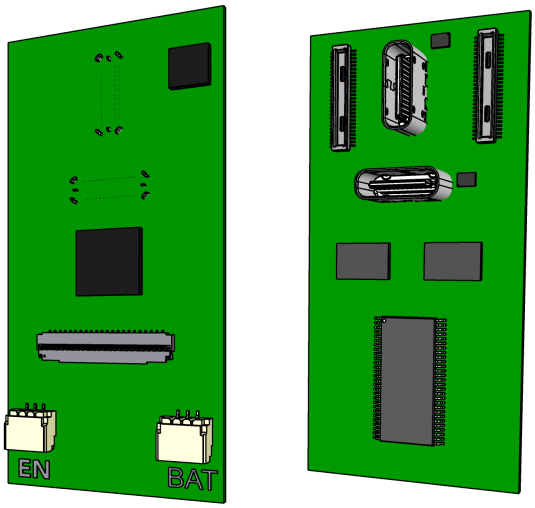
292 Power Module

The power module provides VSOM power to the Faceboard and routes data signals from the Faceboard through two USB plugs. A set of plugs are front facing and another set is back facing. Only one set can be used at a time.

The Power Module has specific power and data functions

- Supply the system with VSOM power(LiPo voltage range)
- Receive(sink role) power from OTG USB-C connector or a LiPo battery
- No need receiving(sink role) of power from Host USB-C for now
- Deliver max. 900mA to devices on Host USB, typically 200mA
- No power delivery(source role) on OTG USB
- Charge the connected LiPo battery
- Provide Alt. Mode support on Host USB port while powered
- Provide data signals from the Faceboard in the system over two USB-C connectors
- Manage autonomous system functions and waking state in collaboration with MSP430 MCU on faceboard

The Power Module exposes two vertical USB-C sockets and connects to the carrier/face board through two 50 pin B2B connectors. A 45 pin connector is used to experiment with Alt. Mode over the Host USB connector. The signal voltage on the board is 3.3V. The board can be laid out as 4 layer or 6 layer as needed.



Components

- 2 * 50 pin connectors Hirose DF40-50DP-0.4V mated height 1.5mm Mouser
- 4 * Hirose USB-C CX80B1-24P

- 1 * TPS65988 Dual Port USB Type-C® and USB PD Controller, Power Switch, and High-Speed Multiplexer. Mouser
- 1 * W25X40CLSNIG NOR-Flash spiFlash, 4M-bit, 4Kb Uniform Sector - Mouser - In stock
- 1 * BQ24250RGER battery charger $2 JLCPCB (4x4 mm package) Mouser
- 1 * 3 pin JST SH socket SM03B-SRSS-TB - JLCPCB - Farnell (Matched by JST PHR-3)
- 1 * 3 pin JST ACH socket BM03B
- 2 * TE Connectivity 45PIN 0.3MM 571-4-2328724-5 FPC 3-2328724-5 $0.41
- 2 * TPD6S300ARUKR ESD protection for USB-C port HD3SS3220IRNHT) WQFN (RNH) | 30 pin 250 tray Mouser
- 2 * TUSB546 Alt. Mode switch
- 2 * TS5USBC410 Dual 2:1 USB 2.0 Mux/DeMux Switch. Mouser
- Smaller JST connector for buttons to avoid plugging battery in wrong.

Board

50 mm x 24 mm (height x width)

The two 50 pin connectors are placed with a gap of 16 mm between their midpoint. These two connectors are vertically centered on the center of the vertical USB-C connector. The placement of these 4 connectors in the PCB design must not be changed as other designs depend on them. If needed they can be rotated 180deg, but it will result in several design documents needing revision.

Components on the underside can be max 1.2mm thick. The expected DF40 socket the board inserts into creates 1.5mm clearing height.

A half hole(like M.2 modules) should be added at the end of the board between the two 3 pin connectors.

Outstanding work

- Wire TSP65988 I2C address
- Voltage regulators
- Half hole between connectors
- BQ24250 inductor and resistor choices
- BQ24250 LED with modest light level
- Temp. sensor spec requirements added in this document
- Review connector selection (should be different to avoid insert mistakes)
- Verify PD Controller doesn't need external power path for our requirements
- Check CC/BC 1.2 routing
- Check HDMI HPD signal routing
- Ensure there is sufficient ESD components
- Reference diagrams have been pasted as images to help revision
- Ensuring components used are in general stock
- Component placement
- Routing
- Updating GitHub KiCAD lib with any changes to symbols/footprints/3dshapes

Review

- More ground pins on connectors. VSOM pins should have the same effect as ground pins for isolating high speed signals.
- I2C SOM pull up resistors: I would add the pull up resistors on the base board where the SOM is placed.
- BAT_STAT/STAT on 50 pin connectors are mainly for test setups, but yes any LED on the base board must be carefully designed.
- Could VCC_RTC be driven directly off the LiPo and downregulated to 3V3. VCC_RTC is intended for the SOM. It must be 1.5V - 3.0 V. At 3V3 it could be used to drive low power MCUs for system supervision during deep sleep.
- IN operating voltage. I imagine limiting voltage in TPS65988 firmware.
- TUSB456 is spec'd to consume 335mW for USB communication. USB would mostly be
- PP_CABLE: see the requirements for Sink/Source. Can external paths be reduced from the reference schema? Assuming a different config is uploaded to TPS65988
- What is OTG 2.0 fault for? Signals can be connected to TSP65988. One line is already connected to GPIO3, another could be to GPIO0. The two USB connectors have dedicated roles of acting as a device and a host. Is it only relevant for one of them?
- Connecting the two D+ and D- pins together is meant to be done with a USB 2.0 switch to allow passing two lines per connector.

Refs

- i.MX8M processor pins pull-up /down configuration
- I2C Bus Pullup Resistor Calculation

I2C Bus

The board has 3 I2C busses. SYS, Stem and Power. Key chipsets on the board are on the Power bus, which by default is bridged onto the SYS I2C, so the two must take care to not clash on addresses.

Chips on the Power I2C bus

- TPS65988 PD Controller
- BQ24250 LiPo Charger
- TUSB546 Alt Mode Control
- USB 2.0 switches

PD Controller I2C

The TPS PD Controller can be accessed and master various I2C busses. I2C1 connects to STEM as slave or master. I2C2 is a slave on SYS, allowing an API to be exposed to the i.MX8 CPU. I2C3 is on the POWER I2C bus, so it can master the other chips on the T-USB power board. The PD Controller firmware can be patched over I2C, or the flash can be written to directly via the 50 pin connector while the board is otherwise not powered or the PD Ctrl is kept in a shut down state.

By default the chipsets can be controlled by Linux Device Driver Bindings(on i.MX SoM) via the SYS I2C. The future direction is to control them by the local MSP430 MCU, which exposes information in the STEM I2C bus.

SYS I2C

The System I2C bus is mastered by the SoM whenever it is operating. The SoM has a M7 core that runs awareness routines while the system is resting. This means it can in principle be operating at all times. The Awareness MCUs make themselves available on the bus. To find other MCUs the addresses 0x200 to 0x20F are scanned. It connects to PD Controller I2C #2, which is always a slave.

Stem I2C

The Stem I2C bus is multi-master shared by listening on the I2C bus before claiming it. It connects to PD Controller I2C #1, which is either master or slave. To find other MCUs the addresses 0x200 to 0x20F are scanned. The master will be one of the Awareness MCUs that keep the system running under the covers and updates the awareness state. Sensors such as Ambient Light/Sound and Motion are accessed on the Stem. LED patterns are also controlled by Stem I2C. By default 3V3.

Day I2C

The SoM controls the Daytime camera module with range sensor via the Day I2C5 bus. MCUs do not access this bus. By default 1V8. The sensors on the bus are on camera modules.

Night I2C

The SoM controls the Nightime camera module with ambient sensor via the Night I2C6 bus while the system is awake. When resting MCUs are responsible for monitoring the visual environment by using Night I2C sensors. If the Night Camera Module has an MCU the T-USB MCU will assume that it will do the monitoring. By default 1V8. The sensors on the bus are on camera modules.

Power I2C

This bus is internal to the T-USB Power board. It can optionally be connected to the SYS I2C. It connects to PD Controller I2C #3, which is always a master.

SYS I2C addresses

Reduced the devices connected to SYS bus

Address	Chipset	Description
0x20	PCA9555	16 bit expander EX0
0x25	PCA9450	Reserved 7 bit address
0x38	TPS65988	On chips USB Port 1 with default address
0x3F	TPS65988	On chips USB Port 2 with default address
0x4A 0x4B	PCA9450	Power Management IC
0x68	PI6CG18200	PCIe clock generator
0xD2/D3	RTC	AM1805 real time clock (RTC)

POWER I2C adresses which may be exposed to SYS I2C. When not they are exclusively mastered by the PD Controller I2C3.

Address	Chipset	Description
0x0F	TUSB546	OTG Alt. Mode
0x47	TUSB546	Host Alt. Mode
0x67	HD3SS3220	OTG USB C orientation and PD Controller
0x6A	BQ24250	LiPO Battery Charger

1st Music Sculpture

GPIO exposed to SoM

- TPS65988 nINT
- TPS65988 USB-C endpoint?
- BQ24250 INT
- TUSB546 ?

USB-C state change interrupt?

Device Tree

device tree bindings for

- TPS65988. A variant of this controller known as Apple CD321x or Apple ACE is also present on hardware with Apple SoCs such as the M1.
- BQ24250

Linux kernel support

- BQ24250
- TPS65988 Linux
- BQ2425x Linux
- Linux Getting Driver For USB Type-C DisplayPort Alternate Mode
- API for USB Type-C Alternate Mode drivers

TPS65988

Interrupt pin = SYS_EX_nINT

```
    i2c0 {
        #address-cells = <1>;
        #size-cells = <0>;

        tps6598x: tps6598x@38 {
            compatible = "ti,tps6598x";
            reg = <0x38>;

            interrupt-parent = <&msmgpio>;
            interrupts = <107 IRQ_TYPE_LEVEL_LOW>;
            interrupt-names = "irq";
```

```
            pinctrl-names = "default";
            pinctrl-0 = <&typec_pins>;

            //
https://code.googlesource.com/linux/torvalds/linux/+/942cb357ae7d9249088e3
687ee6a00ed2745a0c7/Documentation/devicetree/bindings/connector/usb-
connector.yaml
            typec_con: connector {
                compatible = "usb-c-connector";
                label = "USB-C";
                port {
                    typec_ep: endpoint {
                        remote-endpoint = <&otg_ep>;
                    };
                };
            };
        };
    };
```

BQ24250

See Bindings

```
config CHARGER_BQ24257
    tristate "TI BQ24250/24251/24257 battery charger driver"
    depends on I2C
    depends on GPIOLIB || COMPILE_TEST
    select REGMAP_I2C
    help
      Say Y to enable support for the TI BQ24250, BQ24251, and BQ24257
battery
      chargers.
```

```
bq24250 {
    compatible = "ti,bq24250";
    reg = <0x6a>;
    interrupt-parent = <&gpio1>;
    interrupts = <16 IRQ_TYPE_EDGE_BOTH>;

    ti,battery-regulation-voltage = <4200000>;
    ti,charge-current = <500000>;
    ti,termination-current = <50000>;
    ti,current-limit = <900000>;
    ti,ovp-voltage = <9500000>;
    ti,in-dpm-voltage = <4440000>;
};
```

HD3SS3220

See Linux Documentation

Power

One key role of the board is to deliver power to the main board/faceboard that it slots into. It delivers VSOM to an i.MX 8 system module and 3V3 for always on chipsets such as MCP430, sensors and a stereo camera subsystem. When the overall system is in resting state the system module is in a suspended state, potentially with the low power core running, or VSOM may be completely switched off. The sensors and camera subsystem must hower run in order to determine when to wake up from the resting state.

The connected LiPo battery would have multiple options. One would be a lightweight option such as a single NCR18650. Another options might be a 125054 pack with 4000mAh. A heavy duty option would be made by combining two or three balanced cells in parallel to reach 10000mAh. Resistors should be chosen for common temperature sensor, and the details provided as a correction to this document. The chosen battery pack might have to be modified to add a temperature sensor.

The ability for the USB connectors to act as Power Sink and Power Source is essential so the engineering review must consider how to provide at least 1A sinking and sourcing by CC/PD negotiation or setting I2C registers. It is acceptable to only allow one port to sink and one port to source at a time.

USB DRP means dual-role power.

Provided Power

VSOM is 3.45V to 4.4V regardless of USB VBUS supply supported. VSOM is primarily used to power an UCM-iMX8M-Plus module. In the initial design VSOM is always supported directly from the LiPo BQ module. In the future a FET may be added to allow switching off VSOM while still supplying other voltage lines.

5V supplies a minimal current(perhaps 100mA) to support signalling LED and LED matrix chip along with an HDMI socket used for development. Logic will be added eventually to switch the delivery of 5V on/off.

3V3 supplies a limited current(up to 250mA) to support sensors and the camera subsystem connected to the main/faceboard which must be able to run even when the overall system is resting. The only case for switching off this supply is in a very low battery situation.

PWR_CHARGE and BAT_LDO is provided over the 50 pin connectors to allow board functionality verification and will not be used under normal operating conditions.

Internal Power

TPS65988 LDO_3V3(PD) provides up to 25mA to drive the SPI flash and other essential circuits: LIVE_3V3 is downregulated from LiPo BQ SYS

LDO_3V3 budget:

- Flash 15mA

LIVE_3V3 budget:

- TUSB456 2 * 250mA

- Exposed power on 50 pin PD Ctrl connector 500mA

LIVE_5V budget:

- HDMI 50mA
- LED matrix 200mA (10 fully lit LEDs at a time)

BQ25240 LDO(LiPo) provides up to 50mA, 4.9V for temp/LED.

VCONN on PPx_CABLE input is needed to support alternate mode negotiation over CC pins.

PD Control signals

Apparently the communication over CC pins is the new way. The previous BC 1.2 approach requires communication over USB 2.0 pins. The PD Controller supports both. BC 1.2 is supported by connecting it to OTG and Host D+/D- lines along with the connection to the 50 pin connector.

- Can you do type-C USB DRP, UFP data, sourcing device with CC controller only?

USB 2.0/3.0 data

The default connection of USB signals is that:

- USB1 3.0 goes from the High-Speed 50 pin connector to the OTG Type-C connector.
- USB2 3.0 goes from the High-Speed 50 pin connector to the Host Type-C connector.
- USB1 2.0 goes from the PD Ctrl 50 pin connector to the OTG Type-C connector.
- USB2 2.0 goes from the PD Ctrl 50 pin connector to the Host Type-C connector.
- BC 1.2 signals are combined with the USB1 and USB2 2.0 signals and passed to the Type-C connectors.

Alt. Mode signals

Alternate Data flows are controlled by the PD Controller or an External Controller via the PD Ctrl 50 pin connector.

- Alternate signals route from the 45 pin connector over the TUSBC546 chipset and then Host Type-C connector
- Alternate high speed signals are not currently supported for the OTG connector
- Type-C Alt. Mode is managed over Power I2C
- A second USB 2.0 signal can be routed from the PD Ctrl 50 pin connector over the B side of the Type-C connectors

Type-C Alt. Mode is meant to be implemented using addidtional chipsets connected via the 45 pin connector

Consider msg trail eDP over Type-C: CM4

- SN65DSI86 Dual-channel MIPI® DSI to embedded DisplayPort™ (eDP) bridge with Linux Kernel Driver
- CYPD3120: HDMI over Type-C (No Display Port)