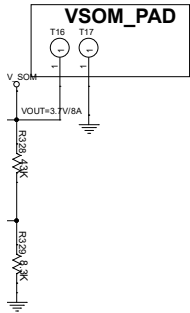
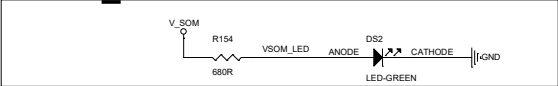


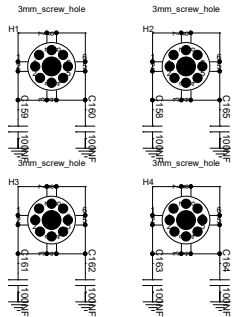
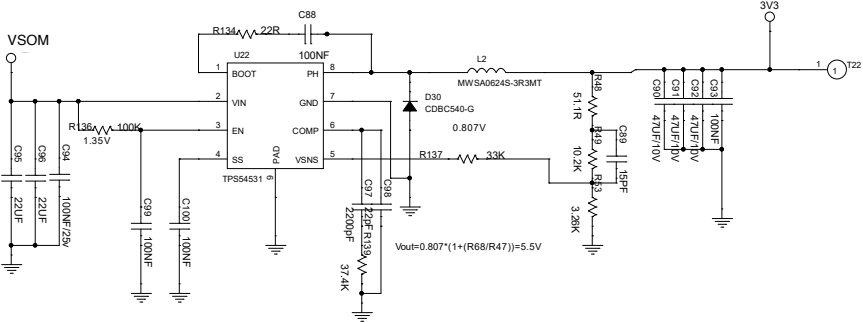
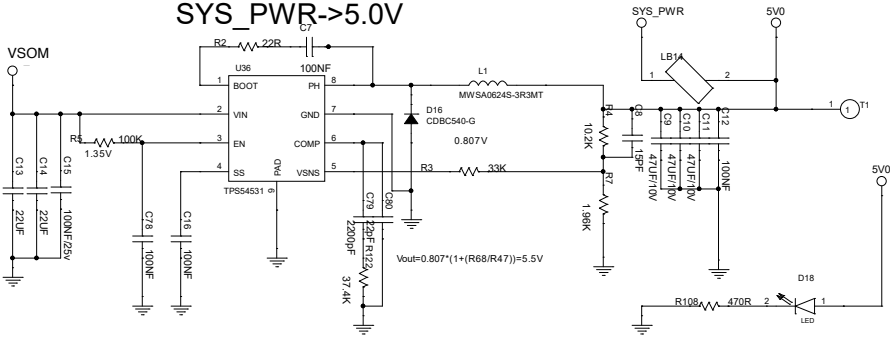
Power Supply1



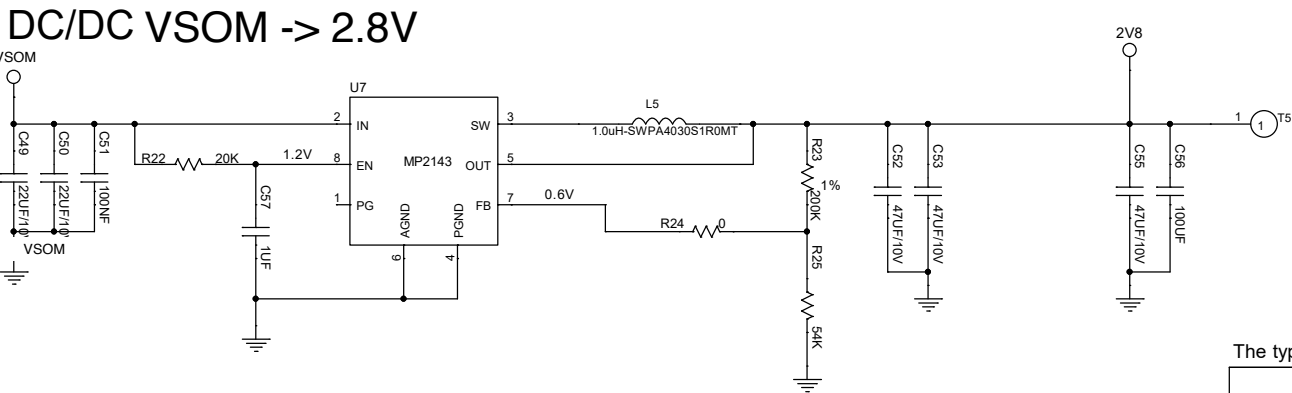
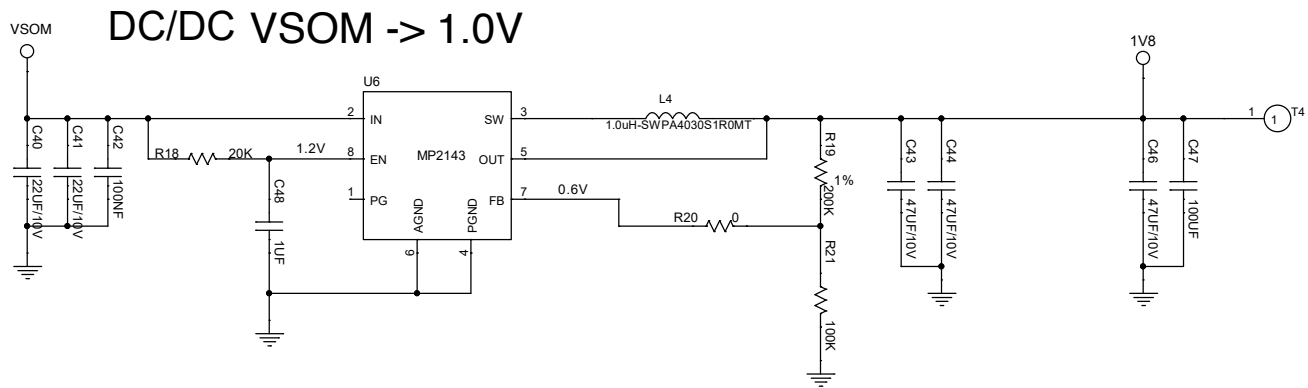
Power_LED



SYS_PWR->5.0V



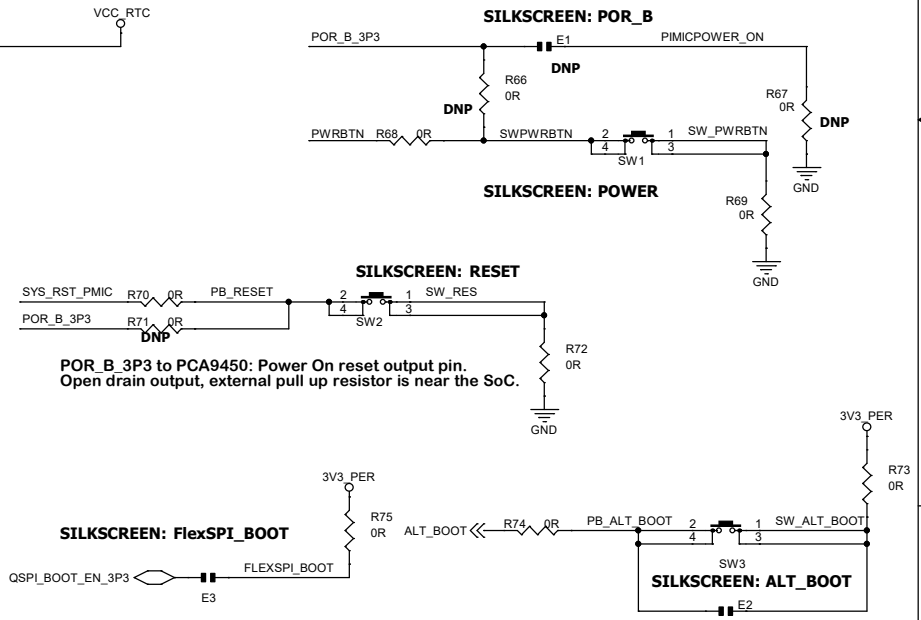
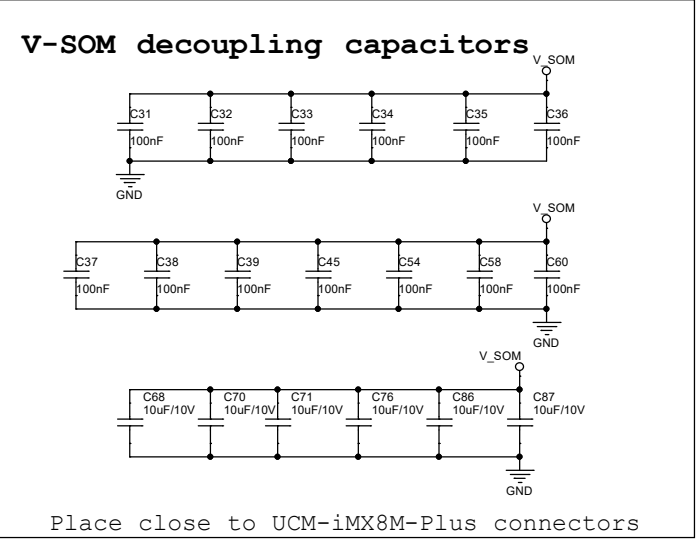
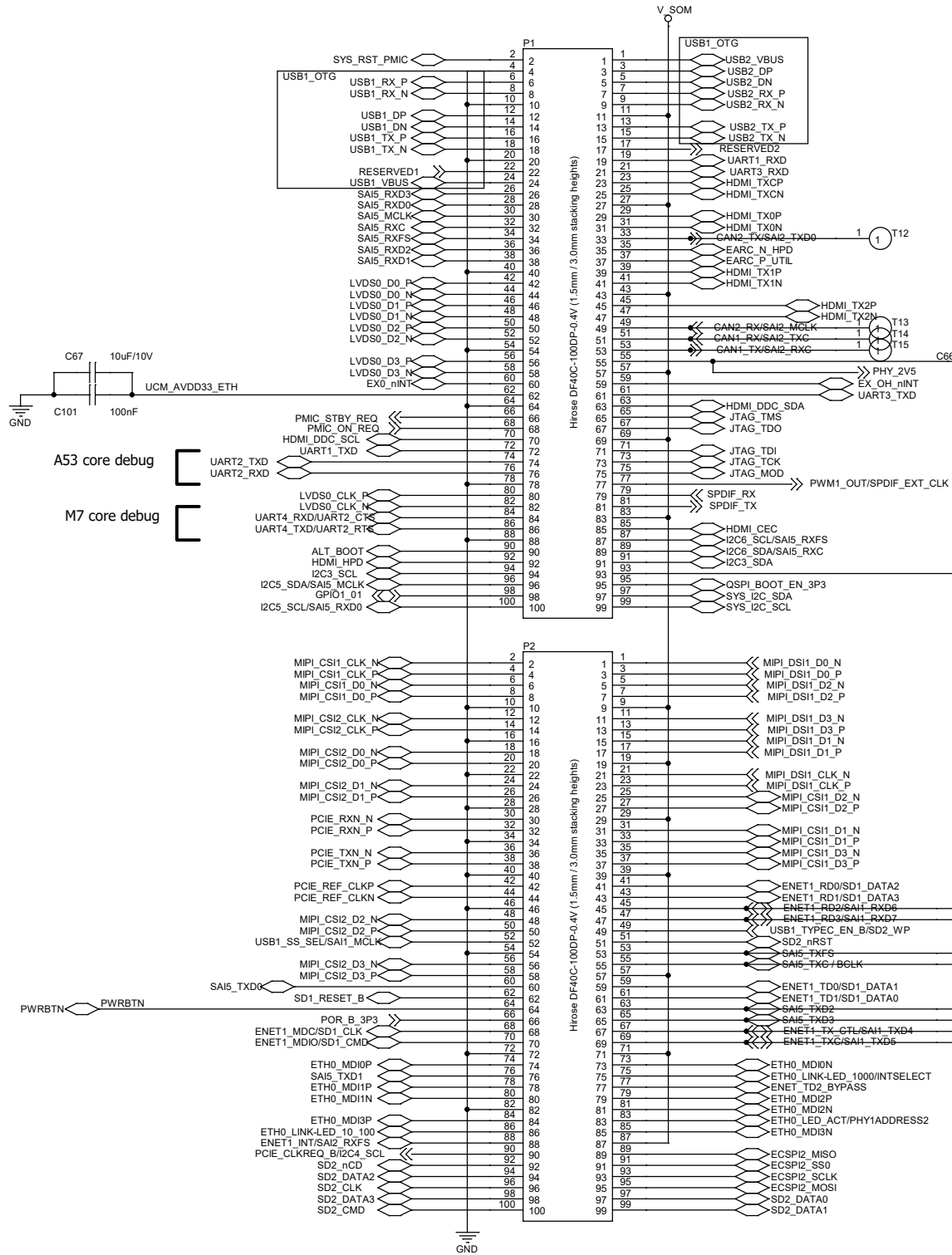
Power Supply2



The type and specification of the components refer to the BOM

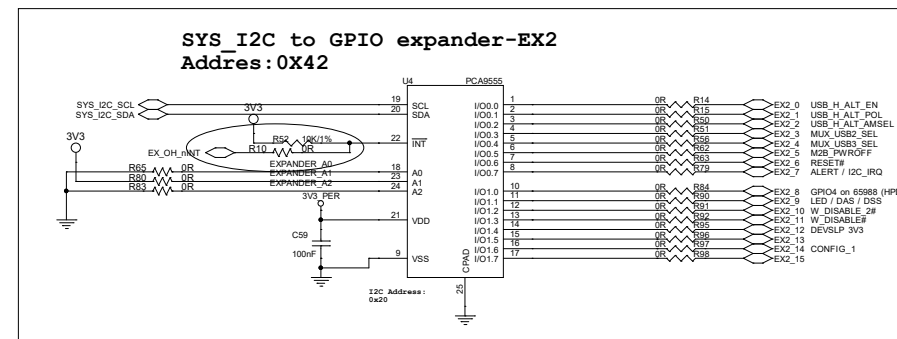
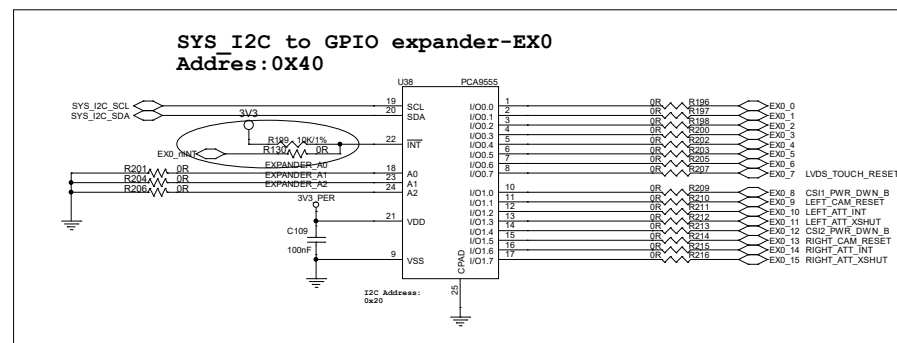
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DESIGNED	XKC20201222	CM4 MODE			
REVIEWED	XKC				
		VER	PART_NUMBER	SHEET 7 OF 34	
		B			

[illegible][illegible]



The type and specification of the components refer to the BOM

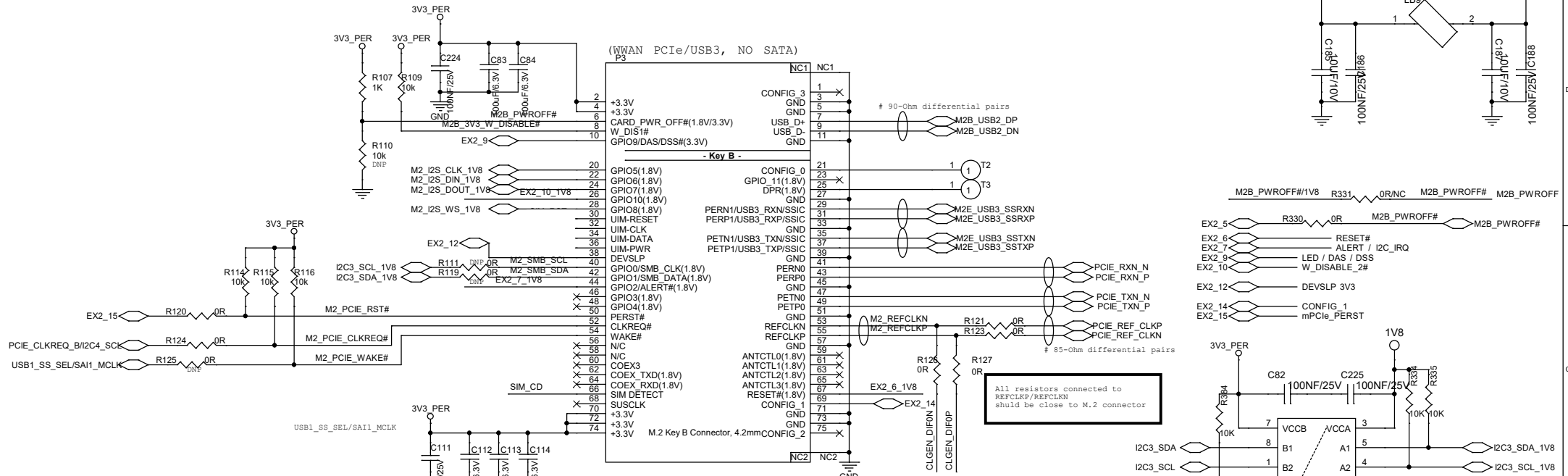
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REVIEWED	XKC			B		



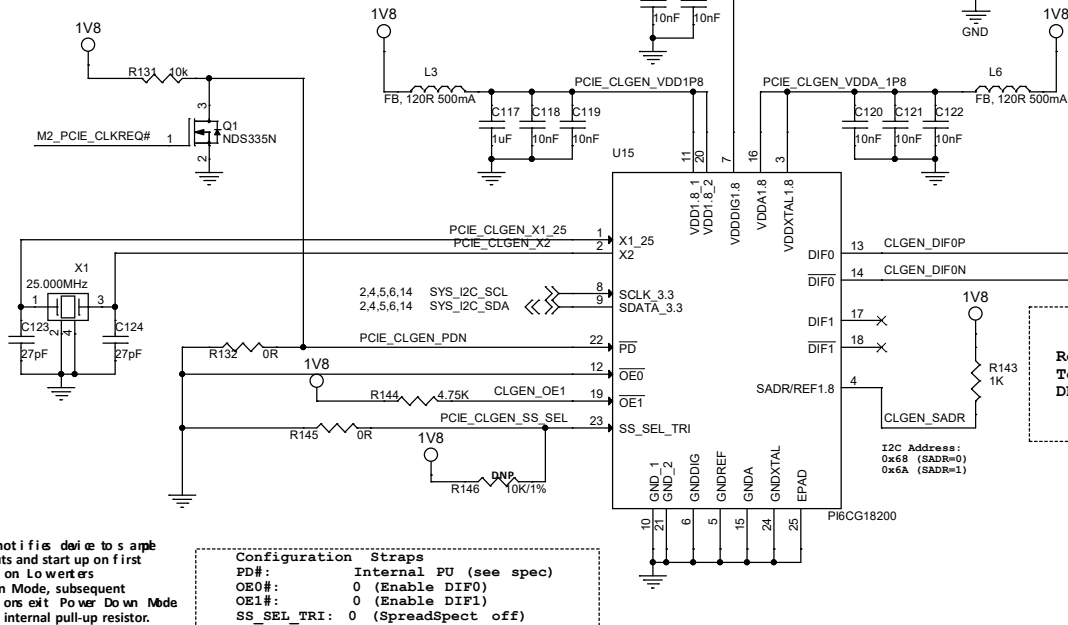
The type and specification of the components refer to the BOM

				NA			
				ECA NO		DATE	
DESIGNED	XKC20201222	CM4 MODE					
REVIEWED	XKC						
		VER	PART NUMBER	SHEET 9 OF 34			
		B					

M.2 Socket - Key B

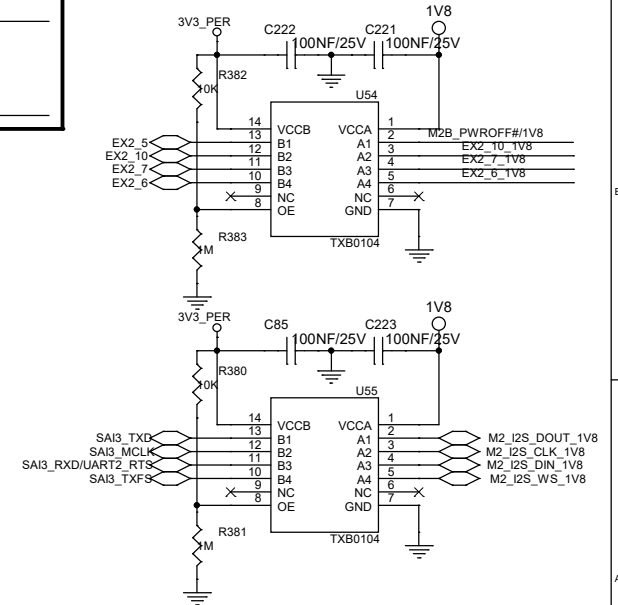
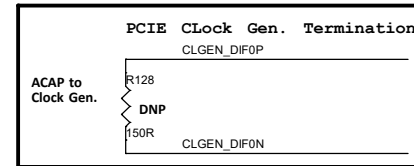


PCIe clock generator - DNP

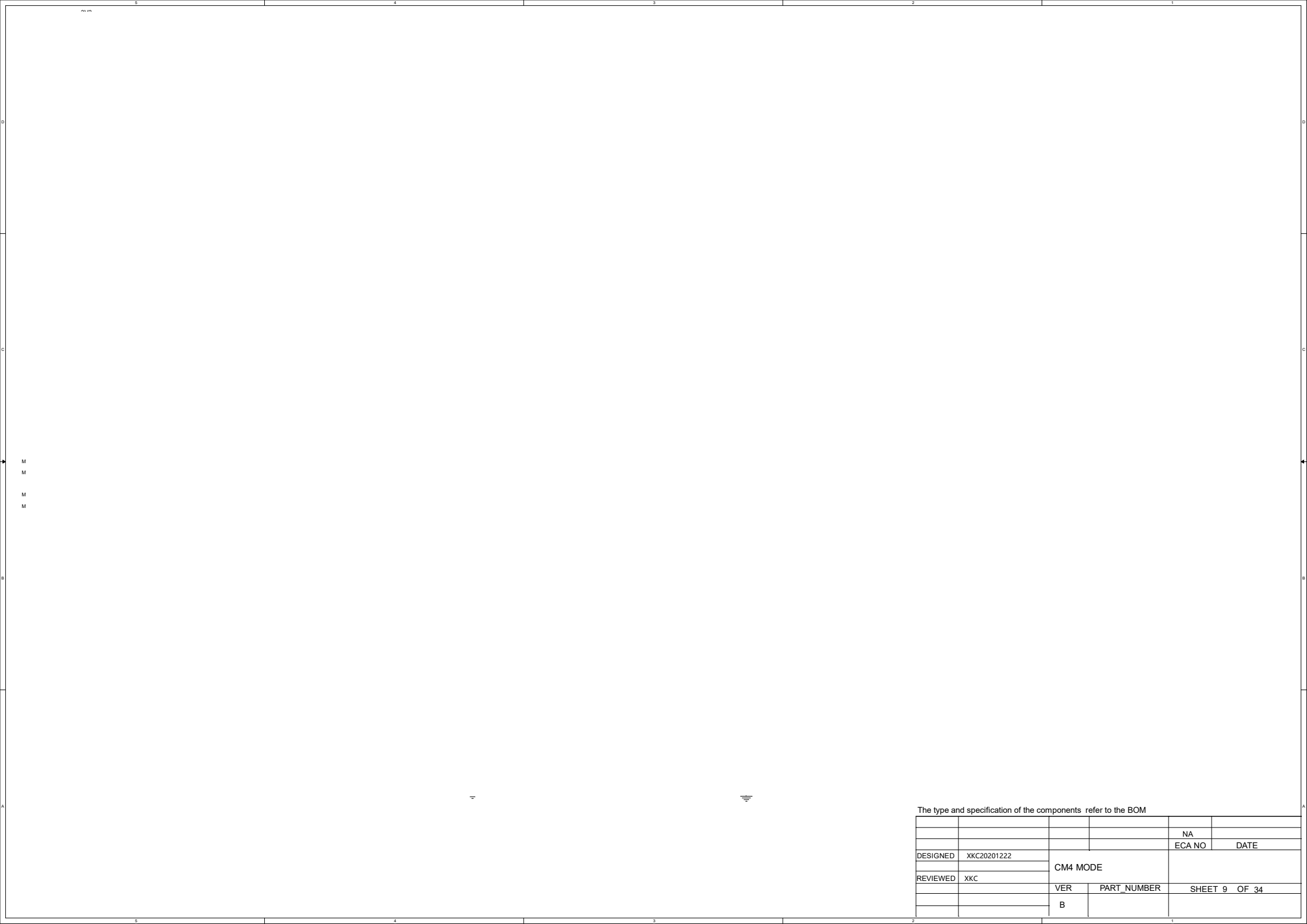


PD#: Input notifies device to sample
 latched inputs and start up on first
 high assertion. Low enters
 Power Down Mode, subsequent
 high assertions exit Power Down Mode.
 This pin has internal pull-up resistor.

```
-----
Configuration Straps
PD#:          Internal PU (see spec)
OE0#:         0 (Enable DIF0)
OE1#:         0 (Enable DIF1)
SS SEL TRI:   0 (SpreadSpect off)
-----
```



Ref. Design
Terminations to
DNP by default

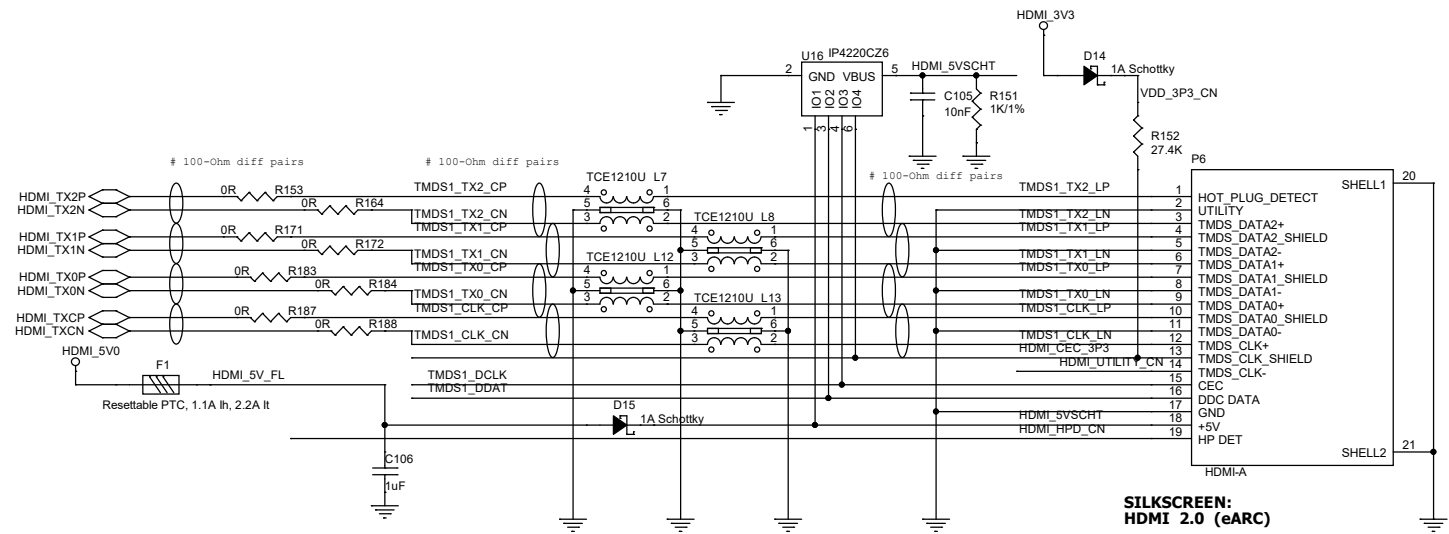


M
M

M
M

The type and specification of the components refer to the BOM

				NA	
				ECA NO	DATE
DESIGNED	XKC20201222	CM4 MODE			
REVIEWED	XKC				
		VER	PART_NUMBER	SHEET 9 OF 34	
		B			



100-Ohm diff pairs

EARC_P_UTIL

EARC_N_HPDI

C107

C108

1uF

1uF

EARC_P

EARC_N

R193

1.2K

HDMI_HPDI_5V

R194

47K

TCE1210U L14

HDMI_UTILITY_CN

HDMI_HPDI_CN

The schematic diagram illustrates the TXS0102 HDMI level shifter circuit. It includes two 3V3 HDMI inputs, a 5V_SCHT input, and two 3V3 HDMI outputs. The circuit features resistors R238, R239, R240, R241, and R442, capacitors C130 and C131, and a TXS0102 level shifter (U31). The TXS0102 is configured with VCCA and VCCB to 3V3, and OE_DDC_LS to 3V3 via R442. The TXS0102 pins are connected to HDMI_DDC_SCL, HDMI_DDC_SDA, TMDS1_DCLK, and TMDS1_DDAT.

				NA	
				ECA NO	DATE
DESIGNED	XKC20201222	CM4 MODE			
REVIEWED	XKC				
		VER	PART_NUMBER	SHEET 9 OF 34	
		B			

The diagram illustrates the electrical connections for a bootable Micro-SD socket. Key components and connections include:

- Power and Grounding:** A 3V3_PER supply is connected to the VBUS pin of the IP4220C26 USB-to-UART bridge and the VBUS pin of the U65 IC. A 100nF capacitor (C235) is connected between 3V3_PER and ground. Grounding is established through pins 2 and 5 of the IP4220C26 and pin 2 of the U65.
- Signal Connections:**
 - SD2_DATA0 through SD2_DATA3 are connected to R245 through R249 and then to the SDCARD_DATA0 through SDCARD_DATA3 pins of the CPU.
 - SD2_CLK is connected to R340 and then to the SDCARD_CLK pin of the CPU.
 - SD2_CMD and SD2_nCD are connected to R341 and then to the SDCARD_CMD pin of the CPU.
- Micro-SD Card Interface:** The card is connected via J4 (TF-CARD) to the SDCARD pins of the CPU. The card's pins are labeled: 1 (DAT2), 2 (CD/DAT3), 3 (CMD), 4 (VIO), 5 (VIO), 6 (CLK), 7 (VSS), 8 (DAT0), 9 (DAT1), 10 (GND1), 11 (GND2), 12 (POL), 13 (DET), and 14 (GND3).
- Other Components:** Capacitors C236, C237, C238, C239, and C240 are connected to the 3V3_PER supply. The IP4220C26 (U64) and U65 ICs are connected to the 3V3_PER supply and ground.

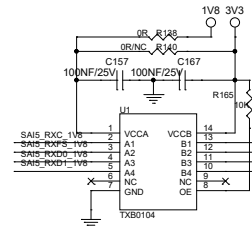
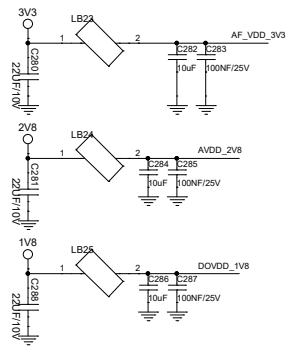
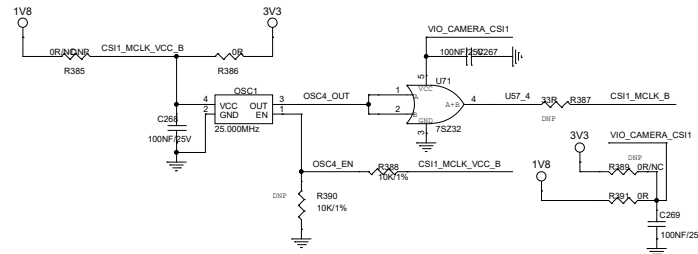
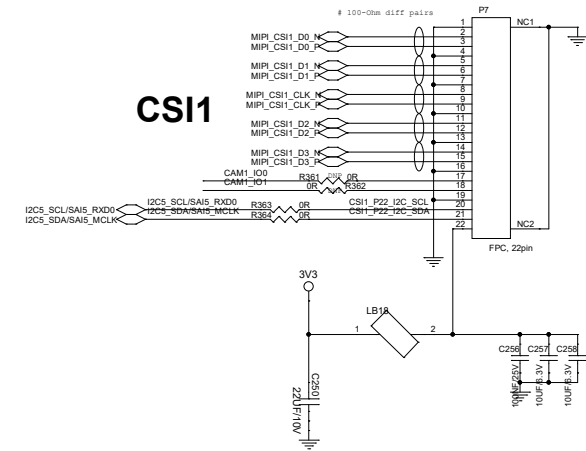
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DESIGNED	XKC20201222	CM4 MODE			
REVIEWED	XKC				
			VER	PART_NUMBER	SHEET 9 OF 34
			B		

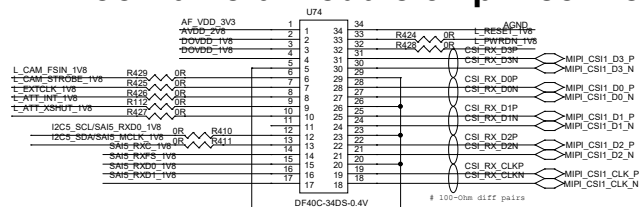
RPI FPC 22 pins

SILKSCREEN:
MIPI-CSI1 (22-pin, 3.3V)

22-pin Connector for RPi cameras
Four MIPI-CSI lanes connected

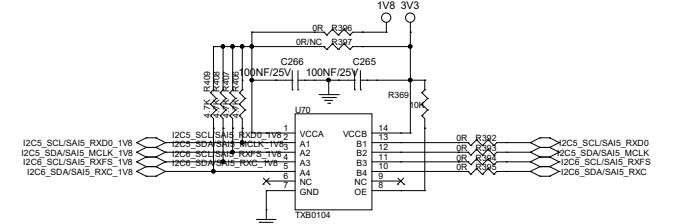
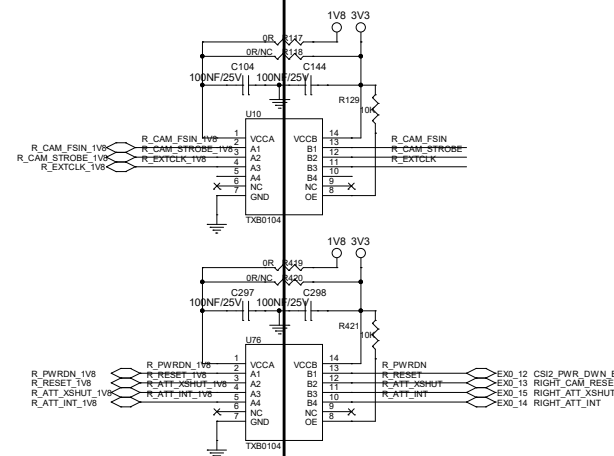
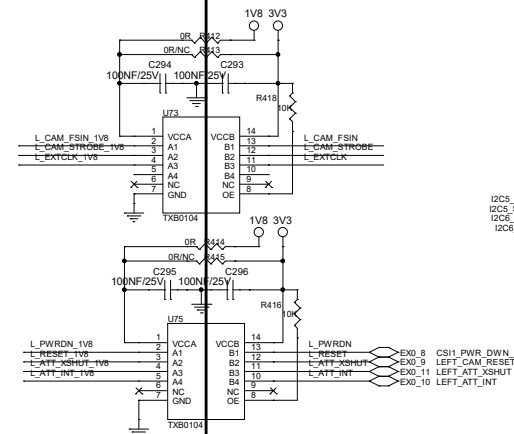


Ziloo Camera Module 34 pin connector

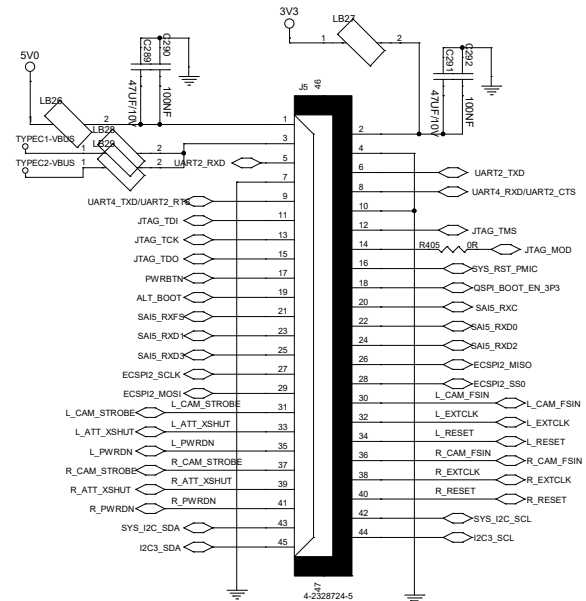


CSI1

6P



Debugging Breakout connector 45P





The type and specification of the components refer to the BOM				
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DESIGNED	XKC20201222	CM4 MODE		
REVIEWED	XXC			
		VER	PART_NUMBER	SHEET 9 OF 34
		B		