# Stembus Expander

The Stembus Expander is a standard module similar to an I/O Expander. It accesses local control pins and state to provide remote control capability over the Stem I2C bus. It rules over a distinct domain and will raise Stem INT events(1-Wire) when the domain is affected.

It can,

- Reset components
- Power on/off/suspend components
- Change component state and mode selection
- Raise relevant event flags

Ziloo has three expanders with distinct domains;

- T-USB Expander monitors and controls Module runtime, Battery charging, USB Power Delivery, and USB Alt. Mode.
- Faceboard Expander monitors IMU, m.2 modules
- The Smart Ambient Night Eye also monitors and controls sensors to determine change in ambient state. Sound, light and vision a monitored.

Available actions,

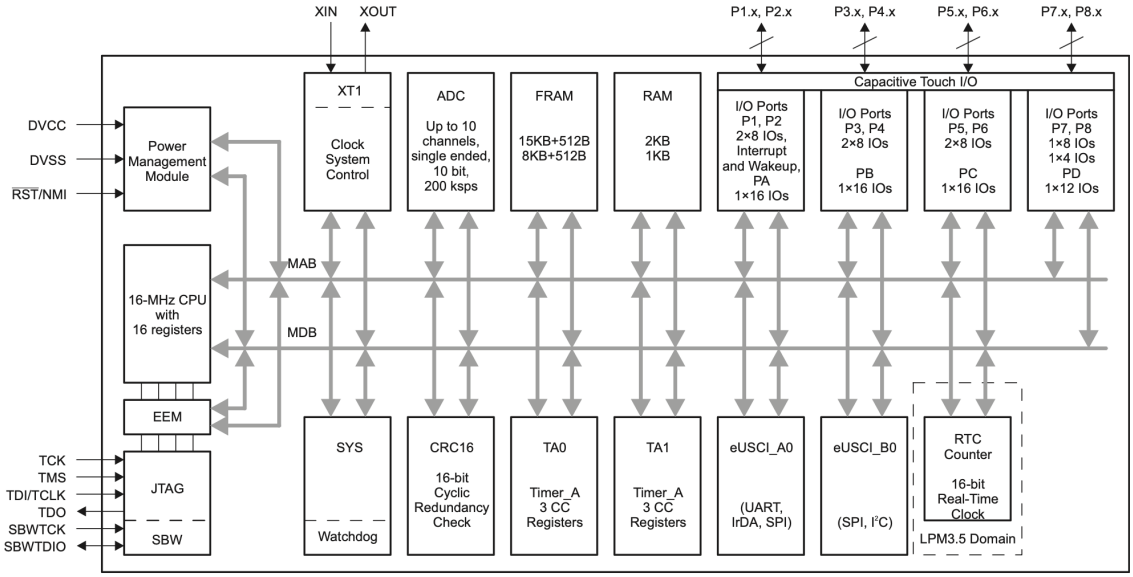
- Set T-USB 2.0 Alt. modes state (byte)
- Set T-USB 3.0 Alt. modes state (byte)
- Request

## Open Points

- 2 * UART for programming MSP with SoM
-

## Components

- 1 * MSP430 FR2032 IG56 TSSOP DGG56. Inventory 4870 at TO. @1000 $0.766. 52 IO pins, 1 UART/I2C, 1 UART/SPI.

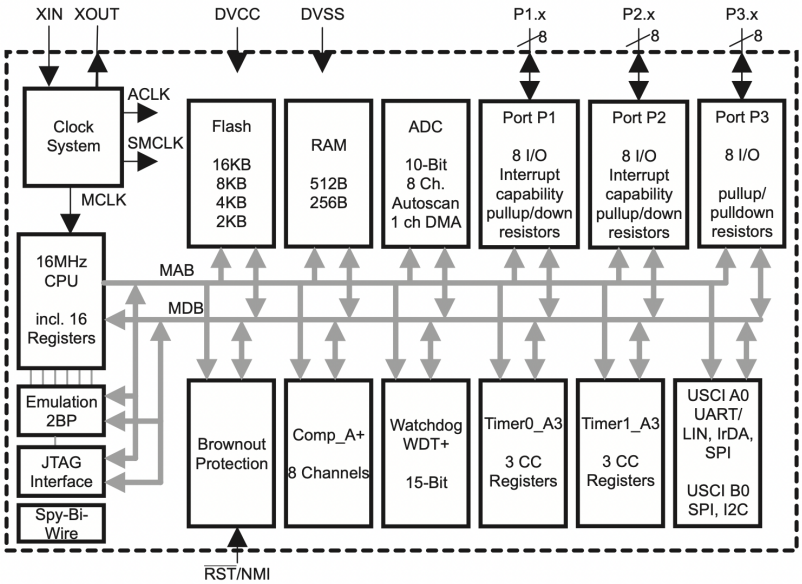



## Alt. Components

- 3 * 74HC595 PW,118 shift register TSSOP-16. @1000 $0.15, 15k in stock.
- 3 * compact 74HC595BQ,115 DHVQFN-16 that are not available until 2023.
- 3 * 771-74HC595D-Q100 SOIC-16
- 1 * MSP430FR4131IPMR low mem, 60 IO, in stock
- 1 * MSP430 FR2032 IPMR - Available Aug 2023. $1.2 @1000. 60 IO pins, P1 .. P8. Fast permanent storage. (Only UART bootloader). LQFP (64). Direct JTAG and sbw pins pins.
- 1 * MSP430 G2553 IRHB32R - 2300 in stock. @1000 $1.7. Large app 16KB. (Only UART bootloader)
- 1 * MSP430 G2433 IRHB32R VQFN-32 5mm x 5mm. Inventory 1238 at mouser. @1000 $1.45. 24 IO pins, 1 UART/I2C, 1 UART/SPI. (Only UART bootloader)

There seem to be no 74HC595 alternatives.

**Functional Block Diagram, MSP430G2x53**




NOTE: Port P3 is available on 28-pin and 32-pin devices only.

The G2553 routes debugging and programming over RST/TEST (even if not shown in diagram).

### Programming

The MSP430 is programmed using the Bootloader. See bootloader section in the specific datasheet for pins.

Bootloader mode is triggered by a specific timing signal over the RST/DTR and TEST/RTS pins. Once in bootloader mode the UART_EX_TXD and UART_EX_RXD are used to upload the new firmware. These pins are exposed on the 50 pin connector and available to the i.MX SoM and Picoprobe socket. The SoM will use this to update firmware without opening the case. One the Expander has been flash a unique password is set on future writing. Future updates must use this password to be applied.

One way to program the MSP430 is via the Picoprobe running pico-uart-brige. This make it available as a Comm port over USB to a Linux host on Raspberry Pi or other CI Runner. See example code for implementation at MSP430TM Bootloader With SitaraTM Embedded Linux Host. Also consider How to securely update firmware in the field and MSP430FRBoot – Main Memory Bootloader and Over-the-Air Updates for MSP430TM FRAM Large Memory Model Devices.

Simple sample video Programming MSP430G2553 through BSL | MSP430 on a breadboard | UART bridge programmer

The BSL Scripter is a PC application that allows to easily communicate with the BSL on MSP430 and MSP432 devices to modify the device's memory via UART, I2C, SPI or USB. Download MSPBSL_Scripter 3_04_00_02. Bootloader (BSL) Scripter (SLAU655) documentation.

### I2C access

The primary I2C bus, where the Expander exposes its connected gpio output and input, is the Stem I2C. The Stem I2C is mastered by one of the MCUs connected such as RT core in SoM or the RP2040 in the Smart Camera Module. The expander can also provide its service on the SYS I2C.

#### Interrupt events

It is important to consider the overall system interrupt events

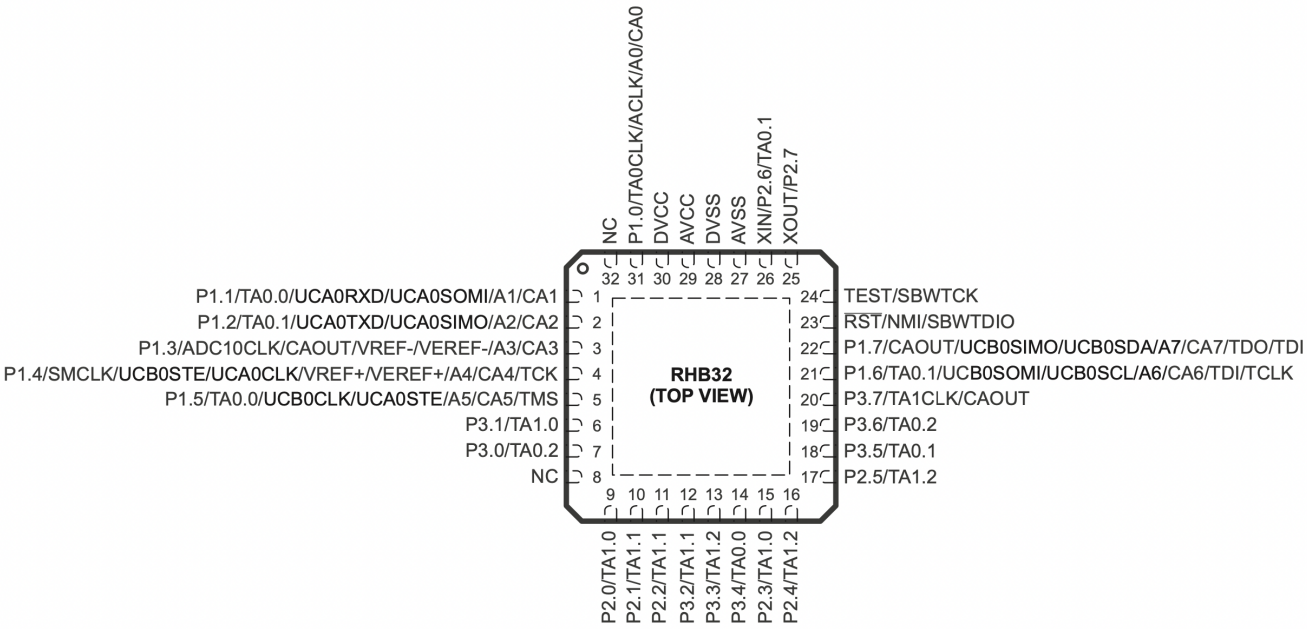
- T-USB PD state change -> T-USB module raises STEM INT with a 1 wire origin signal.
- T-USB Charging state change -> T-USB module raises STEM INT with a 1 wire origin signal.
- Faceboard sensor event -> Faceboard module raises STEM INT with a 1 wire origin signal and MOTION_INT
- Faceboard m.2 event -> Faceboard module raises STEM INT with a 1 wire origin signal

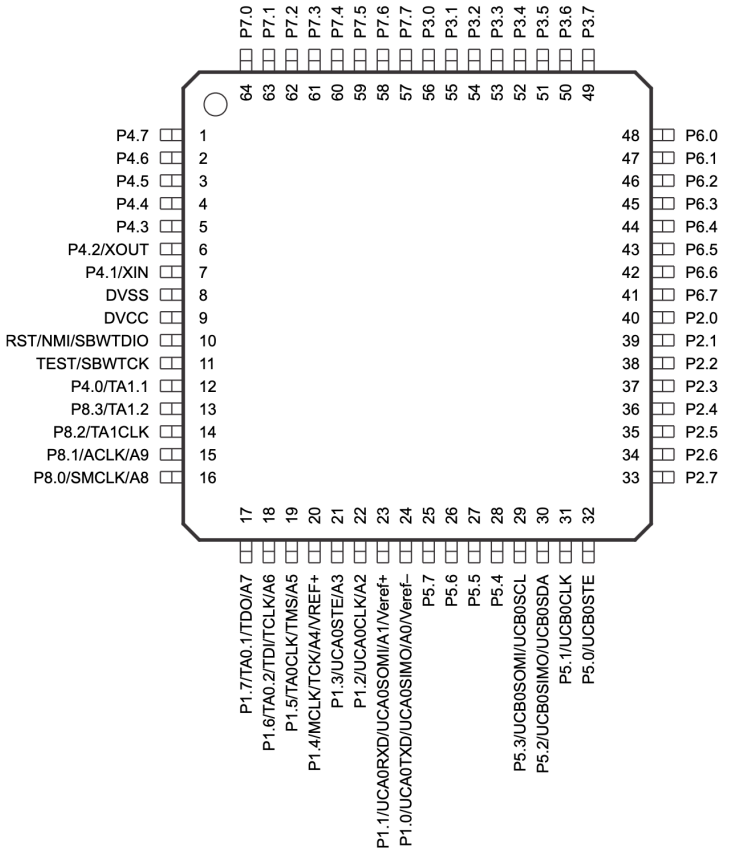
After an MCU has raised a Stem INT it may not do so for again for 10ms. This allows other MCUs to raise their events.

## I2C Interface (read/write)

## T-USB Expander pin allocations for MSP430 G2553/G2x33/FR2032

**Device Pinout, MSP430G2x13 and MSP430G2x53, 32-Pin Devices, QFN**




TSSOP56: 14mm x 6.1mm x 1.2mm

Programming pins

| Expander | VQFN32 | LQFP | G56 | Connected to |
|---|---|---|---|---|
| RST / NMI / T_SBWTDIO | 23 | 10 | 16 | Reset. Nunmaskable interrupte input. T_SWBTDIO on 50 pins, DTR on Comms |

| Expander | VQFN32 | LQFP | G56 | Connected to |
|---|---|---|---|---|
| TEST / SBWTCK | 24 | 11 | 17 | T_SWBTCK on 50 pins, RTS on Comms. Sel. test mode for JTAG pins on Port 1. Device protection fuse cnnctd to TEST |
| UART_T_TXD | 1 | 24 | 28 | Firmware transmit (see Bootloader section in datasheet) |
| UART_T_RXD | 5 | 23 | 27 | Firmware receive (see Bootloader section in datasheet) |

The programming UART pins are not consistent across models. This matches FR2032(G56), FR413x(LQFP), G2433/G2553(VQFN32 P1.1 and P1.5).

## MSP430 pin allocations

The intended FR2032 chip uses a TSSOP-56 (G56) package.

These pins are used in a special role

| Function | VQFN32 | LQFP | G56 | Connected to |
|---|---|---|---|---|
| STEM INT | 31 | 24 | 28 | P1.0. 1-Wire event raising line between MCUs |
| UART3 RX | 1 | 23 | 27 | P1.1. USCI_A0. UCA0RXD. |
| UART3 TX | 2 | 22 | 26 | P1.2. USCI_A0. UCA0TXD. |
| MCU SYS INT | 3 | 21 | 25 | P1.3. 1-Wire event raising line between MCUs |
| SYS SCL | 4 | 20 | 24 | P1.4. 50 pin connector. TCK. JTAG test clock, input terminal for device programming and test |
| SYS SDA | 5 | 19 | 23 | P1.5. 50 pin connector. TMS. JTAG test clock, input terminal for device programming and test |
| MSP_TDI/analog | 21 | 18 | 22 | P1.6 TDI/TCLK. Host Alt. JTAG test data input or test clock input during programming and test. |
| MSP_TDO/analog | 22 | 17 | 21 | P1.7 TDO/TDI. Host Alt. JTAG test data output terminal or test data during programmign and test |
| UCB0_CE | nc | 32 | 34 | P5.0. nc |
| UCB0_CLK | nc | 31 | 33 | P5.1. nc |
| STEM SCL | | 29 | 31 | P5.3. USCI_B0. |
| STEM SDA | | 30 | 32 | P5.2. USCI_B0. |
| TA1.1/Cp | nc | 12 | 18 | P4.0 / Host Alt connector |
| XIN | nc | 7 | 13 | P4.1/XIN / Host Alt connector |
| XOUT | nc | 6 | 12 | P4.2/XOUT / Host Alt connector |
| TA1CLK/Compare | nc | 14 | 20 | P8.2 TA1CLK / Host Alt connector |

| Function | VQFN32 | LQFP | G56 | Connected to |
|---|---|---|---|---|
| TA1.2/Compare | nc | 13 | 19 | P8.3 / Host Alt connector |

Pins used as GPIO

| Function | VQFN32 | LQFP | G56 | Connected to |
|---|---|---|---|---|
| SHUTDOWN_BTN | 9 | 40 | 42 | P2.0. Shudown button pin on 3 pin Power Enable Connector |
| LOCK_BTN | 10 | 39 | 41 | P2.1. Lock button pin on 3 pin Power Enable Connector |
| POR_B_3P3 | 11 | 38 | 40 | P2.2. Power on reset Input from PMIC. 50 pin connector |
| BOTH_VSOM | 15 | 37 | 39 | P2.3. Input from faceboard. 50 pin connector |
| T_USB_O_ALT_POL | 16 | 36 | 38 | P2.4. HD3SS460 (default = high-im) |
| T_USB_O_ALT_AMSEL | 17 | 35 | 37 | P2.5. HD3SS460 (default = high-im) |
| T_USB_H_ALT_POL | 26 | 34 | 36 | P2.6. HD3SS460 (default = high-im) |
| T_USB_H_ALT_AMSEL | 25 | 33 | 35 | P2.7. HD3SS460 (default = high-im) |
| T_USB_O_ALT_EN | SH1.0 | 56 | 56 | P3.0. HD3SS460 (default = high-im) |
| T_USB_H_ALT_EN | SH1.1 | 55 | 55 | P3.1. HD3SS460 (default = high-im) |
| HXA_SEL | SH1.2 | 54 | 54 | P3.2. Select Host Extra A6/A7 |
| HXB_SEL | SH1.3 | 53 | 53 | P3.3. Select Host Extra B6/B7 |
| HX_OE | SH1.4 | 52 | 52 | P3.4. Select Host Extra Enable |
| OXA_SEL | SH1.5 | 51 | 51 | P3.5. Select OTG Extra A6/A7 |
| OXB_SEL | SH1.6 | 50 | 50 | P3.6. Select OTG Extra B6/B7 |
| OX_OE | SH1.7 | 49 | 49 | P3.7. Select OTG Extra Enable |
| PWRBTN | SH2.0 | 5 | 11 | P4.3. 50 pin connector |
| ALT_BOOT | SH2.1 | 4 | 10 | P4.4. 50 pin connector |
| QSPI_BOOT_EN_3P3 | SH2.2 | 3 | 9 | P4.5. 50 pin connector |
| VSOM_LOCK_EN | SH2.3 | 2 | 8 | P4.6. Data output enabling VSOM_LOCK(300mA VSOM). |
| SYS_RST_PMIC | SH2.4 | 1 | 7 | P4.7. 50 pin connector |
| PMIC_ON_REQ | SH2.5 | 28 | 30 | P5.4. 50 pin connector |
| PMIC_STBY_REQ | SH2.6 | 27 | 29 | P5.5. 50 pin connector |
| | SH2.7 | | | |

| Function | VQFN32 | LQFP | G56 | Connected to |
|---|---|---|---|---|
| BOTH_VSOM2 | | 48 | 48 | P6.0. 50 pin connector |
| BAT_INT | | 47 | 47 | P6.1. BQ24250 |
| PD_CTL_INT_1 | | 46 | 46 | P6.2. TPS PD Controller |
| PD_CTL_INT_2 | | 45 | 45 | P6.3. TPS PD Controller |
| T_EXTRA | SH3.0 | 44 | 44 | P6.4. 50 pin connector |
| BAT_CE | SH3.1 | 43 | 43 | P6.5. BQ24250 |
| BAT_EN1 | SH3.2 | 6 | 6 | P7.0. BQ24250 |
| BAT_EN2 | SH3.3 | 5 | 5 | P7.1. BQ24250 |
| PD_CTL_RESET | SH3.4 | 4 | 4 | P7.2. TPS PD Controller |
| PD_EXT1 | SH3.5 | 3 | 3 | P7.3. TPS PD Controller |
| PD_EXT2 | SH3.6 | 60 | 2 | P7.4. TPS PD Controller |
| PD_VIN_EN | SH3.7 | 59 | 1 | P7.5. TPS PD Controller |

56 pin package excludes 8 pins: P8.0 P8.1 P5.6 P5.7 P6.6 P6.7 P7.6 P7.7 (only usable at 64 pin package)

## Alt. Design using Shift registers (output only)

If a 48+ IO MSP430 chip is not available a setup is used with 24 IO. In this setup shift registers are used.

Three shift registers are chained off the 7 shift pins. Individual pins triggers the update of output for 8 bytes. A fourth output trigger pin is reserved for a future bank. This lessens the requirement to remember existing state. For the 64 pin package shift registers are not used.

| Function | VQFN32 | LQFP | G56 | Connected to |
|---|---|---|---|---|
| SH1_DS | 6 | | | P3.1. 74HC595 DS |
| SH1_SHCP | 12 | | | P3.2. 74HC595 SHCP |
| SH1_MR | 13 | | | P3.3. 74HC595 MR |
| SH1_STCP | 14 | | | P3.4. 74HC595 STCP |
| SH2_STCP | 18 | | | P3.5. 74HC595 STCP |
| SH3_STCP | 19 | | | P3.6. 74HC595 STCP |
| SH4_STCP | 20 | | | P3.7. 74HC595 STCP |

The output pins on the shift registers are grouped as,

- SH1 Alt mode bits,
- SH2 SoM Runtime control shift reg
- SH3 PD And Charging control shift reg

- SH4 unallocated shift register.

| Function | VQFN32 | Connected to |
|---|---|---|
| STEM INT | 31 | P1.0. 1-Wire event raising line between MCUs |
| UART3 RX | 1 | P1.1. USCI_A0. UCA0RXD. |
| UART3 TX | 2 | P1.2. USCI_A0. UCA0TXD. |
| MCU SYS INT | 3 | P1.3. 1-Wire event raising line between MCUs |
| SYS SCL | 4 | P1.4. 50 pin connector. TCK. JTAG test clock, input terminal for device programming and test |
| SYS SDA | 5 | P1.5. 50 pin connector. TMS. JTAG test clock, input terminal for device programming and test |
| STEM SCL | 21 | P1.6 USCI_B0. TDI/TCLK. JTAG test data input or test clock input during programming and test. |
| STEM SDA | 22 | P1.7 USCI_B0. TDO/TDI. JTAG test data output terminal or test data during programmign and test |

## Faceboard expander pin allocations

Pins used as GPIO

| Function | VQFN32 | LQFP | G56 | Connected to |
|---|---|---|---|---|
| IMU_INTM | 9 | 40 | 42 | P2.0. IMU Motion Interrupt |
| IMU_INTA | 10 | 39 | 41 | P2.1. IMU Accelerator Interrupt |
| POR_B_3P3 | 11 | 38 | 40 | P2.2. Power on reset Input from PMIC. 50 pin connector |
| (BOTH_VSOM) | 15 | 37 | 39 | P2.3. Input from faceboard. 50 pin connector |
| | 16 | 36 | 38 | P2.4. |
| | 17 | 35 | 37 | P2.5. |
| LEFT_ATT_INT | 26 | 34 | 36 | P2.6. |
| RIGHT_ATT_INT | 25 | 33 | 35 | P2.7. |
| LED_SHUTDOWN - SDB | SH1.0 | 56 | 56 | P3.0. |
| | SH1.1 | 55 | 55 | P3.1. |
| CSI1_PWR_DWN_B | SH1.2 | 54 | 54 | P3.2. |
| LEFT_CAM_RESET | SH1.3 | 53 | 53 | P3.3. |

| Function | VQFN32 | LQFP | G56 | Connected to |
|---|---|---|---|---|
| LEFT_ATT_XSHUT | SH1.4 | 52 | 52 | P3.4. |
| CSI2_PWR_DWN_B | SH1.5 | 51 | 51 | P3.5. |
| RIGHT_CAM_RESET | SH1.6 | 50 | 50 | P3.6. |
| RIGHT_ATT_XSHUT | SH1.7 | 49 | 49 | P3.7. |
| PWRBTN | SH2.0 | 5 | 11 | P4.3. 50 pin connector |
| ALT_BOOT | SH2.1 | 4 | 10 | P4.4. 50 pin connector |
| QSPI_BOOT_EN_3P3 | SH2.2 | 3 | 9 | P4.5. 50 pin connector |
| | SH2.3 | 2 | 8 | P4.6. |
| SYS_RST_PMIC | SH2.4 | 1 | 7 | P4.7. 50 pin connector |
| PMIC_ON_REQ | SH2.5 | 28 | 30 | P5.4. 50 pin connector |
| PMIC_STBY_REQ | SH2.6 | 27 | 29 | P5.5. 50 pin connector |
| | SH2.7 | | | |
| (BOTH_VSOM2) | | 48 | 48 | P6.0. 50 pin connector |
| B_CONFIG_1 | | 47 | 47 | P6.1. m.2 Key B |
| B_LED / DAS / DSS | | 46 | 46 | P6.2. m.2 Key B |
| | | 45 | 45 | P6.3. m.2 Key B |
| M2B_PWROFF | SH3.0 | 44 | 44 | P6.4. m.2 Key B |
| DEVSLP | SH3.1 | 43 | 43 | P6.5. m.2 Key B |
| | SH3.2 | 6 | 6 | P7.0. on m.2 Key E |
| M2E_PWROFF | SH3.3 | 5 | 5 | P7.1. on m.2 Key E |
| W_DISABLE1# | SH3.4 | 4 | 4 | P7.2. on m.2 Key E |
| W_DISABLE2# | SH3.5 | 3 | 3 | P7.3. |
| | SH3.6 | 60 | 2 | P7.4. |
| | SH3.7 | 59 | 1 | P7.5. |

56 pin package excludes 8 pins: P8.0 P8.1 P5.6 P5.7 P6.6 P6.7 P7.6 P7.7 (only usable at 64 pin package)

| Expander | Connected to |
|---|---|
| EX6.0 | E_COEX4 |
| EX6.1 | E_DEV_WLAN_WAKE |
| EX6.2 | E_ALERT / I2C_IRQ |

| Expander | Connected to |
|---|---|
| EX6.3 | E_LED / DAS / DSS |
| EX6.4 | E_UART WAKE |
| EX6.5 | E_SDIO WAKE |
| EX6.6 | E_LED2# |
| EX6.8 | B_RESET# |
| EX6.9 | B_ALERT / I2C_IRQ |
| EX6.10 | |

The system expander #0 is used by the SoM via SYS I2C. The system expander input triggers interrupt via SYS_nINT (GPIO4_IO19). This expander deals with activity relevant during waking state.

This first expander, which is also on the dev. board maps,

| Expander | Connected to |
|---|---|
| EX0.0 | mPCIe_PERST on M2 Key B |
| EX0.1 | - reserved for second mPCIe - |
| EX0.3 | |

- LED Controller
- Motion Sensor
- Sound Sensor
- Nighttime camera attached sensors
-

The EX4 expander input triggers interrupt via STEM_INT.

| Expander | Pin | Connected to |
|---|---|---|
| EX4.0 | | |
| EX4.1 | O0.1 | SD Card Chip Select SPI |
| EX4.2 | O0.2 | SD Card Chip Select SDIO |
| EX4.8 | I1.0 | MIC VM3011 DOUT |

Enable CS SD Card connector LCD CS SPI MMC CS m.2 WiFi CS SDIO

The EX6 expander input triggers interrupt via SYS_nINT (GPIO4_IO19).

## Articles

- 1-Wire - OneWire implementation for MSP430
- MSP430 CCS Code Examples

- MoaT owslave
- Three-state logic
- MSP430 IO Expander Firmware
- MSP430 build on Raspberry Pi
- Programming the MSP430 using docker
- mspdebug
- A BETTER USI I2C LIBRARY FOR THE MSP430 - Jan's blog post: I2C using USI on the MSP430
- msp430 USI I2C lib
- TI MSP 430, UART, I2C & ADCs, 7-Segments....
- MSP430F5438A-EP: Writing and Reading MSP430 Flash using MSP-FET
- MSP430Flasher compiled to run on ARM architecture
- MSPDS — MSP Debug Stack Developers Package
- Guide and script to install mspdebug on Raspberry Pi in order to flash and debug MSP430 devices
- UART with MSP430
- Rust Quickstart for MSP430
- Riot OS with MSP430
- Software UART example for MSP430 using mps430-gcc on Linux
- 74HC125 tri-state conversion of 4 signals

## Other MSP430 options

MSP430FR2033IPMR - inventory 893 @1000 $1.55 60 pins, 15KB / 2KB, 1 I2C, 1 SPI alt SMD package LQFP-64

MSP430 FR4132 - Available january $1.32. 60 IO.