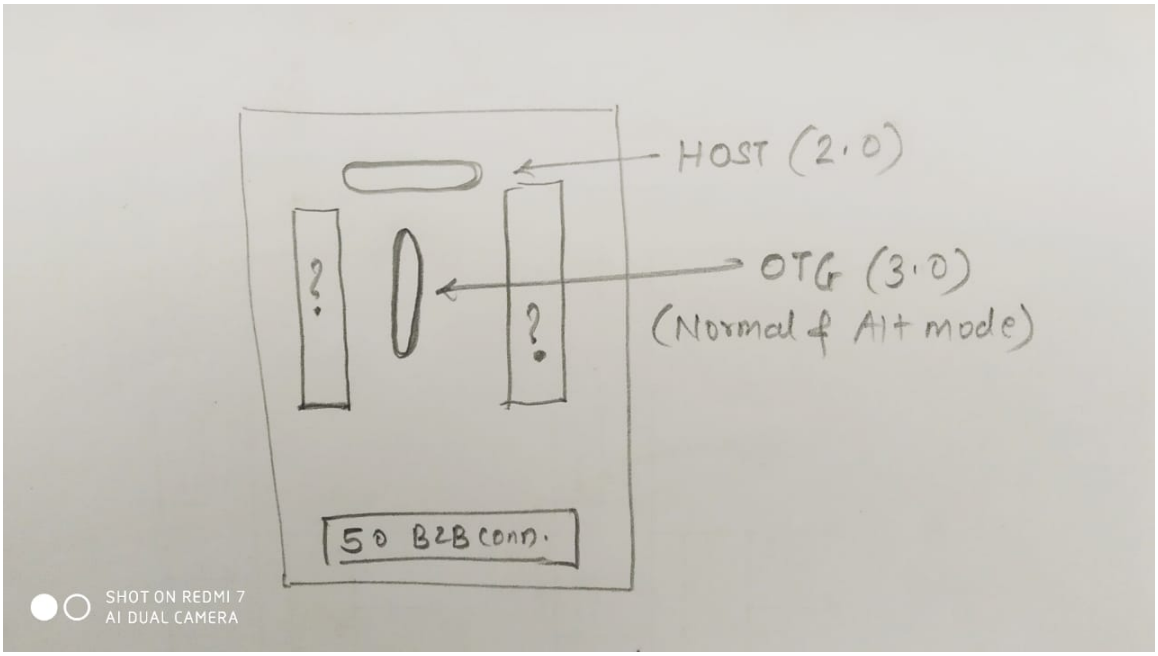
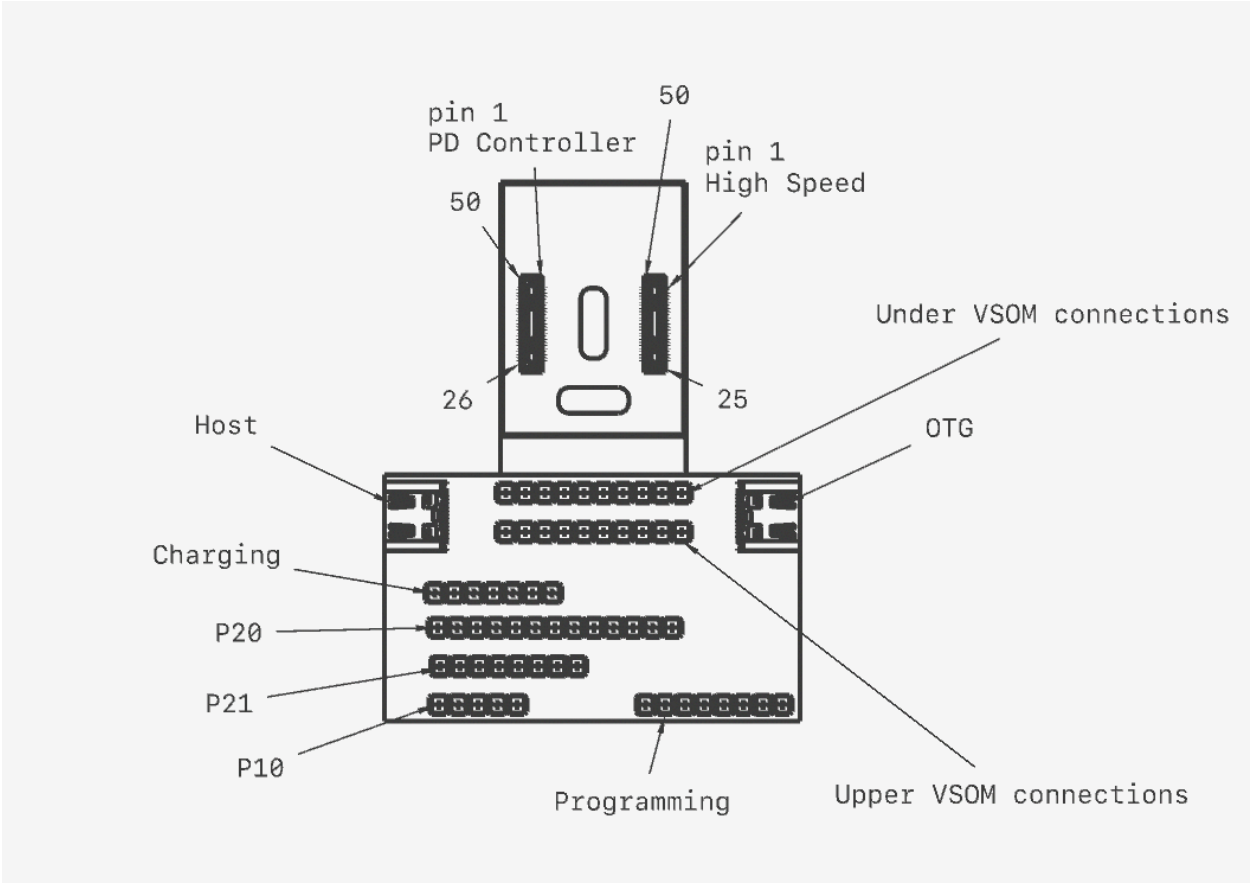
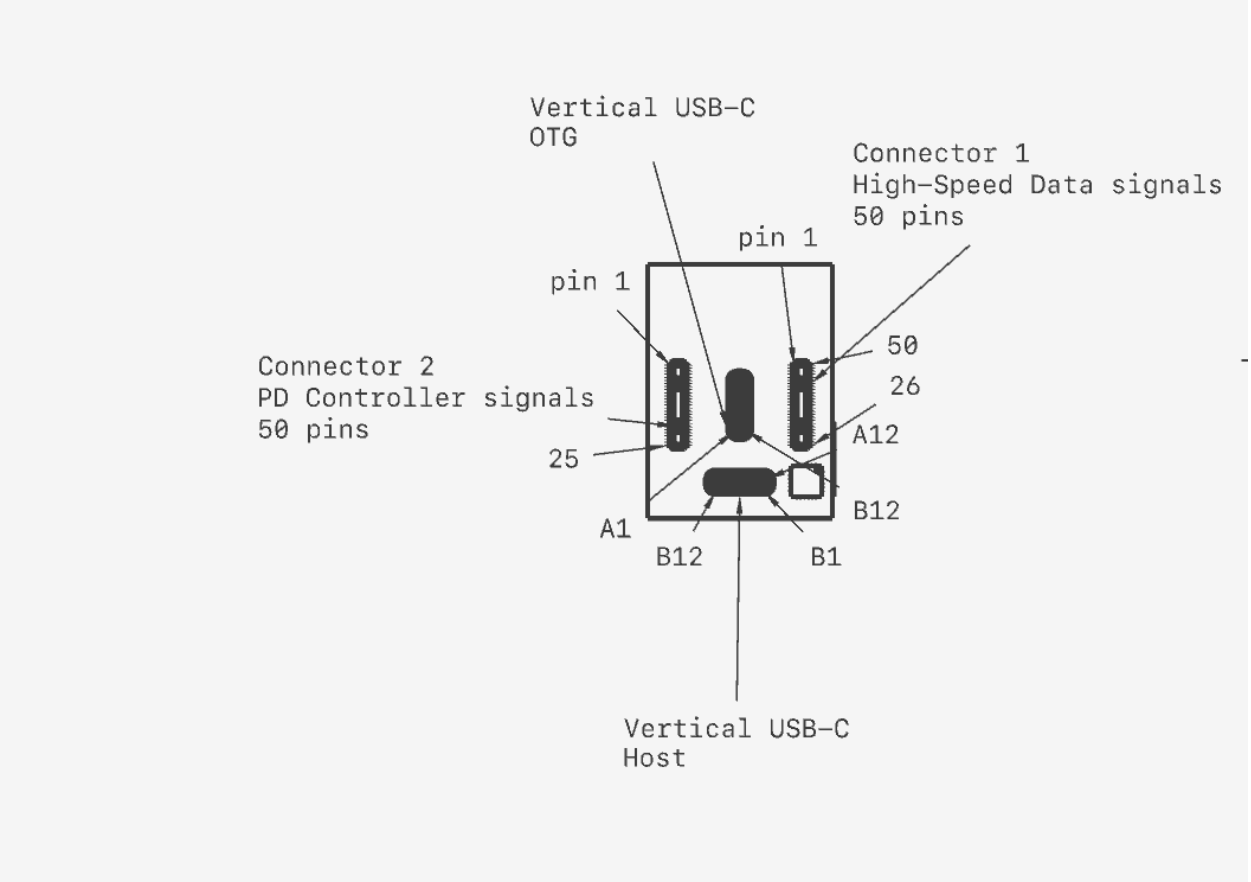
1. Is this correct?



No it isn't there are two 50 pin connectors. One for High speed and one for low speed signals.





2. Is the HOST is with USB2.0 and OTG is with USB3.0?

Both Host and OTG connectors have USB v2.0 and v3.0 signals

3. The last line on **page3** says OTG USB3.0 is multiplexed in Normal and Alt mode via the **HD3SS460** chip. Is Host(USB2.0) supposed to be connected via one more **HD3SS460** as well.

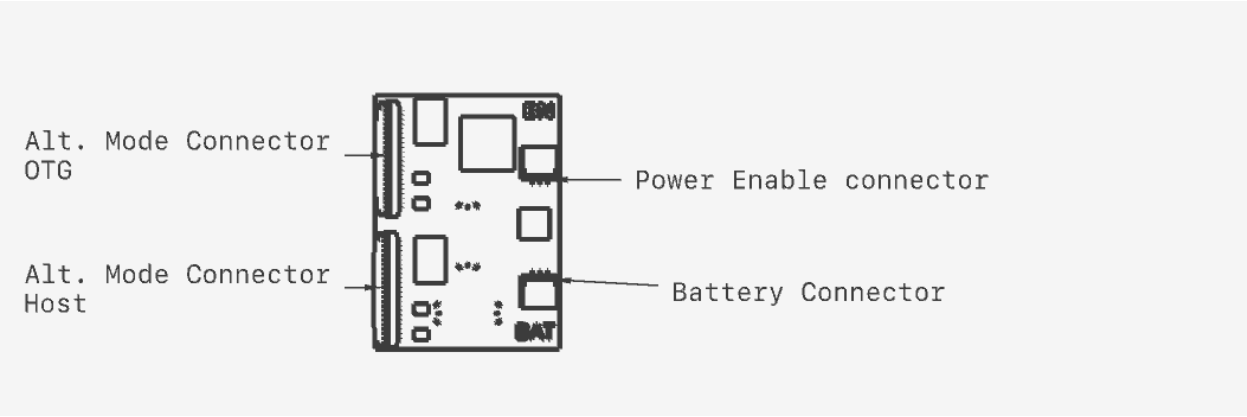
No. HD3SS460 is used to Alt mode switch USB 3.0 signals. Both connectors have them.
USB 2.0 are multiplexed using T5USBC410.

4. **Page4 Image1** shows both the USB connectors via **HD3SS460.** What is exactly expected?

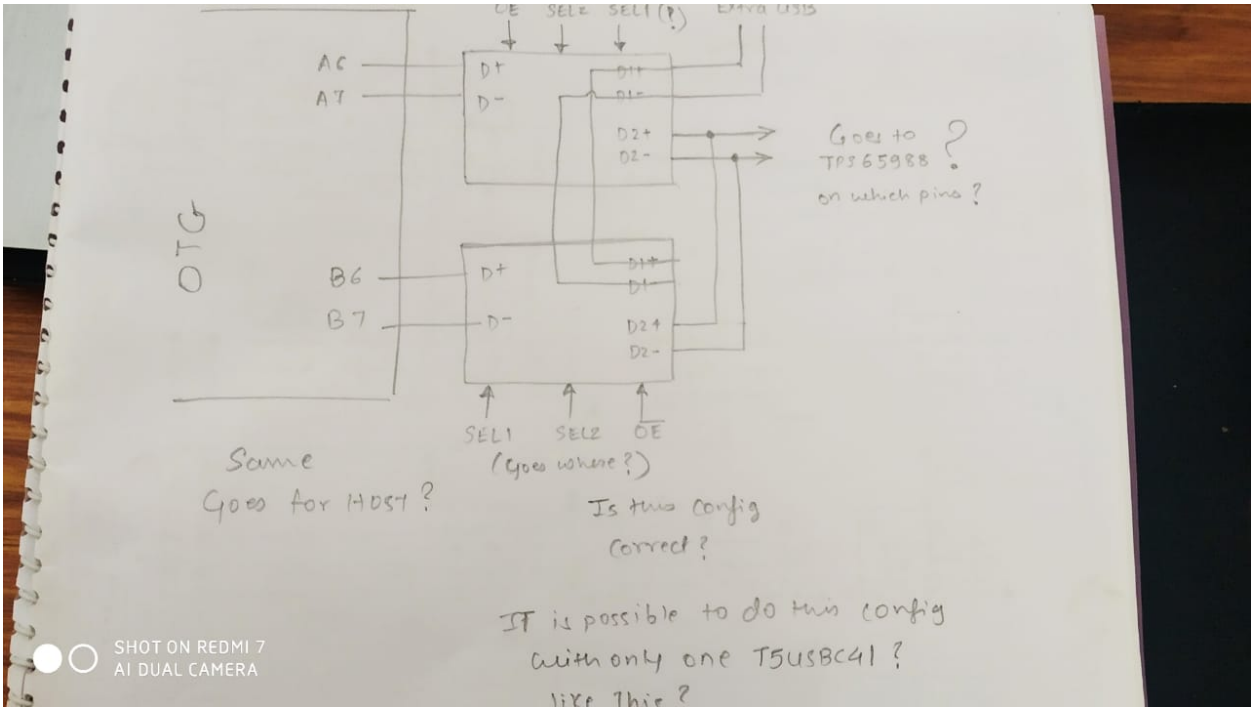
I've added a high level diagram, does that help?

5. What is HOST breakout connector and OTG breakout connector? Is it different from a 50pin B2B connector? Where will it be placed on the board?

45 pin connectors.

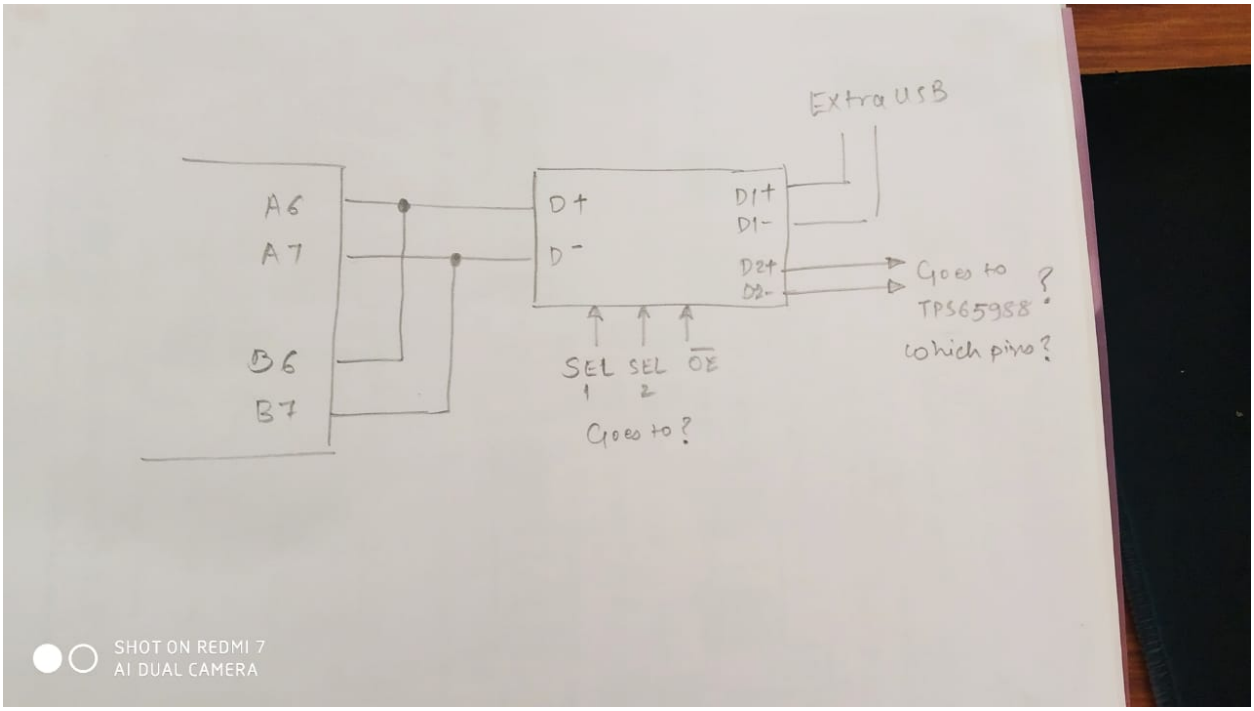


6. **Page 4 "***The USB-C connector USB 2.0 signals(A/B 6/7) are managed separately and multiplexed using TS5USBC41. This allows routing an Extra USB 2.0 signal selectively via the Debug Breakout connector."* **T5USBC410** is basically a USB MUX/DEMUX having 1-INPUT and 2-OUTPUTs so the correct representation of the diagram of connections for USB connector via **T5USBC410** would be like this?



For controlling the **T5USBC410** three pins are needed, SEL1, SEL2 and !OE which chip is supposed to control these pins? If it is considered that the above diagram is correct, then it is possible to reduce one chip of **T5USBC410** and use the following schematics as

I will review the documentation on SEL1, SEL2 and get back to you



Both the cases will yield same results? Please share your thoughts on this.

No, that won't work. The first diagram seems similar to what I had intended, but I think it best for me to review it to ensure it is ideal. The purpose is to be able to use the USB-C directionally to use the alternate pins on the connectors for additional data lines.

7. **Page5: Power Output Vs Input**

The board is primarily a USB power sink, it isn't meant to be a significant source of USB power output (Isn't the T_USB Board is supposed to supply the power to the rest of the boards? Then how does it sink and not a source?)

8. Which connector provides two **VIN_5V** pins? What is **PWR_SYS** and why it is being upscaled and how? Which parameter is being upscaled? Voltage or current?

9. "*The board itself can be a source of 5V on one port, if it is a sink on the other port. For this purpose a direct connection is drawn from PWR_CHARGE to VIN_5V."*
   Contradicts to point 7?

10. Thes system power comes from the PD controller, meaning the **BQ24250** chip? While charging the battery. And when the battery is not charging what will be the source of power?
11. **Page6: Combined T-USB control I/O Exapander**

    801(This board) has 5 **PCA9555?**
    What is **EX3?** What is T-USB Daughter board? The testing board?

12. **Page7** Which chip is supposed to control the **HD3SS460** pins: **AMSEL, POL and EN?** What is the meaning of referencing them as **'H', 'M' and 'L'**? What is **EX3** connector and where is it placed on the PCB?
13. "*OTG and Host USB 2.0 connectivity options. 2 bit switching of USB 2.0 mode. It may be combined with Alt Modes to be 3 bit."*
    Contradicts to ***point3*** which directs to ***last line on page 3*** which states that OTG is USB3.0. Please clarify
14. What are the tables given on **page7** describe?
15. **Page11** what is the power enable connector and where it is supposed to be plpaced on PCB?
16. Page:12
    Table:1
    Pin: 2 and 3
    Description: USB1 RX D+
    USB1 RX D-
    From which chip these connections come from?
17. Pin: 5 and 6
    Description: USB1 TX D+
    USB1 TX D-
    From which chip these connections come from?

18. Pin: 8 and 9 *uses same code as that of pin 2 and 3*
    Description: USB2 RX D+
    USB2 RX D-
    From which chip these connections come from?
19. Pin: 11 and 12 *uses same code as that of pin 2 and 3*
    Description: USB2 RX D+
    USB2 RX D-
    From which chip these connections come from?
20. What is **Exposed EX3?** Is it associated with point 12?
21. Which **LVDS** Connections are brought on to the other side of first 50pin B2B connector? Which chip gives out this LVDS connections?
22. **Page13** What is PD controller connector and where it is supposed to be placed on the board? Is the the other 50 pin B2B connector? Which contains connections from **BQ24250** Chip?
23. Please explain the source of the following connections on the connector 2, meaning to which chip they are associated with
    12-20, 22-25, and 48 - 35
24. **Page 16** Image of schematics is not readable
25. **Page17**
    Table:1
    Contradicts to the images shared on **Page4 Image 1** which shows both the USB connectors (OTG and HOST) going thru **HD3SS460** Chip. Are these connectors different than those explained earlier?
26. **Page17**
    Table:1

Contradicts to the connections shown on **Page4 Image2** where both the USB (OTG and HOST) connects to **TPS65988** via Mux IC **T5USBC41**

27. T-USB all mode connector to be implemented?