EVALUATION KIT AVAILABLE

MAX77301

JEITA-Compliant, Li+ Charger with Smart Power Selector, Automatic Detection, and USB Enumeration

General Description

The MAX77301 is a JEITA-compliant* lithium-ion linear battery charger that operates from a USB port, a dedicated charger, or universal adapter. The IC provides automatic adapter-type detection and enumeration with a USB host or hub. The IC integrates independent battery charge switch, current sense circuit, MOSFET pass elements, thermal regulation circuitry, and eliminates the external reverse-blocking Schottky diode to create the simplest and smallest USB-compliant charging solution.

The IC includes automated detection of charge adapter type, making it possible to distinguish USB 2.0 device, USB charger, dedicated charger devices as well as standard input adapters. See Table 2. When enumeration is enabled, the IC automatically negotiates with a USB host, making it possible to achieve the highest-charging current available from a USB 2.0 device or USB charger without processor intervention. The adapter type detection is compliant with USB 2.0 as well as battery charging Specification Revision 1.1.

The IC controls the charging sequence for single-cell Li+ batteries from battery detection, prequalification, fast charge, top-off, and charge termination. Charging is controlled using constant current, constant voltage and constant die-temperature (CCCVCTj) regulation for safe operation under all conditions. The IC is also compliant with JEITA battery charging requirements.

The Smart Power Selector feature makes the best use of limited USB or adapter power. Battery charge current is set independent of the input current limit. Power not used by the system charges the battery. The battery assists the input source when needed. System voltage is maintained by allowing the application to operate without a battery, a discharged battery, or a dead battery. Automatic input selection switches the system from battery to external power.

The I²C interface provides full programmability of battery charge characteristics, input current limit, and protection features. This provides flexibility for use with a wide range of adapter and battery sizes.

Other features include undervoltage lockout (UVLO), overvoltage protection (OVP), charge status flag, charge fault flag, input power-OK monitor, battery detection, JEITA-compliant charging, charge timer, 3.3V/10mA auxiliary output, and an external power-on switch.

Benefits and Features

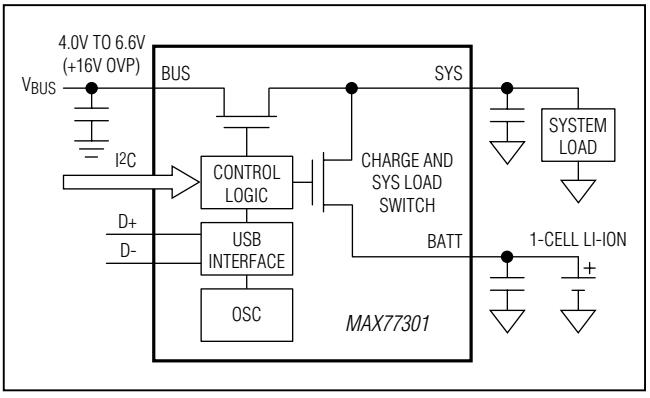
- **Enables Charging from a USB Port**
- **Automatic Detection of Adapter Type**
- **Input Current Up to 1500mA and Charging Current Up to 900mA**
- **Enumeration Without Processor Intervention**
- **Supports USB Low-Speed and Full-Speed**
- **Compliant with USB 2.0 Specification and Battery Charging Specification (Revision 1.1)**
- **Compliant with Next Generation Low-Voltage Li-Ion Battery Profiles**
- **Input Overvoltage Protection Up to 16V**
- **Smart Power Selector™ Allows Power Path Operation with Discharged or No Battery**
- **Battery Detection Including Packs with Open Protectors**
- **Thermal Regulation Prevents Overheating**
- **LED Indicator for Charge Done, Precharge, and Time/Temperature Error**
- **Serial (400kHz) I²C-Compatible Interface**
- **6µA (typ) Shutdown Current**
- **2.44mm x 2.44mm, 25-Bump WLP Package**

Applications

Bluetooth Headsets, PDAs, and MP3 Players

Other Portable Devices

Simplified Operating Circuit



Ordering Information ***appears at end of data sheet.***

Smart Power Selector is a trademark of Maxim Integrated Products, Inc.

**U.S. Patent # 6,507,172.*

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX77301.related.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

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JEITA-Compliant, Li+ Charger with Smart Power Selector, Automatic Detection, and USB Enumeration

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ABSOLUTE MAXIMUM RATINGS

BUS_ to AGND ..... -0.3V to +16.0V
INT_3V3 to AGND ..... -0.3V to +6V
CHG_TYPE, IBUS_DEF, $\overline{ENU\_EN\_HW}$, $\overline{IRQ}$, D+, D-, $\overline{UOK}$, $\overline{CHG\_STAT}$, BAT_, SYS_, CEN, $\overline{STDB\_EN\_HW}$ to AGND ..... -0.3V to +6.0V
XIN, THM, XOUT, to AGND ..... -0.3V to (V_{INT_3V3} + 0.3V)
$\overline{EXT\_PWRON}$, SDA, SCL to AGND ..... -0.3V to (V_{SYS} + 0.3V)
DGND to AGND ..... -0.3V to +0.3V
I_{BUS} and I_{SYS} Continuous Current (Note 1) ..... $2200mA_{RMS}$
I_{BAT} Continuous Current (Note 1) ..... $1800mA_{RMS}$
Continuous Power Dissipation (T_A = +70°C)
WLP (derate 19.2mW/°C above +70°C) 1538mW
Operating Temperature ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Note 1: $I_{BUS} = I_{BUS\_A} + I_{BUS\_B}$; $I_{SYS} = I_{SYS\_A} + I_{SYS\_B}$; $I_{BAT} = I_{BAT\_A} + I_{BAT\_B}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 2)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 52°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(THM = AGND, CEN = INT_3V3, V_{BAT} = 4.2V, $V_{BUS\_}$, $\overline{EXT\_PWRON}$, $\overline{UOK}$, $\overline{IRQ}$, CHG_TYPE, and $\overline{CHG\_STAT}$ are unconnected, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
USB-TO-SYS PREREGULATOR							
USB Operating Range	V_{BUS}	Initial V_{BUS} voltage before enabling charger		4.0		6.6	V
USB Standoff Voltage		V_{BAT} = V_{SYS} = 0V, I_{BUS} < 800µA				14	V
USB_OK Debounce Timer	t_{USB_DB}	Time from BUS within valid range until $\overline{UOK}$ goes high impedance			30	50	ms
USB Undervoltage Lockout Threshold		$\overline{UOK}$ logic-low, V_{BUS} rising, 100mV hysteresis	Before initial detection of external device	3.85	4.0	4.15	V
		$\overline{UOK}$ logic-low, V_{BUS} falling, customer UVLO	For > 500mA adapter and except for ILIM [2:0] = 000, 111	3.40	3.55	3.70	
		$\overline{UOK}$ logic-low, V_{BUS} falling	USB 2.0 low-power device	3.75	3.9	4.05	
		$\overline{UOK}$ logic-low, V_{BUS} falling	USB 2.0 high-power device	3.95	4.1	4.25	
USB Overvoltage Protection Threshold		$\overline{UOK}$ logic-low, V_{BUS} rising, 100mV hysteresis		6.7	6.9	7.1	V

ELECTRICAL CHARACTERISTICS (continued)

(THM = AGND, CEN = INT_3V3, V_{BAT} = 4.2V, $V_{BUS\_}$, $\overline{EXT\_PWRON}$, $\overline{UOK}$, $\overline{IRQ}$, CHG_TYPE, and $\overline{CHG\_STAT}$ are unconnected, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
USB Input Supply Current (Notes 3, 4)	I_{DETECT}	Charge type detection, I_{SYS} = I_{BAT} = 0mA				0.5	mA
	$I_{ENUMERATE}$	USB 2.0 enumeration in progress, I_{SYS} = I_{BAT} = 0mA				100	
	$I_{SUSPEND}$	Suspended mode, I_{SYS} = I_{BAT} = 0mA, $V_{\overline{STDB\_EN\_HW}}$ = 0V				0.5	
	I_{USB_100mA}	USB 2.0 low-power device detected	T_A = 0°C to +85°C			100	
			T_A = -40°C to +85°C			102.5	
	I_{USB_500mA}	USB 2.0 high-power device detected				500	
USB Input Current Limit	I_{SUS}	During suspend			0		mA
	I_{ENU}	During USB enumeration, T_A = +25°C		80	90	98	
	I_{USB_LP}	USB 2.0 low-power device detected, T_A = +25°C		80	90	98	
	I_{USB_HP}	USB 2.0 high-power device detected		460	475	490	
	I_{LIMIT}	ILIM = 000, T_A = +25°C		80	90	98	
		ILIM = 001 (default)		460	475	490	
		ILIM = 010			600		
		ILIM = 011			700		
		ILIM = 100			900		
		ILIM = 101			1000		
		ILIM = 110, T_A = +25°C (Note 3)		1344	1500	1650	
		ILIM = 110, T_A = -40°C to +85°C		1324	1500	1700	
$V_{BUS\_}$ to $V_{SYS\_}$ On-Resistance		V_{BUS} = 5V, I_{SYS} = 400mA			200	320	mΩ
$V_{SYS\_}$ to $V_{BAT\_}$ Reverse Regulation		When SYS is in regulation and charging stops, $V_{SYS\_}$ falling, 50mV typical hysteresis		V_{BAT} - 80mV	V_{BAT} - 50mV	V_{BAT} - 20mV	
Input Limiter Soft-Start Time		Input current ramp time			50	100	µs
Thermal-Limit Start Temperature	T_{DIE_LIM}	THERM_REG = 00			90		°C
		THERM _REG = 01			100		
		THERM _REG = 10			110		
		THERM _REG = 11			120		
Thermal-Limit Triggers $\overline{IRQ}$				T_{DIE_LIM} + 10°C			°C
Thermal-Limit Gain		I_{SYS} reduction/die temperature			5		%/°C
SYS Regulation Voltage		V_{BAT} > 3.45V, I_{SYS} = 1mA to 1.6A			140mV + V_{BAT}	210mV + V_{BAT}	V

ELECTRICAL CHARACTERISTICS (continued)

(THM = AGND, CEN = INT_3V3, V_{BAT} = 4.2V, $V_{BUS\_}$, $\overline{EXT\_PWRON}$, $\overline{UOK}$, $\overline{IRQ}$, CHG_TYPE, and $\overline{CHG\_STAT}$ are unconnected, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Minimum SYS Regulation Voltage	V_{SYS_MIN}	V_{BUS} = 6V, I_{SYS} = 1mA to 1.6A	V_SYS = 00			3.4		V
			V_SYS = 01	T_A = 25°C	4.2	4.35	4.524	
				T_A = -40°C to +85°C	4.185	4.35	4.524	
			V_SYS = 10			4.4		
			V_SYS = 11			4.5		
Undervoltage Lockout	V_{SYS_UVLO}	$V_{BUS\_}$ = 5.5V rising				3.0		V
		$V_{BUS\_}$ = 5.5V falling			2.6	2.85	3.1	
CHARGER								
BAT-to-SYS On-Resistance		V_{BAT} = 4.2V, I_{SYS} = 200mA				55	80	mΩ
BAT Undervoltage Lockout (Register 0x10h, Bit 7 = 0)	$V_{BAT\_UVLO\_F}$	V_{BAT} falling	BAT_UVLO_VPREQ = 1 (Register 0x10h)		2.15	2.40	2.65	V
	$V_{BAT\_UVLO\_R}$	V_{BAT} rising			2.45	2.70	2.95	
	$V_{BAT\_UVLO\_F}$	V_{BAT} falling	BAT_UVLO_VPREQ = 0 (default, Register 0x10h)		1.60	1.85	2.10	
	$V_{BAT\_UVLO\_R}$	V_{BAT} rising			1.85	2.10	2.35	
Charger Soft-Start Time						1		ms
BAT Leakage Current		V_{BAT} = 4.2V	V_{BUS} not connected			2	6	µA
			V_{BUS} connected, V_{CEN} = 0V			6	15	
PRECHARGE MODE								
BAT Precharge Current	I_{PCHG}	V_{BAT} > 1.4V (Note 5)				50*		mA
BAT Prequalification Threshold	$V_{BAT\_PCHG\_F}$	V_{BAT} falling	BAT_UVLO_VPREQ = 1 (Register 0x10h)		2.60	2.70	2.80	V
	$V_{BAT\_PCHG\_R}$	V_{BAT} rising			2.70	2.80	2.95	
	$V_{BAT\_PCHG\_F}$	V_{BAT} falling	BAT_UVLO_VPREQ = 0 (default, Register 0x10h)		2.05	2.15	2.25	
	$V_{BAT\_PCHG\_R}$	V_{BAT} rising			2.15	2.25	2.40	
FAST-CHARGE MODE								
BAT Charge-Current Set Range	I_{FCHG}	I_{FCHG} = 000				100		mA
		I_{FCHG} = 010 (default)				200		
		I_{FCHG} = 001				300		
		I_{FCHG} = 110				370		
		I_{FCHG} = 111				450		
		I_{FCHG} = 011				600		
		I_{FCHG} = 100				800		
		I_{FCHG} = 101				900		

ELECTRICAL CHARACTERISTICS (continued)

(THM = AGND, CEN = INT_3V3, V_{BAT} = 4.2V, $V_{BUS\_}$, $\overline{EXT\_PWRON}$, $\overline{UOK}$, $\overline{IRQ}$, CHG_TYPE, and $\overline{CHG\_STAT}$ are unconnected, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
BAT Fast-Charge Threshold	$V_{BAT\_FCHG\_R}$	V_{BAT} rising threshold, where charging current I_{FCHG} is reduced to I_{TCHG}	BAT_FCHG = 00			3.8		V
			BAT_FCHG = 01			3.9		
			BAT_FCHG = 10 (default)		3.88	4	4.12	
			BAT_FCHG = 11			4.1		
	$V_{BAT\_FCHG\_HYS}$	V_{BAT} hysteresis, the falling threshold where charging current is increased to I_{FCHG} is: $V_{BAT\_FCHG\_HYS} = V_{BAT\_FCHG\_R} - V_{BAT\_FCHG\_F}$	BAT_FCHG_HYS = 00			150		mV
			BAT_FCHG_HYS = 01 default			200		
			BAT_FCHG_HYS = 10			250		
			BAT_FCHG_HYS = 11			300		
TOP-OFF CHARGE MODE								
Top-Off Charge Current	I_{TCHG}	V_{BAT} > 1.4V (Note 5)	TCHG = 00			0.4 x I_{FCHG}		mA
			TCHG = 01			0.6 x I_{FCHG}		
			TCHG = 10			0.8 x I_{FCHG}		
			TCHG = 11 (default)			1.0 x I_{FCHG}		
Charge DONE Qualification (Note 3)	I_{CHG_DONE}	CHG_DONE = 000				10		mA
		CHG_DONE = 001				20		
		CHG_DONE = 010			30	40	50	
		CHG_DONE = 011			37.5	50	62.5	
		CHG_DONE = 100 (default)			45	60	75	
		CHG_DONE = 101				80		
		CHG_DONE = 110				100		
		CHG_DONE = 111				120		
BAT Regulation Voltage	V_{BAT_REG}	$I_{BAT\_}$ = 0mA	BAT_REG = 00			4.05		V
			BAT_REG = 01			4.10		
			BAT_REG = 10			4.15		
			BAT_REG = 11 (default)	T_A = +25°C	4.179	4.200	4.221	
				T_A = 0°C to +85°C	4.158	4.200	4.242	

ELECTRICAL CHARACTERISTICS (continued)

(THM = AGND, CEN = INT_3V3, V_{BAT} = 4.2V, $V_{BUS\_}$, $\overline{EXT\_PWRON}$, $\overline{UOK}$, $\overline{IRQ}$, CHG_TYPE, and $\overline{CHG\_STAT}$ are unconnected, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BAT Recharge Threshold	V_{BAT_RECHG}	With respect to V_{BAT_REG}	BAT_RECHG = 00 (default)		-350		mV
			BAT_RECHG = 10		-300		
			BAT_RECHG = 01		-250		
			BAT_RECHG = 11		-200		
CHARGE TIMER							
Prequalification Timer	t_{PCHG}	From start of precharge until end of prequalification charge model (Figure 10)	PCHG_TMR = 00		30		Minutes
			PCHG_TMR = 01		60		
			PCHG_TMR = 10 (default)		120		
			PCHG_TMR = 11		240		
Fast-Charge Timer	t_{FCHG}	From start of fast charge until maintains charge (Figure 10)	FCHG_TMR = 00		75		Minutes
			FCHG_TMR = 01		150		
			FCHG_TMR = 10		300		
			FCHG_TMR = 11 Default		600		
Maintain-Charge Timer	t_{MTCHG}	(Figure 11)	MTCHG_TMR = 10 (default)		0		Minutes
			MTCHG_TMR = 01		15		
			MTCHG_TMR = 00		30		
			MTCHG_TMR = 11		60		
Timer Accuracy				-30		+30	%
Timer Extend Threshold		Percentage of charge current below which timer clock operates at half speed			50		%
Timer Suspend Threshold		Percentage of charge current below which timer clock pauses			20		%
INSERTION AND REMOVAL DETECTION							
BAT Discharge Current	I_{DIS}	1V ≤ V_{BAT} ≤ 4.2V, C_{BAT} ≤ 10µF		0.375		1.125	mA
BAT Discharge Time	t_{DIS}	Discharge timer expires if V_{BAT} drop > V_{BAT_UVLO} threshold, battery cap ≤ 10µF			150		ms
Charge Debounce Timer	t_{DB}	Delay before checking charge done		100	150	200	ms
Battery Detecting Current	I_{BAT_DET}	Charging in prograss (precharge, fast-charge or maintain charge); if I_{BAT} < I_{BAT_DET} = battery absence		1	3	5	mA
ADAPTER TYPE DETECTION							
D- Current Sink	I_{DM_SINK}			50	100	150	µA
D+ Current source	I_{DP_SRC}			7		13	µA

ELECTRICAL CHARACTERISTICS (continued)

(THM = AGND, CEN = INT_3V3, V_{BAT} = 4.2V, $V_{BUS\_}$, $\overline{EXT\_PWRON}$, $\overline{UOK}$, $\overline{IRQ}$, CHG_TYPE, and $\overline{CHG\_STAT}$ are unconnected, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
D- Weak Current Sink	$I_{DM\_CD\_PD}$				0.1	µA
D+ Source Voltage	V_{DP_SRC}	I_{DP_SRC} = 200µA	0.5	0.6	0.7	V
D+ Detection Threshold	V_{DAT_REF}		0.25	0.32	0.40	V
D- Logic-High Threshold	V_{DM_IH}		0.8		2.0	V
D+ Logic-High Threshold	V_{DP_IH}		0.8		2.0	V
D+/D- Detection Threshold	DP_25% DM_25%	Detection threshold for custom chargers as % of V_{BUS}	23.75	25.0	26.25	%
	DM_34%		32.3	34	35.7	
	DP_47% DM_47%		44.65	47.00	49.4	
	DP_60% DM_60%		57	60	63	
D- Pulldown Resistor	R_{DM_DWN}		14.25		24.8	kΩ
D- Pullup Resistor	R_{DM_PU}	External resistor = 33Ω, low speed only	1.425	1.500	1.575	kΩ
D+ Pullup Resistor	R_{DP_PU}	External resistor = 33Ω, full speed only	1.425	1.500	1.575	kΩ
D+ Charger Detection Pullup Resistor	$R_{DP\_CD\_PU}$	$R_{DP\_CD\_PU}$ connected to INT_3V3	200	330	600	kΩ
Data Contact Detection Debounce Timer	t_{DCD_DBNC}			30		ms
D+ Source On Time	$t_{DP\_SRC\_ON}$		100			ms
D+ Source to High-Current Time	$t_{DP\_SRC\_HC}$		40			ms
Enumeration Time Limit	t_{ENUM}	Time from start of enumeration process until enumeration		10		s
Reenumeration Timer	t_{RE_ENUM}	Time from suspend mode until it re-enumerates, RWU_EN = 1		100		ms
Reconnect Timer	t_{FAULT}	Time from failed enumeration to adapter type detection reenabled, nENU_EN = 0		3		s
Detecting Time		D+/D- open power source nENU_EN = 1		100		ms
Enumeration Fail to Reconnect Timer	t_{ENU_FAULT}	Time from enumeration fail at 500mA until enumeration is retried at 100mA or time from enumeration fail at 100mA until reconnect timer is started		87		ms
XIN, XOUT PINS						
Oscillator Frequency Accuracy		Internal oscillator (low speed), T_A = +25°C	5.91	6.00	6.09	MHz
XIN, XOUT Input Capacitance		With external crystal (full speed)		3		pF

ELECTRICAL CHARACTERISTICS (continued)

(THM = AGND, CEN = INT_3V3, V_{BAT} = 4.2V, $V_{BUS\_}$, $\overline{EXT\_PWRON}$, $\overline{UOK}$, $\overline{IRQ}$, CHG_TYPE, and $\overline{CHG\_STAT}$ are unconnected, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
XIN Input Current		With external crystal (full speed)				10	µA
XIN Logic-High Input Voltage				0.667 x V_{INT_3V3}		V_{INT_3V3}	V
XIN Logic-Low Input Voltage						0.4	V
THERMISTOR MONITOR (THM)							
THM Hot Threshold	T_4	V_{THM} raising, 2% hysteresis			32.2		% of V_{INT_3V3}
THM Warm Threshold	T_3	V_{THM} raising, 2% hysteresis			46.5		
THM Cool Threshold	T_2	V_{THM} falling, 2% hysteresis			81.9		
THM Cold Threshold	T_1	V_{THM} falling, 2% hysteresis			88.7		
THM Disable Threshold		V_{THM} falling, 2% hysteresis			3.4		
THM Input Impedance	THM_{ZIN}	High impedance when no BUS or THM is disabled		500			kΩ
THM Input Leakage		THM = AGND THERM_EN = 0	T_A = +25°C	-1	0.001	+1	µA
			T_A = +85°C		0.01		
$\overline{EXT\_PWRON}$							
Logic-Low Output Voltage		Sinking 10mA			35	100	mV
High-Impedance Time	$t_{EXT\_PWR\_RESET}$	Time where $\overline{EXT\_PWRON}$ is high-impedance during transition between two $\overline{EXT\_PWRON}$ low states			63		ms
CHARGER STATUS ($\overline{CHG\_STAT}$)							
Logic-Low Output Voltage		Sinking 10mA			35	100	mV
Blink Period for Temperature Suspend Mode		50% duty cycle, battery present			1.5		s
Blink Period for Timeout Mode		50% duty cycle, battery present			0.15		s
LOGIC I/O: $\overline{UOK}$, CEN, $\overline{ENU\_EN\_HW}$, CHG_TYPE, IBUS_DEF, $\overline{IRQ}$, SDA, SCL, $\overline{STDB\_EN\_HW}$							
Logic Input Voltage		High level		1.3			V
		High level for SDA and SCL		1.4			
		Low level				0.4	
Logic Input-Leakage Current		V_{BUS} = 0V to 5.5V	T_A = +25°C		0.001	1	µA
			T_A = +85°C		0.01		
Logic-Low Output Voltage (CHG_TYPE, $\overline{IRQ}$, $\overline{UOK}$, Only)		Sinking 10mA			35	100	mV

ELECTRICAL CHARACTERISTICS (continued)

(THM = AGND, CEN = INT_3V3, V_{BAT} = 4.2V, $V_{BUS\_}$, $\overline{EXT\_PWRON}$, $\overline{UOK}$, $\overline{IRQ}$, CHG_TYPE, and $\overline{CHG\_STAT}$ are unconnected, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Logic-High Output-Leakage Current (CHG_TYPE, $\overline{IRQ}$, $\overline{UOK}$, Only)		V_{SYS} = 5.5V	T_A = +25°C		0.001	1	µA
			T_A = +85°C		0.01		
$\overline{UOK}$ Blink Period During USB Suspend		Only for USB automatically entering suspend mode, 50% duty cycle			1.5		s
$\overline{UOK}$ Blink Period with Open D+/D- Detected		50% duty cycle			0.15		s
I²C INTERFACE (See Figure 19) (Note 3)							
Clock Frequency						400	kHz
Bus-Free Time Between START and STOP	t_{BUF}			1.3			µs
Hold Time Repeated START Condition				0.6			µs
SCL Low Period	t_{LOW}			1.3			µs
SCL High Period	t_{HIGH}			0.6			µs
Setup Time Repeated START Condition	t_{SU_STA}			0.6			µs
SDA Hold Time	t_{HD_DAT}			0			µs
SDA Setup Time	t_{SU_DAT}			100			ns
Maximum Suppressed Pulse Width		Width of spikes that must be suppressed by the input filter of both SDA and SCL signals			50		ns
Setup Time for STOP Condition	t_{SU_STO}			0.6			µs
USB DATA INTERFACE							
Differential-Receiver Input Sensitivity	$\lvert V_{D+} - V_{D-} \rvert$			0.2			V
Differential-Receiver Common-Mode Voltage				0.8		2.5	V
D+, D- Input Impedance				300			kΩ
D+, D- Output Low Voltage	V_{OL}	R_{LOAD} = 1.5kΩ from V_{D-} to 3.6V				0.3	V
D+, D- Output High Voltage	V_{OH}	R_{LOAD} = 15kΩ from D+ and D- to AGND		2.8		3.6	V
Driver Output Impedance		Excludes external resistor		2	7	11	Ω
BUS Idle Time	t_{IDLE}	Only valid when an adapter type is detected as a USB 2.0 device; time BUS is inactive until charging current is reduced to $I_{SUSPEND}$			3		ms

ELECTRICAL CHARACTERISTICS (continued)

(THM = AGND, CEN = INT_3V3, V_{BAT} = 4.2V, $V_{BUS\_}$, $\overline{EXT\_PWRON}$, $\overline{UOK}$, $\overline{IRQ}$, CHG_TYPE, and $\overline{CHG\_STAT}$ are unconnected, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
USB Host Remote Wake-Up Timer	t_{RWU}	Time delay from suspend mode until it requests the host for a remote wake-up		100		ms
D+, D- Rise Time (Note 3)	t_{RISE}	C_L = 50pF to 600pF, low speed only	75		250	ns
		C_L = 50pF, full speed only	4		20	
D+, D- Fall Time (Note 3)	t_{FALL}	C_L = 50pF to 600pF, low speed only	75		250	ns
		C_L = 50pF to 600pF, full speed only	4		20	
Rise/Fall-Time Matching (Note 3)		C_L = 50pF to 600pF, low speed only	80		120	%
		C_L = 50pF to 600pF, full speed only	90		110	
Output-Signal Crossover Voltage		C_L = 50pF to 600pF, low speed only	1.3		2.0	V
INT_3V3 REGULATOR						
INT_3V3 Voltage		V_{BUS} = 5V, I_{INT_3V3} = 0 to 10mA	3.0	3.3	3.6	V
ESD PROTECTION (D+, D-, BUS_)						
Human Body Model		BUS bypassed with 1µF to AGND		±8		kV

Note 2: Specifications are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.

Note 3: Guaranteed by design. Limits not production tested.

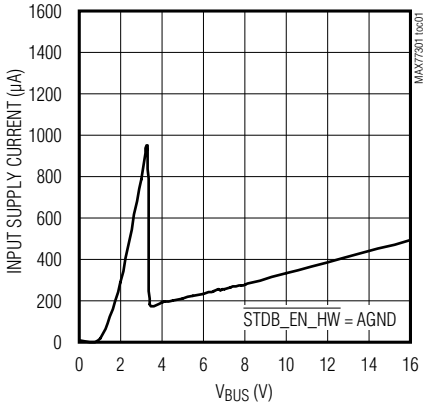
Note 4: Sum of input current limit and current used for INT_3V3.

Note 5: Maximum charging current is adaptively regulated to I_{ILIM} - I_{SYS} though maximum I_{CHG}.

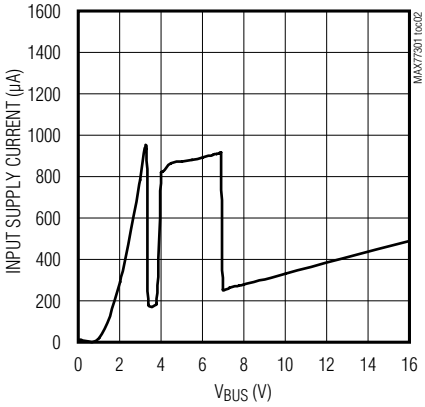
Typical Operating Characteristics

(Circuit of Figure 1, T_A = +25°C unless otherwise noted.)

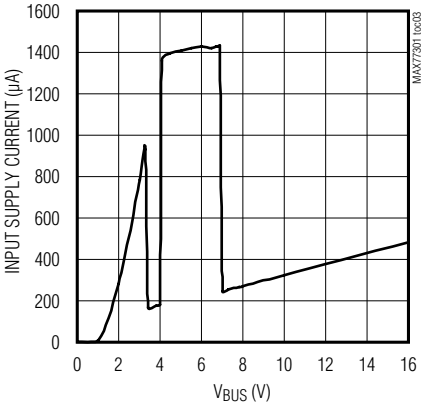
V_{BUS} INPUT SUPPLY CURRENT vs. V_{BUS} (SUSPEND MODE)



V_{BUS} INPUT SUPPLY CURRENT vs. V_{BUS} (FULL SPEED)



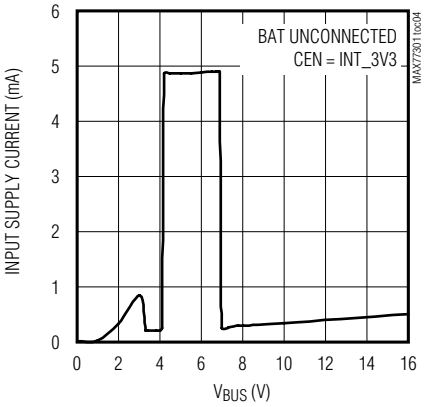
V_{BUS} INPUT SUPPLY CURRENT vs. V_{BUS} (LOW SPEED)



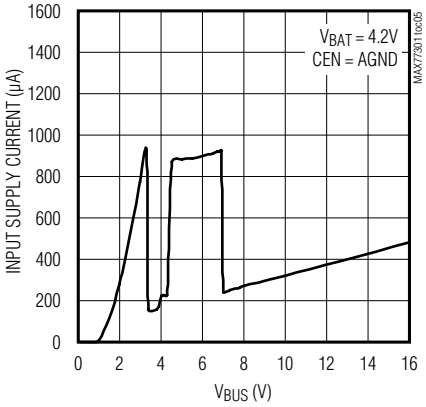
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C unless otherwise noted.)

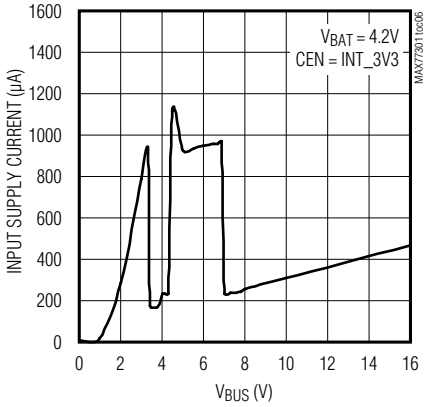
V_{BUS} INPUT SUPPLY CURRENT vs. V_{BUS} (CHARGER ENABLED)



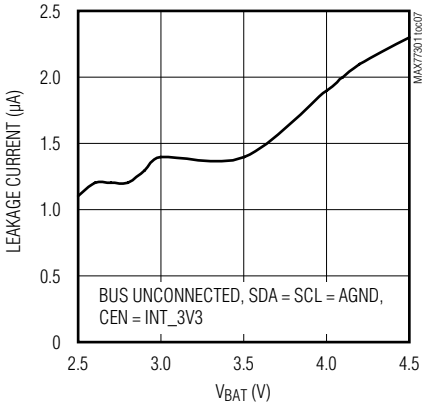
V_{BUS} INPUT SUPPLY CURRENT vs. V_{BUS} (CHARGER DISABLED)



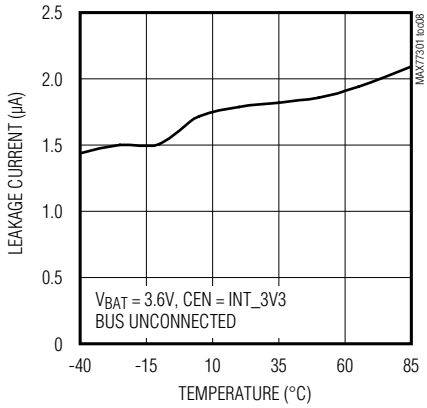
V_{BUS} INPUT SUPPLY CURRENT vs. V_{BUS} (CHARGER DISABLED)



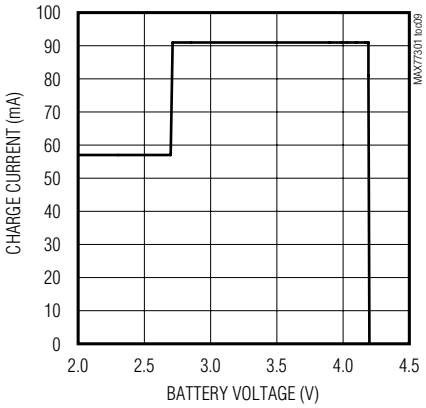
BATTERY LEAKAGE CURRENT vs. BATTERY VOLTAGE



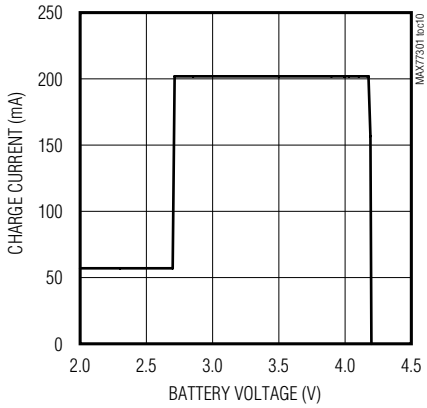
BATTERY LEAKAGE CURRENT vs. TEMPERATURE



CHARGE CURRENT vs. BATTERY VOLTAGE (LOW-POWER MODE)



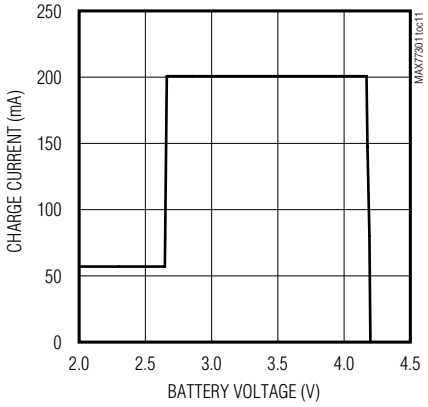
CHARGE CURRENT vs. BATTERY VOLTAGE (HIGH-POWER MODE)



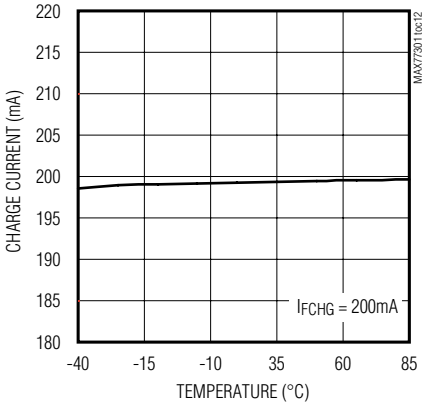
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C unless otherwise noted.)

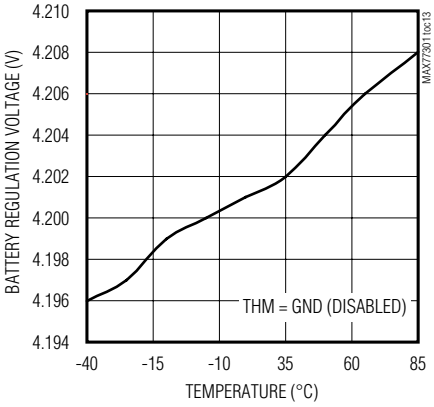
CHARGE CURRENT vs. BATTERY VOLTAGE (1A DEDICATED CHARGER)



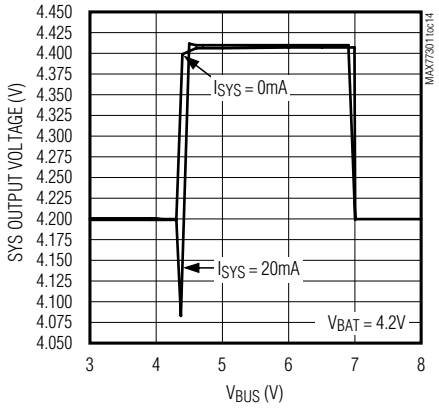
CHARGE CURRENT vs. AMBIENT TEMPERATURE



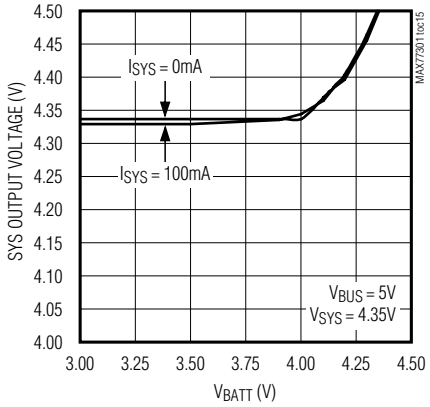
BATTERY REGULATION VOLTAGE vs. AMBIENT TEMPERATURE



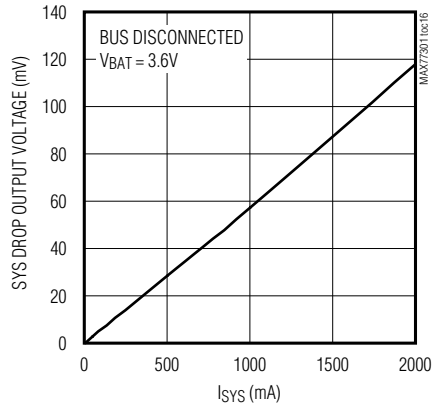
SYS OUTPUT VOLTAGE vs. V_{BUS}



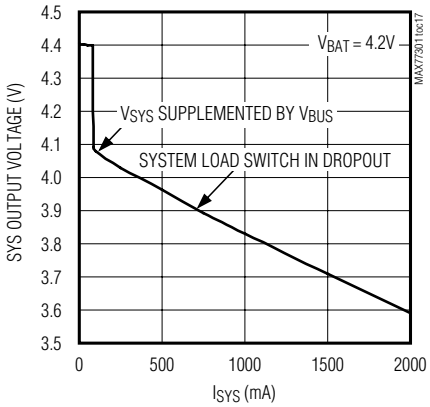
SYS OUTPUT VOLTAGE vs. BATTERY VOLTAGE



BAT-SYS VOLTAGE DROP vs. SYS CURRENT



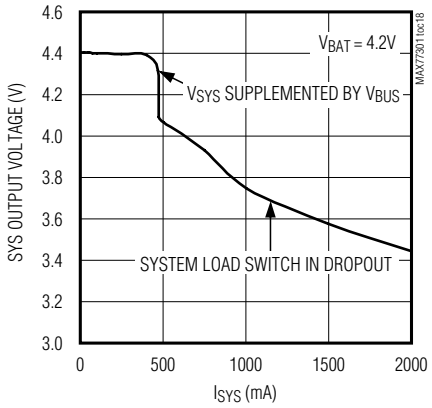
SYS OUTPUT VOLTAGE vs. LOAD CURRENT (USB LOW-POWER MODE)



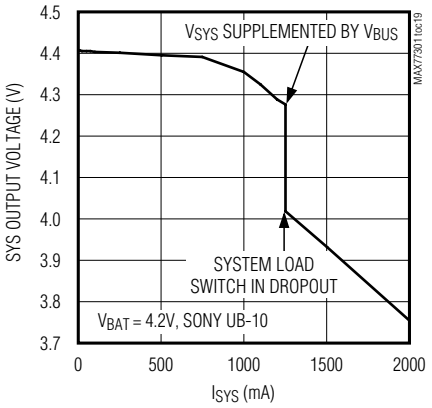
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C unless otherwise noted.)

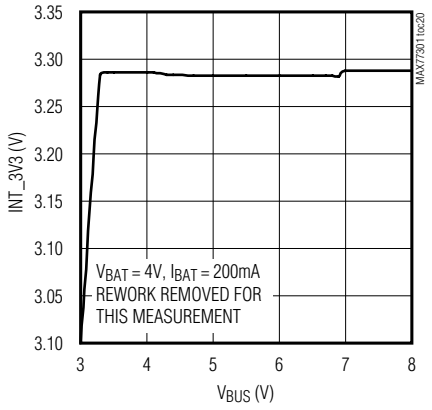
SYS OUTPUT VOLTAGE vs. LOAD CURRENT (USB HIGH-POWER MODE)



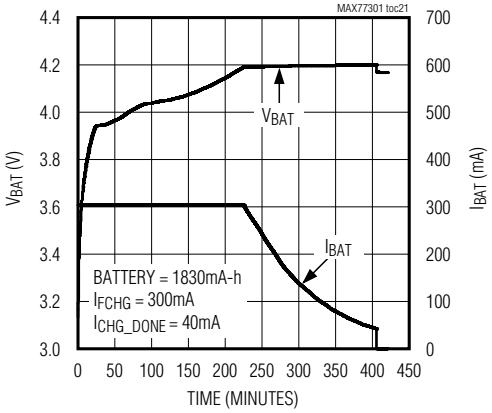
SYS OUTPUT VOLTAGE vs. LOAD CURRENT (DEDICATED CHARGER)



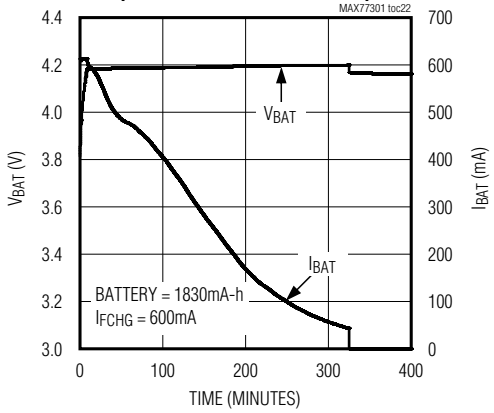
INT_3V3 VOLTAGE vs. BUS VOLTAGE



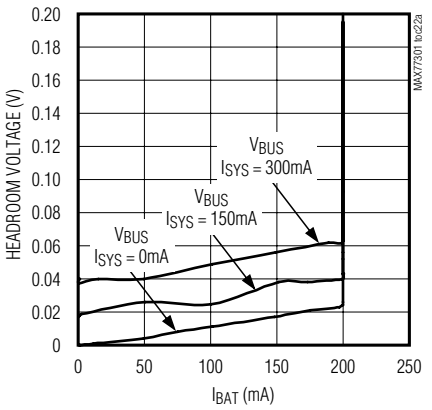
BATTERY CHARGE PROFILE



CHARGE PROFILE (HIGH-POWER USB CHARGER)



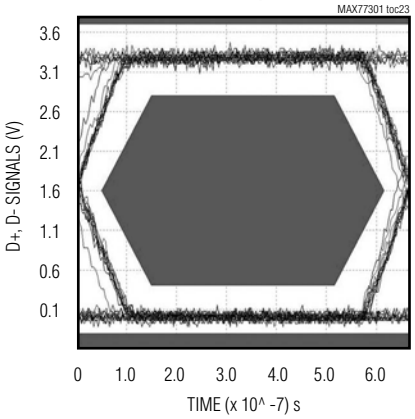
HEADROOM VOLTAGE vs. BATTERY CURRENT SYS VOLTAGE = 4.35V, I_{FCHG} = 200mA



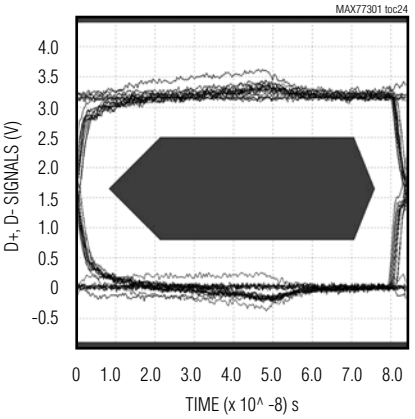
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C unless otherwise noted.)

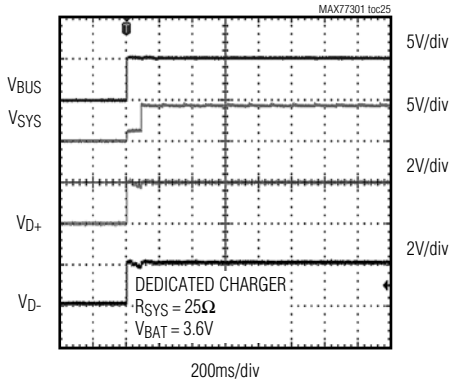
EYE DIAGRAM (LOW SPEED)



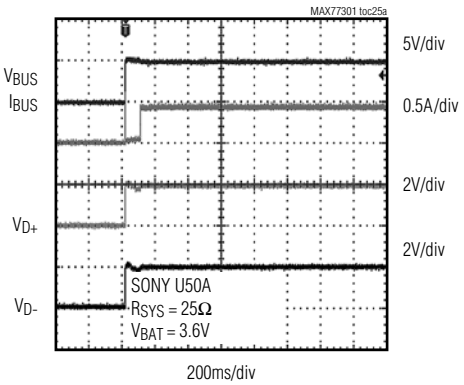
EYE DIAGRAM (FULL SPEED)



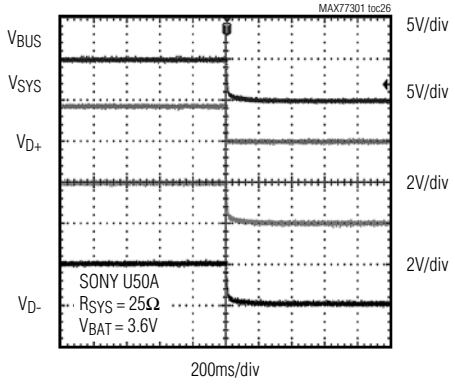
DEDICATED CHARGER CONNECT



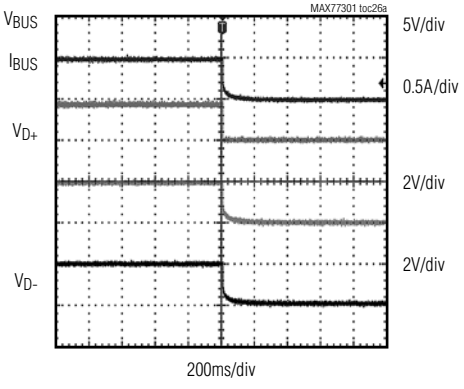
DEDICATED CHARGER CONNECT



DEDICATED CHARGER DISCONNECT



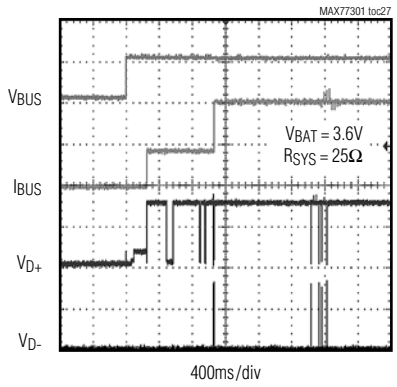
DEDICATED CHARGER DISCONNECT



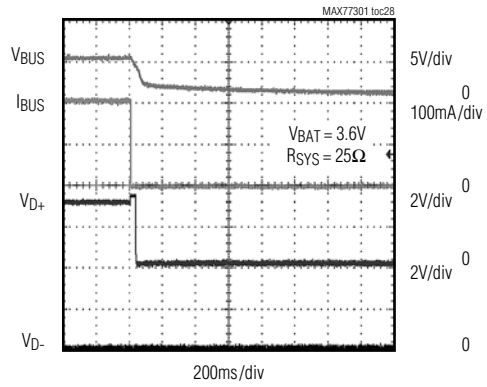
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C unless otherwise noted.)

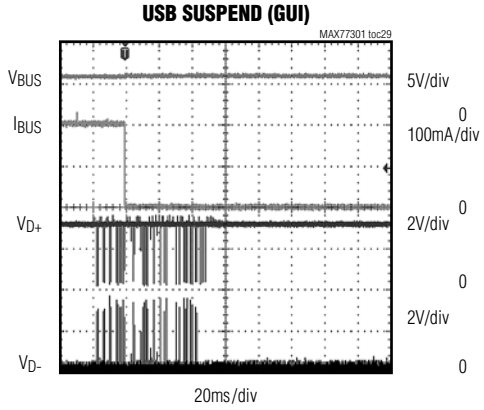
USB HIGH-POWER 2.0 CONNECT



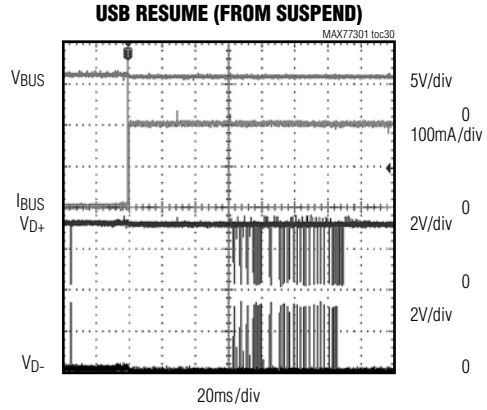
USB HIGH-POWER 2.0 DISCONNECT



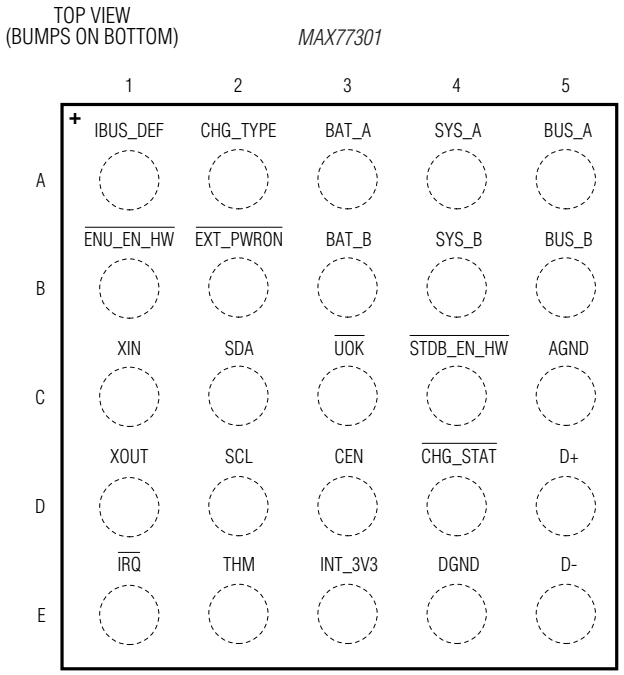
USB SUSPEND (GUI)



USB RESUME (FROM SUSPEND)



Bump Configuration



WLP
(0.4mm PITCH)

Bump Description

BUMP	NAME	FUNCTION	
A1	IBUS_DEF	Logic Input that Sets Input Current Limit. Only valid when enumeration is disabled or D+/D- are open. Logic-high programs the ILIM[2:0] register value. Logic-low sets the input current limit at 100mA.	
		Low	Input current limit = 100mA
		High	Input current limit = ILIM[2:0] (default = 500mA)
A2	CHG_TYPE	Open-drain Output. Used to signal to the processor the current capability of the external adapter. Connect this pin to ground if not used.	
		CHG_TYPE	**ADPATER TYPE**
		Low	USB 2.0 host 100mA or ILIM = 100mA
		High impedance	ILIMIT ≥ 500mA
A3, B3	BAT_A BAT_B	Li+ Battery Connection (V_{BAT}). Connect a single-cell Li+ battery from V_{BAT} to ground. Bypass V_{BAT} to DGND with a 10µF X5R or X7R ceramic capacitor. Both BAT_A and BAT_B must be connected together externally.	

Bump Description (continued)

BUMP	NAME	FUNCTION
A4, B4	SYS_A SYS_B	System Supply Output (V_{SYS}). Connect SYS_A and SYS_B to the system load. When a valid voltage is present at V_{BUS}, V_{SYS} is programmed by the greater of register V_SYS[1:0] or V_{BAT} + 0.14V (typ). When V_{BUS} is not present the SYS voltage is set to the battery voltage minus a small voltage drop determined by the system load. Bypass V_{SYS} to DGND with a 10µF X5R or X7R ceramic capacitor. SYS_A and SYS_B must be connected together externally.
A5, B5	BUS_A BUS_B	USB Power Input (V_{BUS}). Connect input power source to BUS_A and BUS_B. Bypass V_{BUS} to DGND with a 10µF X5R or X7R ceramic capacitor. BUS_A and BUS_B must be connected together externally.
B1	$\overline{\text{ENU\_EN\_HW}}$	Automatic Enumeration Enable. $\overline{\text{ENU\_EN\_HW}}$ is a logic-low input used to enable USB enumeration. Connect $\overline{\text{ENU\_EN\_HW}}$ to AGND to allow the IC to automatically perform enumeration. Connect to INT_3V3 or drive logic-high to disable automatic enumeration and enable adapter detection. In case of USB host/hub, do not initiate USB enumeration, but set input current according to IBUS_DEF. The nENU_EN_HW_MASK bit is used to determine if nENU_EN is controlled by $\overline{\text{ENU\_EN\_HW}}$ logic input or if controlled by I²C directly.
B2	$\overline{\text{EXT\_PWRON}}$	Open-Drain Output. Used to enable other parts of the system when valid supply is present. Connect this pin to ground if not used.
C1	XIN	Crystal Oscillator Input. For full-speed operation, connect XIN to one side of a parallel resonant 12MHz ±0.25% crystal and a 33pF capacitor to AGND. XIN can also be driven by an external clock referenced to INT_3V3. For low-speed operation only, a crystal or clock signal is not required. Connect XIN to AGND and connect XOUT to INT_3V3. In this case the internal oscillator is used, and only low-speed operation is supported.
C2	SDA	Data Input for I²C Serial Interface. Connect an external 2.2kΩ pullup resistor from SDA to the logic supply. SDA is high impedance when off.
C3	$\overline{\text{UOK}}$	Active-Low Adapter Type Detection. $\overline{\text{UOK}}$ is an open-drain output that pulls low when adapter detection is successfully completed. In USB suspend mode, $\overline{\text{UOK}}$ flashes with a duty cycle of 50% and a period of 1.5s. When D+/D- open is detected and bit nENU_EN = 1, the $\overline{\text{UOK}}$ pin flashes with a duty cycle of 50% and a period of 0.15s. When no adapter is detected, $\overline{\text{UOK}}$ is high impedance. Connect this pin to ground if not used.
C4	$\overline{\text{STDB\_EN\_HW}}$	Standby Mode Enable. $\overline{\text{STDB\_EN\_HW}}$ is a logic-low input used to force the IC into suspend mode. Connect $\overline{\text{STDB\_EN\_HW}}$ to INT_3V3 or drive logic high for automatic detect mode. In automatic detect mode the IC determines when to enter suspend mode depending on the status of SUS_EN register and USB conditions. The nSTDB_EN_HW_MASK bit determines if nSTDB_EN is controlled by $\overline{\text{STDB\_EN\_HW}}$ logic input or if controlled by I²C directly.
C5	AGND	Analog Ground. Connect AGND to quiet ground, including crystal oscillator and INT_3V3 ground nodes.
D1	XOUT	Crystal Oscillator Output. For full-speed operation, connect XOUT to one side of a parallel resonant 12MHz ±0.25% crystal and a 33pF capacitor to AGND. Connect XOUT unconnected if XIN is driven by an external clock. For low-speed operation only, a crystal or clock signal is not required. Connect XOUT to INT_3V3 and connect XIN to AGND. In this case the internal oscillator is used, and only low-speed operation is supported.

Bump Description (continued)

BUMP	NAME	FUNCTION
D2	SCL	Clock Input for Serial Interface. Connect an external 2.2kΩ pullup resistor from SCL to the logic supply. SCL is high impedance when off.
D3	CEN	Charger Enable Input. Logic-high input used to control charge status. Connect CEN to logic-high to enable battery charging when a valid source is connected at V_{BUS}. Connect to AGND or drive logic-low to disable battery charging. The $\overline{CEN\_MASK}$ bit is used to determine if CHG_EN is controlled by CEN logic input or if controlled by I²C directly.
D4	$\overline{CHG\_STAT}$	Charge Status Output. Logic-low open drain output indicating battery charging. When a temperature fault is detected, the output is pulsed at 50% duty cycle with a period of 1.5s. When a charge timer fault is detected $\overline{CHG\_STAT}$ is pulsed at 50% duty cycle with a period of 0.15s. When no battery is connected, $\overline{CHG\_STAT}$ is pulsed at a 0.1s period and 10%–20% duty cycle. Connect this pin to ground if not used.
D5	D+	USB D+ Signal. Connect a 33Ω resistor between D+ a USB connector to add signal integrity.
E1	$\overline{IRQ}$	Interrupt Request. Logic-low open-drain output that indicates when an interrupt has occurred.
E2	THM	Thermistor Input. Battery temperature detect input. Connect a negative temperature coefficient (NTC) thermistor close to the battery pack. Connect the other thermistor lead to AGND. Connect a pullup resistor from THM to INT_3V3 (47kΩ pullup resistor is recommended with a 100kΩ thermistor). Connect to AGND to disable this feature. Note the thermistor and pullup resistor are required for battery NTC detection mode.
E3	INT_3V3	3.3V Logic Supply Output. Connect a 1µF capacitor from INT_3V3 to AGND. The output is rated for up to a 10mA load. The INT_3V3 output is active whenever a valid voltage is present on BUS_ pins.
E4	DGND	Digital Ground. Connect DGND to power ground, including input capacitor, system capacitor, and battery capacitor ground nodes.
E5	D-	USB D- Signal. Connect a 33Ω resistor between D- a USB connector.

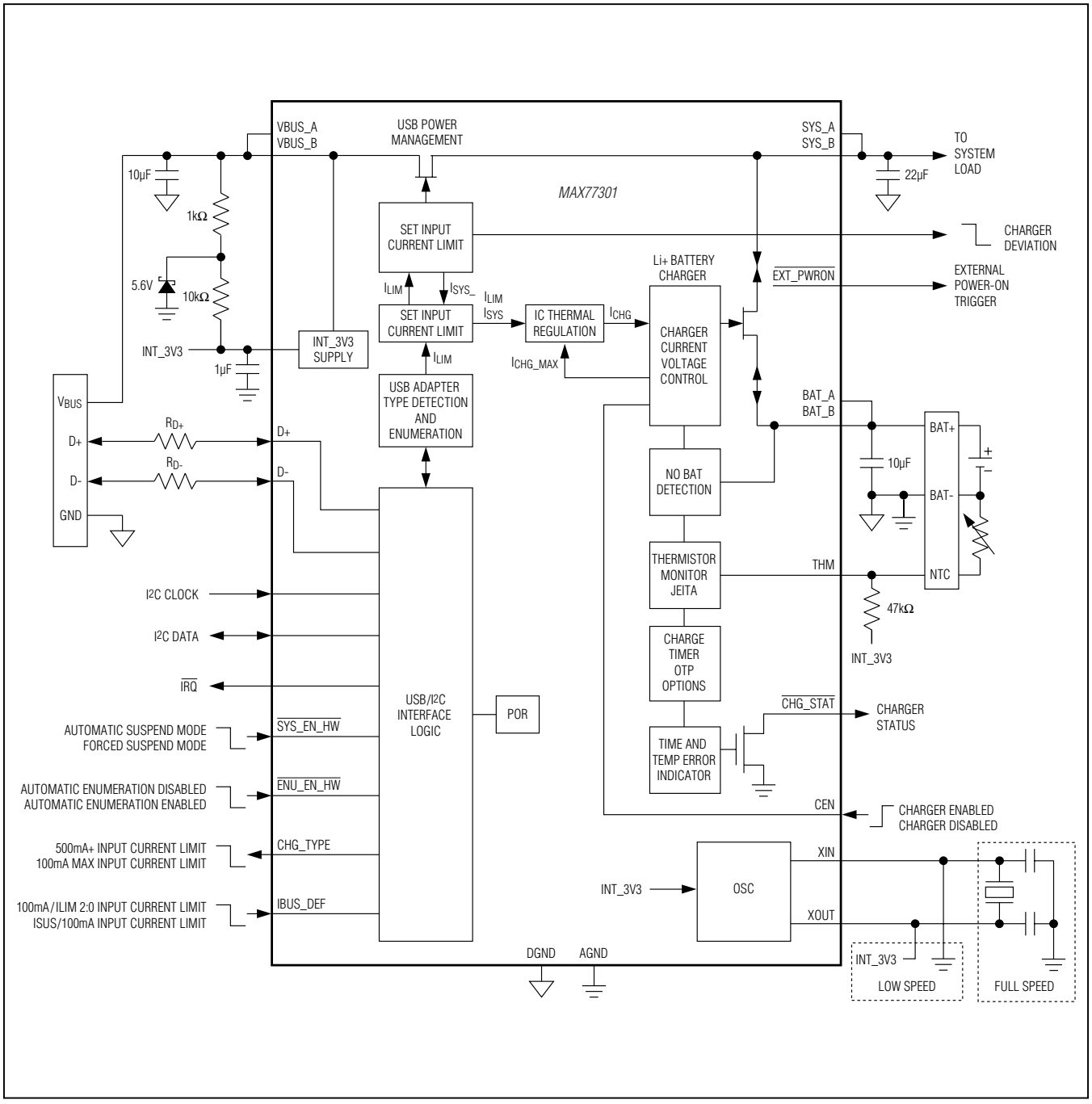


Figure 1. Block Diagram and Typical Application Circuit

Detailed Description

The MAX77301 is a USB-compliant linear battery charger that operates from a USB port, a dedicated charger, or a universal adapter. The IC provides automatic detection of adapter type and enumeration with a USB host. All power switches and charging circuitry is integrated.

The IC is capable of negotiating more than 100mA of charging current from a USB host or hub without processor intervention. Alternatively, the IC automatically detects a dedicated charger and sets the input current limit accordingly. The battery charge current and the input current limit can be set up to 900mA and 1500mA, respectively. If enumeration is disabled or a nonvalid adapter is connected to the IC the current depends on the logic level of IBUS_DEF (IBUS_DEF logic-low sets the current limit to 100mA; logic-high sets the current limit to register value ILIM[2:0] (default = 500mA).

Data Contact Detection

USB plugs are designed so that when the plug is inserted into the receptacle, the power pins make contact before the data pins make contact. This ensures that BUS voltage is applied to data pin contact.

To detect when the data pins have made contact, the data pins are prebiased so at least one of the data pins changes state. When this change is detected, the IC is allowed to check which type of port is attached.

The IC has two different modes of operation during the data contact detection.

The first mode allows up to 3s (see the *Electrical Characteristics* table) for the D+/D- to be connected. If D+/D- are still open after 3s, an interrupt is issued and the IC allows the input current to be user defined. The IC continues to monitor D+ and D- for connection.

The second mode occurs when enumeration is disabled. In this mode, the IC initiates with user defined current limit and then transitions to the ideal charging current determined by the USB enumeration engine.

Power-On Reset

To guarantee the correct startup, the IC triggers power-on reset when a valid adapter or battery is detected. Power-on reset ensures that all I²C registers are set to the default values.

When only a battery is connected to the IC and the battery voltage is above $V_{BAT\_UVLO\_F}$ all internal circuitry is powered down except the internal BAT to SYS switch, UVLO comparator, and I²C. If the battery voltage drops below $V_{BAT\_UVLO\_F}$, the I²C interface and the BAT to SYS switch are disabled.

If a valid power source is present at the BUS input, the mode of operation depends on the battery voltage.

For battery voltage above $V_{BAT\_UVLO\_F}$: The system is supported by battery power when the external adapter current limit is exceeded.

For battery voltage below $V_{BAT\_UVLO\_F}$: The system cannot be supported by an external adapter and battery power. The IC enters fault mode and the charger input current is disabled. This is done to ensure that system does not continuously attempt to start up with an underpowered adapter. Exit this mode by disconnecting the adapter. Use this mode to disconnect the charger.

Interrupt Request ($\overline{IRQ}$)

$\overline{IRQ}$ is an active-low, open-drain output signal that indicates an interrupt event has occurred and status information is available in the EVENT_ and STATUS_ registers. Interrupts indicate temperature and voltages and current fault conditions. Events are triggered by a state change in the associated register. The event registers are reset to default condition when read. When the EVENT_ registers are read in page mode the $\overline{IRQ}$ is not released until the last bit been read. New interrupt events are held until a complete read of all registers has occurred.

USB Interface

An integrated USB peripheral controller provides autoenumeration in full-speed and low-speed modes. The USB controller completes the following tasks:

- Adapter type detection, or
- USB enumeration with USB type inputs

With no crystal oscillator, the IC operates in USB low-speed mode. An external 12MHz crystal oscillator and decouling capacitors are required for USB full-speed mode. This flexibility allows the IC to interface with any USB connector type.

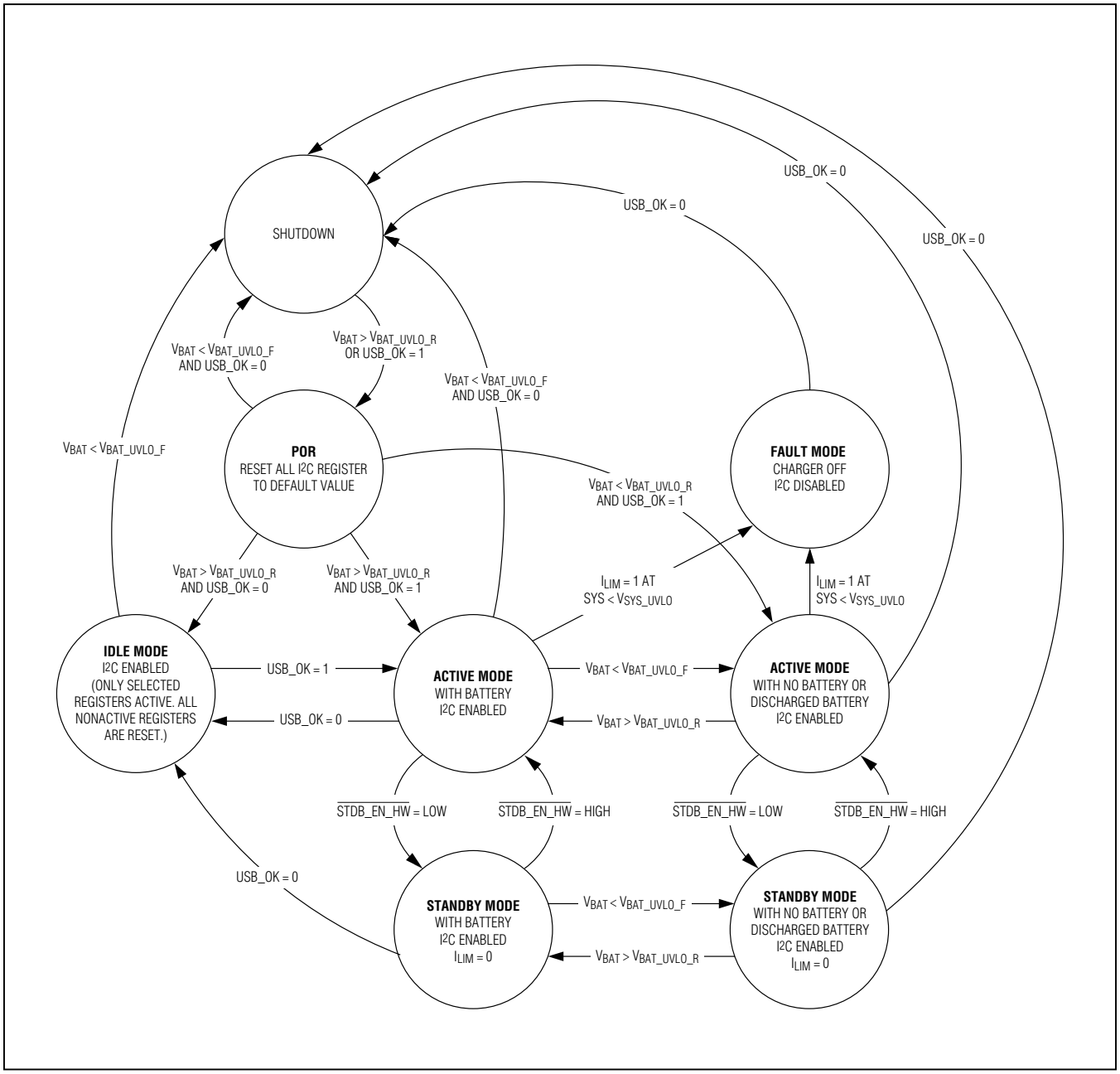


Figure 2. Power-On Reset State Diagram

Table 1. Status Registers

PIN	CONTROL REGISTER	STATUS REGISTER	DESCRIPTION
$\overline{\text{STDB\_EN\_HW}}$	0x09	0x04	During power-on reset of the IC, the logic status of the input $\overline{\text{STDB\_EN\_HW}}$ is used to set the default value of nSTDB_EN. The standby control is always controlled by the value of the nSTDB_EN I²C bit. The nSTDB_EN bit can be set using HW input $\overline{\text{STDB\_EN\_HW}}$ or by writing directly to the nSTDB_EN bit using I²C. The mode of operation is determined by nSTDB_EN_MASK. Setting this bit to 0 forces the nSTDB_EN to always be equal to the logic input $\overline{\text{STDB\_EN\_HW}}$. Setting nSTDB_EN_MASK to 1 disables the $\overline{\text{STDB\_EN\_HW}}$ logic input and only I²C can be used to change the value of the nSTDB_EN bit. The status of $\overline{\text{STDB\_EN\_HW}}$ can always be read from register 0x04h.
$\overline{\text{ENU\_EN\_HW}}$	0x09	0x04	During power-on reset of the IC, the logic status of the input $\overline{\text{ENU\_EN\_HW}}$ is used to set the default value of nENU_EN. The enable of automatic enumeration is always controlled by the value of the ENU_EN I²C bit. The nENU_EN bit can be set using HW input $\overline{\text{ENU\_EN\_HW}}$ or by writing directly to the nENU_EN bit using I²C. The mode of operation is determined by the nENU_EN_MASK. Setting this bit to 0 forces nENU_EN to always be equal to the logic input nENU_EN_HW. Setting nENU_EN_MASK to 1 disables the $\overline{\text{ENU\_EN\_HW}}$ logic input so only I²C can be used to change the value of the nENU_EN bit. The status of $\overline{\text{ENU\_EN\_HW}}$ can always be read using the nENU_EN_HW in 0x04h.
IBUS_DEF	N/A	0x04	When the nENU_EN bit = 1, the logic stat on the IBUS_DEF pin sets the input current limit for certain type of chargers. This type of charger is: • D+/D- open • nENU_EN is set to 1 and adapter type is DCP or SDP For this type of adapter, the input current limit is set to following: IBUS_DEF = L: 100mA IBUS_DEF = H: Determined by contents of register, ILIM[2:0]
CEN	0x0C	0x04	During power-on reset of the IC, the logic status of CEN is used to used to set the default value of CHG_EN. The status of the charger is always equal to the CHG_EN bit. The CHG_EN bit can be set using HW input CEN or by writing directly to the CHG_EN bit using I²C. The mode of operation is determined by the CEN_MASK. Setting the CEN_MASK bit to 0 forces CHG_EN to always be equal to the logic input CEN. Setting CEN_MASK to 1 disables CEN so only I²C can be used to change the value of the CHG_EN bit. The status of CEN can always be read using the CEN in 0x04h.
XIN/XOUT	N/A	0x04	The FS_DET bit register 0x04 is used to read the status of the external crystal connection. A 0 indicates only low speed operation is active. A 1 indicates full speed is supported.

Table 2. Adapter Type

ADAPTER TYPE	OUTPUT VOLTAGE	OUTPUT CURRENT
Dedicated charger	4.75V to 5.25V at I_{LOAD} < 500mA 2.0V to 5.25V for $I_{LOAD} \geq$ 500mA	500mA to 1.8A
Charger downstream port	4.75V to 5.25V at I_{LOAD} < 500mA 2.0V to 5.25V for $I_{LOAD} \geq$ 500mA	500mA to 900mA for low speed, full speed, and full speed 500mA to 1.5A for low speed and full speed
Apple 500mA	4.75V to 5.25V at I_{LOAD} < 500mA	500mA (max)
Apple 1A	4.75V to 5.25V at I_{LOAD} < 1A	1A (max)
Apple 2A	4.75V to 5.25V at I_{LOAD} < 2A	2A (max)
Sony 500mA	4.75V to 5.25V at I_{LOAD} < 500mA	500mA (max)
Sony 500mA Type B	4.75V to 5.25V at I_{LOAD} < 500mA	500mA (max)
USB 2.0 low power	4.25V to 5.25V	100mA (max)
USB 2.0 high power	4.75V to 5.25V	500mA (max)

D+ and D-

D+ and D- are the I/O data pins for the internal USB transceiver. These pins are ESD protected up to ±8kV. Connect D+ and D- to a USB B or custom connector through external 33Ω series resistors. The IC automatically configures D+/D- with an automatic switchable 1.5kΩ pullup resistor for D- for low-speed and D+ for full-speed.

Low/Full Speed

The IC can operate as a low-speed or a full-speed slave device. Full-speed mode requires an external 12MHz crystal oscillator connected to XIN and XOUT.

The IC has an 6MHz internal clock for use in low-speed mode. For low-speed mode, tie XIN and the AGND pin and XOUT to the INT_3V3 pin.

Adapter Detection

Upon insertion, the IC identifies the type of adapter.

Adapter types include:

- Dedicated charger
- Noncompliant dedicated chargers
- Charger downstream port (host or hub)
- USB 2.0 (host or hub) low power
- USB 2.0 (host or hub) high power

The IC determines the adapter type and programs the appropriate current limit and battery charge level, as shown in Figure 3.

Low-Power Mode

The nSTDB_EN bit forces the system to operate from battery power. The current drawn in this mode is less than 500nA for the low-speed mode and 2.5mA for the full-speed mode. In this mode, the D+ and D- lines are high impedance. The I^2C interface is maintained.

USB Suspend

According to USB 2.0 specifications, when a USB host stops sending traffic for more than 3ms, the peripheral must enter a power-down state called SUSPEND after no more than 10ms of inactivity. Once suspended, the peripheral must have enough of its internal logic active to recognize the host's resume signaling, or for generating remote wakeup.

When no activity is present on D+/D- for 3ms (typ) ,the IC automatically enters suspend mode to be complaint with the USB specification. To enter suspend mode, SUS_EN must be enabled by a logic 1 in register 0x09h. When entering suspend mode, the charger is disabled and SYS is powered from BAT to reduce the input current drawn from BUS to less than 500µA. In low-speed suspend state, the bus is IDLE: D+ is low and D- is kept high by a pullup resistor. In full-speed suspend state, the bus is IDLE: D- is low and D+ is kept high by a pullup resistor.

During suspend mode $\overline{UOK}$ pulses with a 1.5s period and 50% duty cycle.

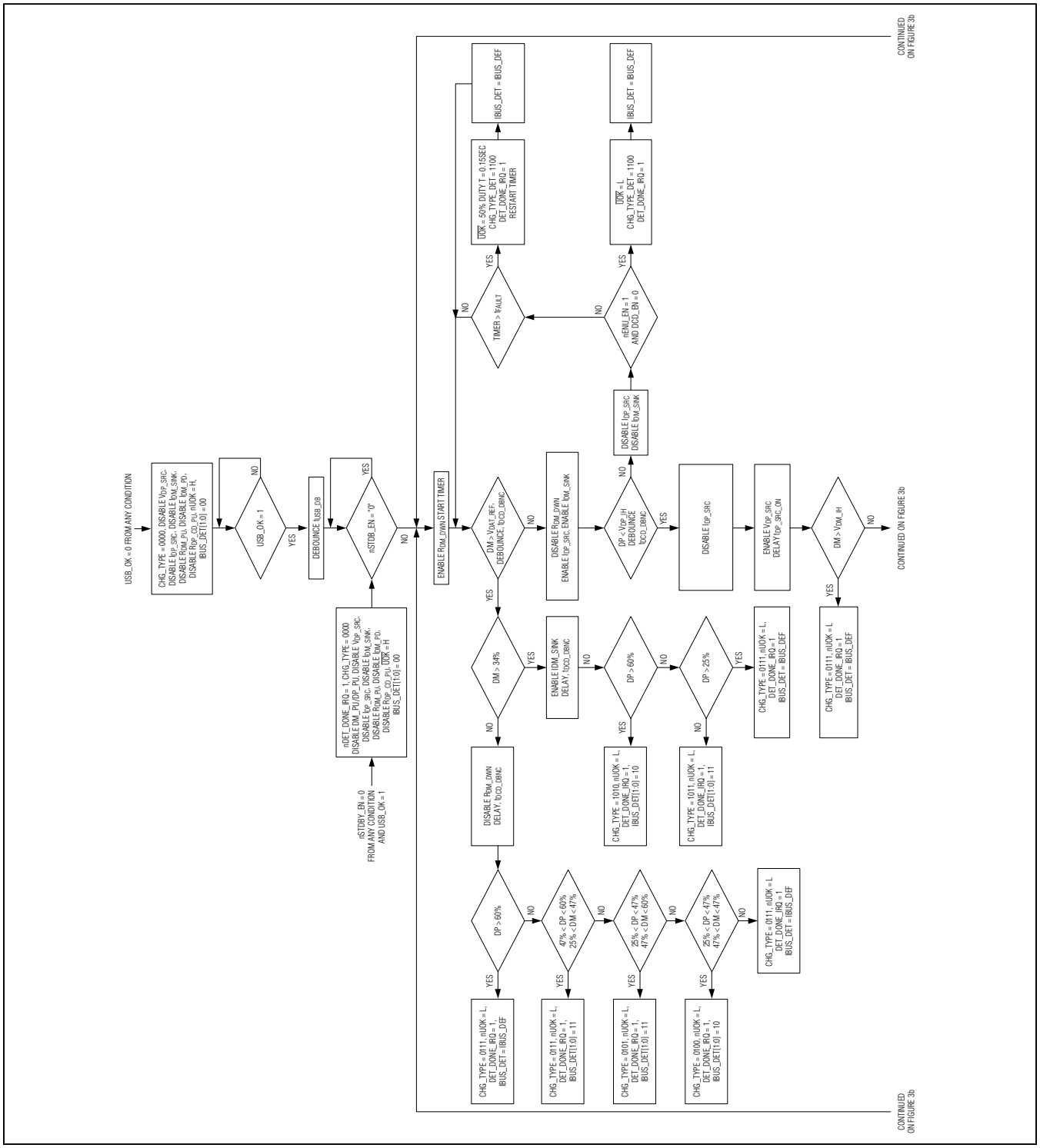


Figure 3a. Adapter Detection Flow Chart

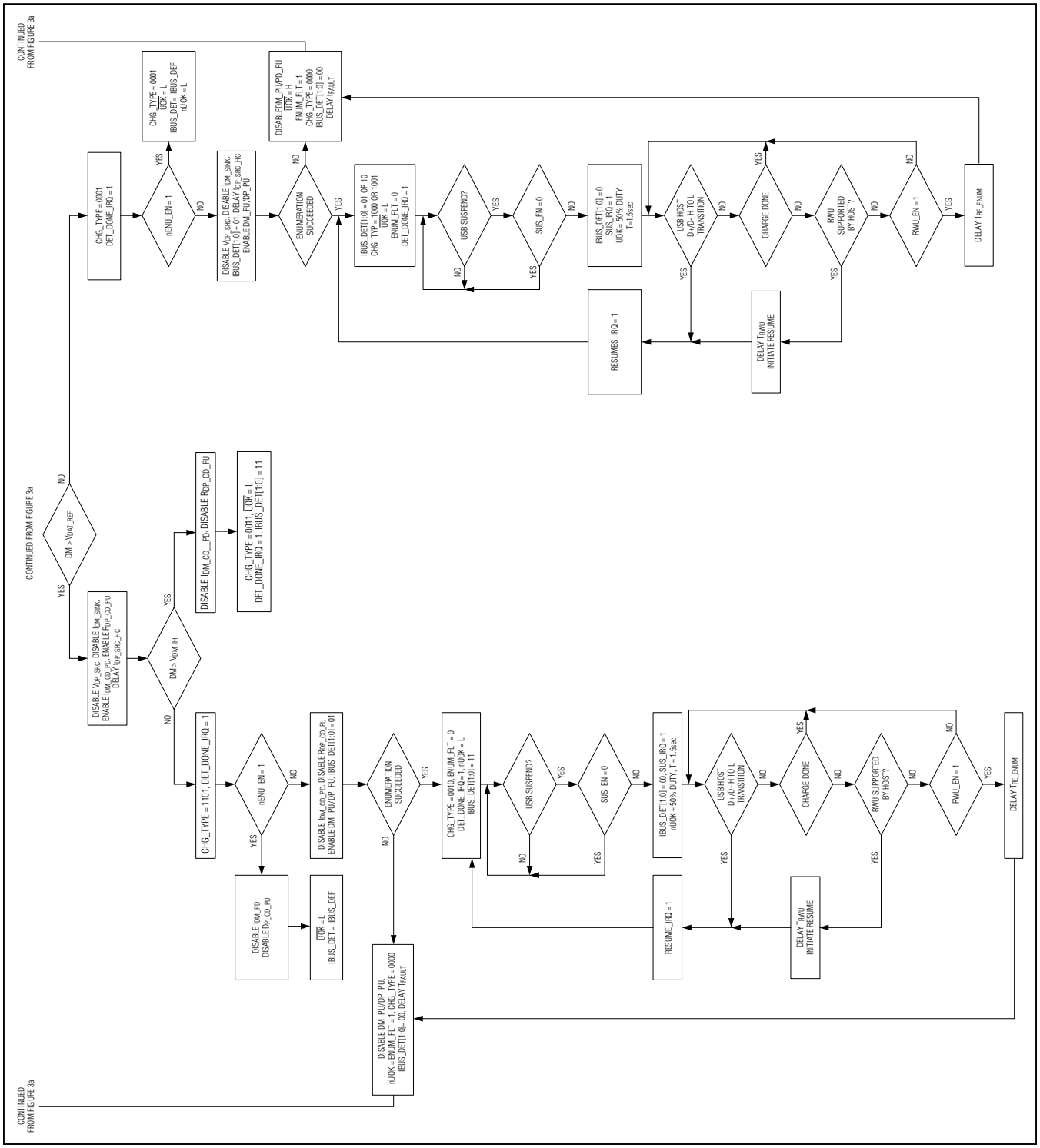


Figure 3b. Adapter Detection Flow Chart

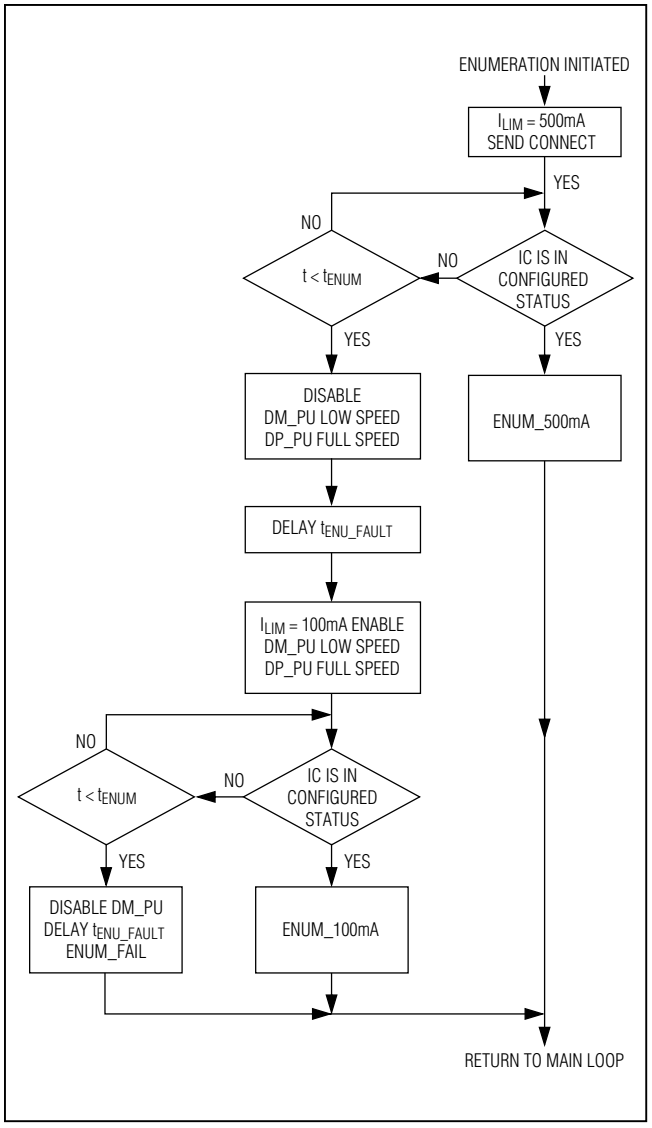


Figure 4. Enumeration Flow Chart

Keyboard Test Mode

In normal operation, keyboard test mode is disabled. This function is only used during USB certification.

Writing a 1 to the KB_TM_EN bit while writing a 0 to nENU_EN_HW_MASK enters keyboard test mode and disables the logic input $\overline{ENU\_EN\_HW}$. Toggling this logic input while in keyboard test mode sends a mute command that is used to generate traffic on the USB interface as well as verification of golden tree commands.

Wake-Up and USB Resume

The IC can wake up from suspend mode four ways:

- By setting nSTDB_EN to 0 followed by 1 to initiate redetection of the adapter type.
- If nSTDB_EN is 1 and SUS_EN is 1, the IC monitors the bus activity on the D+/D- line. If the host resumes bus activity the IC detects this as a 1 to 0 transition on D+/D-. Once this occurs, the device restarts the oscillator and waits for it to stabilize.
- Remote wake-up can be enabled by the host during the enumeration process. Once suspended the state of the battery charger is monitored. If the charger is not in the DONE state, the IC initiates a remote wake-up signal. If the charger is in the DONE state, a remote wake-up is not initiated until the RESTART threshold is reached.

  When the IC initiates a remote wake-up, it first restarts the oscillator and waits for the oscillator to stabilize. Then it sends the remote wake-up event to signal the host that it needs to be driven out of the suspend status.
- If RWU_EN is a logic 1 in register 0x09 and the remote wake-up feature has not been set by the host during enumeration, the IC waits t_{RE_ENUM} after entering suspend mode, then disconnects the pullup resistor from D+ or D- and reinitiates the charger-type detection.

USB Enumeration

When the USB 2.0 host/hub or charger downstream port detects a peripheral (MAX77301), it interrogates the device to learn about its capabilities and requirements, and configures it to bring it online. This process is known as enumeration. USB bus enumeration identifies and assigns unique addresses to the devices connected to the bus.

Once the IC detects V_{BUS} is valid for t_{USB_DB}, the IC initiates the detection process to determine the type of device connected. If the device is a USB 2.0 host/hub or charger downstream port and nENU_EN is logic 0, the IC connects a 1.5kΩ pullup resistor from D- (low speed) or D+ (full speed) to INT_3V3. If nENU_EN is set to 1, the pullup resistor from D-/D+ to INT_3V3 is disabled and the current limit is set according to IBUS_DEF logic input.

During enumeration the host sends multiple requests to the device (MAX77301) requesting for a descriptor (stored in ROM table data) that defines the device.

The enumeration is managed by the IC's serial interface engine (SIE) without any processor intervention.

The SIE supports the following features:

- USB 2.0 low speed (1.5Mb/s), D- pulls high to indicate to the host that it is a low-speed device
- Full speed (12Mb/s) operation, D+ pulls high to indicate to the host that it is a full-speed device
- Human interface device (HID) in the consumer page (the IC does not require any custom driver)
- 8 bytes endpoint zero (control endpoint)
- 1 byte endpoint one (INT-IN endpoint)
- USB suspend/resume support
- Remote wake-up capability

At the end of enumeration (if successful), the IC is ready to transfer data (if needed) and enabled to sink the negotiated current from BUS.

Figure 5 shows USB bus traffic as captured by a CATC USB bus analyzer. The traces show a PC (host) enumerating the peripheral. Notice that the LS field indicates the low-speed (1.5Mb/s) operation of IC's low-speed configuration.

1) The host uses the default CONTROL endpoint EP0 (shown in the ENDP boxes) to send request to the device. The host initially sends requests to address 0 (shown in the ADDR boxes) to communicate with a device to which it has not yet assigned a unique address.
2) The host begins by sending a Get_Descriptor_Device request (Transfer 0 in Figure 5). It does this to determine the maximum packet size of the device's EP0 buffer. The host then resets the device by issuing a bus reset (packet 69).
3) In Transfer 1, the host assigns a unique address to the peripheral by using the Set_Address request. The assigned address depends on how many other USB host/hubs are currently attached to the host. In this case, the address assigned to our peripheral device is 3. Thereafter, the IC responds only to requests directed to address 3. This address remains in force until the host does a bus reset or the device is disconnected. Notice that the peripheral address field (ADDR) in the bus traces change from 0 to 3 after Transfer 1.
4) In transfers 2 to 11, the host asks for various descriptors. The device FSM needs to determine from the eight setup bytes which descriptor to send, use this information to access one of several character arrays (ROMs) representing the descriptor arrays.
5) In transfer 12, the host requests the device to use the specified configuration (1) and the device enters the Configured state.

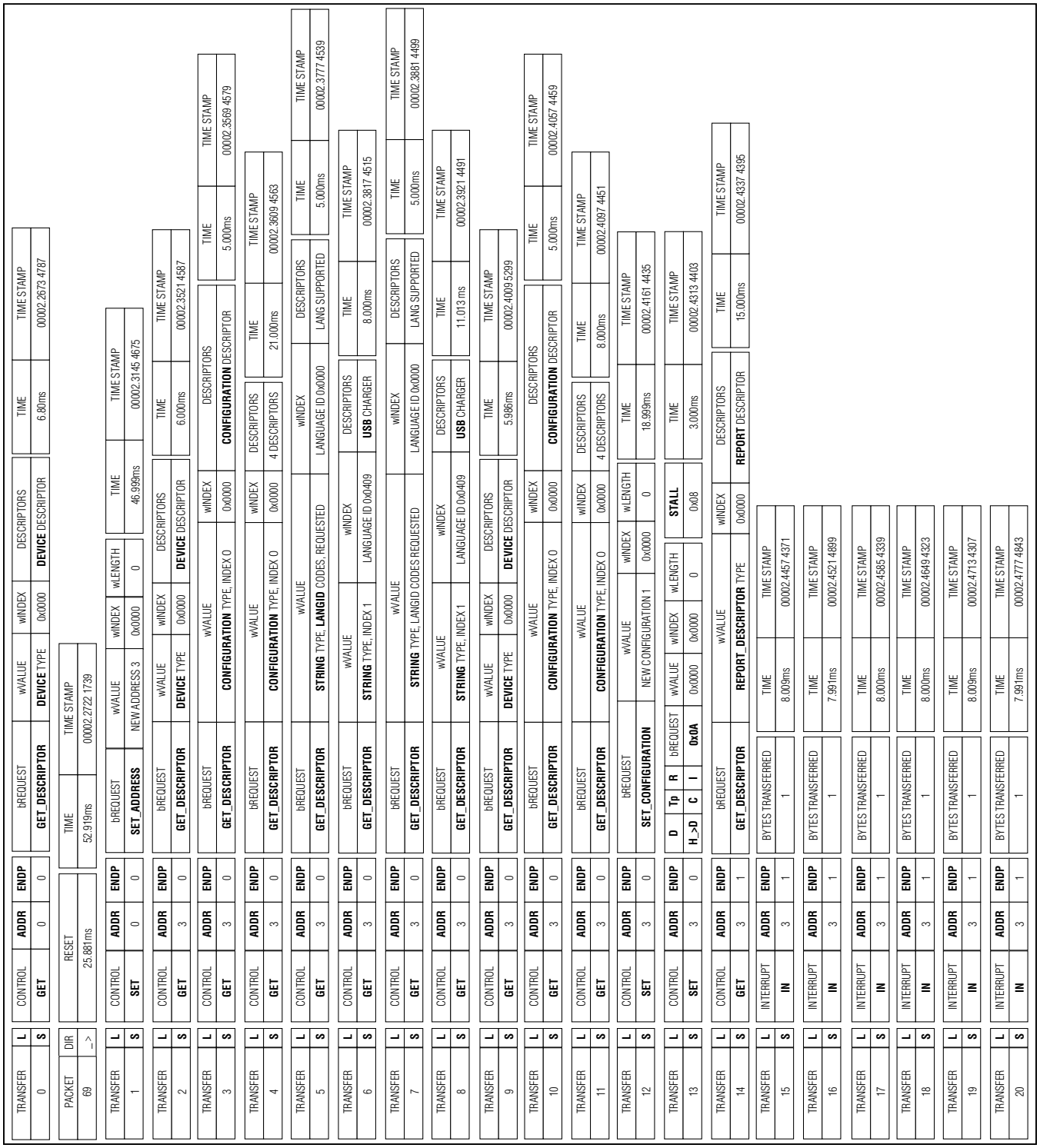
According to the USB 2.0 specification, a bus powered device can be either low power (it cannot draw more than 100mA) or high power (it cannot draw more than 500mA).

All devices must default to low power: the transition to high power is under software control (running on the host side). It is the responsibility of software to ensure adequate power is available before allowing devices to consume high-power.

The IC initiates enumeration by asking for 500mA of current. If the IC does not enter configured status before the t_{ENUM} (10s typ), it interprets this as an indication that the host is not able to support the requested current.

The IC disconnects the pullup resistor on D-/D+, respectively, waits for t_{ENU_FAULT} and then retries to enumerate, but now as a low current device (100mA). If the IC has still not reached the configured status after t_{ENUM}, the IC assumes that either the host is nonresponsive or a wrong adapter type is detected. In this case, the IC disables the pullup resistor on D- if it is configured as low speed and D+ if configured as full speed, waits for t_{ENU_FAULT} + t_{FAULT} before starting the adapter detection process again.

Figure 6 shows the USB traffic captured during the full-speed enumeration. Notice the field FS indicates the full-speed (12Mb/s) operation.



TRANSFER	L	CONTROL	ADDR	ENDP	bREQUEST	wVALUE	wINDEX	DESCRIPTORS	TIME	TIME STAMP
0	S	GET	0	0	GET_DESCRIPTOR	DEVICE TYPE	0x0000	DEVICE DESCRIPTOR	6.80ms	00002.2673 4787

PACKET	DIR	RESET	TIME	TIME STAMP
69	–>	25.881ms	52.919ms	00002.2722 1739

TRANSFER	L	CONTROL	ADDR	ENDP	bREQUEST	wVALUE	wINDEX	wLENGTH	TIME	TIME STAMP
1	S	SET	0	0	SET_ADDRESS	NEW ADDRESS 3	0x0000	0	46.999ms	00002.3145 4675

TRANSFER	L	CONTROL	ADDR	ENDP	bREQUEST	wVALUE	wINDEX	wLENGTH	DESCRIPTORS	TIME	TIME STAMP
2	S	GET	3	0	GET_DESCRIPTOR	DEVICE TYPE	0x0000	0	DEVICE DESCRIPTOR	6.000ms	00002.3521 4587

TRANSFER	L	CONTROL	ADDR	ENDP	bREQUEST	wVALUE	wINDEX	DESCRIPTORS	TIME	TIME STAMP
3	S	GET	3	0	GET_DESCRIPTOR	CONFIGURATION TYPE, INDEX 0	0x0000	CONFIGURATION DESCRIPTOR	5.000ms	00002.3569 4579

TRANSFER	L	CONTROL	ADDR	ENDP	bREQUEST	wVALUE	wINDEX	DESCRIPTORS	TIME	TIME STAMP
4	S	GET	3	0	GET_DESCRIPTOR	CONFIGURATION TYPE, INDEX 0	0x0000	4 DESCRIPTORS	21.000ms	00002.3609 4563

TRANSFER	L	CONTROL	ADDR	ENDP	bREQUEST	wVALUE	wINDEX	DESCRIPTORS	TIME	TIME STAMP
5	S	GET	3	0	GET_DESCRIPTOR	STRING TYPE, LANGID CODES, REQUESTED	LANGUAGE ID 0x0000	LANG SUPPORTED	5.000ms	00002.3777 4539

TRANSFER	L	CONTROL	ADDR	ENDP	bREQUEST	wVALUE	wINDEX	DESCRIPTORS	TIME	TIME STAMP
6	S	GET	3	0	GET_DESCRIPTOR	STRING TYPE, INDEX 1	LANGUAGE ID 0x0409	USB CHARGER	8.000ms	00002.3817 4515

TRANSFER	L	CONTROL	ADDR	ENDP	bREQUEST	wVALUE	wINDEX	DESCRIPTORS	TIME	TIME STAMP
7	S	GET	3	0	GET_DESCRIPTOR	STRING TYPE, LANGID CODES REQUESTED	LANGUAGE ID 0x0000	LANG SUPPORTED	5.000ms	00002.3881 4499

TRANSFER	L	CONTROL	ADDR	ENDP	bREQUEST	wVALUE	wINDEX	DESCRIPTORS	TIME	TIME STAMP
8	S	GET	3	0	GET_DESCRIPTOR	STRING TYPE, INDEX 1	LANGUAGE ID 0x0409	USB CHARGER	11.013ms	00002.3921 4491

TRANSFER	L	CONTROL	ADDR	ENDP	bREQUEST	wVALUE	wINDEX	DESCRIPTORS	TIME	TIME STAMP
9	S	GET	3	0	GET_DESCRIPTOR	DEVICE TYPE	0x0000	DEVICE DESCRIPTOR	5.986ms	00002.4009 5299

TRANSFER	L	CONTROL	ADDR	ENDP	bREQUEST	wVALUE	wINDEX	DESCRIPTORS	TIME	TIME STAMP
10	S	GET	3	0	GET_DESCRIPTOR	CONFIGURATION TYPE, INDEX 0	0x0000	CONFIGURATION DESCRIPTOR	5.000ms	00002.4057 4459

TRANSFER	L	CONTROL	ADDR	ENDP	bREQUEST	wVALUE	wINDEX	DESCRIPTORS	TIME	TIME STAMP
11	S	GET	3	0	GET_DESCRIPTOR	CONFIGURATION TYPE, INDEX 0	0x0000	4 DESCRIPTORS	8.000ms	00002.4097 4451

TRANSFER	L	CONTROL	ADDR	ENDP	bREQUEST	wVALUE	wINDEX	wLENGTH	TIME	TIME STAMP
12	S	SET	3	0	SET_CONFIGURATION	NEW CONFIGURATION 1	0x0000	0	18.999ms	00002.4161 4435

TRANSFER	L	CONTROL	ADDR	ENDP	D	Tp	R	bREQUEST	wVALUE	wINDEX	wLENGTH	STALL	TIME	TIME STAMP
13	S	SET	3	0	H->D	C	I	0x0A	0x0000	0x0000	0	0x08	3.000ms	00002.4313 4403

TRANSFER	L	CONTROL	ADDR	ENDP	bREQUEST	wVALUE	wINDEX	wLENGTH	DESCRIPTORS	TIME	TIME STAMP
14	S	GET	3	1	GET_DESCRIPTOR	REPORT_DESCRIPTOR TYPE	0x0000	REPORT DESCRIPTOR	15.000ms	00002.4337 4395

TRANSFER	L	INTERRUPT	ADDR	ENDP	BYTES TRANSFERRED	TIME	TIME STAMP
15	S	IN	3	1	1	8.009ms	00002.4457 4371

TRANSFER	L	INTERRUPT	ADDR	ENDP	BYTES TRANSFERRED	TIME	TIME STAMP
16	S	IN	3	1	1	7.991ms	00002.4521 4899

TRANSFER	L	INTERRUPT	ADDR	ENDP	BYTES TRANSFERRED	TIME	TIME STAMP
17	S	IN	3	1	1	8.000ms	00002.4585 4339

TRANSFER	L	INTERRUPT	ADDR	ENDP	BYTES TRANSFERRED	TIME	TIME STAMP
18	S	IN	3	1	1	8.000ms	00002.4649 4323

TRANSFER	L	INTERRUPT	ADDR	ENDP	BYTES TRANSFERRED	TIME	TIME STAMP
19	S	IN	3	1	1	8.009ms	00002.4713 4307

TRANSFER	L	INTERRUPT	ADDR	ENDP	BYTES TRANSFERRED	TIME	TIME STAMP
20	S	IN	3	1	1	7.991ms	00002.4777 4843

Figure 5. USB BUS Traffic: Low-Speed Enumeration

JEITA-Compliant, Li+ Charger with Smart Power Selector, Automatic Detection, and USB Enumeration

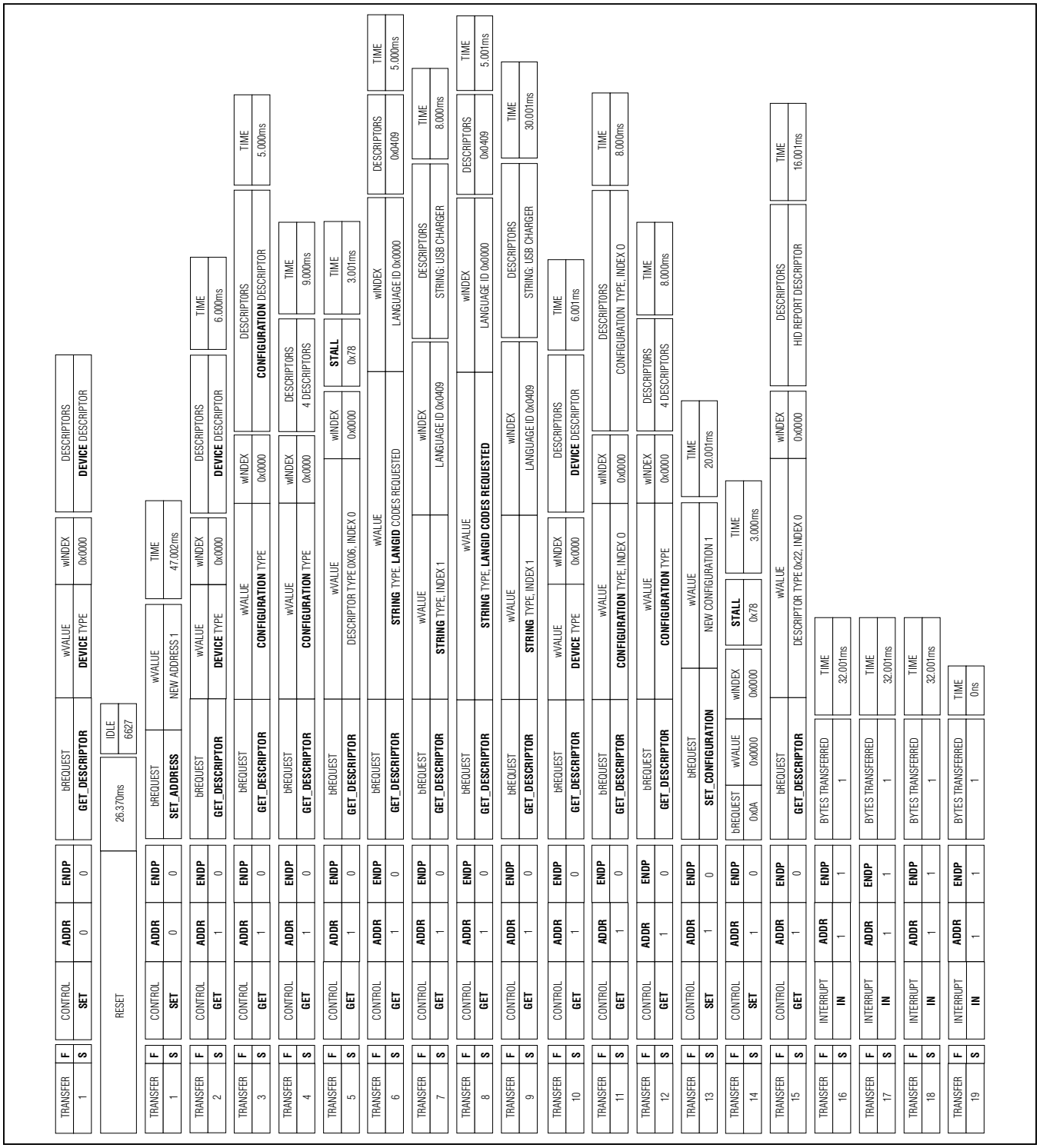


Figure 6. USB BUS Traffic: Full-Speed Enumeration

Table 3. Device Descriptor

FIELD	LENGTH (BITS)	OFFSET (BITS)	DECODED	HEX VALUE	DESCRIPTION
bLength	8	0	0x12	0x12	Descriptor size is 18 bytes.
bDescriptorType	8	8	0x01	0x01	DEVICE descriptor type.
bcdUSB	16	16	0x0200	0x0200	Device compliant to the USB specification version 2.00
bDeviceClass	8	32	0x00	0x00	Each interface specifies its own class information
bDeviceSubClass	8	40	0x00	0x00	Each interface specifies its own subclass information
bDeviceProtocol	8	48	0x00	0x00	No protocols the device basis
bMaxPacketSize0	8	56	0x08	0x08	Maximum packet size for end point zero is 8
idVendor	16	64	*	*	Vendor ID is set using I²C interface*
idProduct	16	80	*	*	Product ID is set using I²C interface*
bcdDevice	16	96	0x0100	0x0100	The device release number is 1.00 code is 0x0100
iManufacturer	8	112	0x00	0x00	The device does not have the string descriptor describing the manufacturer
iProduct	8	120	0x01	0x01	The product stringed descriptor index is 1
iSerialNumber	8	128	0x00	0x00	The device does not have the string descriptor describing the serial number
bNumConfigurations	8	136	0x01	0x01	The device has 1 possible configuration

**Contact factory for available preset values.*

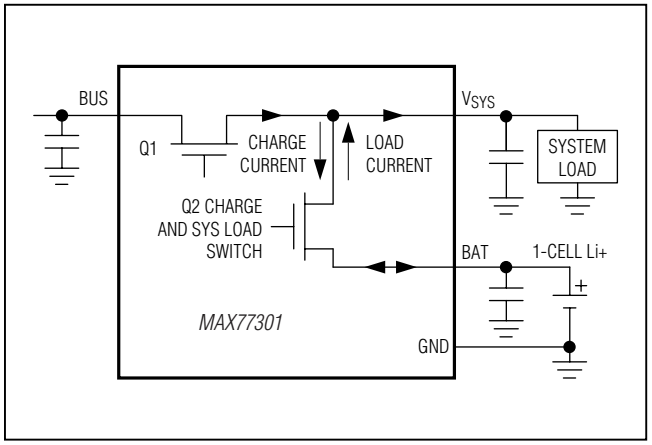


Figure 7. Smart Power Selector Block Diagram

Smart Power Selector

The Smart Power Selector seamlessly distributes power among the external BUS input, the battery BAT, and the system load SYS (Figure 7). The Smart Power Selector basic functions are:

- With both an external adapter and battery connected:
  a) When the system load requirements are less than the input current limit, the battery is charged with residual power from the input.
  b) When the system load requirements exceed the input current limit, the battery supplies supplemental current to the load.
- When the battery is connected and there is no external power input, the system is powered from the battery.
- When an external power input is connected and there is no battery, the system is powered from BUS.

System Load Switch

An internal 200mΩ (typ) MOSFET connects SYS to BAT (Q2 of Figure 7) when no voltage source is available on BUS. When an external source is detected at BUS, this switch opens and SYS is powered from the input source through the input current limiter.

The SYS to BAT switch also prevents V_{SYS} from falling below V_{BAT} when the system load exceeds the input current limit. If V_{SYS} drops to V_{BAT} due to the current limit, the load switch turns on so the load is supported by

the battery. If the system load continuously exceeds the input current limit the battery is not charged. This is useful for handling loads that are nominally below the input current limit, but have high current peaks exceeding the input current limit. During these peaks battery energy is used, but at all other times the battery charges.

The user can select undervoltage and precharge settings as required by new, low voltage lithium-ion, or standard lithium-ion batteries. The battery undervoltage lockout and precharge threshold voltages are identified in the *Electrical Characteristics* table and can be toggled through the BAT_CNTL register (0x10), bit 7.

Input Limiter

The input limiter distributes power from the external adapter to the system load and battery charger. In addition to the input limiter's primary function of passing power to the system load and charger, it performs several additional functions to optimize use of available power:

Invalid BUS voltage protection: If V_{BUS} is above the overvoltage threshold (V_{BUS_OVP}), the IC enters overvoltage protection (OVP). OVP protects the IC and downstream circuitry from high-voltage stress up to 16V at BUS. During OVP, INT_3V3 remains on and an interrupt is sent to the host. During OVP, the charger turns off and the system load switch closes, allowing the battery to power SYS. V_{BUS} is also invalid if it is less than V_{BAT}, or less than the USB undervoltage threshold ($V_{BUS\_UVLO\_F}$). With an invalid input voltage, the system load switch closes, allowing the battery to power SYS.

BUS input current limit: The BUS input current is limited to prevent input overload. The input current limit is automatically selected to match the capabilities of the source, whether it's a 100mA/500mA USB 2.0 source, a 500mA to 2.0A dedicated adapter, or a charger downstream port.

Thermal limiting: The IC reduces the input current by 5%/°C when its die temperature exceeds T_{DIE_LIM}. The system load (I_{SYS}) has priority over charger current, so the input current is first reduced by lowering the charge current. If the junction temperature reaches T_{DIE_LIM} +20°C no input current is drawn from BUS and the battery powers the entire system load.

Setting Input Current Limit

The input current limit is set with IBUS_DET_SW of register 0x0A. See Figure 8. The IC automatically sets the initial value of IBUS_DET_SW according to the device detected. This value can be overwritten using I²C interface if different input current is desired.

If IBUS_DET_SW is set to ILIM the input current limit is set to the value specified in ILIM of register 0x0A. This gives the user more options to meet specific needs.

Minimum V_{SYS} Threshold

The minimum V_{SYS} regulating threshold is programmable using V_SYS of register 0x0A. The V_{SYS} is adapted to the battery voltage, maintaining a value of 140mV (typ) above V_{BAT} with the minimum voltage determined by the value programmed in V_SYS. See Figure 9. The V_SYS minimum voltage regulation reduces the ripple on V_{SYS} during peak load conditions where the input current limit is tripped.

The minimum V_{SYS} regulating threshold is programmable by V_SYS bits. The VSYS is adapted to the battery voltage with a delta value of V_{SYS} 140mV (typ) above V_{BAT} with a minimum voltage determined by V_SYS. The voltage on V_SYS is maintained at or above the programmed voltage. This allows the system to operate with a discharged or damaged battery and provides at the optimum voltage setpoint.

Input Current Limit

If the connected adapter is a USB 2.0 device, the input current limit is default set to 100mA by default. The IC proceeds to enumerate to determine if the external USB host/hub is a low- or high-power device and set the input current limit to 100mA or 500mA, respectively.

For a dedicated charger, charger downstream port, or generic adapter, the optimum current limit is set for the specific value.

When the input current limit is reached, the battery charge current is reduced so as to maintain the system load without exceeding the input current limit. If the charge current is reduced to zero and I_{SYS} exceeds the input current limit, V_{SYS} begins to fall. When V_{SYS} drops to 50mV above V_{BAT}, the SYS to BAT switch turns on, powering the system load from the battery during the load peak.

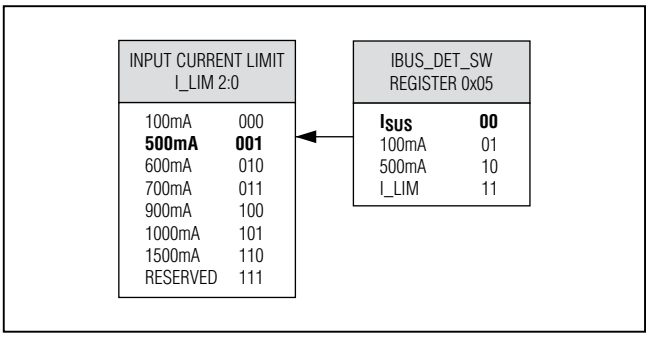


Figure 8. Input Current Limit Settings

Power Monitor Output ($\overline{UOK}$)

$\overline{UOK}$ is an open-drain output that pulls low when V_{BUS} is valid and a valid adapter type is detected. This event also issues an interrupt to the host and sets a flag in the event register. The $\overline{UOK}$ monitor has several different thresholds, depending of type of adapter detected. See Table 4.

The initial detection threshold allows all type of adapters to be detected on BUS. Once the type of adapter is determined the UVLO threshold is changed.

- For any USB 2.0 device, the UVLO thresholds are set to be compliant with USB specification.
- In adaptive mode, the UVLO threshold is lowered to V_{SYS} + 150mV to allow for supporting collapsing charger types that allow the IC to operate with lower power dissipation.

Note: Since the BUS UVLO threshold is changed after initial detection of the device type there are conditions where the IC can toggle between BUS valid and not valid. This is an indication of that the adapter is not within the specified limits.

Soft-Start

To prevent input transients that can cause instability in the USB power source, the rate of change of input current and charge current is limited. When a valid USB 2.0 input is connected, the input current limit is ramped from 0 to 100mA in 50µs. Once enumeration is complete the current can be ramped to 500mA or to the new input current limit value in 50µs.

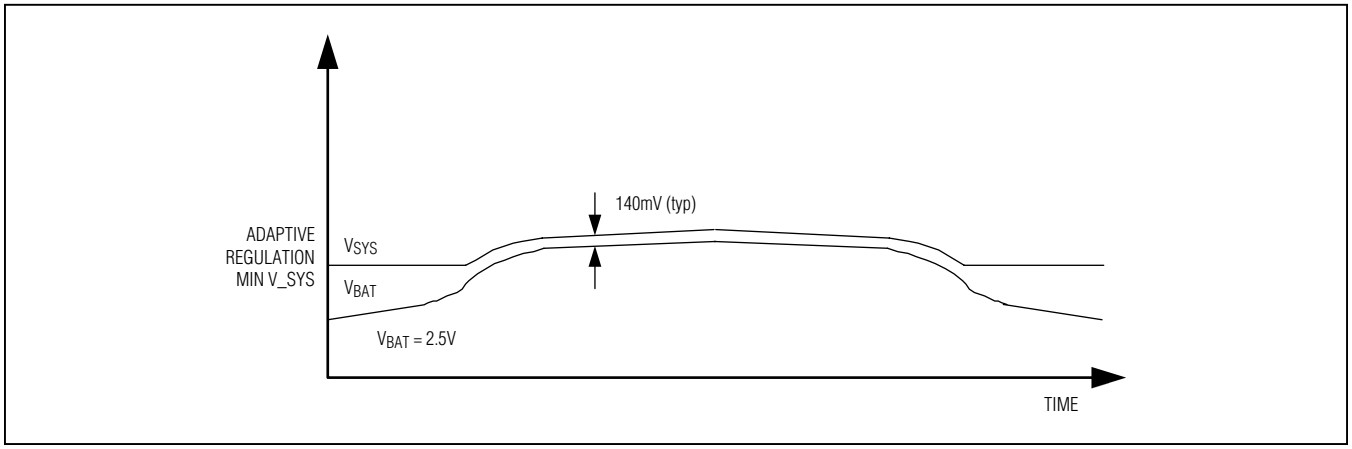


Figure 9. SYS Regulation

Table 4. V_{BUS} Valid Input Range (Rising)

	UVLO (V)	OVLO (V)
Initial V_{BUS} detection (V_{BUS} rising)	4.0 (typ)	6.9 (typ) (V_{BUS} rising)
For USB 2.0 low power (V_{BUS} falling)	3.9 (typ)	
For USB 2.0 high power (V_{BUS} falling)	4.1 (typ)	

Table 5. $\overline{UOK}$ States

BUS STATUS	$\overline{UOK}$ BEHAVIOR
Valid adapter detected on BUS	Low (continuous)
Suspended mode	Pulses low with 1.5s period and 50% duty cycle
D+/D- open detected and nENU_EN = 1	Pulses low with 0.15s period and 50% duty cycle
No valid adapter detected	High impedance

When the charger is enabled, the charge current ramps from zero to the final value in typically 1.5ms. Charge current also ramps when transitioning to fast charge from prequalification and when changing the USB charge current from 100mA to 500mA.

Battery Charger

The battery charger has several different states of operation as shown in the charge profile (Figure 10) and state diagram (Figure 11).

- **Prequalification:** Prequalification is used to gently charge a deeply discharged battery until its voltage is high enough to safely begin fast charge. Prequalification occurs while the battery voltage is below V_{BAT_PCHG} and the battery is charged at maximum I_{PCHG}. If $I_{PCHG} > I_{LIM}$, then the charging current is determined by the I_{LIM} (input current limit). Prequalification mode prevents charging a Li+ battery at a high rate when it is fully discharged, which can cause the battery to become unstable and potentially dangerous and can also reduce life cycle of the Li+ battery. The user can select precharge and under-voltage settings as required by new, low voltage lithium-ion, or standard lithium-ion batteries. The battery undervoltage lockout and precharge threshold voltages are identified in the *Electrical Characteristics* table and can be toggled through the BAT_CNTL register (0x10), bit 7.
- **Fast charge:** In fast-charge mode, the maximum charging current is set to I_{FCHG}. The actual charging current is also constrained by the input current limit, so the charge current is the lesser of I_{FCHG} and I_{LIM}-I_{SYS}.
- **Top-off charge:** Top-off mode begins when the battery voltage reaches the set point. During top-off, the battery voltage is regulated and the charge current declines. This prevents overcharging of the battery, and also minimizes the power dissipation in the battery.
- **Maintains charge:** The charger enters this mode when the charging current has dropped below I_{CHG_DONE} threshold. The charger continues to charge for t_{MTCHG} time to insure battery is fully charged before charger is disabled.
- **Charge done:** Charger is disabled and only engages again if the battery voltage drops below the V_{BAT_RECHG} threshold.

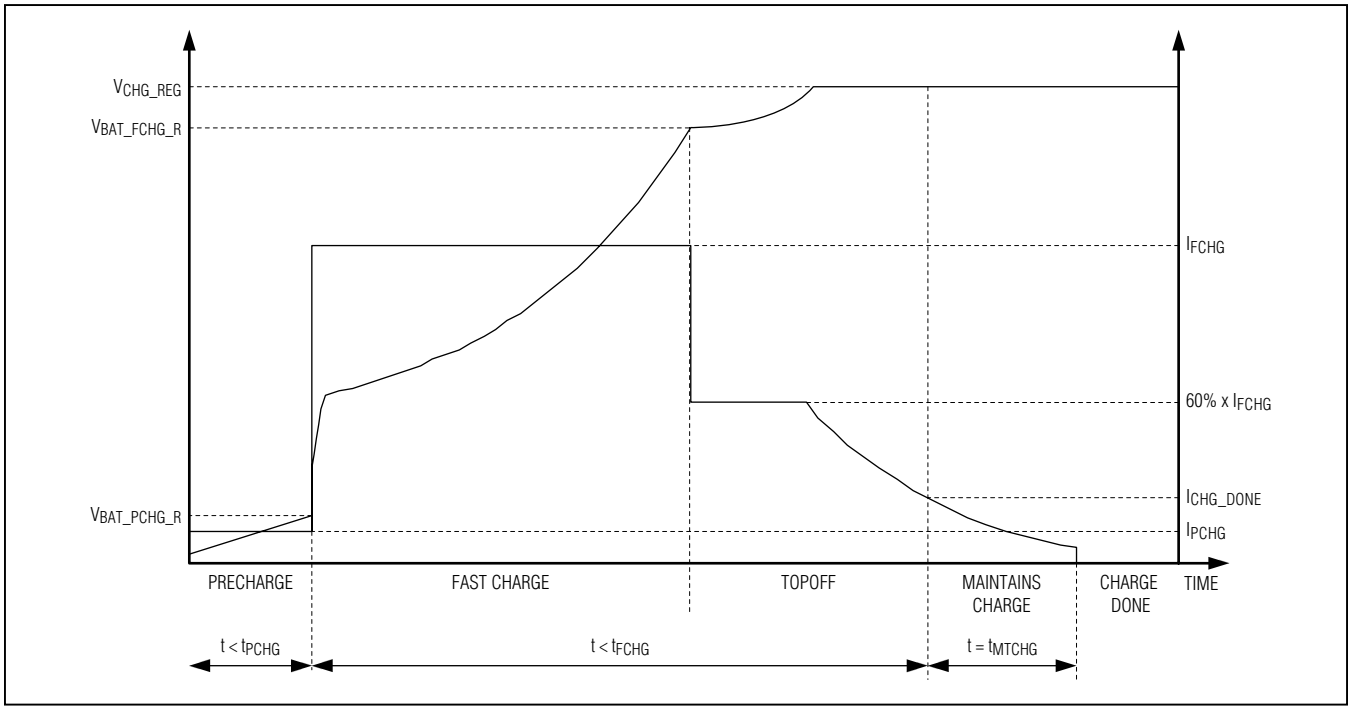


Figure 10. Charge Profile

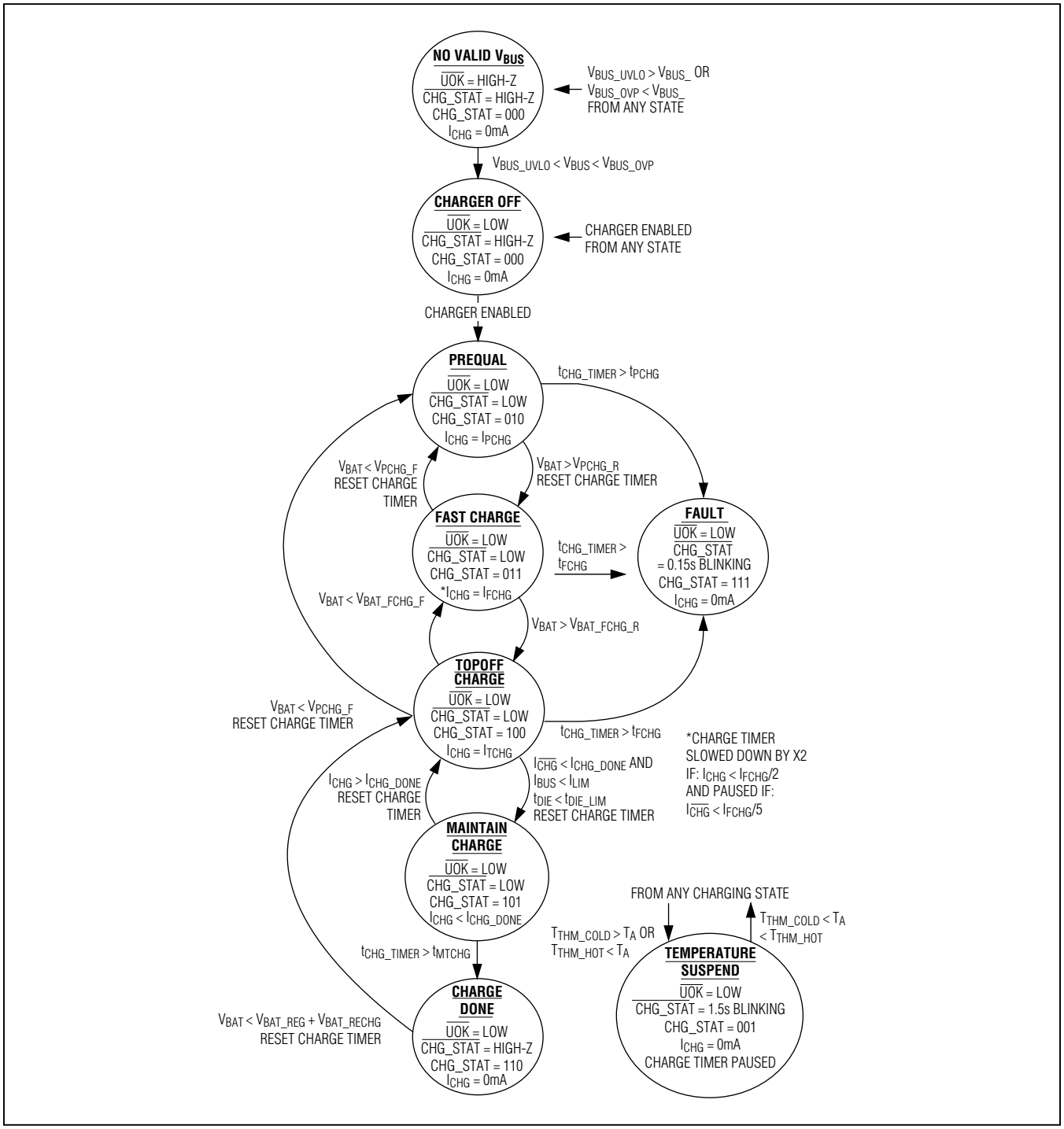


Figure 11. Charger State Diagram

Charge Enable

The charger is enabled using either logic input CEN or with I²C bit CHG_EN, determined by the state of the nCEN_MASK bit.

Set nCEN_MASK to 0 to enable the use of the logic input CEN. Drive CEN logic-high to enable the charger or logic-low to disable the charger.

Set nCEN_MASK to 1 to control charger enable by writing directly to the CHG_EN bit. Write 1 to CHG_EN to enable the charger or 0 to disable the charger.

Enabling or disabling the charger does not affect V_{SYS}. In many systems, there is no need for the system controller (typically a microprocessor) to disable the battery charger, because the IC's Smart Power Selector circuitry independently manages charging and USB-battery power handover.

Charge Termination (EOC)

When the charger is in top-off mode and the charge current falls below the charge done threshold (I_{CHG_DONE}), an interrupt is sent to the host. Charging continues in maintains-charge mode for t_{MTCHG} and then enters the DONE state where charging stops. I_{CHG_DONE} and t_{MTCHG} are programmable through I²C.

Note that if charge current falls to I_{CHG_DONE} as a result of the input current limit or thermal regulation, the charger does not enter the DONE state. For the charger to enter DONE, charge current must be less than I_{TERM}, the charger must be in top-off mode (voltage regulation), and the input current limit or thermal regulation must not be reducing charge current. The charger exits the DONE state and top-off or fast-charge resumes if the battery voltage subsequently drops by V_{BAT_RECHG}.

While in fast-charge mode, a large system load or device self-heating can cause the IC to reduce charge current. Under these circumstances, the fast-charge timer adjusts to ensure that adequate charge time is still allowed. Consequently, the fast-charge timer is slowed by 2x if charge current is reduced below 50% of the programmed fast-charge level. If charge current is reduced to below 20% of the programmed level, the fast charge timer is paused. The fast-charge timer is not adjusted when the charger is in top-off mode where charge current reduces due to current tapering under normal charging. The timer settings are programmable through I²C and if the timer expires, charging is terminated and an interrupt is sent to the host and a flag is set in the event register.

To exit a fault state, toggle CEN, CHG_EN, or remove and reconnect the BUS input source.

CHG_TYPE

CHG_TYPE is an open-drain output that is used to signal to the processor the current capability of the external adapter. CHG_TYPE is low for 100mA or high-impedance for 500mA or greater.

IBUS_DEF

The IBUS_DEF input is only valid when nENU_EN is set to 1 or when D+/D- are unconnected. In this case, the adapter type detection is activated. If the adapter type is detected as a USB 2.0 device, the input current is set to IBUS_DEF value and does not initiate USB enumeration. See Table 7.

Charge Status ($\overline{CHG\_STAT}$)

The charge status is indicated by an open-drain output $\overline{CHG\_STAT}$. See Table 8. A temperature fault or timers expiring changes the charge state immediately and thus changes the output status.

Table 6. CHG_TYPE

CHG_TYPE	INPUT CURRENT LIMIT (mA)
0	100 or less
1	500 or more

Table 7. IBUS_DEF

IBUS_DEF, nENU_EN = 1 OR D+/D- OPEN	INPUT CURRENT LIMIT
0	100mA
1	ILIM

Table 8. CHG_STAT Output

CHARGER STATUS	$\overline{CHG\_STAT}$ BEHAVIOR
Charge in progress	Low (continuous)
Charge suspend (due to temperature fault(s))	Pulses with 1.5s period and 50% duty cycle
Timer fault	Pulses with 0.15s period and 50% duty cycle
Charge done	High impedance
Battery removed	Pulses with 0.1s period, 10%–20% duty cycle

Battery Detection

The IC reliably detects insertion and removal of battery packs under various conditions. This includes battery packs with open or closed protection circuit. A normal Li-ion battery pack includes protection circuitry that ensures the battery is protected against overload. If an overload occurs the protection circuitry opens its internal MOSFETs making the battery pack output high impedance. To reset the protection, a voltage must be applied to the battery pack. The protector detects this and closes the MOSFETs after a time delay.

When a valid power source is detected on BUS the battery detection state machine is enabled. The first task is to determine the type of detection method used for predicting battery present condition.

The two methods are automatic detection and NTC detection. The type of algorithm used is determined by the I²C bit BAT_DET_CNTL. Any change in the state of this bit reinitiates the detection algorithm as shown in Figure 12.

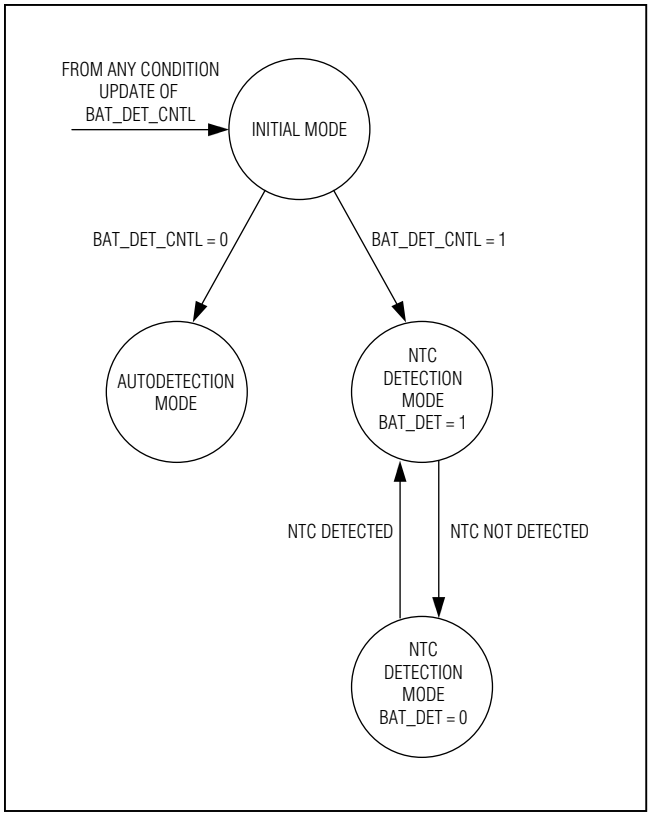


Figure 12. Battery Detection State Diagram

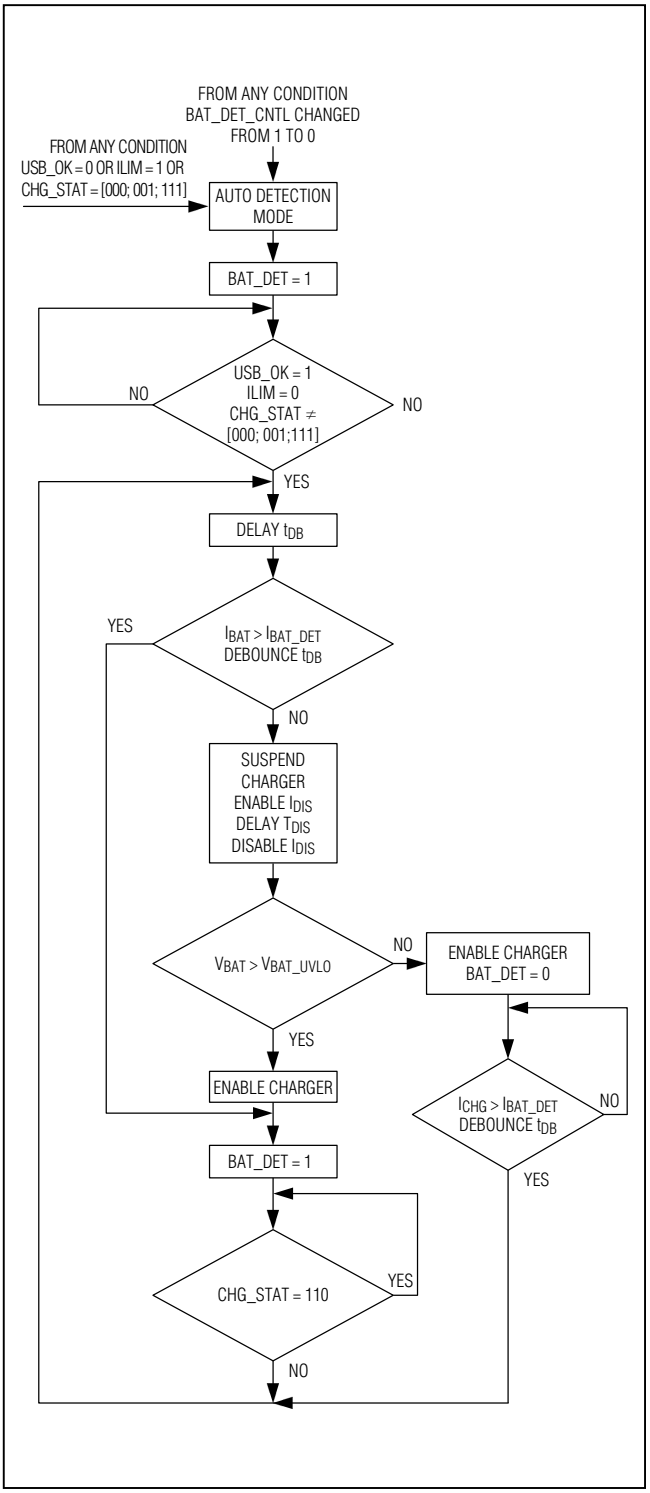


Figure 13. Battery Present Flow Chart

Automatic Detection Mode

Automatic battery detection is used when the BAT_DET_CNTL bit is cleared. The automatic detection starts by discharging the battery with I_{DIS} for t_{DIS}. Then it looks at the battery voltage. If the battery voltage is above $V_{BAT\_UVLO\_F}$, it indicates that a battery is present. If the battery voltage is below $V_{BAT\_UVLO\_F}$ then no battery is detected.

Automatic detection continues to monitor V_{BAT} as long as one of the following conditions exists:

- USB_OK = 0 no valid device connected to BUS
- ILIM = 1 input current limit active
- CHG_STAT = [000, charger disabled: 001, charger in temperature suspend; 111 charger fault]

If none of the conditions above exist, automatic detection continues into the next phase.

In the second phase the charger is enabled for t_{DB}. This is to allow a battery pack with open protection circuits to detect the presence of the charger and reset itself.

After the t_{DB} if the charging current is less than I_{BAT_DET} it indicates that no battery is present. In this case the IC suspends the charger and discharges the battery with a current sink of I_{DIS} for t_{DIS}. If only a capacitor is present at BAT, the capacitor is discharged during the t_{DIS}. After t_{DIS} the battery voltage is compared to recharge threshold. If V_{BAT} is still above 2.4V, it indicates that a battery is present and the charger is enabled again. If the battery voltage drops below the restart threshold this indicates that no battery is present, the status is latched into the I²C register, and the automatic battery detection algorithm now only monitors the charging current. As long as the charging current is below I_{BAT_DET}, it indicates that no battery is present. If the charging current increases above I_{BAT_DET}, the algorithm restarts the battery detection.

If the automatic detection algorithm determines that a battery is present and that charger is in the DONE state, no further action is taken as long as the charge remains in the DONE state (CHG_STAT is 110).

NTC Detection Mode

In NTC detection mode, the THM input is used to determine when a battery is connected. NTC detection mode is used when the THERM_EN and BAT_DET_CNTL bits are set. If BAT_DET_CNTL = 1 and THERM_EN = 0, the IC presumes that battery is present and sets BAT_DET to 1.

NTC detection monitors the voltage on the THM input to determine if an external NTC is present or not. This information is used to control the status of BAT_DET. See Figure 12.

Thermistor Input (THM)

V_{THM} is monitored to provide battery temperature information to the charge controller. The JEITA temperature profiles shown in Figure 14 utilize a 47kΩ bias resistor between the INT_3V3 and THM pins. The thermistor is a 100kΩ NTC NTC-type beta of 4250K, which is tied from NTC to ground.

The IC is compliant with the JEITA specification for safe use of secondary lithium ion batteries (*A Guide to the Safe Use of Secondary Lithium Ion Batteries in Notebook type Personal Computers,* JEITA and Battery Association of Japan, April 20, 2007). Once the JEITA parameters have been initialized for a given system, no software interaction is required. The four temperature thresholds change the battery charger operation: T1, T2, T3, and T4. When the thermistor input exceeds the extreme temperatures (< T1 or > T4), the charger shuts off and all respective charging timers are suspended. While the thermistor remains out of range, no charging occurs, and the timer counters hold their state. When the thermistor input comes back into range, the charge timers continue to count. The middle

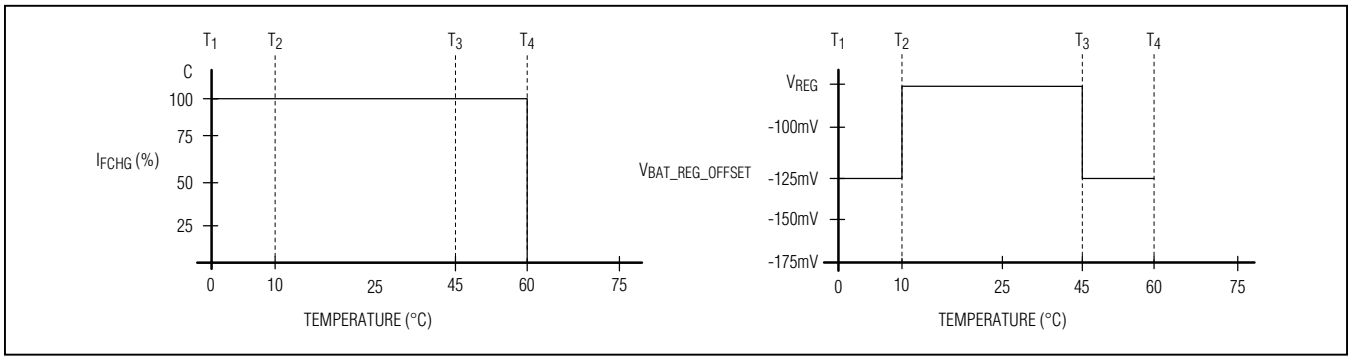


Figure 14. JEITA Battery Safety Regions

thresholds (T2 and T3) do not shut the charger off, but have the capability to adjust the current/voltage targets to maximize charging while reducing battery stress.

The behavior when the battery temperature is between T1 and T2 is controlled by THM_T1_T2 and the behavior when it is between T3 and T4 is controlled by THM_T3_T4.

The JEITA specification recommends that systems reduce all loading on the battery when the battery temperature exceeds the maximum battery temperature for discharge (TMD). The IC generates an interrupt and sets the WHIGH_BAT_T_IRQ bit when the battery temperature exceeds the T_4 threshold.

If the THM disable threshold is exceeded, an interrupt is generated and the BAT_DET_IRQ bit is cleared in the event register.

If the thermistor functionality is not required, clearing the THERM_EN disables temperature sensing and the thermistor input is then high impedance.

The IC is compatible with a 100kΩ thermistor with a ß of 4250K. The general relation of thermistor resistance to temperature is defined by the following equation:

$$R_T = R_{25} \times e^{\left\{\beta\left(\frac{1}{T+273} - \frac{1}{298}\right)\right\}}$$

where R_T is the resistance in Ω of the thermistor at temperature T in Celsius, R_{25} is the resistance in Ω of the thermistor at +25°C, ß is the material constant of the thermistor (typically ranges from 3000K to 5000K), and T is the temperature of the thermistor in °C.

Thermal Overload Protection

Thermal overload protection limits total power dissipation in the IC. If the junction temperature exceeds 160°C, the device turns off, allowing the IC to cool. Continuous thermal-overload can result in a pulsed charge current condition. Thermal overload protection operates independent of the thermal regulation feature for additional protection. Typically, thermal regulation prevents the die temperature from reaching the point where thermal overload protection is activated.

External Clock (Full Speed Only)

USB 2.0 full-speed operation requires that the system clock of the transceiver is within ±2500ppm, over temperature, aging, etc. Therefore, an external crystal, resonator, or clock source is required to stay within this limit. The IC local oscillator and internal digital clocks are derived from the reference clock at the XIN input.

USB Low-Speed Operation

For USB low-speed operation, the internal GMz clock can be used and no external crystal or external source is required. Connect XIN to AGND and XOUT pin to INT_3V3 pin to enable USB low-speed mode.

External Crystal or Ceramic Resonator

XIN and XOUT connect to an external 12MHz crystal or ceramic resonator. Connect 33pF load capacitors from both XIN/XOUT to analog ground.

Requirements for the external resonator/crystal for full speed:

Frequency: 12MHz ±0.25%
C_{LOAD}: 33pF ±20%
Drive level: 200µW
Series resonance resistance: 60Ω (max), 30Ω (typ)

Note: Series resonance resistance is the resistance observed when the resonator is in the series resonant condition. This is a parameter often stated by quartz crystal vendors and is called R1. When a resonator is used in the parallel resonant mode with an external load capacitance, as is the case with the IC's oscillator circuit, the effective resistance is sometimes stated. The effective resistance at the loaded frequency of oscillation is:

$$R_{EFF} = R1 \times \left[1 + \left(\frac{C_O}{C_{LOAD}}\right)\right]^2$$

where R1 is the series resonance resistance, C_O is the crystal capacitance, and C_{LOAD} is the external load capacitance.

For typical C_O and C_{LOAD} values, the effective resistance can be greater than R1 by a factor of 2.

External Clock

The IC can also be driven from an external clock. The external clock can be a digital level square wave or sinusoidal and can be directly coupled to XIN without the need for additional components. If the peaks of the reference clock are above V_{INT_3V3} or below ground, the clock signal must be driven through a DC-blocking capacitor (approximately 33pF) connected to XIN.

The external clock source can be enabled using either the $\overline{UOK}$ or INT_3V3 signals depending on if the clock source is active-low or active-high enabled.

Clock Timing Accuracy

USB 2.0 specification requires the system clock to be within ±2500ppm over temperature, aging, etc. It is recommended to use a clock source with tighter initial accuracy to ensure that over time an accuracy of ±2500ppm is maintained.

External Power-On Signal

The $\overline{\text{EXT\_PWRON}}$ output is used to enable power to other external circuits.

$\overline{\text{EXT\_PWRON}}$ is an open-drain output, and is high impedance (high impedance) when no battery is detected or when a valid adapter is detected.

If a valid battery is detected, the IC pulls $\overline{\text{EXT\_PWRON}}$ low. This signal can be used to enable other parts of the system. If a valid adapter is connected to the system while the battery is below the V_{BAT_UVLO} threshold, the $\overline{\text{EXT\_PWRON}}$ transitions from high impedance to low as soon as the adapter type is determined and $\overline{\text{UOK}}$ goes from high impedance to low.

From battery only or adapter only mode, the IC can enter adapter and battery mode, for this to occur, the IC must detect a valid battery and at the same time a valid adapter type on the V_{BUS} input. Once this occurs the IC generates a 63ms high-impedance pulse on $\overline{\text{EXT\_PWRON}}$. This signal can be used to wake up the remainder of the system.

See Figure 15 for the $\overline{\text{EXT\_PWRON}}$ state diagram.

ESD Protection

D+, D-, and $V_{BUS\_}$ possess extra preotection against static electricity to protect the IC up to ±8kV (HBM). The ESD structures withstand high ESD in all operating modes: normal operation, suspend mode, and powered down. BUS requires 1µF ceramic capacitors connected to ground as close to BUS_A and BUS_B as possible.

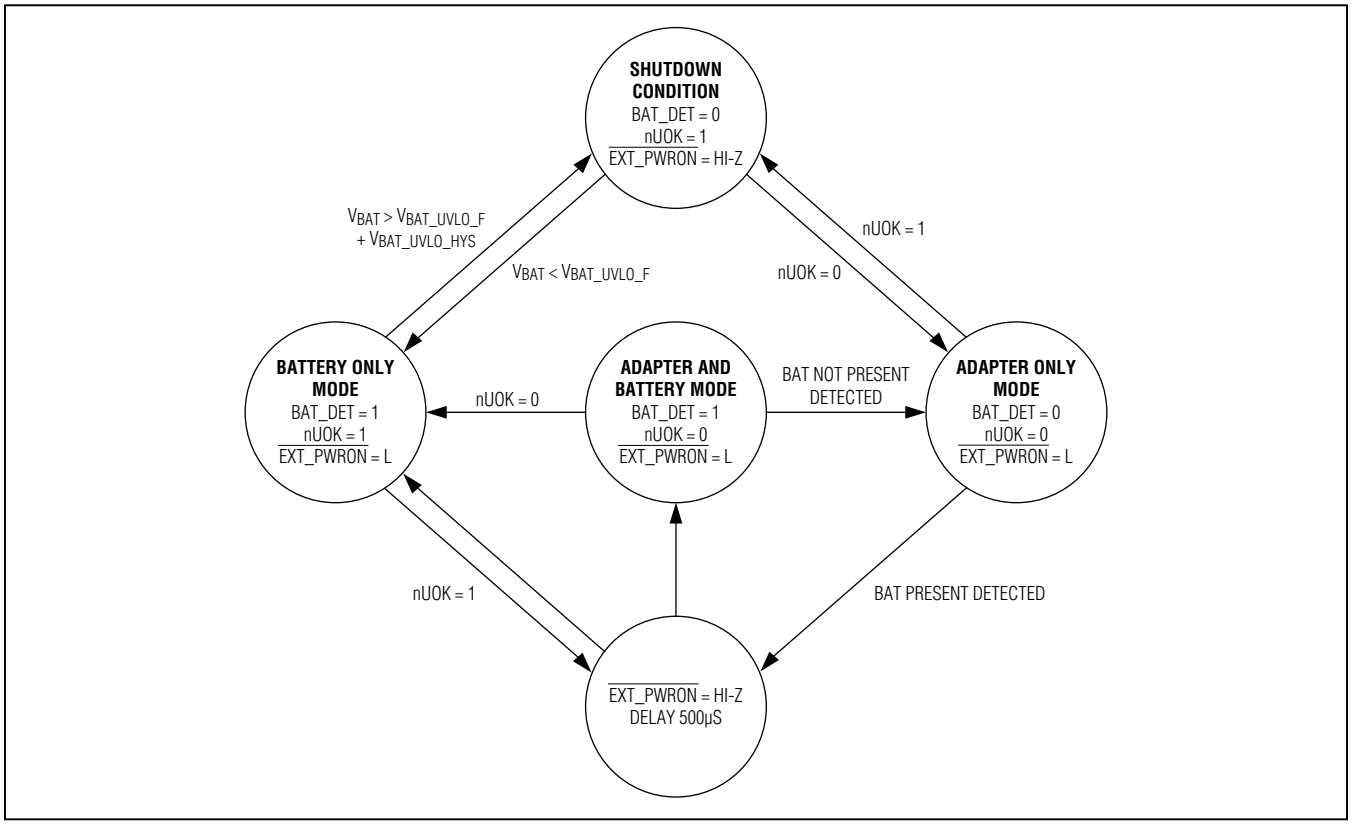


Figure 15. EXT_PWRON State Diagram

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results. The Figure 16 shows the Human Body Model, and Figure 17 shows the current waveform generated when discharged into low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which then discharges into the test device through a 1.5kΩ resistor.

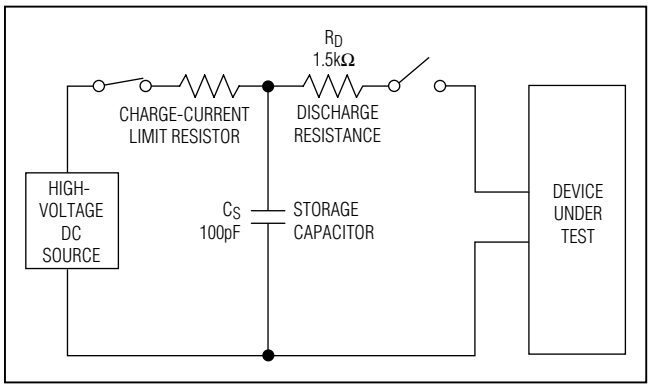


Figure 16. Human Body ESD Test Models

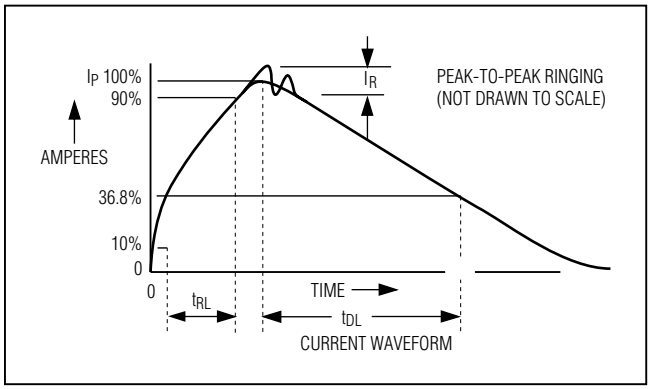


Figure 17. Human Body Model Current Waveform

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. It does not specifically refer to integrated circuits. The major difference between tests done using the Human Body Model and IEC 61000-4-2 is a higher peak current in IEC 61000-4-2, due to lower series resistance. Hence, the ESD withstand voltage measured to IEC 61000-4-2 generally is lower than that measured using the Human Body Model. Figure 18 shows the IEC 61000-4-2 model. The Contact-Discharge method connects the probe to the device before the probe is charged. The Air-Gap Discharge test involves approaching the device with a charged probe.

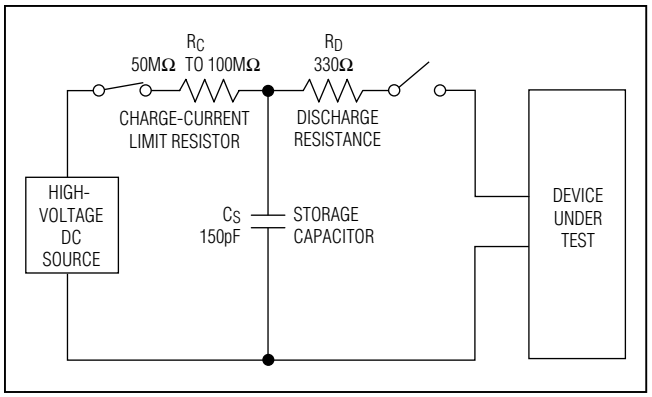


Figure 18. IEC61000-4-2 ESD Test Model

I²C Functional Description

An I²C-compatible, 2-wire serial interface controls the charger settings as well as read back of adapter detection. The serial bus consists of a bidirectional serial-data line (SDA) and a serial-clock input (SCL). The IC is a slave-only device, relying upon a master to generate a clock signal. The master initiates data transfer to and from the IC and generates SCL to synchronize the data transfer.

I²C is an open-drain bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage through a pullup resistor. They both have Schmitt triggers and filter circuits to suppress noise spikes on the bus to assure proper device operation. A bus master initiates communication with the IC as a slave device by issuing a START condition followed by the IC address. The IC address byte consists of 7 address bits and a read/write bit ($R\overline{W}$). After receiving the proper address, the IC issues an acknowledge bit by pulling SDA low during the ninth clock cycle.

I²C Slave Address

A bus master initiates communication with a slave device (MAX77301) by issuing a START condition followed by the slave address. The slave address byte consists of 7 address bits (0b0000010) followed by a read/write bit (R/W). So the complete address byte is 0x05 for read operations and 0x04 for write operations. After receiving the proper address, the IC issues an acknowledge by pulling SDA low during the ninth clock cycle.

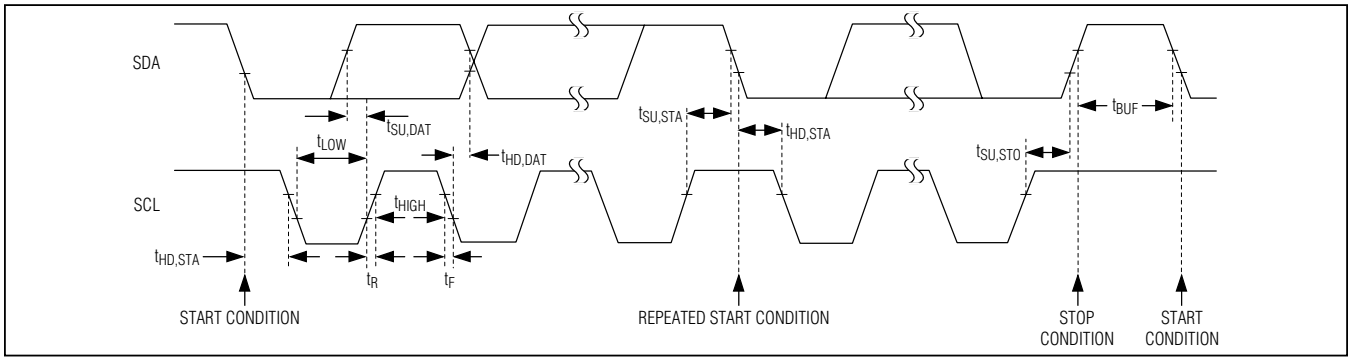


Figure 19. I²C Interface Timing Diagram

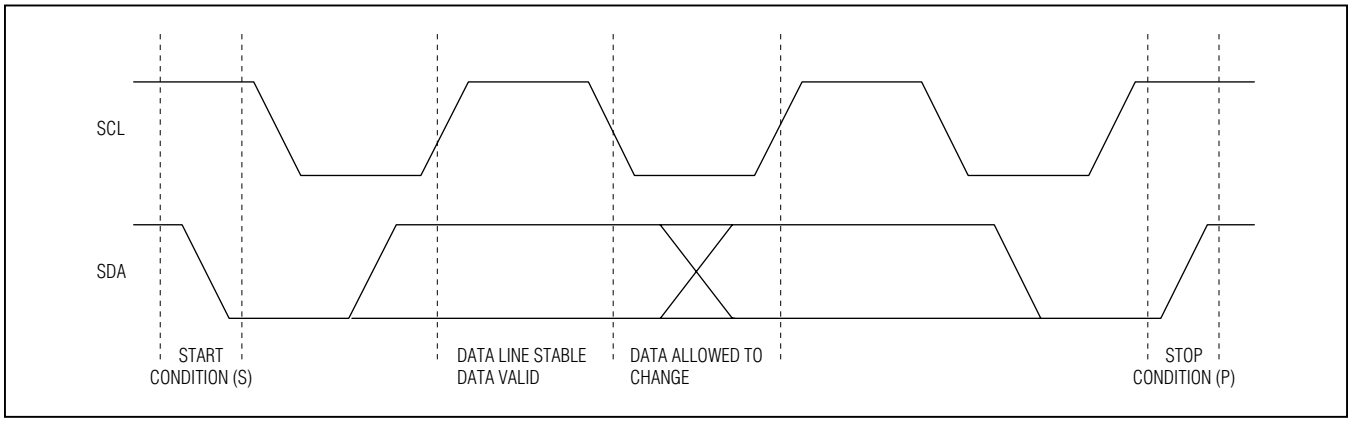


Figure 20. I²C Bit Transfer

I²C Bit Transfer

Each data bit, from the most significant bit to the least significant bit, is transferred one by one during each clock cycle. During data transfer, the SDA signal is allowed to change only during the low period of the SCL clock and it must remain stable during the high period of the SCL clock (Figure 20).

START and STOP Conditions

Both SCL and SDA remain high when the bus is not busy. The master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the IC, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 21). Both START and STOP conditions are generated by the bus master.

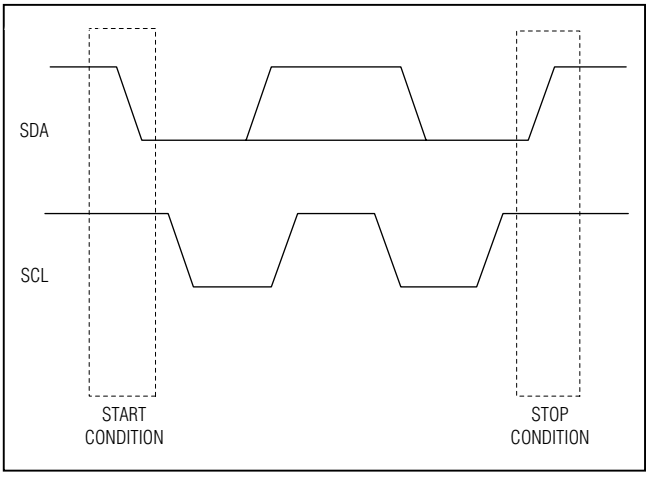


Figure 21. I²C START and STOP Conditions

Acknowledge

The acknowledge bit is used by the recipient to handshake the receipt of each byte of data (Figure 22). After data transfer, the master generates the acknowledge clock pulse and the recipient pulls down the SDA line during this acknowledge clock pulse so that the SDA line stays low during the high duration of the clock pulse. When the master transmits the data to the IC, it releases the SDA line and the IC takes the control of the SDA line and generates the acknowledge bit. When SDA remains high during this ninth clock pulse, this is defined as the not acknowledge signal. The master can then generate either a STOP (P) condition to abort the transfer, or a REPEATED START (Sr) condition to start a new transfer.

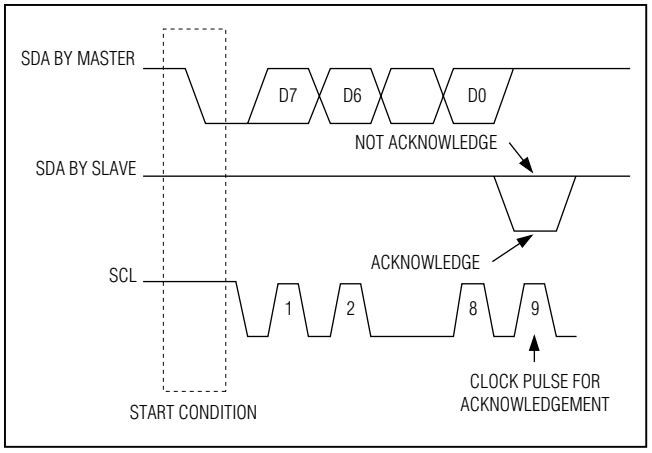


Figure 22. I²C Acknowledge

Write Operations

The IC recognizes the write byte protocol as defined in the SMBus specification and shown in section A of Figure 23. The write byte protocol allows the I²C master device to send 1 byte of data to the slave device. The write byte protocol requires a register pointer address for the subsequent write. The IC acknowledges any register pointer even though only a subset of those registers actually exists in the device.

The write byte protocol is as follows:

1) The master sends a START command.
2) The master sends the 7-bit slave address followed by a write bit (0x04).
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave updates with the new data.
8) The slave acknowledges the data byte.
9) The master sends a STOP condition.

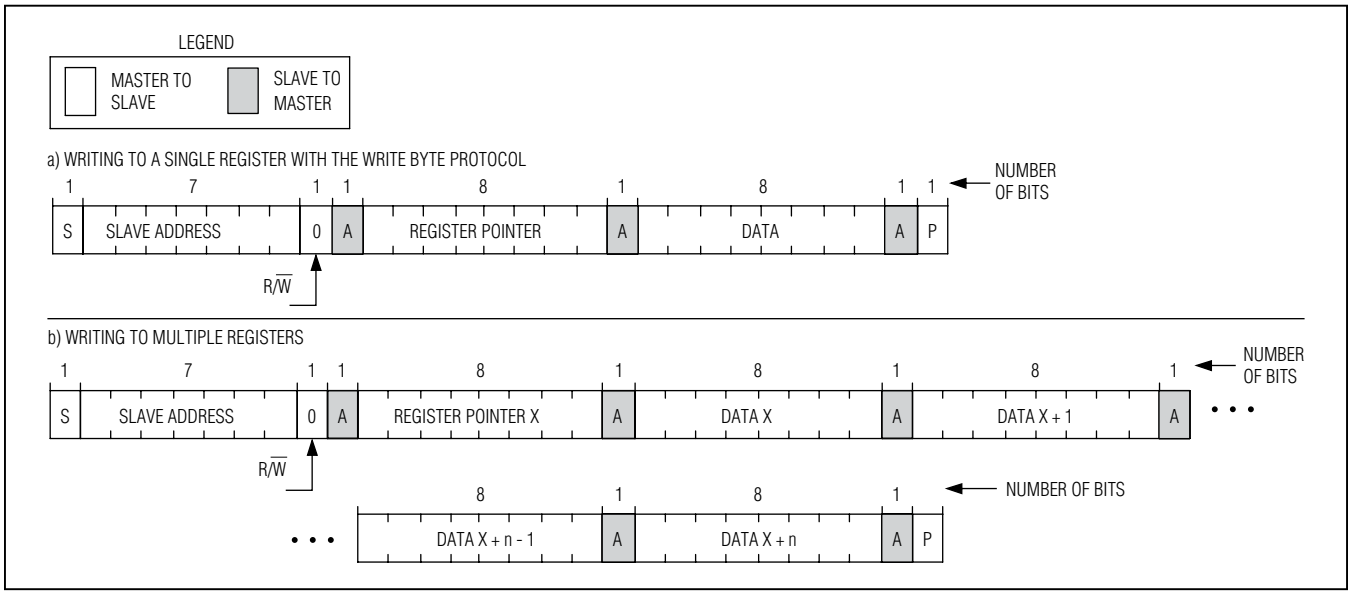


Figure 23. I²C Write Operations

In addition to the write-byte protocol, the IC can write to multiple registers as shown in section B of Figure 23. This protocol allows the I2C master device to address the slave only once and then send data to a sequential block of registers starting at the specified register pointer.

Use the following procedure to write to a sequential block of registers:

1) The master sends a START command.
2) The master sends the 7-bit slave address followed by a write bit (0x04).
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends the 8-bit register pointer of the first register to write.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave updates with the new data.
8) The slave acknowledges the data byte.
9) Steps 6 to 8 are repeated for as many registers in the block, with the register pointer automatically incremented each time.
10) The master sends a STOP condition.

Read Operations

The method for reading a single register (byte) is shown in section A of Figure 24. To read a single register:

1) The master sends a START command.
2) The master sends the 7-bit slave address followed by a write bit (0x04).
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a repeated START condition.
7) The master sends the 7-bit slave address followed by a read bit (0x05).
8) The slave assets an acknowledge by pulling SDA low.
9) The slave sends the 8-bit data (contents of the register).
10) The master assets an acknowledge by pulling SDA low.
11) The master sends a STOP condition.

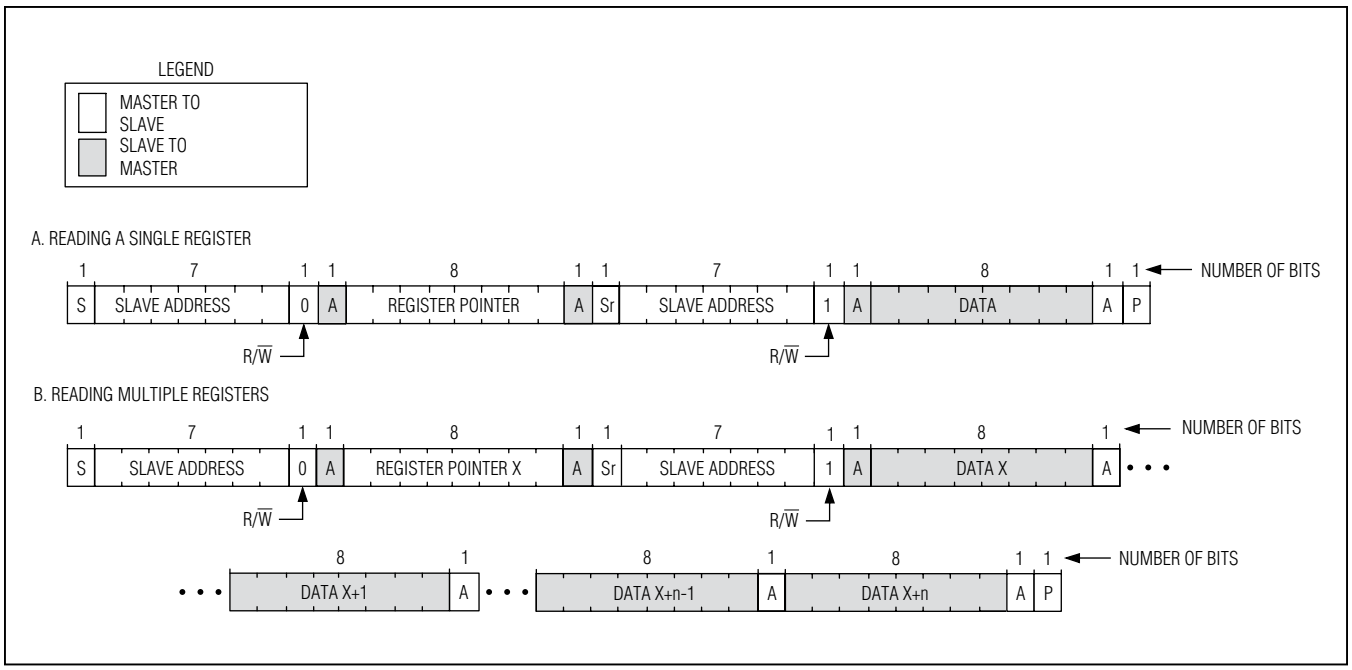


Figure 24. I2C Read Operations

In addition, the IC can read a block of multiple sequential registers as shown in section B of Figure 24. Use the following procedure to read a sequential block of registers:

1) The master sends a START command.
2) The master sends the 7-bit slave address followed by a write bit (0x04).
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends an 8-bit register pointer of the first register in the block.
5) The slave acknowledges the register pointer.
6) The master sends a repeated START condition.
7) The master sends the 7-bit slave address followed by a read bit (0x05).
8) The slave assets an acknowledge by pulling SDA low.
9) The slave sends the 8-bit data (contents of the register).
10) The master assets an acknowledge by pulling SDA low.
11) Steps 9 and 10 are repeated for as many registers in the block, with the register pointer automatically incremented each time.
12) The master sends a STOP condition.

Table 9. I²C Register Map

FUNCTION	R/W	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CHIP_ID	R	0x00	DIE_TYPE[7:4]				DIE_TYPE[3:0]			
CHIP_REV	R	0X01	DASH[3:0]				MASK_SET[3:0]			
STATUS_A	R	0x02	CHG_TYPE[3:0]				BAT_DET	CHG_STAT[2:0]		
STATUS_B	R	0x03	SUS	ILIM	Reserved	ENUM_FLT	USB_OK	THERM_STAT[2:0]		
STATUS_C	R	0x04	IBUS_DEF	nENU_EN_HW	nSTDB_EN_HW	nCEN	THER_SD	FS_DET	nUOK	nEXT_PWR_ON
EVENT_A	R	0x05	DET_DONE_IRQ	Reserved	HW_OUT_IRQ	HW_IN_IRQ	BAT_DET_IRQ	CHG_STAT_IRQ	THERM_REG_IRQ	TIME_OUT_IRQ
EVENT_B	R	0x06	SUS_IRQ	RESUME_IRQ	ILIM_IRQ	ENUM_FLT_IRQ	BUS_OK_IRQ	WHIGH_BAT_T_IRQ	HIGH_BAT_T_IRQ	LOW_BAT_T_IRQ
IRQ_MASK_A	R/W	0x07	DET_DONE_IRQ_MASK	Reserved	HW_OUT_IRQ_MASK	HW_IN_IRQ_MASK	BAT_DET_IRQ_MASK	CHG_STAT_IRQ_MASK	THERM_REG_IRQ_MASK	TIME_OUT_IRQ_MASK
IRQ_MASK_B	R/W	0x08	SUS_IRQ_MASK	RESUME_IRQ_MASK	ILIM_IRQ_MASK	ENUM_FLT_IRQ_MASK	BUS_OK_IRQ_MASK	WHIGH_BAT_T_IRQ_MASK	HIGH_BAT_T_IRQ_MASK	LOW_BAT_T_IRQ_MASK
USB_CNTL	R/W	0x09	RWU_EN	SUS_EN	nSTDB_EN	nSTDB_EN_HW_MASK	nENU_EN	nENU_EN_HW_MASK	DCD_EN	KB_TM_EN
IBUS_CNTL	R/W	0x0A	IBUS_LIM	V_SYS[1:0]		ILIM[2:0]			IBUS_DET_SW[1:0]	
CHARGER_CNTL_A	R/W	0x0B	Reserved	TCHG[1:0]		IFCHG[2:0]			THERM_REG[1:0]	
CHARGER_CNTL_B	R/W	0x0C	THERM_EN	BAT_DET_MASK	BAT_DET_CNTL	CHG_EN	nCEN_MASK	CHG_DONE[2:0]		
CHARGE_TMR	R/W	0x0D	Reserved	Reserved	MTCHG_TMR[1:0]		FCHG_TMR[1:0]		PCHG_TMR[1:0]	
CHARGER_VSET	R/W	0x0E	BAT_RECHG[1:0]		BAT_REG[1:0]		BAT_FCHG_HYS[1:0]		BAT_FCHG[1:0]	
CHARGER_JEITA	R/W	0x0F	VBAT_0<T<10[1:0]		VBAT_45<T<60[1:0]		I_CHG_0<T<10[1:0]		I_CHG_45<T<60[1:0]	
BAT_CNTL	R/W	0x10	BT_UVLO_VP REQ		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
PRODUCT_ID_A	R/W	0x11	PRODUCT_ID[7:0]							
PRODUCT_ID_B	R/W	0x12	PRODUCT_ID[15:8]							
VENDOR_ID_A	R/W	0x13	VENDOR_ID[7:0]							
VENDOR_ID_B	R/W	0x14	VENDOR_ID[15:8]							

Table 10. CHIP_ID (Register 0x00)

ADDRESS	0x00	RESET VALUE	N/A
		RESET CONDITION	N/A
		I²C ACCESS	(USB_OK = and $V_{BAT} > V_{BAT\_UVLO}$) or USB_OK = 1

BIT	TYPE	NAME	DESCRIPTION	DEFAULT
0	R	DIE_TYPE[3:0]	Identifies die type, LSB	1
1				
2				
3				
4	R	DIE_TYPE[7:4]	Identifies die type, MSB	9
5				
6				
7				

Table 11. CHIP_REV (Register 0x01)

ADDRESS	0x01	RESET VALUE	N/A
		RESET CONDITION	N/A
		I²C ACCESS	(USB_OK = 0 and $V_{BAT} > V_{BAT\_UVLO}$) or USB_OK = 1

BIT	TYPE	NAME	DESCRIPTION	DEFAULT
0	R	MASK_SET[3:0]	Identifies mask set	0
1				
2				
3				
4	R	DASH[3:0]	Identifies dash level	1
5				
6				
7				

Table 12. STATUS_A (Register 0x02)

ADDRESS	0x02	RESET VALUE	N/A
		RESET CONDITION	N/A
		I²C ACCESS	USB_OK = 1

BIT	TYPE	NAME	DESCRIPTION	DEFAULT
0 1 2	R	CHG_STAT[2:0]	**Status of Charger Mode** 000 = Charger off 001 = Charger suspended due to temperature 010 = Precharge in progress 011 = Fast-charge in progress 100 = Top-off charge in progress 101 = Maintains charge in progress 110 = Charge done 111 = Charger fault condition	N/A
3	R	BAT_DET	**Status of Battery Detection** 0 = No battery detected 1 = Battery detected	N/A
4 5 6 7	R	CHG_TYPE[3:0]	**Adapter Type Detected** 0000 = Not detected yet 0001 = (SDP) No enumeration/enumeration in progress 0010 = Charging downstream port (CDP) 0011 = Dedicated charger port (DCP) 0100 = Apple 500mA 0101 = Apple 1000mA 0110 = Apple 2000mA 0111 = Other charger 1000 = Downstream port 100mA (SDP) 1001 = Downstream port 500mA (SDP) 1010 = Sony charger 500mA 1011 = Sony charger 500mA (Type B) 1100 = DP_DM_ open 1101 = (CDP) No enumeration/enumeration in progress	N/A

Table 13. STATUS_B (Register 0x03)

ADDRESS	0x03	RESET VALUE	N/A
		RESET CONDITION	N/A
		I²C ACCESS	(USB_OK = 0 and V_{BAT} > V_{BAT_UVLO}) or USB_OK = 1

BIT	TYPE	NAME	DESCRIPTION	DEFAULT
0 1 2	R	THRM_STAT[2:0]	**Status of Thermal Monitor** 000 = T < 0°C 001 = 0°C < T < 10°C 010 = 10°C < T < 45°C 011 = 45°C < T < 60°C 100 = 60°C < T 101 = NTC input disabled 110 = Reserved for future use 111 = Reserved for future use	N/A
3	R	USB_OK	**Status of BUS Input** 0 = V_{BUS} not present out of valid range 1 = V_{BUS} present and within valid range	Only bit 3 (USB_OK) is available and the others are not available at the battery only mode
4	R	ENUM_FLT	**Enumeration Fault** 0 = No fault detected 1 = Enumeration fault detected	N/A
5	R	Reserved	Reserved	—
6	R	ILIM	**Input Current Limit** 0 = Input current limit not reach 1 = Input in current limit	N/A
7	R	SUS	**USB Suspend Mode** 0 = USB interface not in suspend mode 1 = USB interface in suspend mode	N/A

Table 14. STATUS_C (Register 0x04)

ADDRESS	0x04	RESET VALUE	N/A
		RESET CONDITION	N/A
		I²C ACCESS	USB_OK = 1

BIT	TYPE	NAME	DESCRIPTION	DEFAULT
0	R	nEXT_PWR_ON	**Logic Status of Hardware Output $\overline{\text{EXT\_PWR\_ON}}$** 0 = Logic-low 1 = Logic-high	N/A
1	R	nUOK	**Logic Status of Hardware Output $\overline{\text{UOK}}$** 0 = Logic-low 1 = Logic-high	N/A
2	R	FS_DET	**Logic Status of Full-Speed Detection** 0 = Only low-speed supported 1 = Full-speed and low-speed supported	N/A
3	R	THRM_SD	**Latched Status of Thermal Shutdown, Only Reset Upon Read** 0 = Normal operation 1 = Thermal shutdown has occurred	N/A
4	R	CEN	**Logic Status of Hardware Input CEN** 0 = Logic-low 1 = Logic-high	N/A
5	R	nSTDB_EN_HW	**Logic Status of Hardware Input $\overline{\text{STDB\_EN\_HW}}$** 0 = Logic-low 1 = Logic-high	N/A
6	R	nENU_EN_HW	**Logic Status of Hardware Input $\overline{\text{ENU\_EN\_HW}}$** 0 = Logic-low 1 = Logic-high	N/A
7	R	IBUS_DEF	**Logic Status of Hardware Input IBUS_DEF** 0 = Logic-low 1 = Logic-high	N/A

Table 15. EVENT_A (Register 0x05)

ADDRESS	0x05	RESET VALUE	0x00
		RESET CONDITION	Reset upon read or POR or USB_OK = 0
		I²C ACCESS	USB_OK = 1

BIT	TYPE	NAME	DESCRIPTION	DEFAULT
0	R	TIME_OUT_IRQ	Charge timer expired caused nIRQ	0
1	R	THERM_REG_IRQ	Charger in thermal regulation caused nIRQ	0
2	R	CHG_STAT_IRQ	Change in charger status caused nIRQ	0
3	R	BAT_DET_IRQ	Change in BAT_DET caused nIRQ	0
4	R	HW_IN_IRQ	Change in HW inputs ($\overline{\text{STDB\_EN\_HW}}$, CEN, $\overline{\text{ENU\_EN\_HW}}$ or IBUS_DEF caused nIRQ)	0
5	R	HW_OUT_IRQ	Change in HW outputs ($\overline{\text{UOK}}$ or $\overline{\text{EXT\_PWRON}}$) caused nIRQ	0
6	R	Reserved	Reserved	0
7	R	DET_DONE_IRQ	Change in CHG_TYPE caused nIRQ	0

Table 16. EVENT_B (Register 0x06)

ADDRESS	0x06	RESET VALUE	0x00
		RESET CONDITION	RESET UPON READ or POR or USB_OK = 0
		I²C ACCESS	USB_OK = 1

BIT	TYPE	NAME	DESCRIPTION	DEFAULT
0	R	LOW_BAT_T_IRQ	Low battery temperature caused nIRQ (T < 0°C)*	0
1	R	HIGH_BAT_T_IRQ	High battery temperature caused nIRQ (45°C < T < 60°C)*	0
2	R	WHIGH_BAT_T_IRQ	Very high battery temperature caused nIRQ (T > 60°C)*	0
3	R	BUS_OK_IRQ	Change in internal signal USB_OK caused nIRQ	0
4	R	ENUM_FLT_IRQ	Enumeration fail caused nIRQ	0
5	R	ILIM_IRQ	Input current limit triggered caused nIRQ	0
6	R	RESUME_IRQ	USB resume	0
7	R	SUS_IRQ	Suspend mode entered caused nIRQ	0

**Temperature values assume a 100kI NTC thermistor with A = 4250K is used.*

Table 17. IRQ_MASK_A (Register 0x07)

ADDRESS	0x07	RESET VALUE	0x00
		RESET CONDITION	POR or USB_OK = 0
		I²C ACCESS	USB_OK = 1

BIT	TYPE	NAME	DESCRIPTION	DEFAULT
0	R/W	TIME_OUT_IRQ_MASK	**nIRQ Mask Bit for TIME_OUT_IRQ** 0 = $\overline{IRQ}$ pin pulled low 1 = $\overline{IRQ}$ pin unchanged	0
1	R/W	THERM_REG_IRQ_MASK	**nIRQ Mask Bit for THERM_REG_IRQ** 0 = $\overline{IRQ}$ pin pulled low 1 = $\overline{IRQ}$ pin unchanged	0
2	R/W	CHG__STAT_IRQ_MASK	**nIRQ Mask Bit for CHG_STAT_IRQ** 0 = $\overline{IRQ}$ pin pulled low 1 = $\overline{IRQ}$ pin unchanged	0
3	R/W	BAT_DET_IRQ_MASK	**nIRQ Mask Bit for BAT_DET_IRQ** 0 = $\overline{IRQ}$ pin pulled low 1 = $\overline{IRQ}$ pin unchanged	0
4	R/W	HW_IN_IRQ_MASK	**nIRQ Mask Bit for HW_IN_IRQ** 0 = $\overline{IRQ}$ pin pulled low 1 = $\overline{IRQ}$ pin unchanged	0
5	R/W	HW_OUT_IRQ_MASK	**nIRQ Mask Bit for HW_OUT_IRQ** 0 = $\overline{IRQ}$ pin pulled low 1 = $\overline{IRQ}$ pin unchanged	0
6	R/W	Reserved	Reserved	0
7	R/W	DET_DONE_IRQ_MASK	nIRQ mask bit for DET_DONE_IRQ 0 = $\overline{IRQ}$ pin pulled low 1 = $\overline{IRQ}$ pin unchanged	0

Table 18. IRQ_MASK_B (Register 0x08)

ADDRESS	0x08	RESET VALUE	0x00
		RESET CONDITION	POR or USB_OK = 0
		I²C ACCESS	USB_OK = 1

BIT	TYPE	NAME	DESCRIPTION	DEFAULT
0	R/W	LOW_BAT_T_IRQ_MASK	**nIRQ Mask Bit for LOW_BAT_T_IRQ** 0 = $\overline{IRQ}$ pin pulled low 1 = $\overline{IRQ}$ pin unchanged	0
1	R/W	HIGH_BAT_T_IRQ_MASK	**nIRQ Mask Bit for HIGH_BAT_T_IRQ** 0 = $\overline{IRQ}$ pin pulled low 1 = $\overline{IRQ}$ pin unchanged	0
2	R/W	WHIGH_BAT_IRQ_MASK	**nIRQ Mask Bit for WHIGH_BAT_IRQ** 0 = $\overline{IRQ}$ pin pulled low 1 = $\overline{IRQ}$ pin unchanged	0
3	R/W	BUS_OK_IRQ_MASK	**nIRQ Mask Bit for BUS_OK_IRQ** 0 = $\overline{IRQ}$ pin pulled low 1 = $\overline{IRQ}$ pin unchanged	0
4	R/W	ENUM_FLT_IRQ_MASK	**nIRQ Mask Bit for ENUM_FLT_IRQ** 0 = $\overline{IRQ}$ pin pulled low 1 = $\overline{IRQ}$ pin unchanged	0
5	R/W	ILIM_IRQ_MASK	**nIRQ Mask Bit for ILIM_IRQ** 0 = $\overline{IRQ}$ pin pulled low 1 = $\overline{IRQ}$ pin unchanged	0
6	R/W	RESUME_IRQ_MASK	**nIRQ Mask Bit for RESUME_IRQ** 0 = $\overline{IRQ}$ pin pulled low 1 = $\overline{IRQ}$ pin unchanged	0
7	R/W	SUS_IRQ_MASK	**nIRQ Mask Bit for DET_DONE_IRQ** 0 = $\overline{IRQ}$ pin pulled low 1 = $\overline{IRQ}$ pin unchanged	0

Table 19. USB_CNTL (Register 0x09)

ADDRESS	0x09	RESET VALUE	N/A
		RESET CONDITION	POR or USB_OK = 0
		I²C ACCESS	USB_OK = 1

BIT	TYPE	NAME	DESCRIPTION	DEFAULT
0	R/W	KB_TM_EN	**Keyboard Test Mode** 0 = Keyboard test mode disabled 1 = If nENU_EN_HW_MASK is 1, then logic input $\overline{\text{ENU\_EN\_HW}}$ is used for generating a KB_TM internal signal.	0
1	R/W	DCD_EN	**Data Contact Detection Enable** 0 = Not enabled 1 = Enabled	1
2	R/W	nENU_EN_HW_MASK	**Mask for Logic Input $\overline{\text{ENU\_EN\_HW}}$** 0 = nENU_EN =$\overline{\text{ENU\_EN\_HW}}$ 1 = $\overline{\text{ENU\_EN\_HW}}$ disabled	0
3	R/W	nENU_EN	**ON/OFF Control for Autoenumeration** For nENU_EN_HW_MASK = 0, the nENU_EN controlled by the $\overline{\text{ENU\_EN\_HW}}$ logic input regardless of what is written to this bit. For nENU_EN_HW_MASK = 1, this bit is controlled by I²C. Status of the nENU_EN bit is as follows: 0 = Self-enumeration enabled 1 = Self-enumeration disabled	$\overline{\text{ENU\_EN\_HW}}$
4	R/W	nSTDB_EN_HW_MASK	**Mask for Logic Input $\overline{\text{STDB\_EN\_HW}}$** 0 = nSTDB_EN = $\overline{\text{STDB\_EN\_HW}}$ 1 = $\overline{\text{STDB\_EN\_HW}}$ disabled	0
5	R/W	nSTDB_EN	**Force Standby Mode** For nSTDB_EN_HW_MASK = 0, the nSTDB_EN is controlled by the $\overline{\text{STDB\_EN\_HW}}$ logic input regardless of what is written to this bit. For nSTDB_EN_HW_MASK = 1, this bit is controlled by I²C. 0 = Forced into standby mode 1 = Normal operation	$\overline{\text{STDB\_EN\_HW}}$
6	R/W	SUS_EN	**Select Suspend Mode Operation** 0 = Do not allow suspend mode 1 = Allow for automatic suspend mode	1
7	R/W	RWU_EN	**Select Remote Wakeup Operation** 1 = If the IC is forced into suspend mode and RWU is not supported when force resumes 0 = Allow the IC to be forced into suspend mode	0

Table 20. BAT_CNTL (Register 0x10)

ADDRESS	0x10	**RESET VALUE**	0x00
		RESET CONDITION	POR or (USB_OK = 0 and V_{BAT} < V_{BAT_UVLO})
		I²C ACCESS	(USB_OK = 0 and V_{BAT} > V_{BAT_UVLO}) or USB_OK = 1

BIT	TYPE	NAME	DESCRIPTION	DEFAULT
0	R/W	Reserved	Reserved	0
1	R/W	Reserved	Reserved	0
2	R/W	Reserved	Reserved	0
3	R/W	Reserved	Reserved	0
4	R/W	Reserved	Reserved	0
5	R/W	Reserved	Reserved	0
6	R/W	Reserved	Reserved	0
7	R/W	BAT_UVLO_VPREQ	**Battery Undervoltage and Prequalification** 0 = Specifies low voltage type battery which sets lower voltage threshold for UVLO (fall/rise) and prequal to fast charge (fall/rise) voltage thresholds. See the *Electrical Characteristics* table. 1 = Specifies typical lithium-ion type battery which sets lower voltage threshold for UVLO (fall/rise) and prequal to fast-charge (fall/rise) voltage thresholds. See the *Electrical Characteristics* table.	0

Table 21. IBUS_CNTL (Register 0x0A)

ADDRESS	0x0A	RESET VALUE	0x24
		RESET CONDITION	POR OR USB_OK = 0
		I²C ACCESS	USB_OK = 1

BIT	TYPE	NAME	DESCRIPTION	DEFAULT
0 1	R/W	IBUS_DET_SW[1:0]	**Actual Current Allowed to be Drawn from V_{BUS}** 00 = I_{SUS} 01 = 100mA 10 = 500mA 11 = Determined by ILIM[2:0]	00
2 3 4	R/W	ILIM[2:0]	**IBUS Input Current Limit for IBUS_DET = 11** 000 = 100mA 001 = 500mA 010 = 600mA 011 = 700mA 100 = 900mA 101 = 1000mA 110 = 1500mA 111 = Reserved	001
5 6	R/W	V_SYS[1:0]	**Set Minimum SYS Voltage when Valid Adapter is Connected** 00 = 3.4V 01 = 4.35V 10 = 4.4V 11 = 4.5V	01
7	R/W	IBUS_LIM	**IBUS Input Current Limit** 0 = Automatic determined using adapter detection state machine (IBUS_DET) 1 = Controlled manually using I2C. Setting of IBUS_DET_SW is used to determine input current limit condition.	0

Table 22. CHARGER_CNTL_A (Register 0x0B)

ADDRESS	0x0B	RESET VALUE	0x6B
		RESET CONDITION	POR OR USB_OK = 0
		I²C ACCESS	USB_OK = 1

BIT	TYPE	NAME	DESCRIPTION	DEFAULT
0 1	R/W	THERM_REG[1:0]	**Thermal Regulation Threshold Selection** 00 = 90°C 01 = 100°C 10 = 110°C 11 = 120°C	11
2 3 4	R/W	IFCHG[2:0]	**Setting the Fast-Charging Current** 000 = 100mA 010 = 200mA 001 = 300mA 110 = 370mA 111 = 450mA 011 = 600mA 100 = 800mA 101 = 900mA	010
5 6	R/W	TCHG[1:0]	**Topoff Charging in % of IFCHG** 00 = 40% 01 = 60% 10 = 80% 11 = 100%	11
7	R/W	Reserved	Reserved	0

Table 23. CHARGER_CNTL_B (Register 0x0C)

ADDRESS	0x0C	RESET VALUE	N/A
		RESET CONDITION	POR or USB_OK = 0
		I²C ACCESS	USB_OK = 1

BIT	TYPE	NAME	DESCRIPTION	DEFAULT
0 1 2	R/W	CHG_DONE[2:0]	**Setting the Charge Done Threshold** 000 = 10mA 001 = 20mA 010 = 40mA 011 = 50mA 100 = 60mA 101 = 80mA 110 = 100mA 111 = 120mA	100
3	R/W	nCEN_MASK	**Mask for Logic Input CEN** 0 = CHG_EN = CEN 1 = CEN is disabled	0
4	R/W	CHG_EN	**On/Off Control for Charger (does not impact SYS note).** For nCEN_MASK = 0, the CHG_EN controlled by the CEN logic input regardless of what is written to this bit. For nCEN_MASK = 1, this bit is controlled by I²C. 0 = Charger disabled 1 = Charger enabled	CEN
5	R/W	BAT_DET_CNTL	**Battery Present Detection** 0 = Use internal circuit to determine battery present condition 1 = Use NTC present to determine battery present condition	1
6	R/W	BAT_DET_MASK	**Battery Detection Mask** 0 = Enable. Battery detection result controls, $\overline{\text{EXT\_PWRON}}$ to be high impedance for 63ms and affects charging function 1 = Disable, no affect on EXTPWRON or charging functions	0
7	R/W	THERM_EN	**On/Off Control for NTC Input** 0 = NTC input disabled 1 = NTC input enabled	1

Table 24. CHARGER_TMR (Register 0x0D)

ADDRESS	0x0D	RESET VALUE	0x2E
		RESET CONDITION	POR or USB_OK = 0
		I²C ACCESS	USB_OK = 1

BIT	TYPE	NAME	DESCRIPTION	DEFAULT
0 1	R/W	PCHG_TMR[1:0]	**Setting the Precharge Timer** 00 = 30min 01 = 60min 10 = 120min 11 = 240min	10
2 3	R/W	FCHG_TMR[1:0]	**Setting the Fast-Charge and Topoff-Charge Timers** 00 = 75min 01 = 150min 10 = 300min 11 = 600min	11
4 5	R/W	MTCHG_TMR[1:0]	**Setting the Maintain Charge Timer** 10 = 0min 01 = 15min 00 = 30min 11 = 60min	10
6	R/W	Reserved	Reserved	0
7	R/W	Reserved	Reserved	0

Table 25. CHARGER_VSET (Register 0x0E)

ADDRESS	0x0E	RESET VALUE	0x36
		RESET CONDITION	POR or USB_OK = 0
		I^2C ACCESS	USB_OK = 1

BIT	TYPE	NAME	DESCRIPTION	DEFAULT
0 1	R/W	BAT_FCHG[1:0]	**Setting the Fast-Charging Threshold** 00 = 3.8V 01 = 3.9V 10 = 4.0V 11 = 4.1V	10
2 3	R/W	BAT_FCHG_HYS[1:0]	**V_{BAT} Falling Threshold, Where Charging Current is Increased to I_{FCHG}** 00 = 150mV 01 = 200mV 10 = 250mV 11 = 300mV	01
4 5	R/W	BAT_REG[1:0]	**Setting the Battery Regulation Threshold** 00 = 4.05V 01 = 4.10V 10 = 4.15V 11 = 4.20V	11
6 7	R/W	BAT_RECHG[1:0]	**Recharge Threshold in Relation to $V_{BAT\_}$ in DONE State Going into Topoff Mode** 00 = -350mV 10 = -300mV 01 = -250mV 11 = -200mV	00

Table 26. CHARGER_JEITA (Register 0x0F)

ADDRESS	0x0F	RESET VALUE	0x50
		RESET CONDITION	POR or USB_OK = 0
		I²C ACCESS	USB_OK = 1

BIT	TYPE	NAME	DESCRIPTION	DEFAULT
0 1	R/W	I_CHG_45<T<60[1:0]	**Percent of Fast-Charge Current in the Temperature Range of +45°C < T < +60°C** 00 = 100% 01 = 75% 10 = 50% 11 = 25%	00
2 3	R/W	I_CHG_0<T<10[1:0]	**Percent of Fast-Charge Current in the Temperature range of 0°C < T < +10°C** 00 = 100% 01 = 75% 10 = 50% 11 = 25%	00
4 5	R/W	VBAT_45<T<60[1:0]	**BAT_REG Offset in the Temperature Range of +45°C < T < +60°C** 00 = -100mV 10 = -125mV 01 = -150mV 11 = -175mV	01
6 7	R/W	VBAT_0<T<10[1:0]	**BAT_REG Offset in the Temperature Range of 0°C < T < +10°C** 00 = -100mV 10 = -125mV 01 = -150mV 11 = -175mV	01

Table 27. PRODUCT_ID_A (Register 0x11)

ADDRESS	0x11	RESET VALUE	N/A
		RESET CONDITION	POR or (USB_OK = 0 and V_{BAT} < V_{BAT_UVLO})
		I²C ACCESS	(USB_OK = 0 and V_{BAT} > V_{BAT_UVLO}) or USB_OK = 1

BIT	TYPE	NAME	DESCRIPTION	DEFAULT
0	R/W	PRODUCT_ID[7:0]		*
1				
2				
3				
4				
5				
6				
7				

**Contact factory for available preset values.*

Table 28. PRODUCT_ID_B (Register 0x12)

ADDRESS	0x12	RESET VALUE	N/A
		RESET CONDITION	POR or (USB_OK = 0 and V_{BAT} < V_{BAT_UVLO})
		I²C ACCESS	(USB_OK = 0 and V_{BAT} > V_{BAT_UVLO}) or USB_OK = 1

BIT	TYPE	NAME	DESCRIPTION	DEFAULT
0	R/W	PRODUCT_ID[15:8]		*
1				
2				
3				
4				
5				
6				
7				

**Contact factory for available preset values.*

Table 29. VENDOR_ID_A (Register 0x13)

ADDRESS	0x13	RESET VALUE	N/A
		RESET CONDITION	POR or (USB_OK = 0 and V_{BAT} < V_{BAT_UVLO})
		I²C ACCESS	(USB_OK = 0 and V_{BAT} > V_{BAT_UVLO}) or USB_OK = 1

BIT	TYPE	NAME	DESCRIPTION	DEFAULT
0	R/W	VENDOR_ID[7:0]	Lower 8 bits of VendorID	*
1				
2				
3				
4				
5				
6				
7				

**Contact factory for available preset values.*

Table 30. VENDOR_ID_B (Register 0x14)

ADDRESS	0x14	RESET VALUE	N/A
		RESET CONDITION	POR or (USB_OK = 0 and V_{BAT} > V_{BAT_UVLO})
		I²C ACCESS	(USB_OK = 0 and V_{BAT} > V_{BAT_UVLO}) or USB_OK = 1

BIT	TYPE	NAME	DESCRIPTION	DEFAULT
0	R/W	VENDOR_ID[15:8]	Higher 8 bits of VendorID	*
1				
2				
3				
4				
5				
6				
7				

**Contact factory for available preset values.*

Figure 25. Recommended PCB Layout for Full Speed

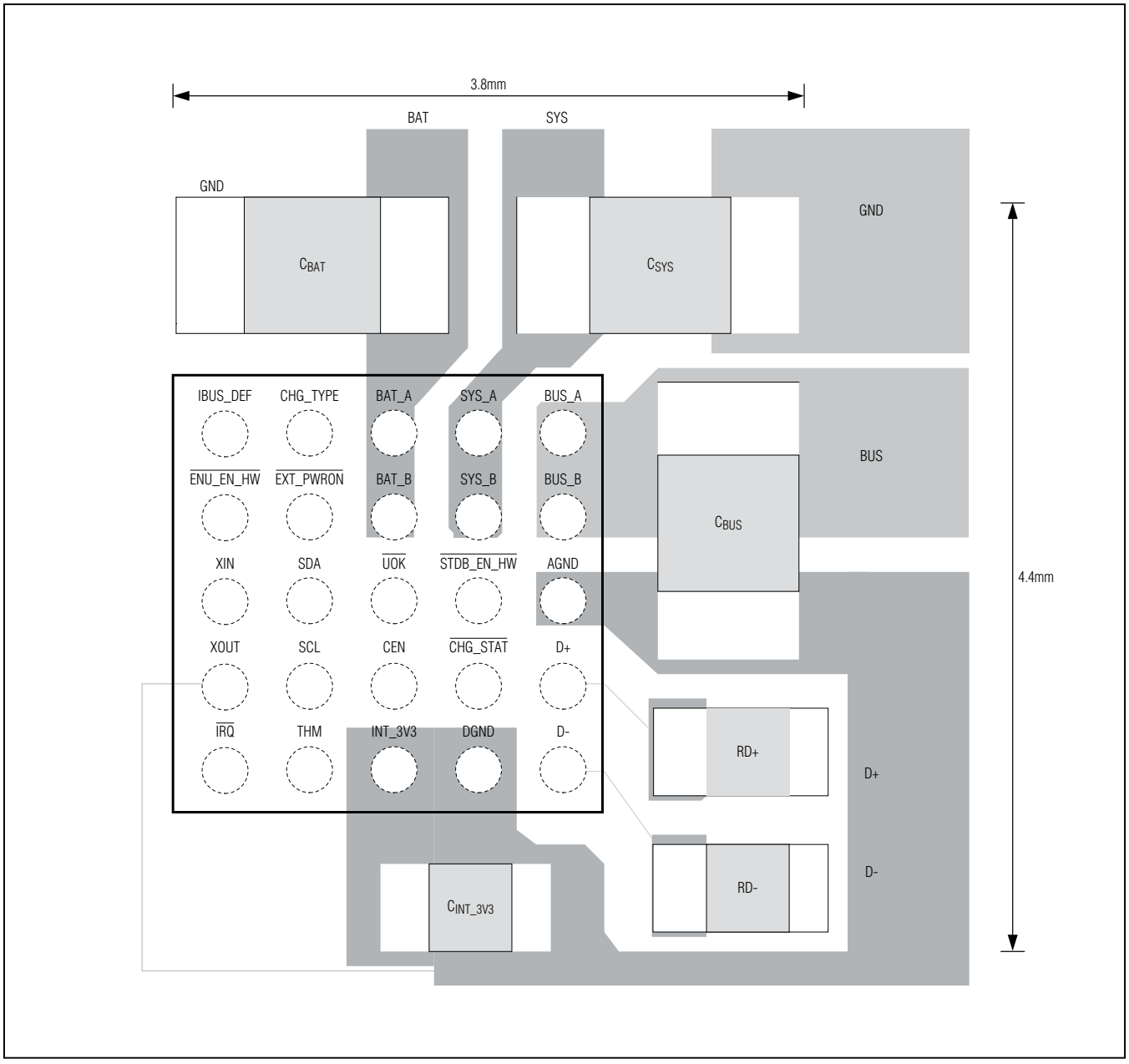


Figure 26. Recommended PCB Layout for Low Speed

Chip Information

PROCESS: BiCMOS

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX77301EWA+T	-40°C to +85°C	25 WLP (0.4mm pitch)

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

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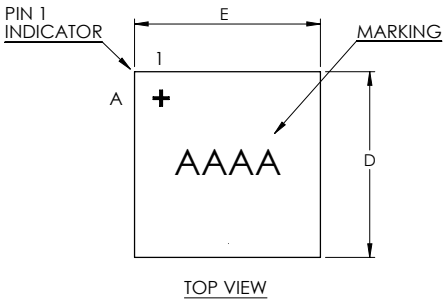
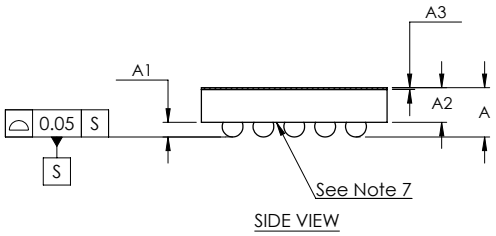
Package Information

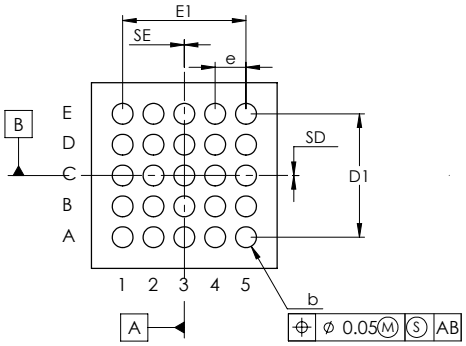
For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
25 WLP (0.4mm pitch)	W252H2+1	21-0453	Refer to Application Note 1891





COMMON DIMENSIONS		
A	0.64	±0.05
A1	0.19	±0.03
A2	0.45	REF
A3	0.025	BASIC
b	Ø0.27	±0.03
D1	1.60	
E1	1.60	
e	0.40	BASIC
SD	0.00	BASIC
SE	0.00	BASIC



PKG. CODE	E MIN	E MAX	D MIN	D MAX	DEPOPULATED BUMPS
W252D2+1	2.25	2.36	2.25	2.36	NONE
W252F2+1	2.02	2.16	2.02	2.16	NONE
W252G2+1	2.32	2.44	2.22	2.34	NONE
W252H2+1	2.41	2.44	2.41	2.44	NONE

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

- DRAWING NOT TO SCALE -

TITLE			
PACKAGE OUTLINE 25 BUMPS, WLP PKG. 0.4mm PITCH			
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0453	D	1/1

JEITA-Compliant, Li+ Charger with Smart Power Selector, Automatic Detection, and USB Enumeration

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/13	Initial release	—