Application Note

TUSB1044 I²C Mode Control and Tuning With TPS6598x and TPS6599x

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ABSTRACT

The TUSB1044 is a linear redriver solution that supports USB Type-C® port signal conditioning at a data rate up to 10Gbps for USB and 8.1Gbps for DisplayPort™ (DP) protocols. It is to be designed in a system with an already integrated internal USB Type-C MUX, so that only four-lane data are routed from the PCH to the USB Type-C port. This application report details the I2C implementation of TUSB1044 control and configuration via the PD controller TPS6598X and TPS6599X family.

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1 Introduction

This application note explains the key USB Type-C control, DP pin assignment configuration, and signal tuning working flow for TUSB1044 with TI PD controller TPS6598X and TPS6599X family.

The TI PD controller TPS6598X and TPS6599X families are highly-integrated PD controller solutions with two power switches integrated for sink and source (TPS6598X) or source (TPS6599X) power paths and compliant for PD3.0 operation. The PD controller acts as a primary and configures the TUSB1044 in the GPIO or the I2C mode depends on the CC and PD communication of the PD controller.

For host (source) or device (sink) applications, the TUSB1044 enables a USB/DP compliant system to pass both USB/DP transmitter electrical compliance and USB receiver jitter tolerance tests.

2 TUSB1044 Configuration and Control Implementation

2.1 TUSB1044 Four-Level Pins

The TUSB1044 has (I2C_EN, UEQ[1:0], DEQ[1:0], CFG[1:0], and A[1:0]) four-level input pins that are used to control the equalization gain, voltage linearity range, and place TUSB1044 into different modes of operation.

The four-level inputs utilize a resistor divider to help set the four valid levels and provide a wider range of control settings. There is an internal pullup and a pulldown resistor. These resistors, together with the external resistor connection combine to achieve the desired voltage level. Table 2-1 defines the external resistors implementation options.

Table 2-1. TUSB1044 Four-Level Pin Configurations

Level	Setting
0	Tie 1 kΩ (5%) to or tie directly to GND
R	Tie 20 kΩ (5%) to GND
F	Pin floating
1	Tie 1 kΩ (5%) to or tie directly to VCC

2.1.1 I2C_EN

The TUSB1044 is in GPIO mode when I2C_EN = “0” or I2C_EN = "F", and in I2C mode when I2C_EN = “1” as shown in Table 2-2.

Table 2-2. I2C_EN Pin Four-Level Configurations

Level	Setting
0	GPIO Mode, Aux Snoop Enabled (I2C disabled)
R	TI Test Mode (I2C enabled)
F	GPIO Mode, Aux Snoop Disabled (I2C disabled)
1	I2C enabled

2.1.2 VIO_SEL

The VIO_SEL selects I/O voltage levels for the two-level GPIO configuration pins and the I²C interface as shown in Table 2-3.

Table 2-3. VIO_SEL Pin Four-Level Configurations

Level	Setting
0	3.3-V configuration I/O voltage, 3.3-V I²C interface (Default)
R	3.3-V configuration I/O voltage, 1.8-V I²C interface
F	1.8-V configuration I/O voltage, 3.3-V I²C interface
1	1.8-V configuration I/O voltage, 1.8-V I²C interface

2.1.3 UEQ[1:0] and DEQ[1:0]

The TUSB1044 receiver equalization (EQ) is to compensate for channel insertion loss and inter-symbol interference in the system. The receiver overcomes these losses by attenuating the low-frequency components of the signals with respect to the high-frequency components. Each channel has a receiver equalizer with selectable gain settings as shown in Table 2-4. Set equalization control for upstream and downstream facing ports using the UEQ[1:0], and DEQ[1:0] pins, respectively.

Figure 2-1 shows the TUSB1044 equalization settings.

	Downstream Facing Ports using 1100mV linearity setting				Upstream Facing Port using 1100mV linearity setting			
EQ Setting #	DEQ1 pin Level	DEQ0 pin Level	EQ GAIN 5GHz (dB)	EQ GAIN 4.05GHz (dB)	UEQ1 pin Level	UEQ0 pin Level	EQ GAIN 5GHz (dB)	EQ GAIN 4.05GHz (dB)
0	0	0	-2.1	-1.4	0	0	-4.4	-3.3
1	0	R	0	0.4	0	R	-2.2	-1.5
2	0	F	1.5	1.7	0	F	0.7	0.0
3	0	1	3.0	3.2	0	1	0.9	1.4
4	R	0	4.0	4.1	R	0	1.9	2.4
5	R	R	5.0	5.2	R	R	3.0	3.5
6	R	F	5.9	6.1	R	F	3.8	4.3
7	R	1	6.7	6.9	R	1	4.7	5.2
8	F	0	7.4	7.7	F	0	5.4	6.0
9	F	R	8.0	8.3	F	R	6.0	6.6
10	F	F	8.5	8.8	F	F	6.5	7.2
11	F	1	9.0	9.4	F	1	7.1	7.7
12	1	0	9.4	9.8	1	0	7.5	8.1
13	1	R	9.8	10.3	1	R	7.9	8.6
14	1	F	10.1	10.6	1	F	8.3	9.0
15	1	1	10.5	11.0	1	1	8.6	9.4

Figure 2-1. TUSB1044 Equalization Settings

Using the given trace lengths and data rate referring to the Figure 2-2 example, the method to select the equalization values for upstream and downstream EQ is to select the closest EQ gain value available to match the trace loss as follows:

- Host to TUSB1044 trace length 8 in (7-dB loss at 5 GHz). UEQ setting of 7.1 dB.
- TUSB1044 to connector trace length 2 in (1.7-dB loss at 5 GHz). DEQ setting of 3 dB

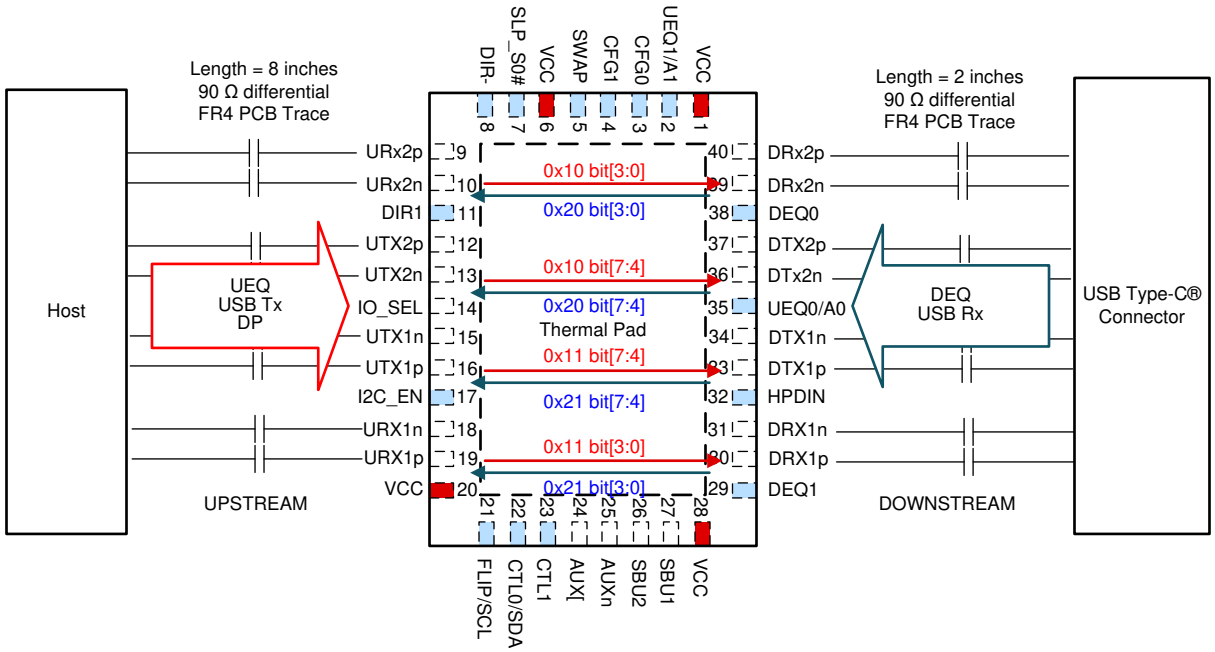

Figure 2-2. Reference Block Diagram for TUSB1044 Equalization Control

In the I²C mode, the equalization settings for each receiver can be independently controlled through I²C registers. For this reason, all of the equalization pins (UEQ[1:0] and DEQ[1:0]) can be left unconnected. If a different I²C slave address is desired, UEQ1/A1 and UEQ0/A0 pins should be set to a level other than 'F' which produces the desired I²C slave address.

2.1.4 CFG[1:0]

The CFG[1:0] can be used to adjust the TUSB1044 output voltage swing linear range and receiver equalization DC gain. Table 2-4 details the available options. For best performance, operate the TUSB1044 within its defined VOD linearity range. Keep the gain of the incoming VID to less than or equal to the TUSB1044 VOD linear range setting. This can be determined using Equation 1:

$$VID\ at\ 5\ GHz = VOD \times 10^{-\left(\frac{Gv}{20}\right)} \quad (1)$$

where

- Gv = TUSB1044 Gain
- VOD = TUSB1044 VOD linearity setting

For example, for a VOD linearity range setting of 1200 mV, the maximum incoming VID signal at 5 GHz with a UEQ[1:0] setting of 5.2 dB is 1200 x ($10^{-(5.2/20)}$) = 659 mVpp. The TUSB1044 can be operated outside its VOD linear range but jitter will be higher.

Table 2-4. TUSB1044 DC Gain and VOD Configuration

Setting #	CFG1 Pin Level	CFG0 Pin Level	Downstream DC Gain(dB)	Upstream DC Gain (dB)	Downstream VOD Linear Range (mVpp)	Upstream VOD Linear Range (mVpp)
0	0	0	1	0	900	900
1	0	R	0	1	900	900
2	0	F	0	0	900	900
3	0	1	1	1	900	900
4	R	0	0	0	1100	1100
5	R	R	1	0	1100	1100
6	R	F	0	1	1100	1100
7	R	1	2	2	1100	1100

Table 2-4. TUSB1044 DC Gain and VOD Configuration (continued)

Setting #	CFG1 Pin Level	CFG0 Pin Level	Downstream DC Gain(dB)	Upstream DC Gain (dB)	Downstream VOD Linear Range (mVpp)	Upstream VOD Linear Range (mVpp)
8	F	0	Reserved	Reserved	Reserved	Reserved
9	F	R	Reserved	Reserved	Reserved	Reserved
10	F	F	0	0	1300	1300
11	F	1	Reserved	Reserved	Reserved	Reserved
12	1	0	Reserved	Reserved	Reserved	Reserved
13	1	R	Reserved	Reserved	Reserved	Reserved
14	1	F	Reserved	Reserved	Reserved	Reserved
15	1	1	Reserved	Reserved	Reserved	Reserved

In the I^2C mode, VOD can be controlled through I^2C register 0x0C. For this reason, CFG[1:0] can be left unconnected.

2.2 TUSB1044 Two-Level Pins

2.2.1 FLIP, CTL0, and CTL1

The PD controller controls the TUSB1044 FLIP depending on the CC communication to support USB Type-C Normal and FLIP orientation. The CTL[1:0] is set by the PD controller depending on the PD communication to operate in USB and DP alternate mode. The combinations of CTL0 and CTL1 support the following configurations: USB3.2 Gen2x1 only, two-lane DP + two-lane USB3.2 Gen2x1, or four-lane DP.

In the I^2C mode, FLIP and CTL0 are designed to work as SCL and SDA respectively and must be connected to the I^2C master of the PD controller. CTL1 can be left as NC. FLIP and CTL[1:0] function are controlled though I^2C register 0x0A.

2.2.2 DIR0 and DIR1

The DIR0 and DIR1 set the data path direction format. The DIR0 chooses between source side (DFP) Alt mode or sink side (UFP) Alt mode. The DIR1 choose between the DP Alt Mode and Custom Alt Mode.

In the I^2C mode, DIR[1:0] can be controlled through I^2C register 0x0C. For this reason, DIR[1:0] can be left unconnected.

2.2.3 SWAP

Further data path direction control can be achieved using the SWAP pin. When set high, the SWAP pin reverses the data path direction on all the channels and swaps the equalization settings of the upstream and downstream facing input ports.

In the I^2C mode, SWAP can be controlled through the I^2C register 0x0A for a global direction swap on all the channels, or register 0x0B for direction swap on individual channels. For this reason, SWAP can be left floating.

2.2.4 HPDIN

The HPDIN works as an input for DisplayPort sink Hot Plug Detect, HPDIN must be high to enable TUSB1044 output in DP mode.

Override the HPDIN with the I^2C register 0x0A to support applications in need of a *virtual* HPD.

2.2.5 SLP_S0#

The SLP_S0# enables and disables RX Detect functionality in USB mode.

While SLP_S0# is low and TUSB1044 is in U2 and U3 mode, TUSB1044 disables LOS and LFPS detection circuitry and RX termination for both channels remains enabled. This allows even lower TUSB1044 power consumption while in the U2 and U3 mode. Once SLP_S0# is asserted high, the TUSB1044 will again start performing far-end receiver detection as well as monitor LFPS so it can determine when to exit the U2 and U3 mode.

When SLP_S0# is asserted low and the TUSB1044 is in disconnect mode, the TUSB1044 remains in Disconnect mode and never performs far-end receiver detection. This allows even lower TUSB1044 power consumption while in the Disconnect mode. Once SLP_S0# is asserted high, the TUSB1044 again starts performing far-end receiver detection so it can determine when to exit the Disconnect mode.

SLP_S0# is typically connected to PCH. If not used, pull SLP_S0# high through a 1-kΩ resistor.

3 TUSB1044 I²C Mode Implementation

When in the I²C mode, the TUSB1044 I²C address is defined by the UEQ0/A0 and UEQ1/A1 pin as shown in Table 3-1.

Table 3-1. TUSB1044 I²C Slave Address Configuration

Pin Combination		TUSB1044 I²C Address	
UEQ1/A1 Pin2 Level	UEQ0/A0 Pin 35 Level	7-bit I²C Address	Bit 0 (W/R)
0	0	0x44	0/1
0	R	0x45	0/1
0	F	0x46	0/1
0	1	0x47	0/1
R	0	0x20	0/1
R	R	0x21	0/1
R	F	0x22	0/1
R	1	0x23	0/1
F	0	0x10	0/1
F	R	0x11	0/1
F	F	0x12	0/1
F	1	0x13	0/1
1	0	0x0C	0/1
1	R	0x0D	0/1
1	F	0x0E	0/1
1	1	0x0F	0/1

Table 3-2 lists the memory-mapped registers for the TUSB1044. Consider all register offset addresses not listed in Table 3-2 as reserved locations and do not modify the reserved register contents.

Table 3-2. TUSB1044 Register Contents

Offset	Acronym	Register Name
Ah	General_1	General Register 1
Bh	General_2	General Register 2
Ch	General_3	General Register 3
10h	UFP2_EQ	UFP2 EQ Control
11h	UFP1_EQ	UFP1 EQ Control
12h	DisplayPort_1	AUX Snoop Status
13h	DisplayPort_2	DP Lane Enable and Disable Control
1Bh	SOFT_RESET	I²C and DPCS Soft Reset
20h	DFP2_EQ	DFP2 EQ Control
21h	DFP1_EQ	DFP1 EQ Control
22h	USB3_MISC	Misc USB3 Controls
23h	USB3_LOS	USB3 LOS Threshold Controls

3.1 TUSB1044 Operating Mode Configuration, General_1 Register, 0x0A

Register 0x0A is the control interface switching the TUSB1044 USB, DP operation mode using bit [2:0]. Table 3-3 lists the bit definitions of register 0x0A. Bit [4] allows the EQ setting to be configured through I2C, overrides the default pin configuration.

Table 3-3. Register 0x0A Bit Definition

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	SWAP_SEL	R/W	0h	Setting this field performs a global direction swap on all the channels. 0h = Channel directions and EQ settings are in normal mode 1h = Reverse all channel directions and EQ settings for the input ports.
4	EQ_OVERRIDE	R/W	0h	Setting this field will allow software to use EQ settings from registers instead of value sampled from pins. 0h = EQ settings based on sampled state of EQ pins. 1h = EQ settings based on programmed value of each of the EQ registers.
3	HPDIN_OVERRIDE	R/W	0h	Overrides HPDIN pin state. 0h = HPD_IN based on HPD_IN pin. 1h = HPD_IN high.
2	FLIP_SEL	R/W	0h	FLIPSEL 0h = Normal Orientation 1h = Flip orientation.
1-0	CTLSEL[1:0]	R/W	1h	Controls the DP and USB modes. 0h = Disabled. All RX and TX for USB3 and DisplayPort are disabled. 1h = USB3.1 only enabled. 2h = Four Lanes of DisplayPort enabled. 3h = USB3.1 and Two DisplayPort Lanes.

3.2 VOD Configuration, General_3 Register 0x0C

General_3 Register 0x0C describes how the VOD and DC Gain are configured through the register.

Specifically, for VOD definition:

- 0x0C bit[6] defines '0' for VOD/DC Gain set by CFG pins and '1' override by I2C
- 0x0C bit[5:4] defines VOD/DC Gain setting mapped to CFG1 (0h='0', 1h='R', 2h='F', 3h='1')
- 0x0C bit[3:2] defines VOD/DC Gain setting mapped to CFG0 (0h='0', 1h='R', 2h='F', 3h='1')
- 0x0C bit[1:0] defined as 0h (as DIR_SEL, for notebook as USB and DP source)

Table 3-4 shows the register 0x0C bit definition.

Table 3-4. Register 0x0C Bit Definition

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	VOD_DCGAIN_OVERRIDE	R/W	0h	Setting of this field will allow software to use VOD linearity range and DC gain settings from registers instead of value sampled from pins 0h = VOD linearity and DC gain settings based on sampled CFG[2:1] pins. 1h = EQ settings based on programmed value of each VOD linearity and DC Gain registers.
5-2	VOD_DCGAIN_SEL	R/W	0h	Field selects VOD linearity range and DC gain for all the channels and in all directions. When VOD_DCGAIN_OVERRIDE = 0b, this field reflects the sampled state of CFG[1:0] pins. When VOD_DCGAIN_OVERRIDE = 1b software can change the VOD linearity range and DC gain for all the channels and in all directions based on value written to this field. Each CFG is a 2-bit value. The register-to-CFG1/0 mapping is: [5:2] = {CFG1[1:0], CFG0[1:0]} where CFGx[1:0] mapping is: 0h = 0 1h = R 2h = F 3h = 1
1-0	DIR_SEL	R/W	0h	Sets the operation mode. 0h = USB + DP Alt Mode Source 1h = USB + DP Alt Mode Sink. 2h = USB + Custom Alt Mode Source 3h = USB + Custom Alt Mode Sink.

3.3 Upstream and Downstream Equalization Configuration Registers, UFP1_EQ, UFP2_EQ, DFP1_EQ, and DFP2_EQ Registers 0x10, 0x11, 0x20, 0x21

UFP2_EQ and UFP1_EQ Register 0x10, 0x11, General_1 Register 0x20, 0x21 are defined to be registers for EQ configuration.

- 0x10 bit[7:4] defines EQ setting for UTx2 channel
- 0x10 bit[3:0] defines EQ setting for URx2 channel
- 0x11 bit[7:4] defines EQ setting for UTx1 channel
- 0x11 bit[3:0] defines EQ setting for URx1 channel
- 0x20 bit[7:4] defines EQ setting for DTx2 channel
- 0x20 bit[3:0] defines EQ setting for DRx2 channel
- 0x21 bit[7:4] defines EQ setting for DTx1 channel
- 0x21 bit[3:0] defines EQ setting for DRx1 channel

4 Benefits of Using the I2C Mode Control

Upon implementation of I2C mode control of TUSB1044, especially for notebooks that have two USB Type-C ports supported by TPS65988 or TPS65994, expect to save 2 × 3 GPIOs of PD controller (pin 21 FLIP for cable orientation control, pin 22 CTL0 for USB3 select, and pin 23 CTL1 for DP mode select which make the PCB design easier with only I2C wires routed to the PD controller and HPD signal routed to the host platform.

Also, during the engineering phase of the project validation, there will always be tuning required to pass the USB and DP compliance test. I2C mode control allows the tuning to happen via a PD FW update which is available in the Operating System for most PD controllers so that engineers do not have to constantly change the resistor configuration and risk the damage to the PCB. Also, I2C mode allows engineers to separately tune the setting for individual lanes and also make USB and DP independent tuning available.

I2C mode allows less configuration resistor placement; therefore saving extra BOM cost and overall PCB space.

Table 4-1 shows the pin configuration comparison between the TUSB1044 in GPIO and I2C mode.

Table 4-1. Pin Configuration Comparison in GPIO and I2C Mode

Pin Definition	GPIO Mode	I2C Mode
CFG0	4-level input	NC
CFG1	4-level input	NC
FLIP/SCL	2-level FLIP input	SCL
CTL0/SDA	2-level CTL0 input	SDA
CTL1	2-level input	NC
DEQ1	4-level EQ input	NC
DEQ0	4-level EQ input	NC
UEQ0/A0	4-level EQ input	4-level I2C address input
UEQ1/A1	4-level EQ input	4-level I2C address input
DIR0	2-level input	NC
DIR1	2-level input	NC

5 TUSB1044 Host Implementation Example

Figure 5-1 shows the TUSB1044 implementation example at the source side. Table 5-1 defines the TUSB1044 pin configuration for this particular example. For AMD platforms, the APU Crossbar and the TUSB1044 are usually controlled by the PD controller using the same I^2C bus. Consider using a level shifter to isolate different power rails and to prevent leakage.

Note

The host platform such as AMD where the rated IO voltage is designed to be 1.8 V, “R” needs to be considered for VIO_SEL pin to support the 1.8-V pull-high for I^2C.

Since the TUSB1044 upstream is connected to the APU and the downstream is connected to the USB Type-C connector, set the SWAP and DIR[0:1] appropriately as shown in Table 5-1. Note that SWAP and DIR[0:1] can also be controlled through I^2C registers.

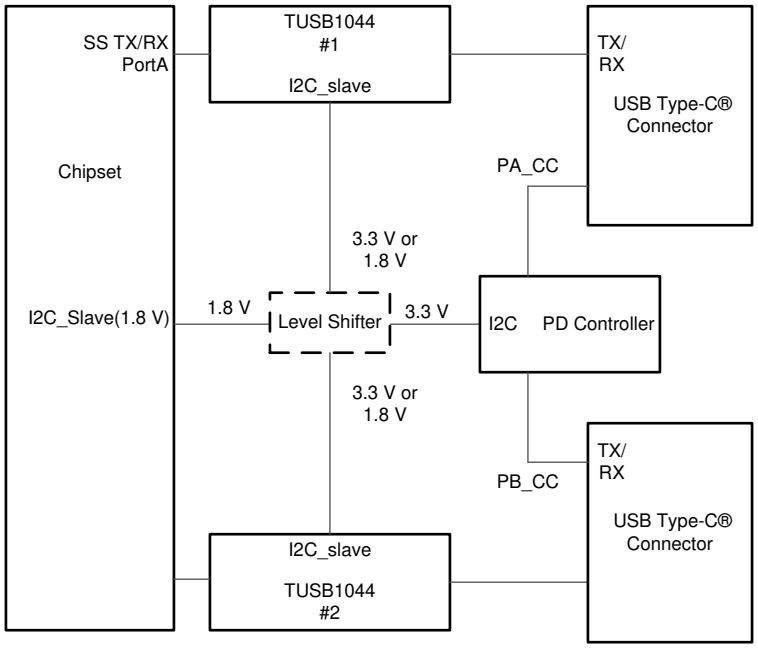

Figure 5-1. TUSB1044 Block Diagram in a DFP System

Table 5-1. TUSB1044 Functional Pins Configurations Example in I^2C Mode

Pin #	Definition	Pin Level
5	Swap	0(Default)
7	SLP_S0#	1(Default)
8	DIR0	0
11	DIR1	0
14	VIO_SEL	R
17	I2C_EN	1

6 TPS6598X, TPS6599X Based I²C Control and Tuning

The PD controller is in-charge of PD communication including handling the message exchange for DP alternate mode entry and pin assignment configuration. The following paragraphs explain how to use the TI PD controller to implement the Display over USB Type-C feature. The TI PD controller has an I²C master that can program the TUSB1044 based on events related to DP alternate mode negotiation. For example, the PD controller sets up the TUSB1044 based on the *POWER_ON_RESET* event.

6.1 Enable PD Controller I²C Control of External Slaves

The TPS6598x and TPS6599x both allow either I2C1 or I2C3 to be I²C master for controlling and configuring the slave devices.

The *Using I2C Master in TPS65987D and TPS65988 PD Controllers* application note introduces the method to initiate a I²C master control through the PD controller configuration GUI.

6.2 Example of I²C Configuration Upon PD Controller PoR Event and Detach Event

The PD controller allows different trigger events to initiate I²C behaviors. On POR, the control register (0x0A), and configuration registers (0x10, 0x11, 0x20, 0x21, part of 0x0C) can be initiated with a pre-defined value.

- 0x0A, write to 0x10 to enable EQ override by I²C, and disable the channels
- 0x0C, write to 0x4C, for example, to enable VOD, DCGain override by I²C, and also to configure the VOD setting to #3 defined in Table 2-4
- 0x10, 0x11, can be configured to 0x77, for example, to set the UEQ to #7 of EQ setting as defined in Figure 2-1
- 0x20, 0x21, could be configured to 0x33, for example, to set the DEQ to #3 of EQ setting defined in Figure 2-1

Note

The settings in the previous list are for reference and the most favorable setting is achieved from PCB design and tuning with SI test and compliance results. The formatted data is as shown in Table 6-1.

Table 6-1. Example of TUSB1044 Configuration Register Setting

Configuration Register Offset	Data	Trigger Event
0x10	0x7710	PoR, *Attach
0x11	0x7711	PoR, *Attach
0x20	0x3320	PoR, *Attach
0x21	0x3321	PoR, *Attach
0x0C	0x4C0C	PoR, *Attach

Figure 6-1 is an example of defining I²C configuration to TUSB1044 over PD controller upon trigger events *Power on Reset*, where “0x10” is the config data for register offset “0x0A” with a total byte count to be ‘2’ defined in the *Data Length*.

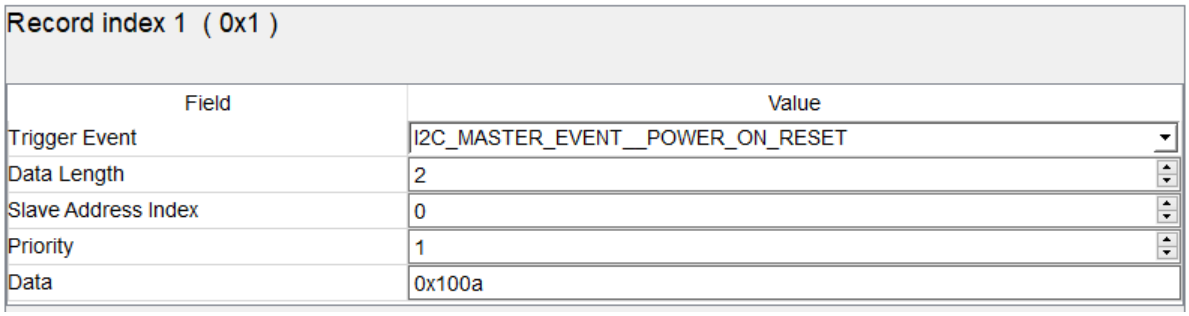

Figure 6-1. Example of TUSB1044 Reset Upon PD Controller PoR

Upon detach event, reset the control register to the same value as PoR.

6.3 Example of I²C Configuration Upon Cable-Orientation Event and DP Configuration Event

The TPS65994 takes over the PD communication to identify whether a USB, USB+DP, four-lane DP device is connected to alert the SOC and also to control the redriver, retimer, or MUX to the corresponding mode based on CC hand-shake results.

TUSB1044 control is based on the configuration to bit[2:0] of 0x0A. Consider a cable attach event with orientation (Attach_UU, Attach_UD, or cable orientation event) to trigger a USB3 configuration and MUX control after PD controller recognized the connection of external device.

Record index 6 (0x6)

Field	Value
Trigger Event	I2C_MASTER_EVENT__ATTACH_UU
Data Length	2
Slave Address Index	0
Priority	1
Data	0x110a

Figure 6-2. Example of USB3 Normal Orientation Configuration to TUSB1044

If the host (as DFP_D) and device (as UFP_D) establish the DP alternate mode connection, the host PD (usually with DFP_D pin C, D, E support based on notebook system design) will acknowledge the device supported pin assignment and preference on multifunction through the ACK message of the device-side PD controller. The PD controller finally selects one of the pin assignments and control or alert the TUSB1044 or SOC accordingly.

Discover Mode	0xC1C47
Reserved (31...24)	0
UFP_D Pin Assignment Supported (23...16)	Pin C, D Supported
DFP_D Pin Assignment Supported (15...8)	Pin C, D, E Supported
USB r2.0 Signaling Not Used (7)	Required on A6–A7/B6–B7 in DP Config
Receptacle Indication (6)	DP ifc is presented on a USB Type-C Receptacle
Signaling for DP Protocol (5...2)	Supports DP v1.3 signaling rates and electrical specification
Port Capability (1...0)	Both DFP_D and UFP_D-capable

Figure 6-3. Example of Discover Mode ACK PD Message (Pin C, D as UFP_D Both Supported)

For a DP connection, there are two trigger events with DP pin A, C, or E, and pin B, D, or F depending on the DP alternate mode negotiation with the connected device.

Record index 8 (0x8)

Field	Value
Trigger Event	I2C_MASTER_EVENT__DP_CONFIG_ACE_UU
Data Length	2
Slave Address Index	0
Priority	0
Data	0x120a

Figure 6-4. Example of a DP Pin A, C, or E Configuration to TUSB1044

Table 6-2 summarizes an example of control data and trigger events respectively.

Table 6-2. Reference TUSB1044 Control Register Setting

Connected Device, Flip	Data	Trigger Event
Unconnected	0x100A	PoR, Detach
USB	0x110A	cable_oriented (cable_attach_UU)
USB_Flip	0x150A	cable_oriented (cable_attach_UD)
Pin B, D, F (for example, USB+DP)	0x130A	DP Config BDF_UU
Pin B, D, F_Flip	0x170A	DP Config BDF_UD
Pin A, C, E (for example, 4-lane DP)	0x120A	DP Config ACE_UU
Pin A, C, E_Flip	0x160A	DP Config ACE_UD

Considering the direction of data transmission, UEQ of the TUSB1044 influences the USB TX and DP test, while DEQ influences only the USB RX compliance test. If in a certain case USB TX and DP compliance require different EQ settings, use the USB3, DP select event as the trigger event to initiate a separate configuration to the EQs.

The *PD Alternate Mode: DisplayPort* application note provides a detailed introduction of DP alternate mode.

6.4 Notes for Application

If the power on event is selected to be the trigger event to initiate the EQ, VOD, and DCGain configuration to TUSB1044, it is important to pay attention to the power sequence of the TUSB1044 and I²C pull-high power rail. A later power on or not stable of pull-high power rail may lead to concern of not successfully setting the TUSB1044. Under these conditions, it helps to use the attach event to trigger the config to 0x10, 0x11, 0x20, 0x21, and 0x0C to secure the successful configuration to the redriver.

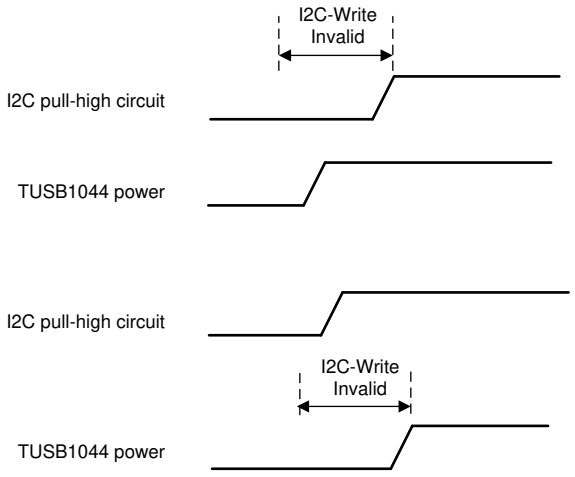

Figure 6-5. Example of Invalid I²C Write Region

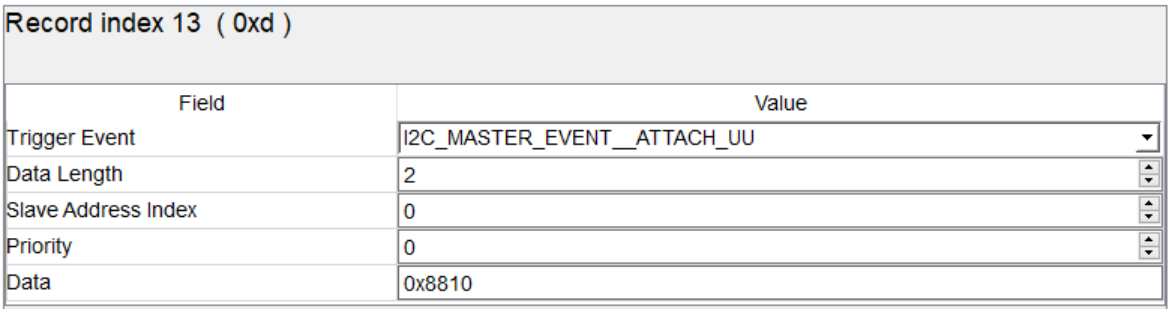

Figure 6-6. Example of TUSB1044 Re-config Upon Attach Event

Figure 6-7 shows where the data sheet required items to achieve lower power consumption in shut down mode.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power						
P_{USB-NC}	Average power when configured for USB3.1 only and nothing connected to TXP/N pins.	No USB device connected; CTL1 = L; CTL0 = H		2.5		mW
$P_{USB-U2U3}$	Average power when configured for USB3.1 only and link in U2 or U3 state.	Link in U2 or U3 state; CTL1 = L; CTL0 = H		2		mW
$P_{SHUTDOWN}$	Average power when device in Shutdown	CTL1 = L; CTL0 = L; I2C_EN = 0;		0.65		mW

Figure 6-7. Power Consumption Information

There is a special notice on the conditions to achieve lower power consumption for a certain shutdown or sleep mode of the system, that CTL1, CTL0, and I2C_EN = 0. It indicates that a special pull-high power rail design for the three IOs to achieve shutdown mode power of TUSB1044 must be considered in the design, especially when I^2C control is enabled (pull high I2C_EN).

7 References

- Texas Instruments, *TUSB1044 USB Type-C® 10 Gbps Multi-Protocol Bidirectional Linear Redriver Data Sheet*
- Texas Instruments, *TUSB1044 Configuration Guidelines Application Report*
- Texas Instruments, *Using I2C Master in TPS65987D and TPS65988 PD Controllers*
- Texas Instruments, *PD Alternate Mode: DisplayPort Application Report*

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