

5 4 3 2 1

VAR-DT8MCustomBoard



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03A.	DART-MX8M
03B.	DART-MX8M-MINI
03C.	DART-MX8M-PLUS
04.	POWER, RTC, BOARDID
05.	ETH, USD, AUDIO,MIPI-CSI
06.	HDMI, eDP
07.	PCIe, MIPI-DSI,UART DBG
08.	USB C OTG, USB HOST
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12.	CAN FD INTERFACE
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Disclaimer:

Schematics are for reference only.
Variscite LTD provides no warranty for the use of these schematics.
Schematics are subject to change without notice.

Revision History

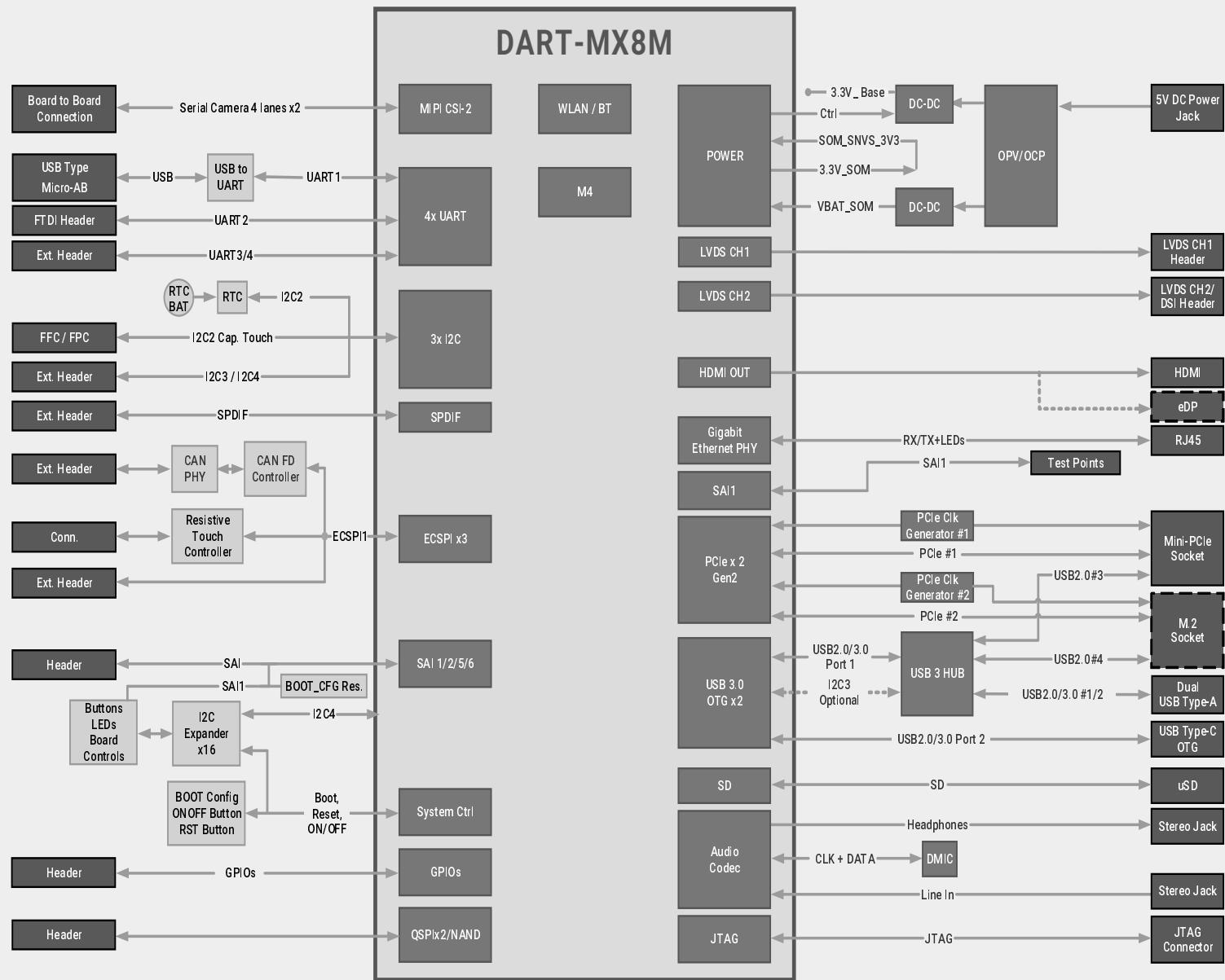
Document	Carrier	Description
1.0	2.0	<p>Changes from DOC 1.9 Carrier 1.4D include:</p> <ul style="list-style-type: none">* Optimisation for DART-MX8MP:- Added external ethernet PHY- Control IOs used on previous version over SAI1 now controlled via I2C expander- Added DS1 header option for DART-MX8MP stock item exposed pins; Pinout compatible to Symphony J7+J8- Native USB ID usage added important note- USB Type C active discharge replaced with bleeder- USB Type C crossbar differential switch simplified.- Removed DT8M NAND option- Added QSPI header J41 - located in location of J25- J27 & J28 pinout aligned to Symphony- Added PD on J1.38 for BSP CustomV2.0 signal.- Added additional CAN PHY on iMX8MP- U44 footprint modified from SOIC to DFN- SD card power switch modified- Main power switch type align to Symphony- DART-MX8M DP connector replaced with 40pin eDP REF. design- HDMI path simplified- PINMUX page deleted - reference to XLS- Added reference design for 12Mb/s CAN-FD transciever- Added M.2. PCIe reference design- Add option on bottom to route PCIe port 1 to M.2 connector- Replace boot config drivers to 3state type- Replace MCP2518 crystal to 40MHz and connect RX_INT- Updated Block Diagrams- VCC_SOM Increased to 3.8V (R145 changed to 18K)- D9, C58 Removed. VCC_BASE_3V3 goes up just after NVCC_3V3
1.1	2.1	<ul style="list-style-type: none">* GPLED4 controlled via FET Q14 to support DART-MX8M-PLUS 1.8V voltage level* Updated GPIO expanders U56,U57 footprint* Added note for U53 recommended P/N



02A. Block Diagram - DART-MX8M

VAR-DT8MCustomBoard V2.x

Doc rev 1.0



I2C BUS ADDRESS:

I2C1: Internal to SOM
 I2C2: PU - 10K on US
 10K on custom
 0x54 BOARD ID EEPROM Page0
 0x55 BOARD ID EEPROM Page1
 0x68 RTC
 0x38 CAPACITIVE TOUCH CTRL
 0x3D USB-C CC Logic PINS150AHXWP
 0x3C CSI P1 Camera (1V8) OV5640

I2C3: PU - 5K on SOM
 0x60 SOM - Int. power ctrl.
 0x2D USB3 HUB
 0XXX Header J12

I2C4: PU - 10K on US
 10K on custom
 0x3C CSI P2 Camera (1V8) OV5640
 0XXX Header J12
 0XXX mPCIe J23 & J32

Important Notes:

- Length match for HS signals according to SOM DS
- USB routed as 90 ohm Diff pairs
- PCIe/SATA routed as 85 ohm Diff pairs
- LVDS routed as 100 ohm Diff pairs
- Other fast changing signals routed as 50 ohm



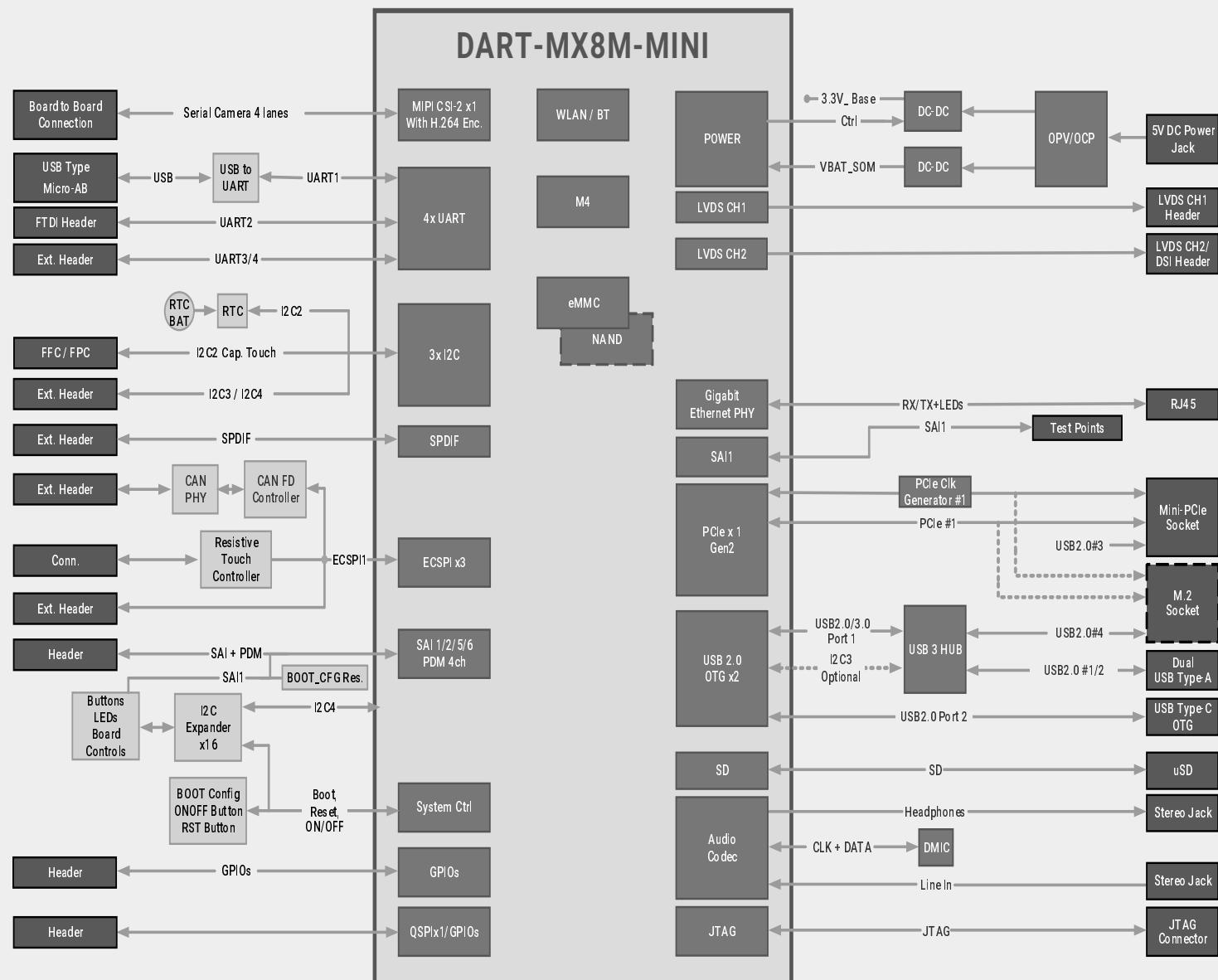
02A. Block Diagram with DART-MX8M

Size	Document Number	Project	Rev
A3	VAR-DT8MCustomBoard	VAR-DT8MCustomBoard	2.1_R1.1
Designer:	Leonid S.	Approved By:	
Date:	Tuesday, May 04, 2021	Sheet	2 of 17

02B. Block Diagram - DART-MX8M-MINI

VAR-DT8MCustomBoard V2.x

Doc rev 1.0



I2C BUS ADDRESS:

I2C1: PU - 10K on US
I2C2: PU - 10K on US
0x54 BOARD ID EEPROM Page0
0x55 BOARD ID EEPROM Page1
0x68 RTC
0x38 CAPACITIVE TOUCH CTRL
0x3D USB-C CC Logic PINS150AHXMP
0x3C CSI P1 Camera (1V8) OV5640

I2C3: PU - 5K on SOM
0x1A SOM - Int. CODEC
0x2D USB3 HUB
0XXX Header J12

I2C4: PU - 10K on US
10K on custom
0x3C CSI P1 Camera (1V8) OV5640
0XXX Header J12
0XXX mPCIe J23 & J32

Important Notes:

- Length match for HS signals according to SOM DS
- USB routed as 90 ohm Diff pairs
- PCIe/SATA routed as 85 ohm Diff pairs
- LVDS routed as 100 ohm Diff pairs
- Other fast changing signals routed as 50 ohm

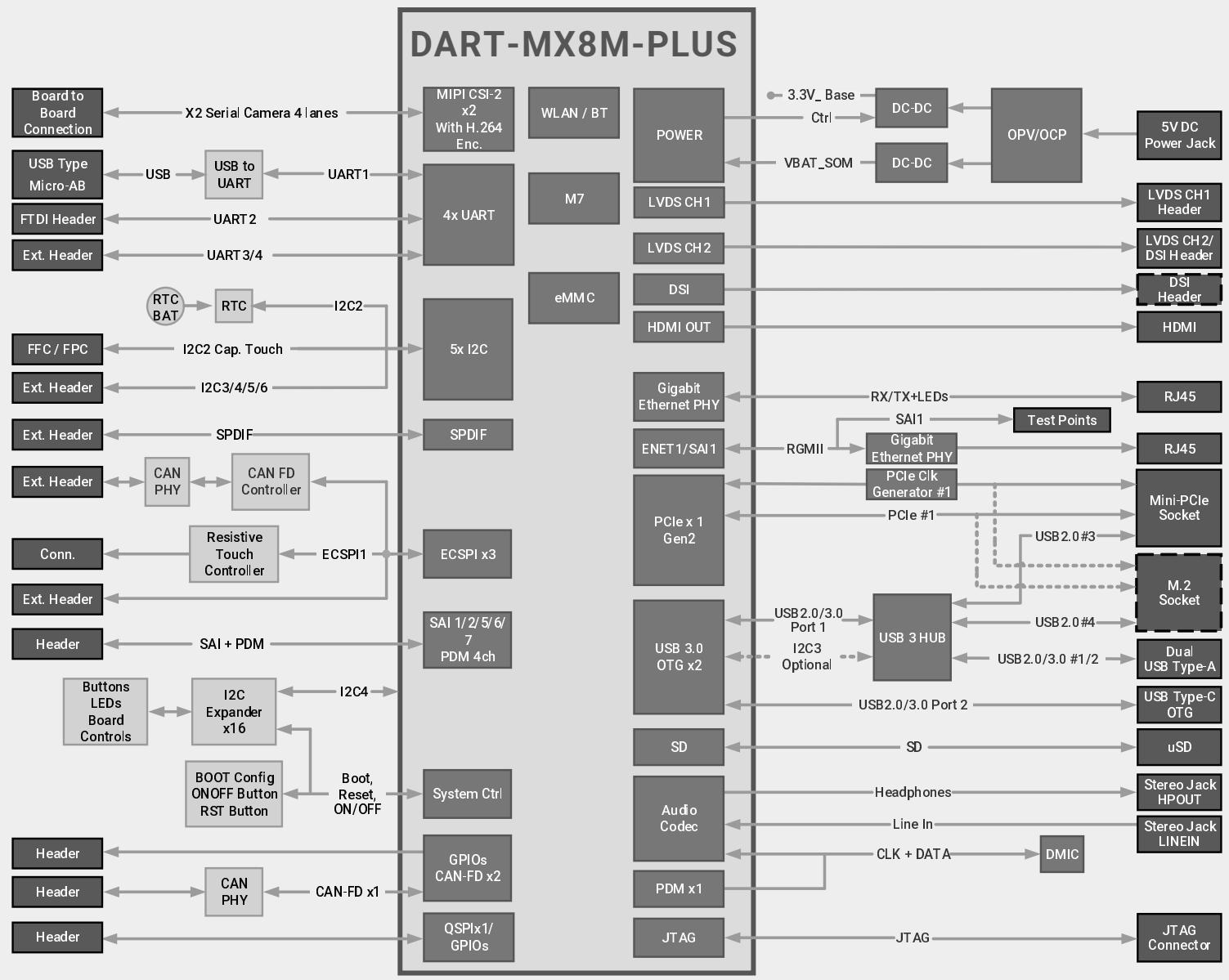


02B. Block Diagram with DART-MX8M-MINI

Size	Document Number	Project	Rev
A3	VAR-DT8MCustomBoard	VAR-DT8MCustomBoard	2.1_R1.1
Designer:	Leonid S.	Approved By:	
Date:	Tuesday, May 04, 2021	Sheet	3 of 17

VAR-DT8MCustomBoard V2.x

Doc rev 1.1



I2C BUS ADDRESS:

I2C1: Internal to SOM

```
i2c2:  PU - 10k on U8  
      10k on custom  
0x54 BOARD ID EEPROM Page0  
0x55 BOARD ID EEPROM Page1  
0x68 RTC  
0x38 CAPACITIVE TOUCH CTRLR  
0x3D USB-C CC Logi PTN5150AHXMP  
0x3C S3 Camera (1V8) OV5640
```

I2C3: PU - 5K on SOM

```
I2C4:    PU - 10K on U8
          10K on custom
          0x3C CSI P1 Camera (1V8) OV5640
          0xXX Header J12
          0xXX mPCIe J23 & J32
```

Important Notes:

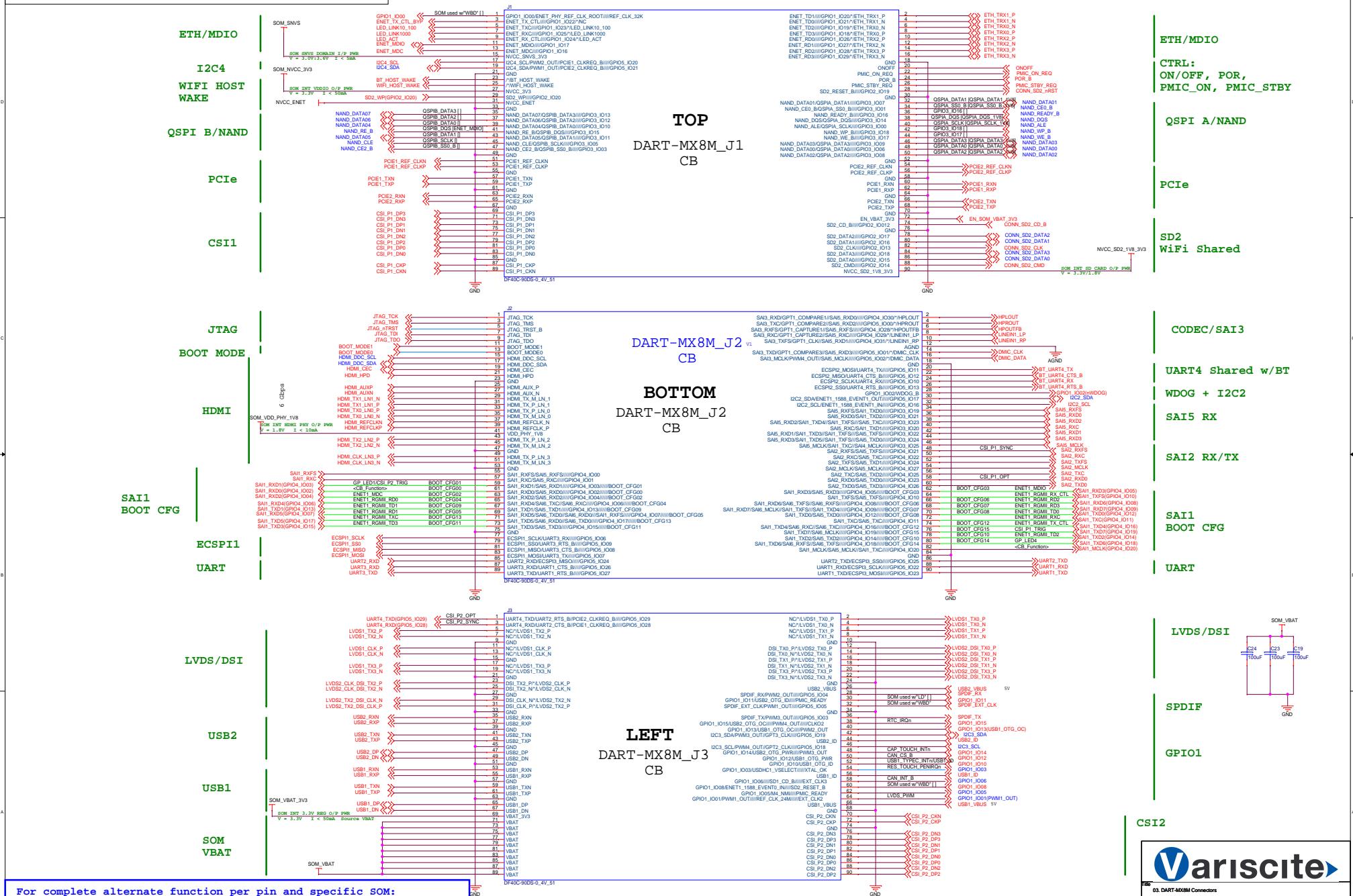
1. Length match for HS signals according to SOM DS
 2. SB routed as 90 ohm Diff pairs
 3. PCIe/SATA routed as 85 ohm Diff pairs
 4. LVDS routed as 100 ohm Diff pairs
 5. Other fast changing signals routed as 50 ohm



Title

02B. Block Diagram with DART-MX8M-MINI				
Size	Document Number	Project	Rev	
A3	VAR-DT8MCustomBoard	VAR-DT8MCustomBoard	2.1_R1	
Designer:	Leonid S.	Approved By:		
Date:	Tuesday, May 04, 2021	Sheet	4	of 17

03A - DART-MX8M Connectors



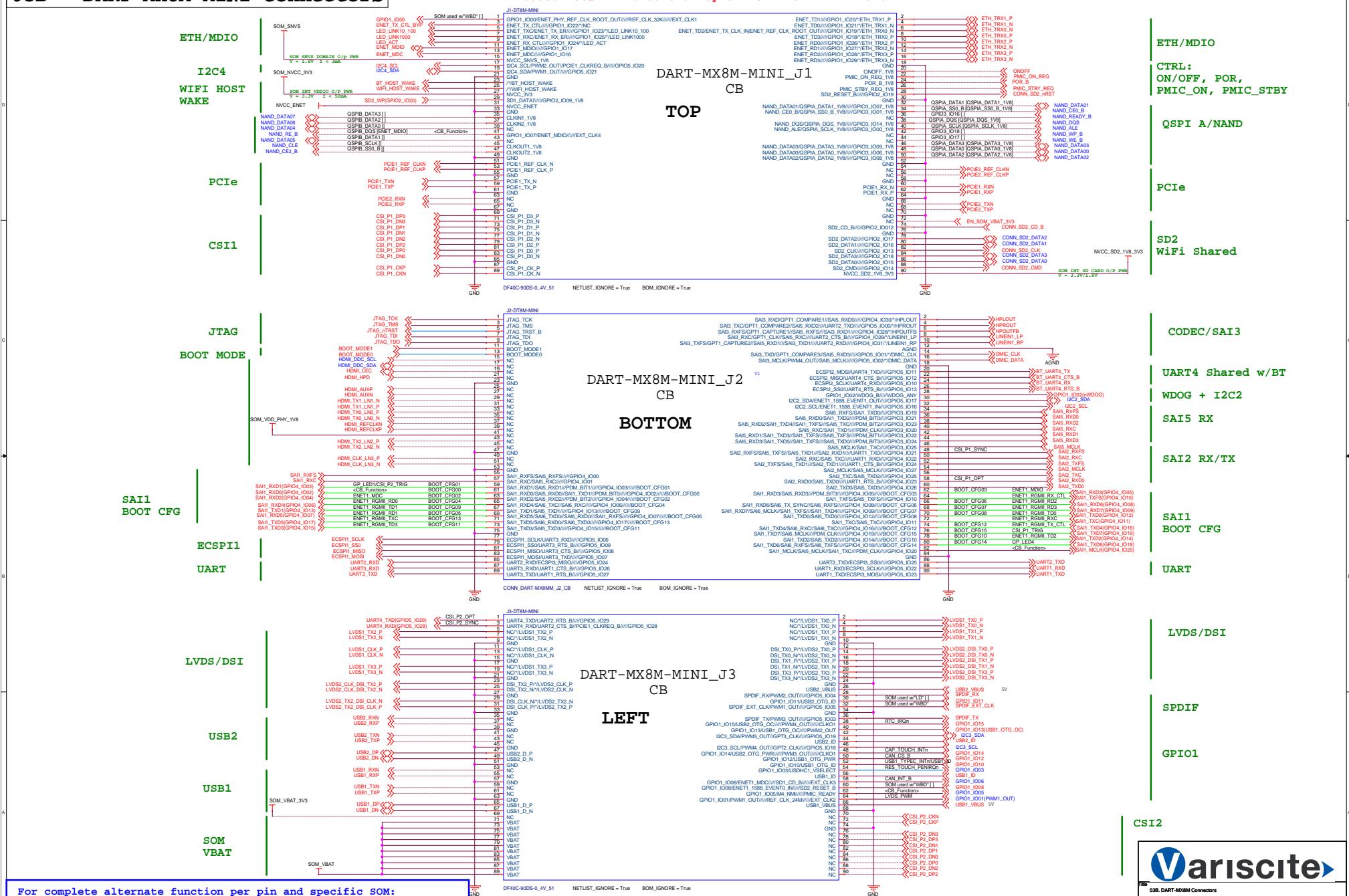
For complete alternate function per pin and specific SOM:
please refer to "DART_Compatibility_and_Pinout.XLS " located at
ftp://ftp.variscite.com/DART_Compatibility

Note: Pinname with /*/ prefix denotes a HW assy option.

03. DART-MX8M Connectors			
Size	Document Number	Project	Rev
A2	VAR-DT8MCustomBoard	VAR-DT8MCustomBoard	2.1_R1.1
Designer:	Leopold S.	Approved By:	
Date:	Tuesday, May 04, 2021	Sheet	5 of 17

03B - DART-MX8M-MINI Connectors

*** Dotted nets - Functionality differ from DART-MX8M. ***



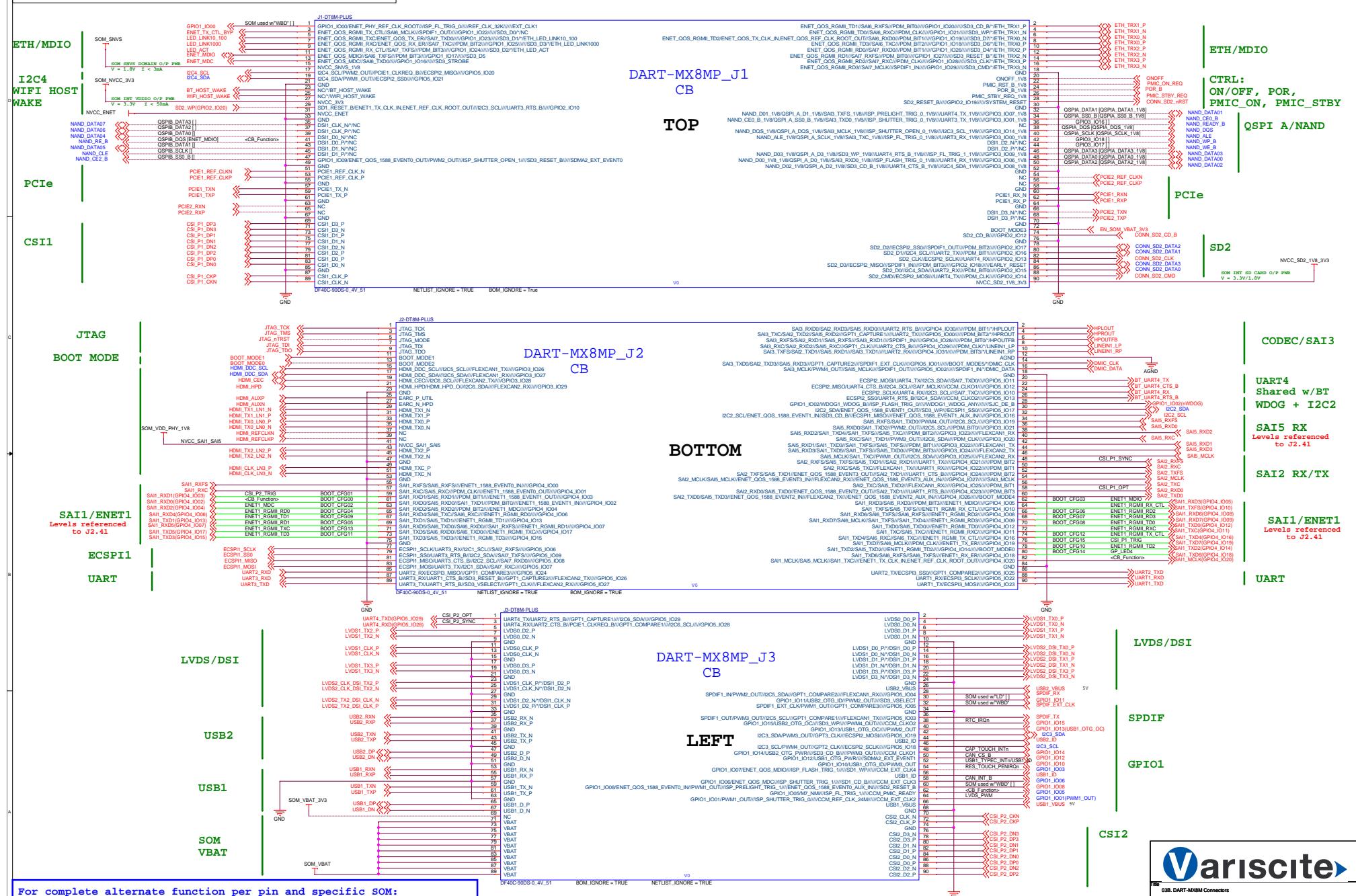
For complete alternate function per pin and specific SOM:
please refer to "DART_Compatibility_and_Pinout.XLS" located at
ftp://ftp.variscite.com/DART_Compatibility

Note: Pinname with /*/ prefix denotes a HW assy option.

Variscite			
Variscite	03B. DART-MX8M Connectors		
Size	Document Number	Project	Key
A2	VAR-DT8M/CustomBoard	VAR-DT8M/CustomBoard	J-141
Designer:	Leontij S.	Approved By:	
	10/20/2010		

03C - DART-MX8M-PLUS Connectors

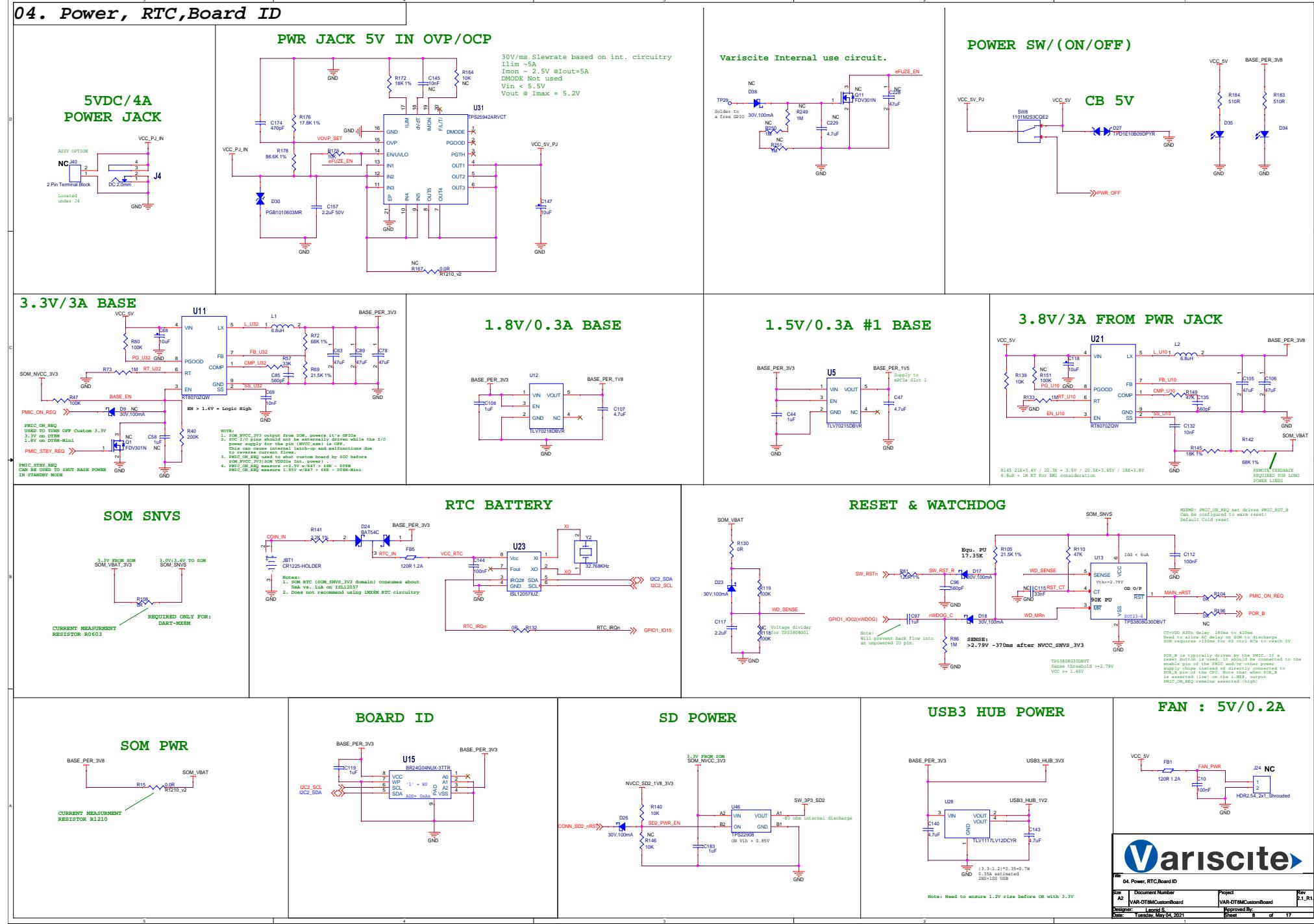
*** Dotted nets - Functionality differ from DART-MX8M. ***



For complete alternate function per pin and specific SOM:
please refer to "DART Compatibility and Pinout.XLS" located at
<ftp://ftp.varisite.com/DART%20Compatibility>

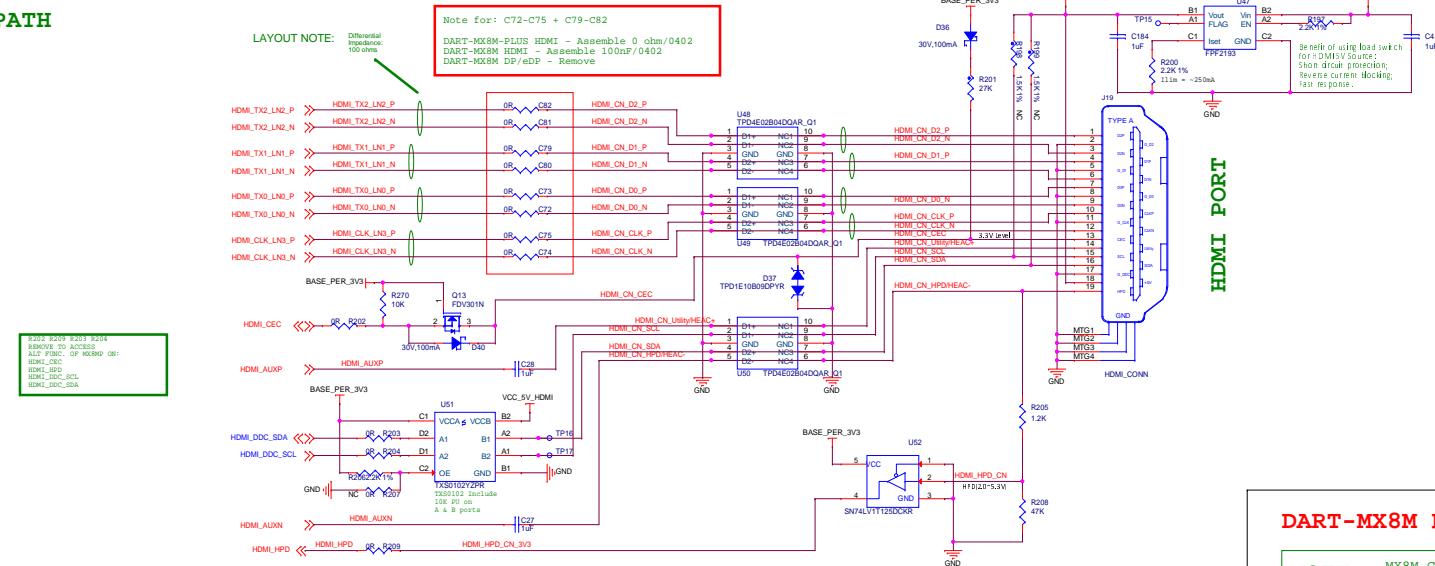
Note: Pinname with /*/ prefix denotes a HW assy option.

04. Power, RTC, Board ID



06. HDMI, eDP - DART-MX8M-PLUS Optimised

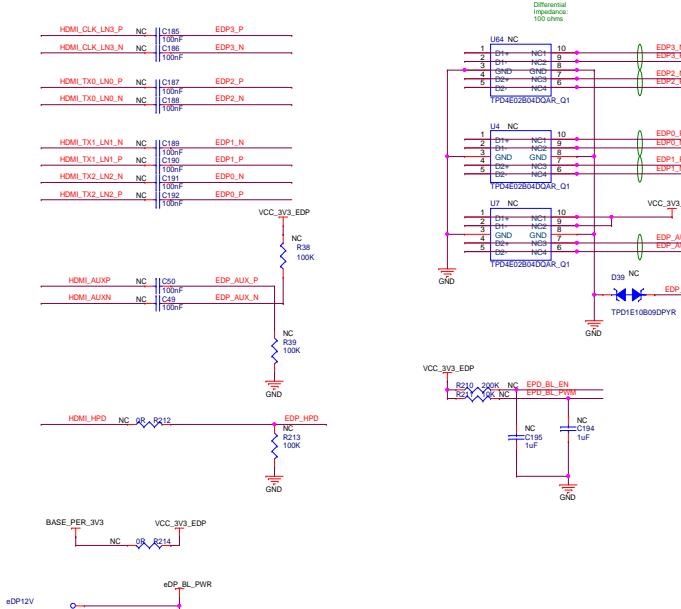
HDMI PATH



DART-MX8M eDP/DP PATH - [Reference Design]

iMX8M REQUIRES CROSS BETWEEN LANE0 & LANE2 !

LAYOUT NOTE: Differential Impedance: 100 ohms

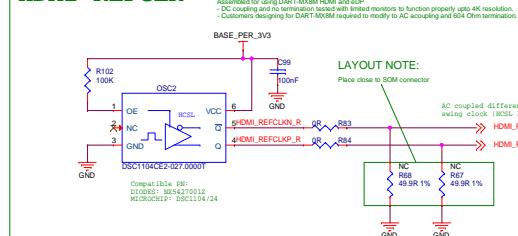


Board Connector: IPEX 20455-040E-76 (44 Pin)
Cable: IPEX 20453-0407-11 Assembly
Display Type: B156ZAN03.1 (H/W:0A)

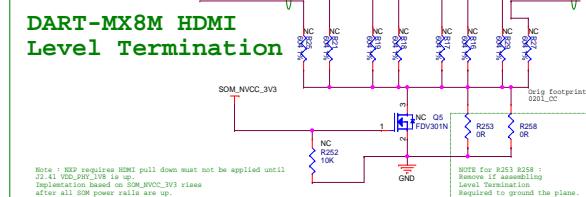
DART-MX8M Notes and required circuitry:

NOTE: MX8M CAN CONNECT DIRECTLY TO :
HDMI_CN_SCL & HDMI_CN_SDA
HDMI_CN_CEC
HDMI_CN_HPD

HDMI REFCLK



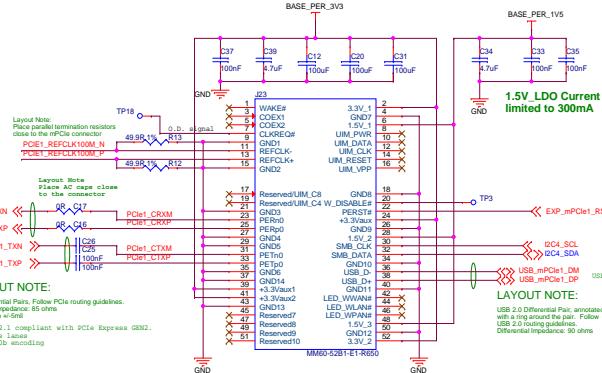
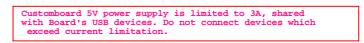
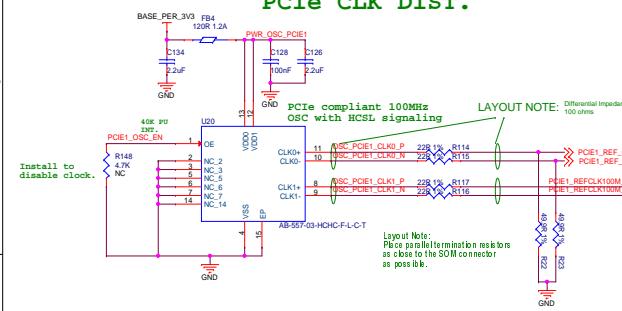
DART-MX8M HDMI Level Termination



07. PCIe, QSPI, MIPI-DSI, USB DEBUG

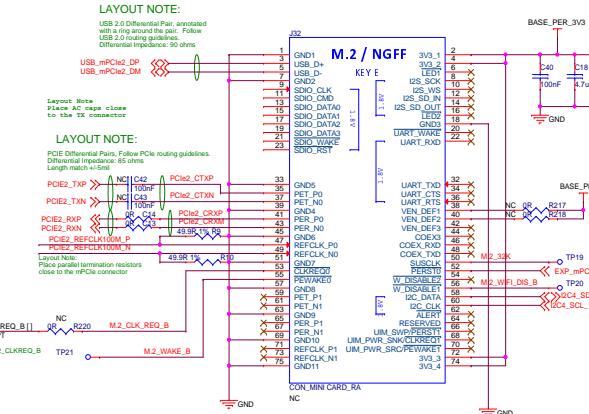
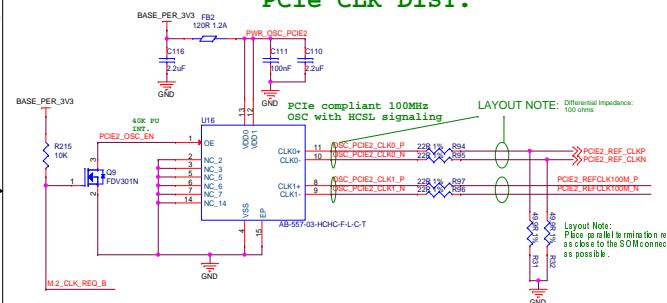
mPCIexp CS

PCIe CLK DIST.



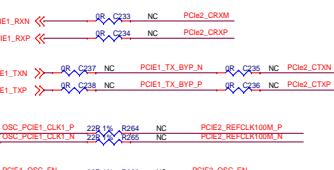
M.2. ON PS - [Reference Design]

PCIe CLK DIST.



DART-MX8MP MIPI-DSI ON PS
Compatible to Symphony J7+J8

PCIe1 TO M.2 PATH



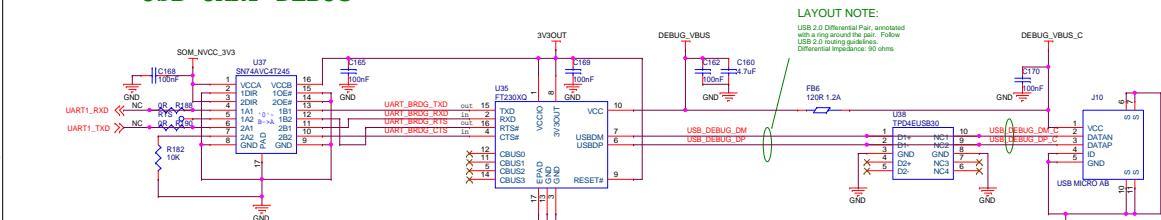
ASSY NOTE:
Customers requiring PCIe on DT8MP and DT8MM routed to M.2.

c16 c17 c26 c25 R116 R1

Assembly
C237 C238 (100nF)
C235 C236 (0 Ohm)
C233 C234 (0 Ohm)

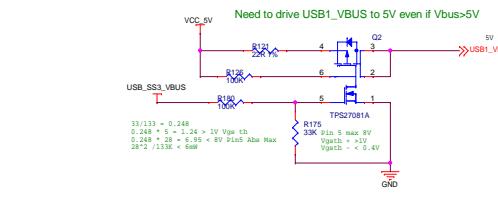
R264 R265 (22 OHM)

USB UART DEBUG

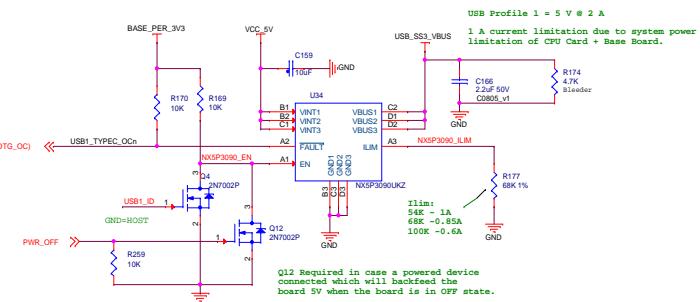


08. USB TYPE C, USB 3 HUB

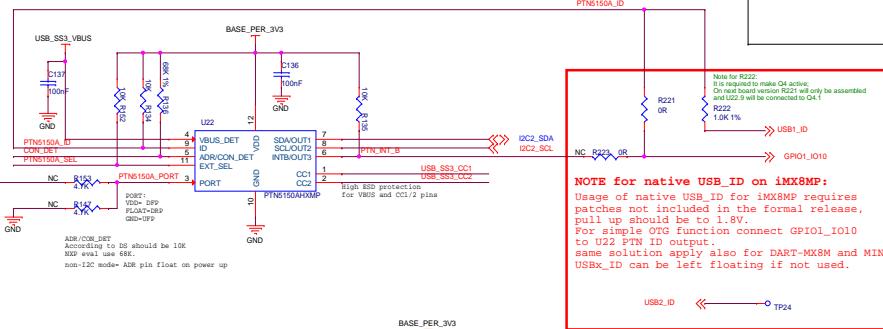
USB#1 - DRP
USB TYPE C



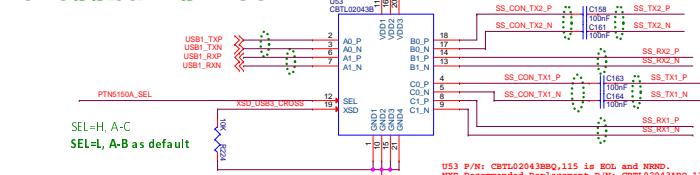
5V Source Load Switch



Config Channel Logic Detection & Indication of Plug Orientation



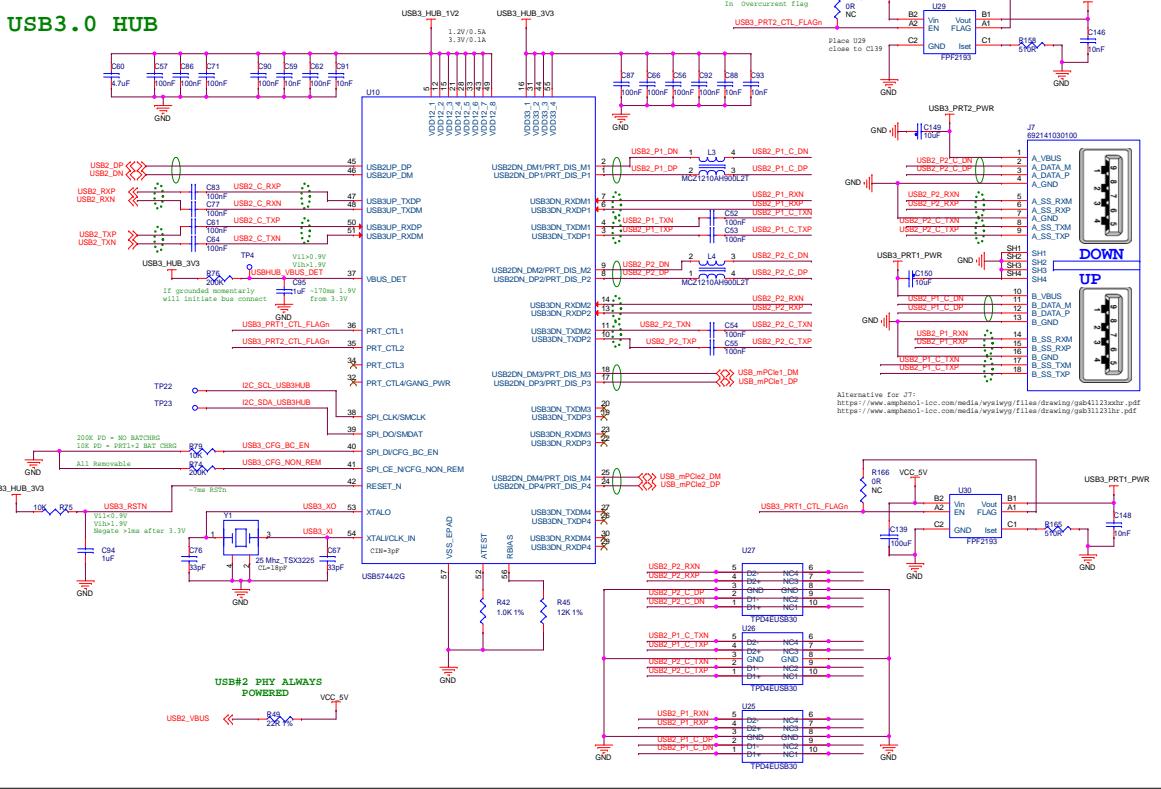
USB3.0 Type-C
crossbar switch



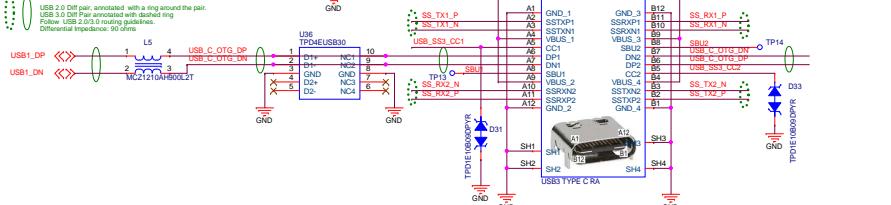
USB#2 - HOST

USB3.0 HUB

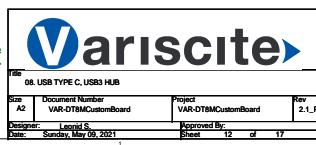
Note:
1.2V should rise before or at the same time as
Straps should be valid >1ms after RST_N negated



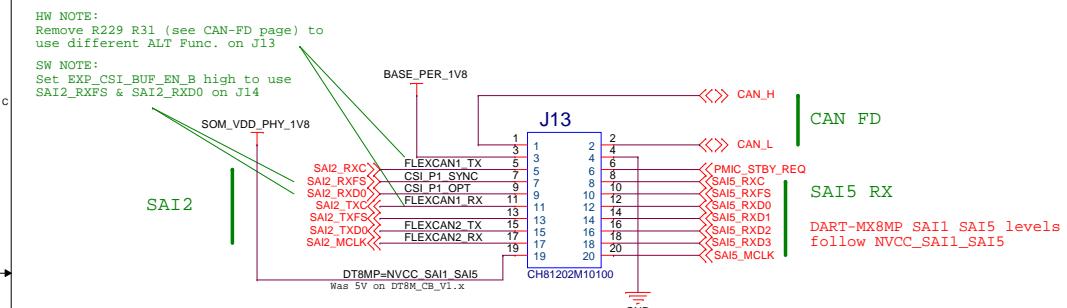
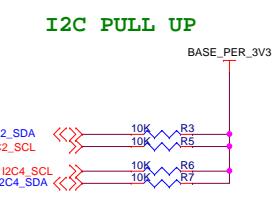
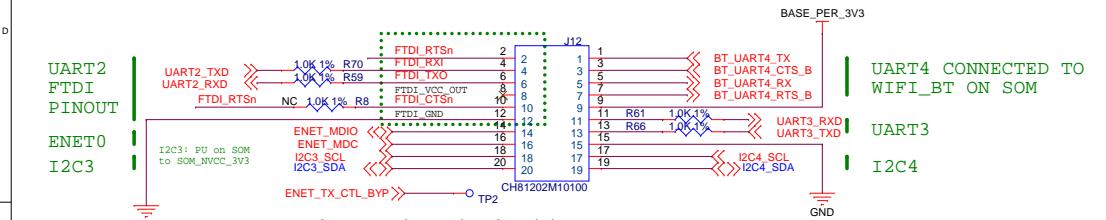
.. LAYOUT NOTE:



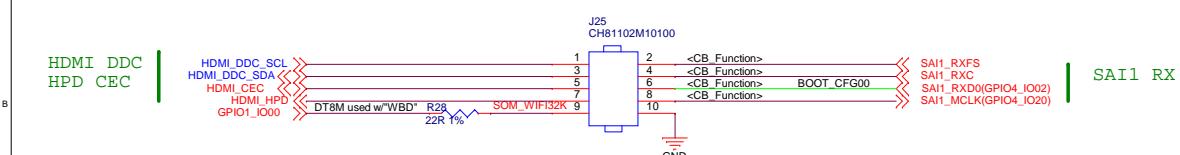
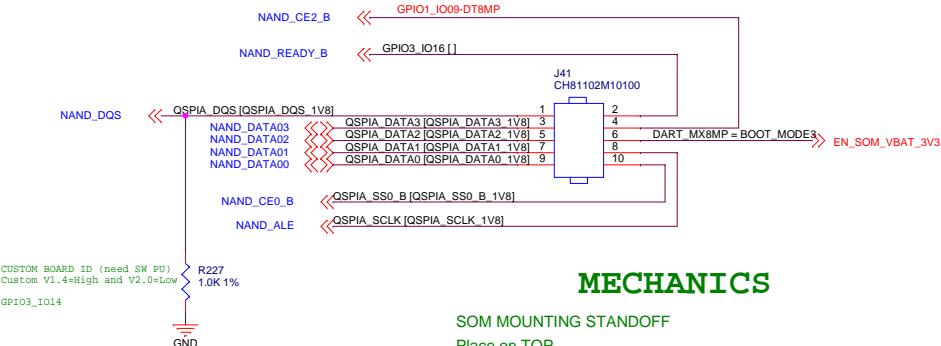
Note:
VBUS active discharge
replaced with bleeder



10. HEADERS, Mechanics, Pull Ups



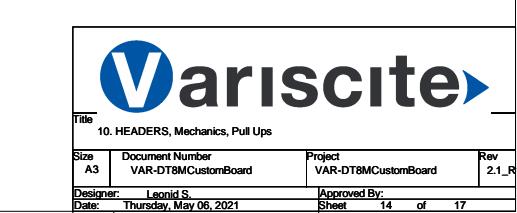
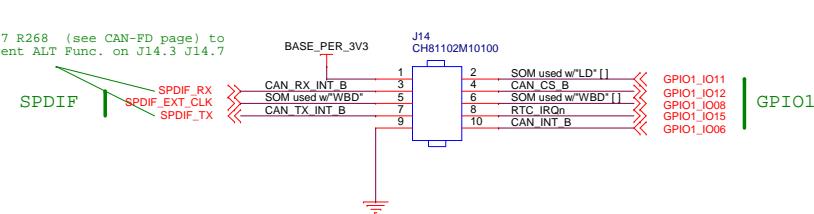
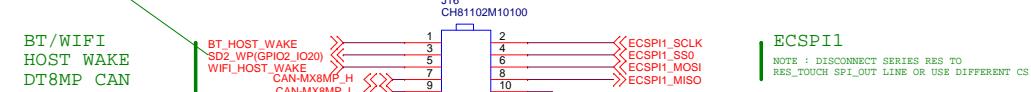
QSPI HEADER



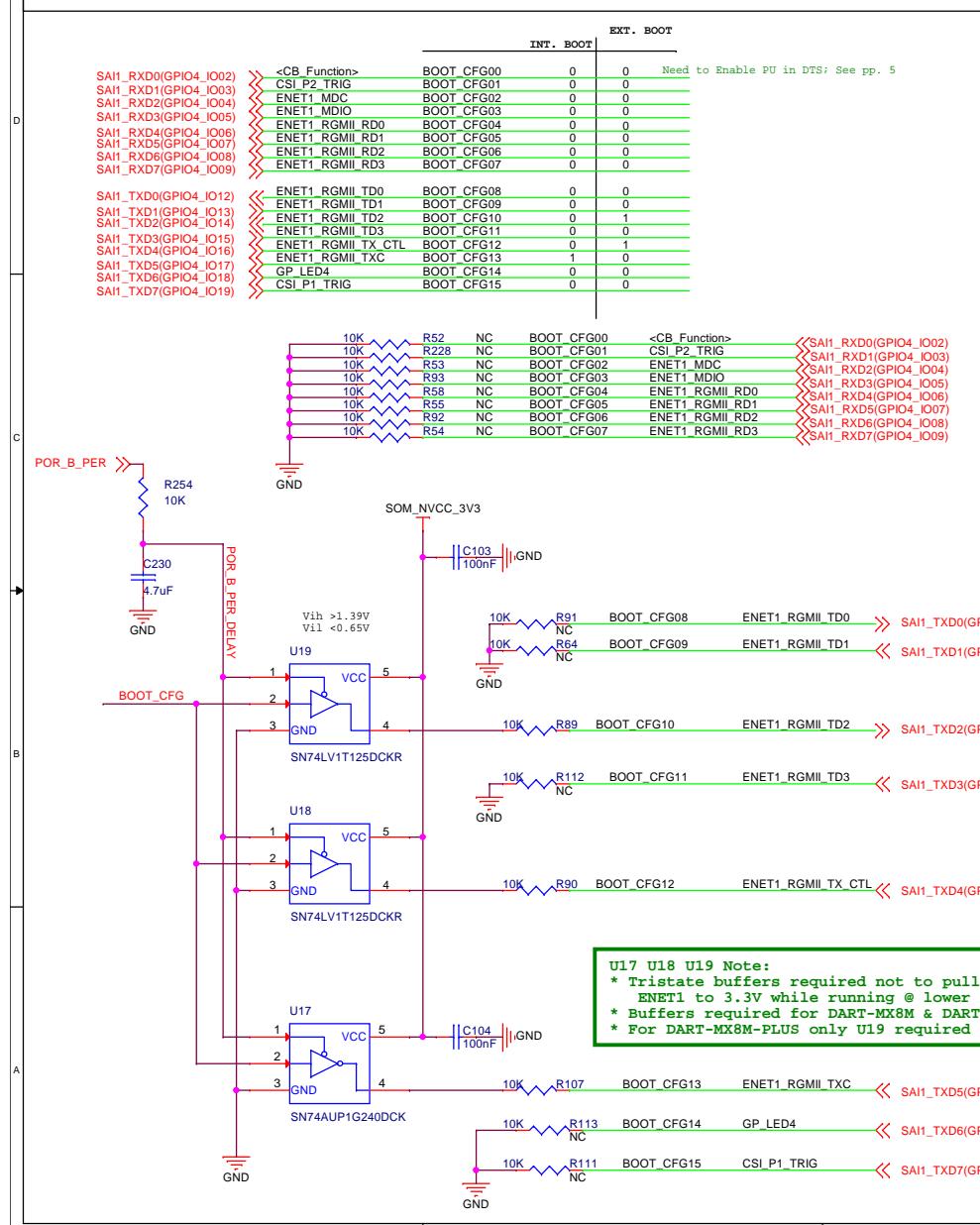
MECHANICS

SOM MOUNTING STANOFF

Place on TOP



11. BOOT CONFIG & MODE



Notes:

- a. Sampled on rising edge of POR_B
- b. SOC PD during POR_B and after on BOOT_CFG[15:0] and BOOTMODE[1:0]
- c. BOOT_MODE[1:0] = "10" is Internal Boot - Always used.
- d. Active boot cfg for one dip sw sel EXTERNAL/INTERNAL

DART-MX8M-MINI Notes:

- b. Boot config lines do not follow the Mini datasheet in full
- DART-MX8M-MINI have added logic to be compatible to DART-MX8M

DART-MX8M-PLUS Notes:

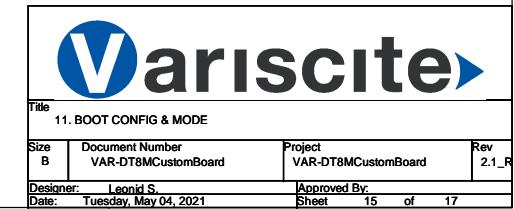
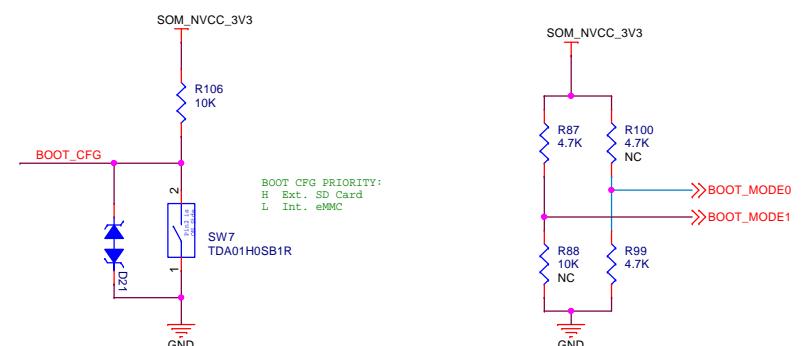
- a. Boot configuration set only by SAI1_TXD2 connected on DART via buffer to BOOT_MODE0

i.MX8M Plus Boot Mode

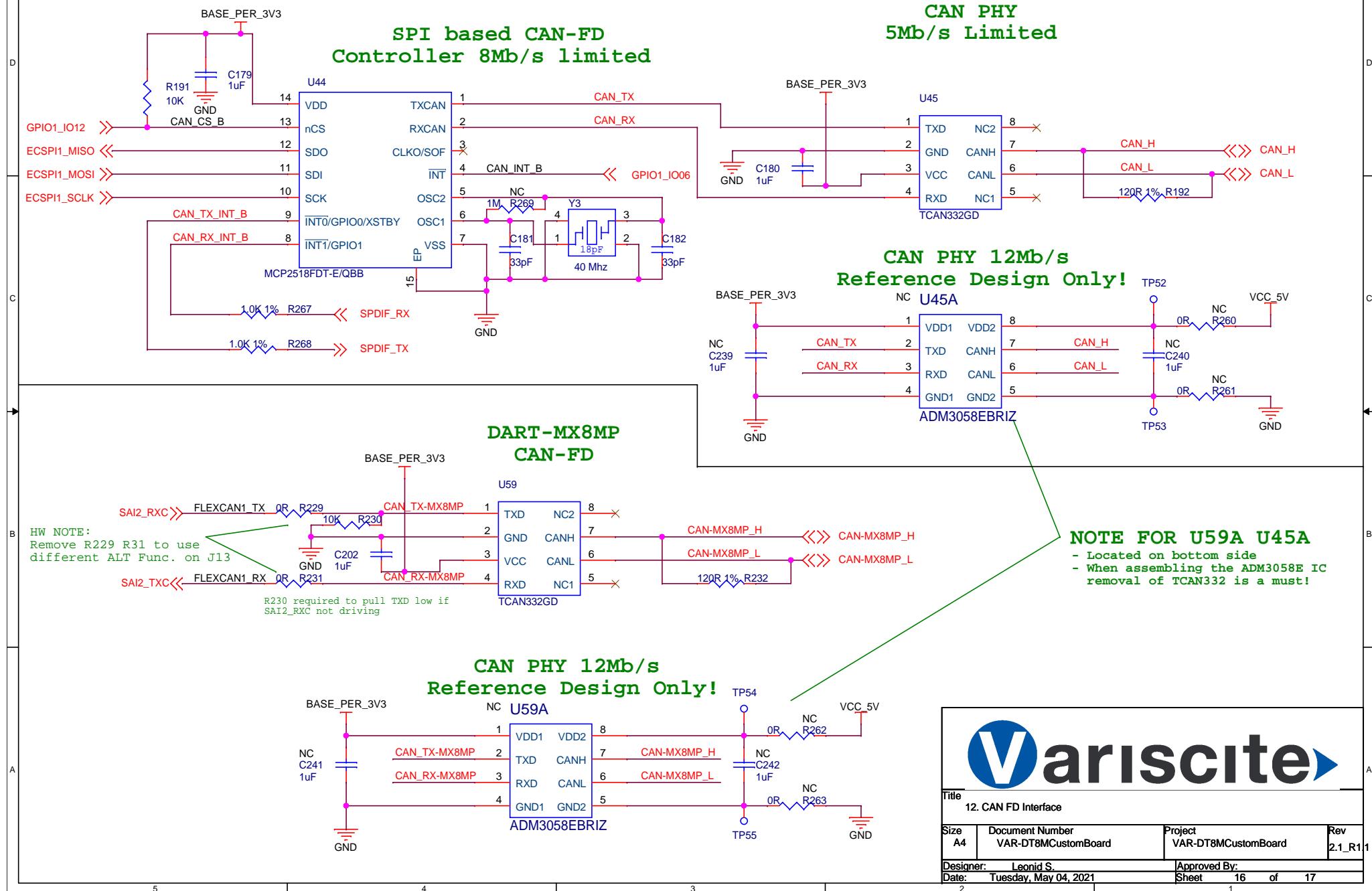
BOOT_MODE3	BOOT_MODE2	BOOT_MODE1	BOOT_MODE0	Boot Modes
0	0	0	0	Boot From Internal Fuses
0	0	0	1	USB Serial Download
0	0	1	0	USDHC3 (eMMC boot only, SD3 8-bit) Default
0	0	1	1	USDHC2 (SD boot only, SD2)

CustomBoard Net: BOOT_MODE0 SAI1_TXD2
EN_SOM_VBATT_3V3 BOOT_MODE1

DART-MX8MP BOOT MODE



13. CAN FD Interface



13. DART-MX8MP- ENET1 Gigabit Ethernet

