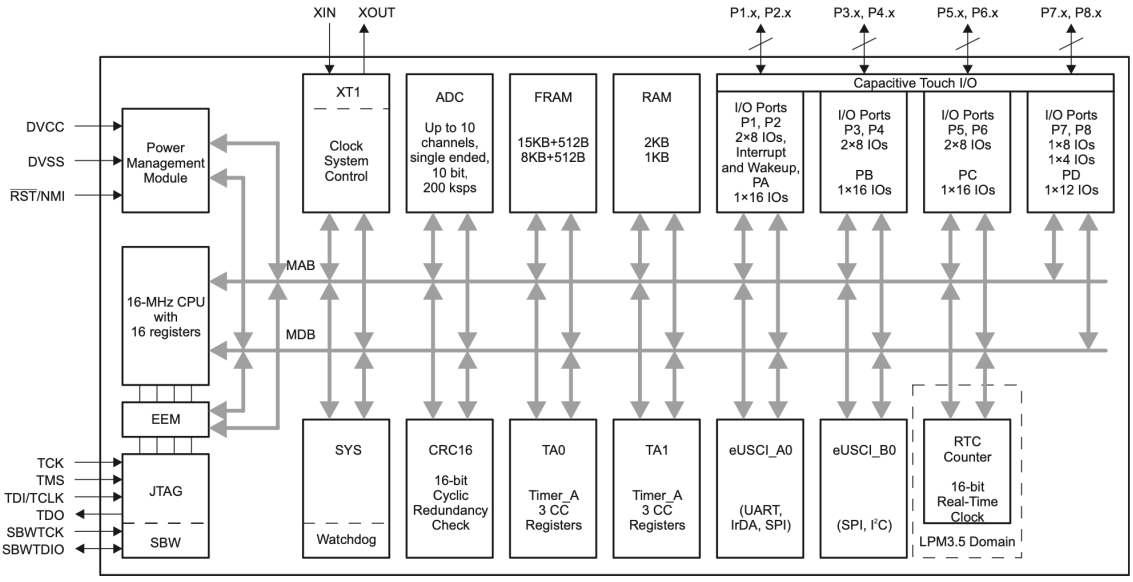
919 Expansion slots (m.2)

On the way to the 701 board two m.2 connectors must be added to 919. A Key B and a Key E connector.

Core Components

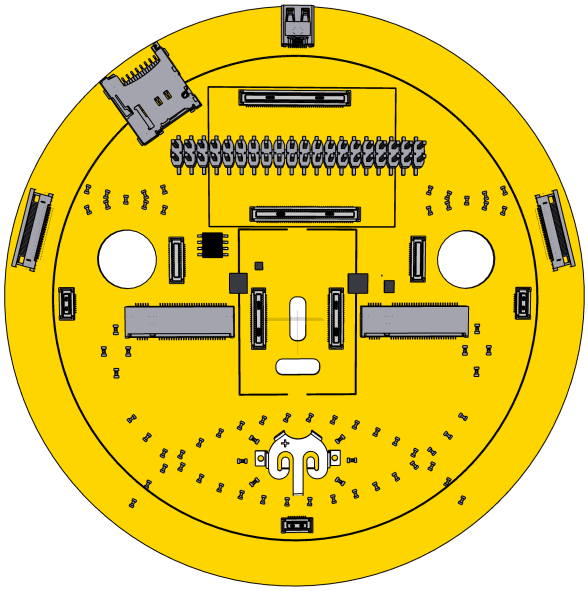
- M.2 key B connector H4.20mm Amphenol ICC 10128793001RLF
- M.2 key E connector H4.20mm Amphenol ICC 10128794001RLF
- 1 * PCA9555 I/O Expander (for legacy)
- 1 * MSP430 FR2032 IG56 TSSOP DGG56. Inventory 4870 at TO. @1000 $0.766. 52 IO pins, 1 UART/I2C, 1 UART/SPI.
- 2 * 74HC595 PW,118 shift register TSSOP-16. @1000 $0.15, 15k in
- 1 * CBTL04083 Multiplexer Switch ICs 3.3V CH 2:1 - Mouser
- 1 * TS5USBC410 Dual 2:1 USB 2.0 Mux/DeMux Switch. Mouser



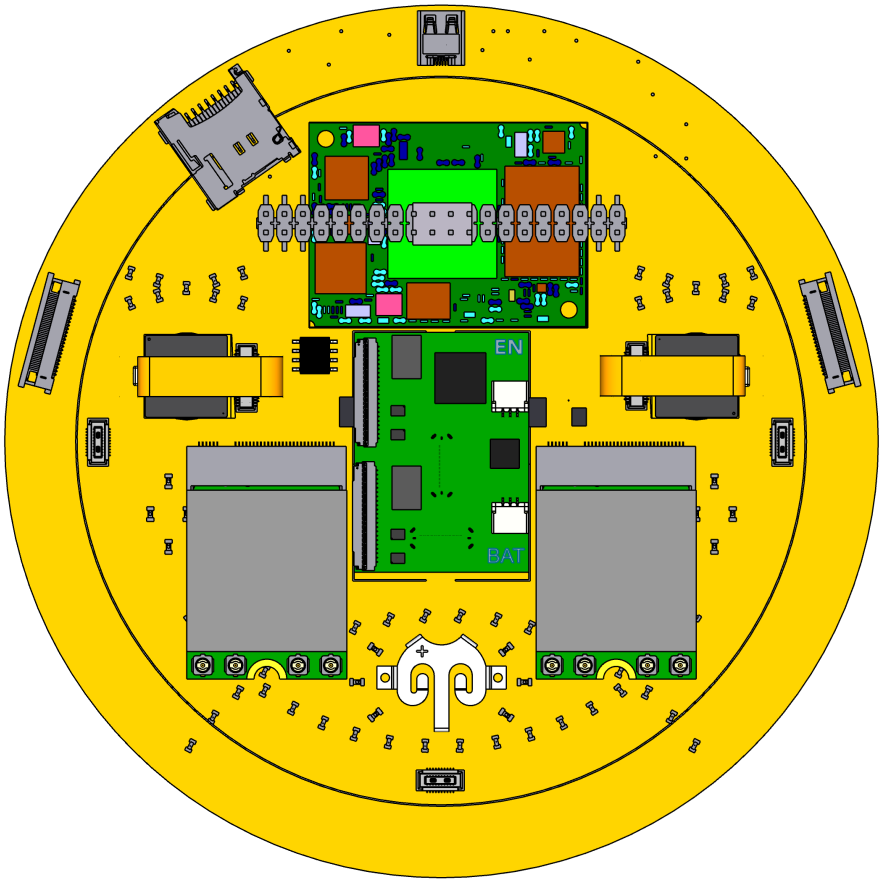
Alternative components

- 1 * USB2513B USB 2.0 hub controller
-
-

Adding m.2



This is how it looks with the modules mounted:



USB Data and m.2 Module Wiring

T-USB Data and M.2 Key E Expansion

Data is routed primarily over the two USB-C connectors via the Power Module, but it is also available over the two M.2 Expansion connectors.

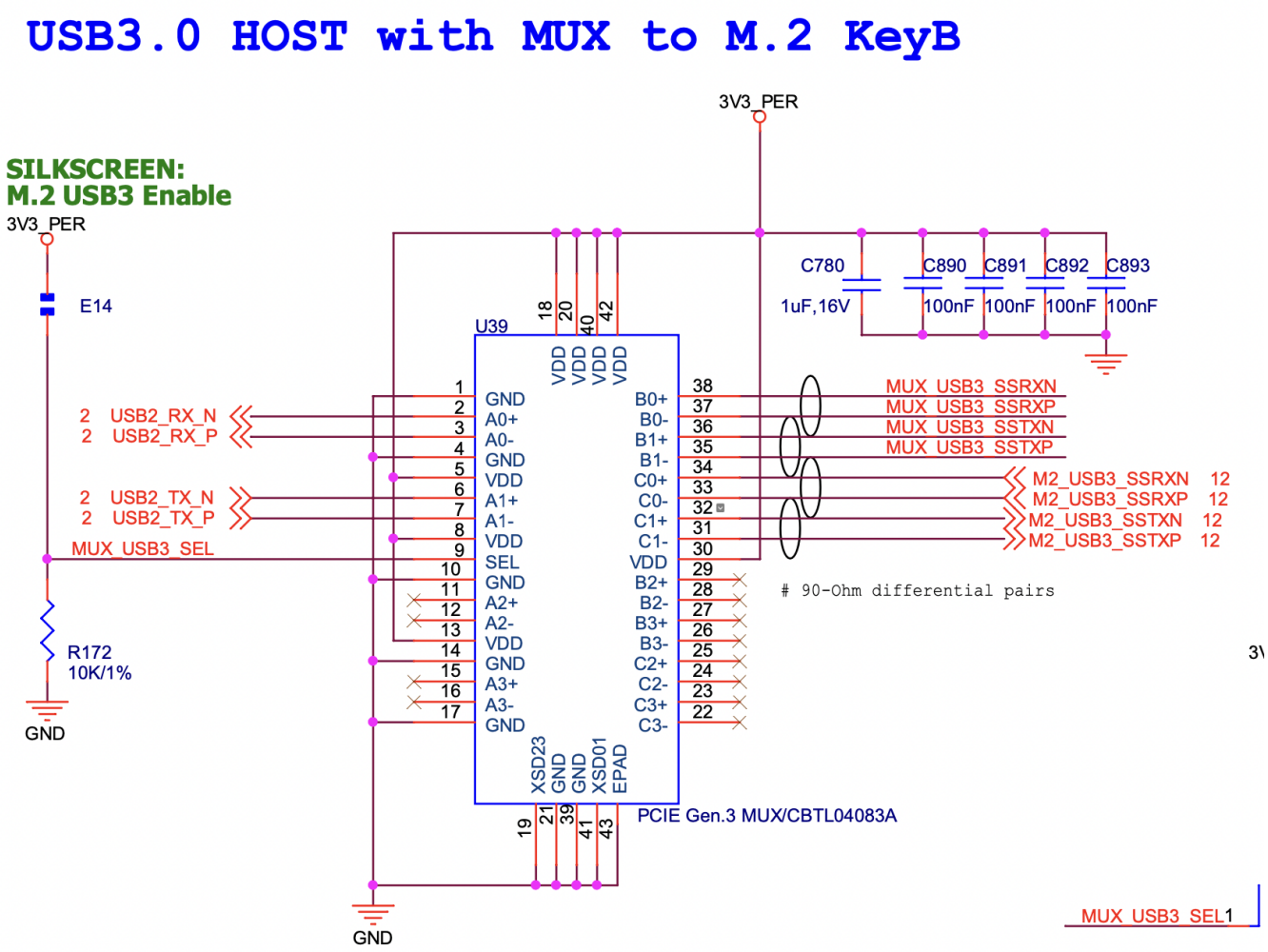
T-USB connector 3.0 data mapping

Two USB-C connectors are arranged in a T shape and the normal way to use it is with a combined connector attached. This means that the wires will normally be connected in a particular orientation. The system takes advantage of this by detecting when both USBs are connected in the normal arrangement.

The USB-C signal lines from the T-USB connector is managed by the Multiplexing chipsets around the PD Controller. The USB-C signal lines for the OTG connector in T-USB come from USB1(OTG cabable 2.0 & 3.0). The SBU1/SBU2 are connected to AUX-/AUX+ pins on the T-USB OTG alt connector. The USB 3.0 superspeed data pairs and SBU1/SBU2 are passed from USB-C connectors to HD3SS460.

The Host USB-C connector is similarily connected. The HD3SS460 chips are controlled over I2C by the MCU using SYS I2C.

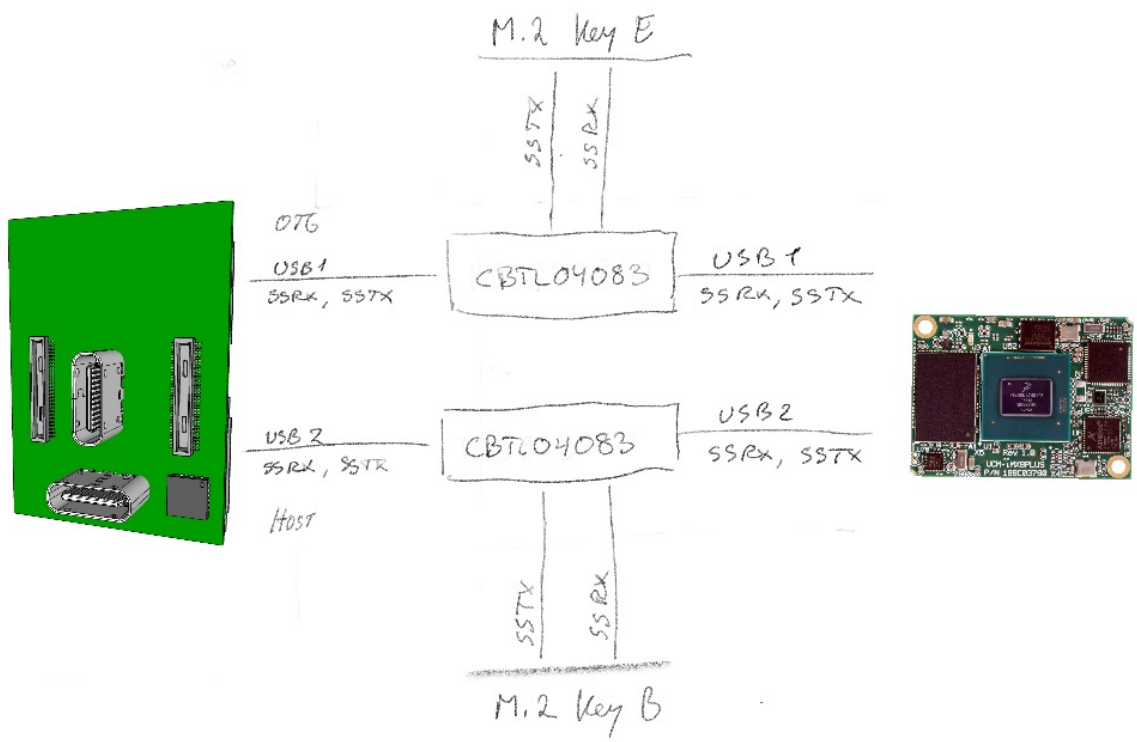
One side of the RX/TX pins are carried to the T-USB alt connector, and not connected to USB1 signals. (Should the side be muxed?)



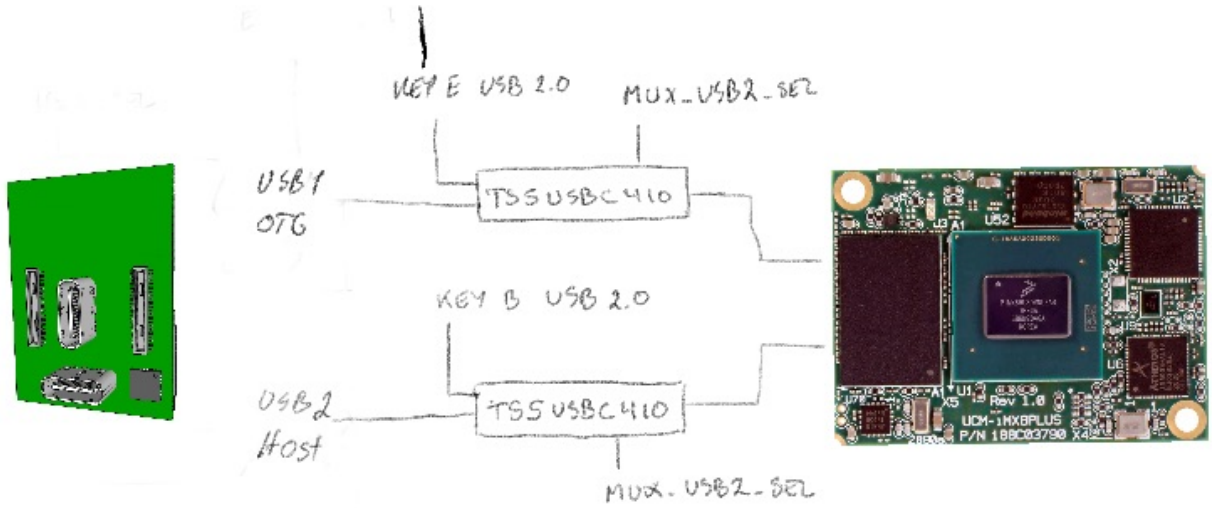
Multiplexing USB

The i.MX8 has two USB busses. USB1(supports OTG) and USB2(Host mode only).

The USB 3.0 superspeed USB1/USB2 from the SoM are multiplexed using CBTL04083 and controlled by MUX_USB3_SEL pins. The USB-C connector Alt. mode is managed by HD3SS460. The default(SEL = low?) state is to connect USB2 to USB-C plug via HD3SS460.



The USB 2.0 USB1/USB2 from the SoM are multiplexed using TS5USBC41 and controlled by MUX_USB2_SEL pins. The USB-C connector USB 2.0 signals(A/B 6/7) are managed separately and multiplexed using TS5USBC41. This allows routing an Extra USB 2.0 signal selectively via the Debug Breakout connector.



SEL	Connect to
High	m.2
Low	USB-C via HD3SS460

Key E

See EXPANSION document for more information.

M.2 Slot Features and Pins

Standard SSD modules on Key B would be M.2 B+M modules. This would use a single PCIe lane. SATA modules are not supported. While generic SSD module is present USB3.1 lanes are not enabled.

Incompatible cards

- KingSpec SSDs, they just offer SATA
- Modern NVMe as they are 4 lane, which is pointless
- Intel 530 B+M SATA technical
- SK Hynix Client SSD overview, are they going high end?

SATA pins A+ A- B+ B- GND

- Device Activity Signal / Disable Staggered Spin-Up DA/DSS
- Presence detection. GND on the card inserted.
- pin 56/58 uses Two Wire Interface on Intel Card
- DEVSLP Device Sleep, input. If driven high the host is informing the SSD to enter a low power state. (Serial ATA Specification Rev 3.2 DEVSLP)

Detecting the type of module inserted

Ziloo Supervisor Module sets CONFIG_1 to GND while not registered as a Stem MCU. SSD cards sets CONFIG_2 and CONFIG_3 to GND. WWAN cards either set CONFIG_2 or CONFIG_3 to GND. If CONFIG_1/CONFIG_2/CONFIG_3 are floating no card is inserted. Unsupported configs are: GND GND GND, GND GND nc, GND nc GND. The MSP430 expander must do internal pull up of the CONFIG inputs.

On our own card we use CONFIG_0 to 3 for dynamic state and low speed communication.

Config pins on Key B (Limited WWAN configs, no SATA)

0	1	2	3	Host Interface
0	nc	0	0	SSD-PCIe
0	nc	nc	0	WWAN – PCIe (Port Configuration 1)
0	nc	0	nc	WWAN – PCIe, USB3.1 Gen1 (Port Configuration 1)
nc	0	nc	nc	WWAN – PCIe, USB3.1 (Ziloo Supervisor)
nc	nc	nc	nc	No Add-in card present

If Supervisor is inserted (CONFIG_1 = low) the following pins should be enabled. This is done with 8 bit switch.

- SDIO 59..65, 66, 68
- MFG 56, 58

Bluetooth over USB or UART

Traditionally UART is used for BLE. Newer modules use USB, presumably for faster transfers.

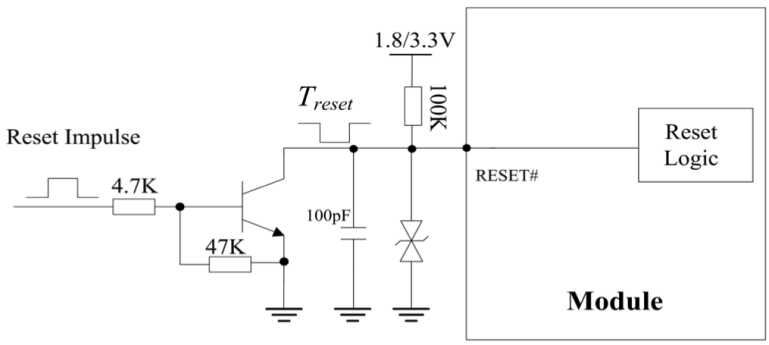
Key B

The Key B socket can support standard modules and a supervisor module.

Notes on the pins:

RESET#

The RESET# need a pull up with a resistor to 1.8V or 3.3V, it is strongly recommended to put a100pF capacitor and an ESD protection diode close to the RESET# pin. Please refer to the following figure for the recommended reference circuit.



Ziloo Specific Submodule Key B

An SSD could be combined with remote monitoring, supervision and remote control. It would extend the features available to the SoM and.

Key M ? cards

- KBG40ZNS128G Kioxia/Toshiba 128GB on Amazon
- KBG40ZNS256G datasheet
- Kioxia/Toshiba BG4 Series

Kioxia seems to have made(still making) B+M 2 lane NVMe SSDs that work fine.

Key E cards

m.2 1620 are embeddable SSD modules

Testing with UCM/Yocto

USB Cameras

> lsusb

Enumerate PCI devices (NVMe SSD)

> lspci

Installing dev support

https://opensource.com/article/21/9/nvme-cli

Connector Pinouts

Key B

M.2 Key B Pin allocations

Pin id.	Upper	Lower	Description	Counterpoint	Voltage Level	Spec Feature
1	CONFIG_3		Defines Module Type	FACE-EX		
2		+3.3V	3.3 V power supply from main board		3.3V	
3	GND		Ground		GND	
4		+3.3V	3.3 V power supply from main board		3.3V	
5	GND		Ground (available?)		GND	
6		M2B_PWROFF	FULL_CARD_POWER_OFF	FACE-EX P6.4	3.3V	
7	USB D+		USB data pair positive USB D+	USB D+		
8		W_DIS1	Wireless disable 1	EXB.3		
9	USB D-		USB data pair negative USB D-	USB D-		
10		LED_1	GPIO9 / WWAN LED_1 / BCLK / SCK	SAI5_TXC/P2.55	3.3V	
11	GND		Ground (available?)		GND	
12 - 19						
20		M2_I2S_TXFS	GPIO5 / SPK I2S LRC	SAI5_TXFS/P2.53	1.8V	
21	CONFIG_0			FACE-EX		
22		M2_I2S_TXD0	GPIO6 / SPK I2S DAT	SAI5_TXD0/P2.60	1.8V	
23	GPIO11		WAKE_ON_WWAN		1.8V	
24		M2_I2S_RXFS	GPIO7 / MIC I2S LRC	SAI5_RXFS/P1.34	1.8V	
25	DPR		WWAN Dynamic Power Reduction		1.8V	
26		GPIO10	SOUND_INT?	INT pin?	1.8V	
27	GND		Ground		GND	
28		M2_I2S_RXD0	GPIO8 / MIC I2S DAT	SAI5_RXD0/P1.28	1.8V	

Pin id.	Upper	Lower	Description	Counterpoint	Voltage Level	Spec Feature
29	USB3 RX-		PER-1 / SSIC M2_USB3_SSRXN	M2_USB3_SSRX-		
30		SIM_RST	UIM RESET	-		
31	USB3 RX+		PER+1 / SSIC M2_USB3_SSRXP	M2_USB3_SSRX+		
32		SIM_CLK	UIM CLK	-		
33	GND		Ground		GND	
34		SIM_DATA	UIM DATA	-		
35	USB3 TX-		PET-1 / SSIC M2_USB3_SSTX-	M2_USB3_SSTX-		
36		SIM_PWR	UIM PWR	-		
37	USB3 TX+		PET+2 / SSIC M2_USB3_SSTX+	M2_USB3_SSTX+		
38		(DEVSLP)	Device Sleep, input. high=sleep	-	3.3V	SATA only
39	GND		Ground		GND	
40		GNSS_SCL	GPIO_0 / GNSS / STEM / SCL	I2C3 SCL	1.8V	
41	PCIE RXN-		PCIE RXN- / PER-0 / SATA-B+	PCIE RXN-		
42		GNSS_SDA	GPIO_1 / GNSS / STEM / SDA	I2C3 SDA	1.8V	
43	PCIE RXN+		PCIE RXN+ / PER+0 / SATA-B-	PCIE RXN+	1.8V	
44		GNSS_IRQ	GPIO_2 / IRQ / ALERT	FACE-EX	1.8V	
45	GND		Ground		GND	
46		GPIO3	GNSS_0	PWM2_OUT	1.8V	
47	PCIE TXN-		PCIE TXN- / PET-0 / SATA-A-	PCIE TXN-	1.8V	
48		GPIO4	GNSS_1	PWM3_OUT	1.8V	
49	PCIE TXN+		PCIE TXN+ / PET-0 / SATA-A+	PCIE TXN+	1.8V	
50		PERST	PCI Reset	mPCIe_PERST	3.3V	

Pin id.	Upper	Lower	Description	Counterpoint	Voltage Level	Spec Feature
51	GND		Ground		GND	
52		CLKREQ	Reference clock request	PCIE_CLKREQ_B	3.3V	
53	REFCLK-		PCIE REFCLK-	REFCLK-		
54		WAKE	PCIe WAKE# Active Low.	PCIE_WAKE_B	3.3V	
55	REFCLK+		PCIE REFCLK+	REFCLK+		
56		MFG_DAT	SYS/MFG SDA	SYS I2C SDA		
57	GND		Ground			
58		MFG_CLK	SYS/MFG SCL	SYS I2C SCL		
59	DATA0		Key M	SD2_DATA0	3.3V	
60		COEX3	Key M	GPIO4_IO21		
61	DATA1		Key M	SD2_DATA1	3.3V	
62		COEX_TXD	Key M/Access to LoRa/ Debug Output	UART2_TXD	1.8V	
63	DATA2		Key M	SD2_DATA2	3.3V	
64		COEX_RXD	Key M/Access to LoRa/ Debug Output	UART2_RXD	1.8V	
65	DATA3		Key M	SD2_DATA3	3.3V	
66		SDCMD/SIMCD	Key M / SDIO CMD / SIM DETECT	SD2_CMD	3.3V	
67	RESET#		RESET	FACE-EX	1.8V	WWAN
68		SDCLK/SUSCLK	SDIO CLK/32.768 kHz prov. by Platform	SD2_CLK	+3.3V	
69	CONFIG_1		Defines module type +	FACE-EX P6.1		
70		VBAT	VSOM/VBAT when SoM powered		+3.1V - +4.4V	
71	GND		Ground		GND	
72		VBAT	VSOM/VBAT when SoM powered		+3.1V - +4.4V	
73	GND		Ground		GND	
74		VBAT	VSOM/VBAT when SoM powered		+3.1V - +4.4V	
75	CONFIG_2		Defines Module Type NC	FACE-EX		

3.3V is used by card to generate signals.

Sound pins are changed to pass DATA0 and use SAI5 instead of SAI3

Key E

M.2 Key E Pin allocations

Pin id.	Upper	Lower	Description	Counterpoint	Voltage
1	GND		Ground		
2		+3.3V	3.3 V power supply from main board		3.3V
3	USB D+		USB data pair positive	USB D+	
4		+3.3V	3.3 V power supply from main board		3.3V
5	USB D-		USB data pair negative	USB D-	
6		M2E_PWROFF	Card PWR OFF	EX4.11	1.8/3.3
7	GND		Ground		GND
8		M2_I2S_CLK	GPIO5 M2_I2S_CLK	SAI5_TXC	1.8V
9	SDIO CLK		SDIO	SD1 CLK	1.8V
10		M2_I2S_WS	GPIO8 M2_I2S_TXFS	SAI5_TXFS	1.8V
11	SDIO CMD		SDIO	SD1 CMD	1.8V
12		M2_I2S_TXD2	GPIO6 M2_I2S_DIN SAI5	SAI5_TXD2	1.8V
13	SDIO DATA0		SDIO	SD1 DATA0	1.8V
14		M2_I2S_RXD2	GPIO7 M2_I2S_DOUT SAI5	SAI5_RXD2	1.8V
15	SDIO DATA1		SDIO	SD1 DATA1	1.8V
16		LED2#	Add RXFS ?		
17	SDIO DATA2		SDIO	SD1 DATA2	1.8V
18		GND	Ground		GND
19	SDIO DATA3		SDIO	SD1 DATA3	1.8V
20		UART WAKE#	Bluetooth uses to wake up platform	EX1.12	3.3V
21	SDIO WAKE#		WiFi uses to wake up platform	EX1.13	1.8V
22		UART RxD		UART2_RXD	1.8V

Pin id.	Upper	Lower	Description	Counterpoint	Voltage
23	SDIO RESET#		Signal to independently reset WiFi	SD1_RESET_B[?]	1.8V
24 - 31					
32		UART TxD		UART2_TXD	1.8V
33	GND		Ground		GND
34		UART CTS		UART4_RXD	1.8V
35	PCIE TXN-		PCIE TXN- / PET-0 / SATA-A-	-	1.8V
36		UART RTS		UART4_TXD	1.8V
37	PCIE TXN+		PCIE TXN+ / PET-0 / SATA-A+	-	1.8V
38		JTAG_TDO	Debugging		1.8V
39	GND		Ground		GND
40		COEX4	Wake up the WiFi	EX6.0	1.8V
41	PCIE RXN-		PCIE RXN- / PER-0 / SATA-B+	-	
42		DEV_BT_WAKE	Wake up the Bluetooth	EX6.1[?]	1.8V
43	PCIE RXN+		PCIE RXN+ / PER+0 / SATA-B-	-	1.8V
44		JTAG_TDI	Debugging		1.8V
45	GND		Ground		GND
46		JTAG_TCK	Debugging		1.8V
47	PCIE REFCLK+		PCIE REFCLK+	-	
48		JTAG_TMS	Debugging		1.8V
49	PCIE REFCLK-		PCIE REFCLK-	-	
50		SUSCLK	32.768 kHz provided by Platform	-	
51	GND		Ground		GND
52		PERST0#	PCI Reset	-	
53	CLKREQ0#		Reference clock request	-	3.3V
54		W_DISABLE2#	Independently reset the Bluetooth	EX1.10 EX4.9	1.8V
55	PE WAKE#		PCIe uses to wake up platform	-	1.8V

Pin id.	Upper	Lower	Description	Counterpoint	Voltage
56		W_DISABLE1#	Full power down Bluetooth + WiFi	EX1.11 EX4.10	1.8V
57	GND		Ground		GND
58		I2C_DATA	I2C DATA	I2C3 SDA	1.8V
59	USB3 TX+		PET+1 / SSIC M2_USB3_SSTX+	M2_USB3_SSTX+	
60		I2C_CLK	I2C CLK	I2C3 SCL	1.8V
61	USB3 TX-		PET-1 / SSIC M2_USB3_SSTX-	M2_USB3_SSTX-	
62		ALERT#		EX1.7	1.8V
63	GND		Ground		GND
64		SWD CLK PD	SWD Clock Power	SWD CLK PD	
65	USB3 RX+		PER+1 / SSIC M2_USB3_SSRXP	M2_USB3_SSRX+	
66		SWD DAT PD	SWD Data Power	SWD DAT PD	
67	USB3 RX-		PER-1 / SSIC M2_USB3_SSRXN	M2_USB3_SSRX-	
68		SWD CLK RP	SWD Clock RP	SWD CLK RP	
69	GND		Ground		GND
70		SWD DAT RP	SWD Data RP	SWD DAT RP	
71	RP UART			UART_RP_RXD	3.3V
72		VRES	Power VRES		+3.3V
73	RP UART			UART_RP_TXD	3.3V
74		VRES	Power VRES		+3.3V
75	GND		Ground		GND

Supports

- WNFB-266XI SDIO Wireless Module via SoM (SD1, UART2)
- Debugging/Probe module
- [?] Consider Which I2C to default: I2C3 or I2C6
- [?] How to support I2S and PCM alternately