Chapter 8
Chip IO and Pinmux

8.1 External Signals and Pin Multiplexing

8.1.1 Overview

The chip contains a limited number of pins, most of which have multiple signal options. These signal-to-pin and pin-to-signal options are selected by the input-output multiplexer called IOMUX. The IOMUX is also used to configure other pin characteristics, such as voltage level, drive strength, and hysteresis.

The muxing options table lists the external signals grouped by the module instance, the muxing options for each signal, and the registers used to route the signal to the chosen pad.

8.1.1.1 Muxing Options

Instance	Port	Pad	Mode
CCM	CCM_CLKO1	ECSPI2_MISO	ALT4
		GPIO1_IO14	ALT6
	CCM_CLKO2	ECSPI2_SS0	ALT4
		GPIO1_IO15	ALT6
	CCM_ENET_PHY_REF_CLK_ROOT	GPIO1_IO00	ALT1
	CCM_EXT_CLK1	GPIO1_IO00	ALT6
	CCM_EXT_CLK2	GPIO1_IO01	ALT6
	CCM_EXT_CLK3	GPIO1_IO06	ALT6
	CCM_EXT_CLK4	GPIO1_IO07	ALT6
	CCM_PMIC_READY	GPIO1_IO05	ALT5
		GPIO1_IO11	ALT5

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Instance	Port	Pad	Mode
	CCM_PMIC_STBY_REQ	PMIC_STBY_REQ	ALT0
	REF_CLK_24M	GPIO1_IO01	ALT5
	REF_CLK_32K	GPIO1_IO00	ALT5
CORESIGHT	CORESIGHT_EVENTI	SD2_WP	ALT6
	CORESIGHT_EVENTO	NAND_WP_B	ALT6
	CORESIGHT_TRACE00	NAND_CE1_B	ALT6
	CORESIGHT_TRACE01	NAND_CE2_B	ALT6
	CORESIGHT_TRACE02	NAND_CE3_B	ALT6
	CORESIGHT_TRACE03	NAND_CLE	ALT6
	CORESIGHT_TRACE04	NAND_DATA00	ALT6
	CORESIGHT_TRACE05	NAND_DATA01	ALT6
	CORESIGHT_TRACE06	NAND_DATA02	ALT6
	CORESIGHT_TRACE07	NAND_DATA03	ALT6
	CORESIGHT_TRACE08	NAND_DATA04	ALT6
	CORESIGHT_TRACE09	NAND_DATA05	ALT6
	CORESIGHT_TRACE10	NAND_DATA06	ALT6
	CORESIGHT_TRACE11	NAND_DATA07	ALT6
	CORESIGHT_TRACE12	NAND_DQS	ALT6
	CORESIGHT_TRACE13	NAND_RE_B	ALT6
	CORESIGHT_TRACE14	NAND_READY_B	ALT6
	CORESIGHT_TRACE15	NAND_WE_B	ALT6
	CORESIGHT_TRACE_CLK	NAND_ALE	ALT6
	CORESIGHT_TRACE_CTL	NAND_CE0_B	ALT6
DRAM	DRAM_AC00	DRAM_AC00	No Muxing
	DRAM_AC01	DRAM_AC01	No Muxing
	DRAM_AC02	DRAM_AC02	No Muxing
	DRAM_AC03	DRAM_AC03	No Muxing
	DRAM_AC04	DRAM_AC04	No Muxing
	DRAM_AC05	DRAM_AC05	No Muxing
	DRAM_AC06	DRAM_AC06	No Muxing
	DRAM_AC07	DRAM_AC07	No Muxing
	DRAM_AC08	DRAM_AC08	No Muxing
	DRAM_AC09	DRAM_AC09	No Muxing
	DRAM_AC10	DRAM_AC10	No Muxing
	DRAM_AC11	DRAM_AC11	No Muxing
	DRAM_AC12	DRAM_AC12	No Muxing
	DRAM_AC13	DRAM_AC13	No Muxing
	DRAM_AC14	DRAM_AC14	No Muxing
	DRAM_AC15	DRAM_AC15	No Muxing
	DRAM_AC16	DRAM_AC16	No Muxing
	DRAM_AC17	DRAM_AC17	No Muxing

Table continues on the next page...

Instance	Port	Pad	Mode
	DRAM_AC19	DRAM_AC19	No Muxing
	DRAM_AC20	DRAM_AC20	No Muxing
	DRAM_AC21	DRAM_AC21	No Muxing
	DRAM_AC22	DRAM_AC22	No Muxing
	DRAM_AC23	DRAM_AC23	No Muxing
	DRAM_AC24	DRAM_AC24	No Muxing
	DRAM_AC25	DRAM_AC25	No Muxing
	DRAM_AC26	DRAM_AC26	No Muxing
	DRAM_AC27	DRAM_AC27	No Muxing
	DRAM_AC28	DRAM_AC28	No Muxing
	DRAM_AC29	DRAM_AC29	No Muxing
	DRAM_AC30	DRAM_AC30	No Muxing
	DRAM_AC31	DRAM_AC31	No Muxing
	DRAM_AC32	DRAM_AC32	No Muxing
	DRAM_AC33	DRAM_AC33	No Muxing
	DRAM_AC34	DRAM_AC34	No Muxing
	DRAM_AC35	DRAM_AC35	No Muxing
	DRAM_AC36	DRAM_AC36	No Muxing
	DRAM_AC37	DRAM_AC37	No Muxing
	DRAM_AC38	DRAM_AC38	No Muxing
	DRAM_ALERT_N	DRAM_ALERT_N	No Muxing
	DRAM_DM0	DRAM_DM0	No Muxing
	DRAM_DM1	DRAM_DM1	No Muxing
	DRAM_DM2	DRAM_DM2	No Muxing
	DRAM_DM3	DRAM_DM3	No Muxing
	DRAM_DQ00	DRAM_DQ00	No Muxing
	DRAM_DQ01	DRAM_DQ01	No Muxing
	DRAM_DQ02	DRAM_DQ02	No Muxing
	DRAM_DQ03	DRAM_DQ03	No Muxing
	DRAM_DQ04	DRAM_DQ04	No Muxing
	DRAM_DQ05	DRAM_DQ05	No Muxing
	DRAM_DQ06	DRAM_DQ06	No Muxing
	DRAM_DQ07	DRAM_DQ07	No Muxing
	DRAM_DQ08	DRAM_DQ08	No Muxing
	DRAM_DQ09	DRAM_DQ09	No Muxing
	DRAM_DQ10	DRAM_DQ10	No Muxing
	DRAM_DQ11	DRAM_DQ11	No Muxing
	DRAM_DQ12	DRAM_DQ12	No Muxing
	DRAM_DQ13	DRAM_DQ13	No Muxing
	DRAM_DQ14	DRAM_DQ14	No Muxing
	DRAM_DQ15	DRAM_DQ15	No Muxing

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Instance	Port	Pad	Mode
	DRAM_DQ16	DRAM_DQ16	No Muxing
	DRAM_DQ17	DRAM_DQ17	No Muxing
	DRAM_DQ18	DRAM_DQ18	No Muxing
	DRAM_DQ19	DRAM_DQ19	No Muxing
	DRAM_DQ20	DRAM_DQ20	No Muxing
	DRAM_DQ21	DRAM_DQ21	No Muxing
	DRAM_DQ22	DRAM_DQ22	No Muxing
	DRAM_DQ23	DRAM_DQ23	No Muxing
	DRAM_DQ24	DRAM_DQ24	No Muxing
	DRAM_DQ25	DRAM_DQ25	No Muxing
	DRAM_DQ26	DRAM_DQ26	No Muxing
	DRAM_DQ27	DRAM_DQ27	No Muxing
	DRAM_DQ28	DRAM_DQ28	No Muxing
	DRAM_DQ29	DRAM_DQ29	No Muxing
	DRAM_DQ30	DRAM_DQ30	No Muxing
	DRAM_DQ31	DRAM_DQ31	No Muxing
	DRAM_DQS0_N	DRAM_DQS0_N	No Muxing
	DRAM_DQS0_P	DRAM_DQS0_P	No Muxing
	DRAM_DQS1_N	DRAM_DQS1_N	No Muxing
	DRAM_DQS1_P	DRAM_DQS1_P	No Muxing
	DRAM_DQS2_N	DRAM_DQS2_N	No Muxing
	DRAM_DQS2_P	DRAM_DQS2_P	No Muxing
	DRAM_DQS3_N	DRAM_DQS3_N	No Muxing
	DRAM_DQS3_P	DRAM_DQS3_P	No Muxing
	DRAM_RESET_N	DRAM_RESET_N	No Muxing
	DRAM_VREF	DRAM_VREF	No Muxing
	DRAM_ZN	DRAM_ZN	No Muxing
EARC	EARC_AUX	EARC_AUX	No Muxing
	EARC_P_UTIL	EARC_P_UTIL	No Muxing
	EARC_N_HPD	EARC_N_HPD	No Muxing
ECSPI1	ECSPI1_MISO	ECSPI1_MISO	ALT0
		I2C2_SCL	ALT3
	ECSPI1_MOSI	ECSPI1_MOSI	ALT0
		I2C1_SDA	ALT3
	ECSPI1_SCLK	ECSPI1_SCLK	ALT0
		I2C1_SCL	ALT3
	ECSPI1_SS0	ECSPI1_SS0	ALT0
		I2C2_SDA	ALT3
ECSPI2	ECSPI2_MISO	ECSPI2_MISO	ALT0
		SD2_DATA3	ALT2
		I2C4_SCL	ALT3

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Instance	Port	Pad	Mode
	ECSPI2_MOSI	ECSPI2_MOSI	ALT0
		SD2_CMD	ALT2
		I2C3_SDA	ALT3
	ECSPI2_SCLK	ECSPI2_SCLK	ALT0
		SD2_CLK	ALT2
		I2C3_SCL	ALT3
	ECSPI2_SS0	ECSPI2_SS0	ALT0
		SD2_DATA2	ALT2
		I2C4_SDA	ALT3
ECSPI3	ECSPI3_MISO	UART2_RXD	ALT1
	ECSPI3_MOSI	UART1_TXD	ALT1
	ECSPI3_SCLK	UART1_RXD	ALT1
	ECSPI3_SS0	UART2_TXD	ALT1
ENET_QOS	ENET_QOS_1588_EVENT0_AUX_IN	GPIO1_IO08	ALT4
	ENET_QOS_1588_EVENT0_IN	GPIO1_IO08	ALT1
	ENET_QOS_1588_EVENT0_OUT	GPIO1_IO09	ALT1
	ENET_QOS_1588_EVENT1_AUX_IN	I2C2_SCL	ALT4
	ENET_QOS_1588_EVENT1_IN	I2C2_SCL	ALT1
	ENET_QOS_1588_EVENT1_OUT	I2C2_SDA	ALT1
	ENET_QOS_1588_EVENT2_AUX_IN	SAI2_TXD0	ALT4
	ENET_QOS_1588_EVENT2_IN	SAI2_TXD0	ALT2
	ENET_QOS_1588_EVENT2_OUT	SAI2_RXD0	ALT2
	ENET_QOS_1588_EVENT3_AUX_IN	SAI2_MCLK	ALT4
	ENET_QOS_1588_EVENT3_IN	SAI2_MCLK	ALT2
	ENET_QOS_1588_EVENT3_OUT	SAI2_TXFS	ALT2
	ENET_QOS_INPUT=ENET_QOS_TX_CLK, OUTPUT=CCM_ENET_QOS_REF_CLK_ROOT	ENET_TD2	ALT1
	ENET_QOS_MDC	ENET_MDC	ALT0
		GPIO1_IO06	ALT1
		I2C1_SCL	ALT1
	ENET_QOS_MDIO	ENET_MDIO	ALT0

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Instance	Port	Pad	Mode
		GPIO1_IO07	ALT1
		I2C1_SDA	ALT1
	ENET_QOS_RGMII_RD0	ENET_RD0	ALT0
	ENET_QOS_RGMII_RD1	ENET_RD1	ALT0
	ENET_QOS_RGMII_RD2	ENET_RD2	ALT0
	ENET_QOS_RGMII_RD3	ENET_RD3	ALT0
	ENET_QOS_RGMII_RX_CTL	ENET_RX_CTL	ALT0
	ENET_QOS_RGMII_RXC	ENET_RXC	ALT0
	ENET_QOS_RGMII_TD0	ENET_TD0	ALT0
	ENET_QOS_RGMII_TD1	ENET_TD1	ALT0
	ENET_QOS_RGMII_TD2	ENET_TD2	ALT0
	ENET_QOS_RGMII_TD3	ENET_TD3	ALT0
	ENET_QOS_RGMII_TX_CTL	ENET_TX_CTL	ALT0
	ENET_QOS_RGMII_TXC	ENET_TXC	ALT0
	ENET_QOS_RX_ER	ENET_RXC	ALT1
	ENET_QOS_TX_ER	ENET_TXC	ALT1
ENET1	ENET1_1588_EVENT0_IN	SAI1_RXFS	ALT4
	ENET1_1588_EVENT0_OUT	SAI1_RXC	ALT4
	ENET1_1588_EVENT1_IN	SAI1_RXD0	ALT4
	ENET1_1588_EVENT1_OUT	SAI1_RXD1	ALT4
	ENET1_INPUT=ENET1_TX_CLK, OUTPUT=CCM_ENET_REF_CLK_ROOT	SD1_RESET_B	ALT1
	ENET1_INPUT=ENET1_TX_CLK, OUTPUT=CCM_ENET_REF_CLK_ROOT	SAI1_MCLK	ALT4
	ENET1_MDC	SD1_CLK	ALT1
		SAI1_RXD2	ALT4
	ENET1_MDIO	SD1_CMD	ALT1
		SAI1_RXD3	ALT4
	ENET1_RGMII_RD0	SD1_DATA2	ALT1
		SAI1_RXD4	ALT4
	ENET1_RGMII_RD1	SD1_DATA3	ALT1
		SAI1_RXD5	ALT4
	ENET1_RGMII_RD2	SAI1_RXD6	ALT4
	ENET1_RGMII_RD3	SAI1_RXD7	ALT4
	ENET1_RGMII_RX_CTL	SD1_DATA6	ALT1
		SAI1_TXFS	ALT4
	ENET1_RGMII_RXC	SAI1_TXC	ALT4
	ENET1_RGMII_TD0	SD1_DATA1	ALT1

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Instance	Port	Pad	Mode
		SAI1_TXD0	ALT4
	ENET1_RGMII_TD1	SD1_DATA0	ALT1
		SAI1_TXD1	ALT4
	ENET1_RGMII_TD2	SAI1_TXD2	ALT4
	ENET1_RGMII_TD3	SAI1_TXD3	ALT4
	ENET1_RGMII_TX_CTL	SD1_DATA4	ALT1
		SAI1_TXD4	ALT4
	ENET1_RGMII_TXC	SAI1_TXD5	ALT4
	ENET1_RX_ER	SD1_DATA7	ALT1
		SAI1_TXD6	ALT4
	ENET1_TX_ER	SD1_DATA5	ALT1
		SAI1_TXD7	ALT4
FLEXCAN1	FLEXCAN1_RX	SAI2_TXC	ALT3
		SPDIF_RX	ALT4
		HDMI_DDC_SDA	ALT4
		SAI5_RXD2	ALT6
	FLEXCAN1_TX	SAI2_RXC	ALT3
		SPDIF_TX	ALT4
		HDMI_DDC_SCL	ALT4
		SAI5_RXD1	ALT6
FLEXCAN2	FLEXCAN2_RX	SAI2_MCLK	ALT3
		UART3_TXD	ALT4
		HDMI_HPD	ALT4
		SAI5_MCLK	ALT6
	FLEXCAN2_TX	SAI2_TXD0	ALT3
		UART3_RXD	ALT4
		HDMI_CEC	ALT4
		SAI5_RXD3	ALT6
GPIO1	GPIO1_IO00	GPIO1_IO00	ALT0
	GPIO1_IO01	GPIO1_IO01	ALT0
	GPIO1_IO02	GPIO1_IO02	ALT0
	GPIO1_IO03	GPIO1_IO03	ALT0
	GPIO1_IO04	GPIO1_IO04	ALT0
	GPIO1_IO05	GPIO1_IO05	ALT0
	GPIO1_IO06	GPIO1_IO06	ALT0
	GPIO1_IO07	GPIO1_IO07	ALT0
	GPIO1_IO08	GPIO1_IO08	ALT0
	GPIO1_IO09	GPIO1_IO09	ALT0
	GPIO1_IO10	GPIO1_IO10	ALT0
	GPIO1_IO11	GPIO1_IO11	ALT0
	GPIO1_IO12	GPIO1_IO12	ALT0

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Instance	Port	Pad	Mode
	GPIO1_IO13	GPIO1_IO13	ALT0
	GPIO1_IO14	GPIO1_IO14	ALT0
	GPIO1_IO15	GPIO1_IO15	ALT0
	GPIO1_IO16	ENET_MDC	ALT5
	GPIO1_IO17	ENET_MDIO	ALT5
	GPIO1_IO18	ENET_TD3	ALT5
	GPIO1_IO19	ENET_TD2	ALT5
	GPIO1_IO20	ENET_TD1	ALT5
	GPIO1_IO21	ENET_TD0	ALT5
	GPIO1_IO22	ENET_TX_CTL	ALT5
	GPIO1_IO23	ENET_TXC	ALT5
	GPIO1_IO24	ENET_RX_CTL	ALT5
	GPIO1_IO25	ENET_RXC	ALT5
	GPIO1_IO26	ENET_RD0	ALT5
	GPIO1_IO27	ENET_RD1	ALT5
	GPIO1_IO28	ENET_RD2	ALT5
	GPIO1_IO29	ENET_RD3	ALT5
GPIO2	GPIO2_IO00	SD1_CLK	ALT5
	GPIO2_IO01	SD1_CMD	ALT5
	GPIO2_IO02	SD1_DATA0	ALT5
	GPIO2_IO03	SD1_DATA1	ALT5
	GPIO2_IO04	SD1_DATA2	ALT5
	GPIO2_IO05	SD1_DATA3	ALT5
	GPIO2_IO06	SD1_DATA4	ALT5
	GPIO2_IO07	SD1_DATA5	ALT5
	GPIO2_IO08	SD1_DATA6	ALT5
	GPIO2_IO09	SD1_DATA7	ALT5
	GPIO2_IO10	SD1_RESET_B	ALT5
	GPIO2_IO11	SD1_STROBE	ALT5
	GPIO2_IO12	SD2_CD_B	ALT5
	GPIO2_IO13	SD2_CLK	ALT5
	GPIO2_IO14	SD2_CMD	ALT5
	GPIO2_IO15	SD2_DATA0	ALT5
	GPIO2_IO16	SD2_DATA1	ALT5
	GPIO2_IO17	SD2_DATA2	ALT5
	GPIO2_IO18	SD2_DATA3	ALT5
	GPIO2_IO19	SD2_RESET_B	ALT5
	GPIO2_IO20	SD2_WP	ALT5
GPIO3	GPIO3_IO00	NAND_ALE	ALT5
	GPIO3_IO01	NAND_CE0_B	ALT5
	GPIO3_IO02	NAND_CE1_B	ALT5

Table continues on the next page...

Instance	Port	Pad	Mode
	GPIO3_IO03	NAND_CE2_B	ALT5
	GPIO3_IO04	NAND_CE3_B	ALT5
	GPIO3_IO05	NAND_CLE	ALT5
	GPIO3_IO06	NAND_DATA00	ALT5
	GPIO3_IO07	NAND_DATA01	ALT5
	GPIO3_IO08	NAND_DATA02	ALT5
	GPIO3_IO09	NAND_DATA03	ALT5
	GPIO3_IO10	NAND_DATA04	ALT5
	GPIO3_IO11	NAND_DATA05	ALT5
	GPIO3_IO12	NAND_DATA06	ALT5
	GPIO3_IO13	NAND_DATA07	ALT5
	GPIO3_IO14	NAND_DQS	ALT5
	GPIO3_IO15	NAND_RE_B	ALT5
	GPIO3_IO16	NAND_READY_B	ALT5
	GPIO3_IO17	NAND_WE_B	ALT5
	GPIO3_IO18	NAND_WP_B	ALT5
	GPIO3_IO19	SAI5_RXFS	ALT5
	GPIO3_IO20	SAI5_RXC	ALT5
	GPIO3_IO21	SAI5_RXD0	ALT5
	GPIO3_IO22	SAI5_RXD1	ALT5
	GPIO3_IO23	SAI5_RXD2	ALT5
	GPIO3_IO24	SAI5_RXD3	ALT5
	GPIO3_IO25	SAI5_MCLK	ALT5
	GPIO3_IO26	HDMI_DDC_SCL	ALT5
	GPIO3_IO27	HDMI_DDC_SDA	ALT5
	GPIO3_IO28	HDMI_CEC	ALT5
	GPIO3_IO29	HDMI_HPD	ALT5
GPIO4	GPIO4_IO00	SAI1_RXFS	ALT5
	GPIO4_IO01	SAI1_RXC	ALT5
	GPIO4_IO02	SAI1_RXD0	ALT5
	GPIO4_IO03	SAI1_RXD1	ALT5
	GPIO4_IO04	SAI1_RXD2	ALT5
	GPIO4_IO05	SAI1_RXD3	ALT5
	GPIO4_IO06	SAI1_RXD4	ALT5
	GPIO4_IO07	SAI1_RXD5	ALT5
	GPIO4_IO08	SAI1_RXD6	ALT5
	GPIO4_IO09	SAI1_RXD7	ALT5
	GPIO4_IO10	SAI1_TXFS	ALT5
	GPIO4_IO11	SAI1_TXC	ALT5
	GPIO4_IO12	SAI1_TXD0	ALT5
	GPIO4_IO13	SAI1_TXD1	ALT5

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Instance	Port	Pad	Mode
	GPIO4_IO14	SAI1_TXD2	ALT5
	GPIO4_IO15	SAI1_TXD3	ALT5
	GPIO4_IO16	SAI1_TXD4	ALT5
	GPIO4_IO17	SAI1_TXD5	ALT5
	GPIO4_IO18	SAI1_TXD6	ALT5
	GPIO4_IO19	SAI1_TXD7	ALT5
	GPIO4_IO20	SAI1_MCLK	ALT5
	GPIO4_IO21	SAI2_RXFS	ALT5
	GPIO4_IO22	SAI2_RXC	ALT5
	GPIO4_IO23	SAI2_RXD0	ALT5
	GPIO4_IO24	SAI2_TXFS	ALT5
	GPIO4_IO25	SAI2_TXC	ALT5
	GPIO4_IO26	SAI2_TXD0	ALT5
	GPIO4_IO27	SAI2_MCLK	ALT5
	GPIO4_IO28	SAI3_RXFS	ALT5
	GPIO4_IO29	SAI3_RXC	ALT5
	GPIO4_IO30	SAI3_RXD	ALT5
	GPIO4_IO31	SAI3_TXFS	ALT5
GPIO5	GPIO5_IO00	SAI3_TXC	ALT5
	GPIO5_IO01	SAI3_TXD	ALT5
	GPIO5_IO02	SAI3_MCLK	ALT5
	GPIO5_IO03	SPDIF_TX	ALT5
	GPIO5_IO04	SPDIF_RX	ALT5
	GPIO5_IO05	SPDIF_EXT_CLK	ALT5
	GPIO5_IO06	ECSPI1_SCLK	ALT5
	GPIO5_IO07	ECSPI1_MOSI	ALT5
	GPIO5_IO08	ECSPI1_MISO	ALT5
	GPIO5_IO09	ECSPI1_SS0	ALT5
	GPIO5_IO10	ECSPI2_SCLK	ALT5
	GPIO5_IO11	ECSPI2_MOSI	ALT5
	GPIO5_IO12	ECSPI2_MISO	ALT5
	GPIO5_IO13	ECSPI2_SS0	ALT5
	GPIO5_IO14	I2C1_SCL	ALT5
	GPIO5_IO15	I2C1_SDA	ALT5
	GPIO5_IO16	I2C2_SCL	ALT5
	GPIO5_IO17	I2C2_SDA	ALT5
	GPIO5_IO18	I2C3_SCL	ALT5
	GPIO5_IO19	I2C3_SDA	ALT5
	GPIO5_IO20	I2C4_SCL	ALT5
	GPIO5_IO21	I2C4_SDA	ALT5
	GPIO5_IO22	UART1_RXD	ALT5

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Instance	Port	Pad	Mode
	GPIO5_IO23	UART1_TXD	ALT5
	GPIO5_IO24	UART2_RXD	ALT5
	GPIO5_IO25	UART2_TXD	ALT5
	GPIO5_IO26	UART3_RXD	ALT5
	GPIO5_IO27	UART3_TXD	ALT5
	GPIO5_IO28	UART4_RXD	ALT5
	GPIO5_IO29	UART4_TXD	ALT5
GPT1	GPT1_CAPTURE1	SAI3_TXC	ALT3
		UART4_TXD	ALT3
	GPT1_CAPTURE2	SAI3_TXD	ALT3
		UART3_RXD	ALT3
	GPT1_CLK	SAI3_RXC	ALT3
		UART3_TXD	ALT3
	GPT1_COMPARE1	SPDIF_TX	ALT3
		UART4_RXD	ALT3
	GPT1_COMPARE2	SPDIF_RX	ALT3
		UART2_TXD	ALT3
	GPT1_COMPARE3	SPDIF_EXT_CLK	ALT3
		UART2_RXD	ALT3
GPT2	GPT2_CLK	I2C3_SCL	ALT2
GPT3	GPT3_CLK	I2C3_SDA	ALT2
HDMI	HDMI_CEC	HDMI_CEC	ALT0
	HDMI_HPD	HDMI_HPD	ALT0
	HDMI_HPD_O	HDMI_HPD	ALT1
	HDMI_SCL	HDMI_DDC_SCL	ALT0
	HDMI_SDA	HDMI_DDC_SDA	ALT0
	HDMI_TX0N	HDMI_TX0_N	No Muxing
	HDMI_TX0P	HDMI_TX0_P	No Muxing
	HDMI_TX1N	HDMI_TX1_N	No Muxing
	HDMI_TX1P	HDMI_TX1_P	No Muxing
	HDMI_TX2N	HDMI_TX2_N	No Muxing
	HDMI_TX2P	HDMI_TX2_P	No Muxing
	HDMI_TXCN	HDMI_TXC_N	No Muxing
	HDMI_TXCP	HDMI_TXC_P	No Muxing
	HDMI_REXT	HDMI_REXT	No Muxing
I2C1	I2C1_SCL	I2C1_SCL	ALT0
		ECSPI1_SCLK	ALT2
		SD1_DATA4	ALT3
	I2C1_SDA	I2C1_SDA	ALT0
		ECSPI1_MOSI	ALT2
		SD1_DATA5	ALT3

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Instance	Port	Pad	Mode
I2C2	I2C2_SCL	I2C2_SCL	ALT0
		ECSPI1_MISO	ALT2
		SD1_DATA6	ALT3
	I2C2_SDA	I2C2_SDA	ALT0
		ECSPI1_SS0	ALT2
		SD1_DATA7	ALT3
I2C3	I2C3_SCL	I2C3_SCL	ALT0
		ECSPI2_SCLK	ALT2
		SD1_RESET_B	ALT3
		NAND_DQS	ALT4
		NAND_READY_B	ALT4
	I2C3_SDA	I2C3_SDA	ALT0
		ECSPI2_MOSI	ALT2
		SD1_STROBE	ALT3
		NAND_CE3_B	ALT4
		NAND_WE_B	ALT4
I2C4	I2C4_SCL	I2C4_SCL	ALT0
		SD2_DATA1	ALT2
		ECSPI2_MISO	ALT2
		SD1_DATA2	ALT3
		NAND_CE1_B	ALT4
		NAND_WP_B	ALT4
	I2C4_SDA	I2C4_SDA	ALT0
		SD2_DATA0	ALT2
		ECSPI2_SS0	ALT2
		SD1_DATA3	ALT3
		NAND_CE2_B	ALT4
		NAND_DATA02	ALT4
I2C5	I2C5_SCL	SPDIF_TX	ALT2
		SD1_CLK	ALT3
		SAI5_RXD0	ALT3
		HDMI_DDC_SCL	ALT3
	I2C5_SDA	SPDIF_RX	ALT2
		SD1_CMD	ALT3
		SAI5_MCLK	ALT3
		HDMI_DDC_SDA	ALT3
I2C6	I2C6_SCL	SD1_DATA0	ALT3
		SAI5_RXFS	ALT3
		HDMI_CEC	ALT3
		UART4_RXD	ALT4
	I2C6_SDA	SD1_DATA1	ALT3

Table continues on the next page...

Instance	Port	Pad	Mode
		SAI5_RXC	ALT3
		HDMI_HPD	ALT3
		UART4_TXD	ALT4
ISP	ISP_FL_TRIG_0	GPIO1_IO00	ALT3
		NAND_ALE	ALT3
	ISP_FL_TRIG_1	GPIO1_IO05	ALT3
		NAND_DATA03	ALT4
	ISP_FLASH_TRIG_0	GPIO1_IO02	ALT3
		NAND_DATA00	ALT3
	ISP_FLASH_TRIG_1	GPIO1_IO07	ALT3
		NAND_DATA05	ALT4
	ISP_PRELIGHT_TRIG_0	GPIO1_IO03	ALT3
		NAND_DATA01	ALT3
	ISP_PRELIGHT_TRIG_1	GPIO1_IO08	ALT3
		NAND_DATA06	ALT4
	ISP_SHUTTER_OPEN_0	GPIO1_IO04	ALT3
		NAND_DQS	ALT3
	ISP_SHUTTER_OPEN_1	GPIO1_IO09	ALT3
		NAND_DATA07	ALT4
	ISP_SHUTTER_TRIG_0	GPIO1_IO01	ALT3
		NAND_CE0_B	ALT3
	ISP_SHUTTER_TRIG_1	GPIO1_IO06	ALT3
		NAND_DATA04	ALT4
JTAG	JTAG_MODE	JTAG_MOD	ALT0
	JTAG_TCK	JTAG_TCK	ALT0
	JTAG_TDI	JTAG_TDI	ALT0
	JTAG_TDO	JTAG_TDO	ALT0
	JTAG_TMS	JTAG_TMS	ALT0
LVDS0	LVDS0_CLKN	LVDS0_CLK_N	No Muxing
	LVDS0_CLKP	LVDS0_CLK_P	No Muxing
	LVDS0_D0N	LVDS0_D0_N	No Muxing
	LVDS0_D0P	LVDS0_D0_P	No Muxing
	LVDS0_D1N	LVDS0_D1_N	No Muxing
	LVDS0_D1P	LVDS0_D1_P	No Muxing
	LVDS0_D2N	LVDS0_D2_N	No Muxing
	LVDS0_D2P	LVDS0_D2_P	No Muxing
	LVDS0_D3N	LVDS0_D3_N	No Muxing
	LVDS0_D3P	LVDS0_D3_P	No Muxing
	LVDS1_CLKN	LVDS1_CLK_N	No Muxing
	LVDS1_CLKP	LVDS1_CLK_P	No Muxing
	LVDS1_D0N	LVDS1_D0_N	No Muxing

Table continues on the next page...

Instance	Port	Pad	Mode
	LVDS1_D0P	LVDS1_D0_P	No Muxing
	LVDS1_D1N	LVDS1_D1_N	No Muxing
	LVDS1_D1P	LVDS1_D1_P	No Muxing
	LVDS1_D2N	LVDS1_D2_N	No Muxing
	LVDS1_D2P	LVDS1_D2_P	No Muxing
	LVDS1_D3N	LVDS1_D3_N	No Muxing
	LVDS1_D3P	LVDS1_D3_P	No Muxing
M7	M7_NMI	GPIO1_IO05	ALT1
MIPI CSI1	MIPI_CSI1_CLK_N	MIPI_CSI1_CLK_N	No Muxing
	MIPI_CSI1_CLK_P	MIPI_CSI1_CLK_P	No Muxing
	MIPI_CSI1_D0_N	MIPI_CSI1_D0_N	No Muxing
	MIPI_CSI1_D0_P	MIPI_CSI1_D0_P	No Muxing
	MIPI_CSI1_D1_N	MIPI_CSI1_D1_N	No Muxing
	MIPI_CSI1_D1_P	MIPI_CSI1_D1_P	No Muxing
	MIPI_CSI1_D2_N	MIPI_CSI1_D2_N	No Muxing
	MIPI_CSI1_D2_P	MIPI_CSI1_D2_P	No Muxing
	MIPI_CSI1_D3_N	MIPI_CSI1_D3_N	No Muxing
	MIPI_CSI1_D3_P	MIPI_CSI1_D3_P	No Muxing
	MIPI1_VREG	MIPI_VREG1_CAP	No Muxing
MIPI CSI2	MIPI_CSI2_CLK_N	MIPI_CSI2_CLK_N	No Muxing
	MIPI_CSI2_CLK_P	MIPI_CSI2_CLK_P	No Muxing
	MIPI_CSI2_D0_N	MIPI_CSI2_D0_N	No Muxing
	MIPI_CSI2_D0_P	MIPI_CSI2_D0_P	No Muxing
	MIPI_CSI2_D1_N	MIPI_CSI2_D1_N	No Muxing
	MIPI_CSI2_D1_P	MIPI_CSI2_D1_P	No Muxing
	MIPI_CSI2_D2_N	MIPI_CSI2_D2_N	No Muxing
	MIPI_CSI2_D2_P	MIPI_CSI2_D2_P	No Muxing
	MIPI_CSI2_D3_N	MIPI_CSI2_D3_N	No Muxing
	MIPI_CSI2_D3_P	MIPI_CSI2_D3_P	No Muxing
	MIPI2_VREG	MIPI_VREG2_CAP	No Muxing
MIPI DSI1	MIPI_DSI1_CLK_N	MIPI_DSI1_CLK_N	No Muxing
	MIPI_DSI1_CLK_P	MIPI_DSI1_CLK_P	No Muxing
	MIPI_DSI1_D0_N	MIPI_DSI1_D0_N	No Muxing
	MIPI_DSI1_D0_P	MIPI_DSI1_D0_P	No Muxing
	MIPI_DSI1_D1_N	MIPI_DSI1_D1_N	No Muxing
	MIPI_DSI1_D1_P	MIPI_DSI1_D1_P	No Muxing
	MIPI_DSI1_D2_N	MIPI_DSI1_D2_N	No Muxing
	MIPI_DSI1_D2_P	MIPI_DSI1_D2_P	No Muxing
	MIPI_DSI1_D3_N	MIPI_DSI1_D3_N	No Muxing
	MIPI_DSI1_D3_P	MIPI_DSI1_D3_P	No Muxing
NAND	NAND_ALE	NAND_ALE	ALT0

Table continues on the next page...

Instance	Port	Pad	Mode
	NAND_CE0_B	NAND_CE0_B	ALT0
	NAND_CE1_B	NAND_CE1_B	ALT0
	NAND_CE2_B	NAND_CE2_B	ALT0
	NAND_CE3_B	NAND_CE3_B	ALT0
	NAND_CLE	NAND_CLE	ALT0
	NAND_DATA00	NAND_DATA00	ALT0
	NAND_DATA01	NAND_DATA01	ALT0
	NAND_DATA02	NAND_DATA02	ALT0
	NAND_DATA03	NAND_DATA03	ALT0
	NAND_DATA04	NAND_DATA04	ALT0
	NAND_DATA05	NAND_DATA05	ALT0
	NAND_DATA06	NAND_DATA06	ALT0
	NAND_DATA07	NAND_DATA07	ALT0
	NAND_DQS	NAND_DQS	ALT0
	NAND_RE_B	NAND_RE_B	ALT0
	NAND_READY_B	NAND_READY_B	ALT0
	NAND_WE_B	NAND_WE_B	ALT0
	NAND_WP_B	NAND_WP_B	ALT0
PCIE1	PCIE1_CLKREQ_B	I2C4_SCL	ALT2
		UART4_RXD	ALT2
	PCIE_REF_PAD_CLK_N	PCIE_REF_PAD_CLK_N	No Muxing
	PCIE_REF_PAD_CLK_P	PCIE_REF_PAD_CLK_P	No Muxing
	PCIE_RESREF	PCIE_RESREF	No Muxing
	PCIE_RXN_N	PCIE_RXN_N	No Muxing
	PCIE_RXN_P	PCIE_RXN_P	No Muxing
	PCIE_TXN_N	PCIE_TXN_N	No Muxing
	PCIE_TXN_P	PCIE_TXN_P	No Muxing
PDM	PDM_BIT_STREAM0	ENET_TD1	ALT3
		ENET_RD1	ALT3
		SAI1_RXD0	ALT3
		SD2_DATA0	ALT4
		SAI5_RXD0	ALT4
		SAI3_RXFS	ALT6
	PDM_BIT_STREAM1	ENET_TD2	ALT3
		ENET_RD0	ALT3
		SAI1_RXD1	ALT3
		SD2_DATA1	ALT4
		SAI5_RXD1	ALT4
		SAI2_RXC	ALT6
		SAI2_TXC	ALT6
		SAI3_RXD	ALT6

Table continues on the next page...

Instance	Port	Pad	Mode
	PDM_BIT_STREAM2	ENET_TD3	ALT3
		ENET_RXC	ALT3
		SAI1_RXD2	ALT3
		SD2_DATA2	ALT4
		SAI5_RXD2	ALT4
		SAI2_RXFS	ALT6
		SAI2_TXFS	ALT6
		SAI3_TXC	ALT6
	PDM_BIT_STREAM3	ENET_MDIO	ALT3
		ENET_RX_CTL	ALT3
		SAI1_RXD3	ALT3
		SD2_DATA3	ALT4
		SAI5_RXD3	ALT4
		SAI2_RXD0	ALT6
		SAI3_TXFS	ALT6
	PDM_CLK	ENET_TD0	ALT3
		ENET_RD2	ALT3
		SAI1_RXC	ALT3
		SAI1_TXD7	ALT3
		SD2_CMD	ALT4
		SAI5_RXC	ALT4
		SAI3_RXC	ALT6
PWM1	PWM1_OUT	GPIO1_IO01	ALT1
		SPDIF_EXT_CLK	ALT1
		I2C4_SDA	ALT1
		GPIO1_IO08	ALT2
		SAI5_MCLK	ALT2
PWM2	PWM2_OUT	SPDIF_RX	ALT1
		I2C4_SCL	ALT1
		GPIO1_IO09	ALT2
		GPIO1_IO11	ALT2
		SAI5_RXD0	ALT2
		GPIO1_IO13	ALT5
PWM3	PWM3_OUT	SPDIF_TX	ALT1
		I2C3_SDA	ALT1
		GPIO1_IO10	ALT2
		SAI5_RXC	ALT2
		GPIO1_IO14	ALT5
PWM4	PWM4_OUT	SAI3_MCLK	ALT1
		I2C3_SCL	ALT1
		SAI5_RXFS	ALT2

Table continues on the next page...

Instance	Port	Pad	Mode
		GPIO1_IO15	ALT5
QSPI	QSPI_A_DATA0	NAND_DATA00	ALT1
	QSPI_A_DATA1	NAND_DATA01	ALT1
	QSPI_A_DATA2	NAND_DATA02	ALT1
	QSPI_A_DATA3	NAND_DATA03	ALT1
	QSPI_A_DATA4	NAND_DATA04	ALT3
	QSPI_A_DATA5	NAND_DATA05	ALT3
	QSPI_A_DATA6	NAND_DATA06	ALT3
	QSPI_A_DATA7	NAND_DATA07	ALT3
	QSPI_A_DQS	NAND_DQS	ALT1
	QSPI_A_SCLK	NAND_ALE	ALT1
	QSPI_A_SS0_B	NAND_CE0_B	ALT1
	QSPI_A_SS1_B	NAND_CE1_B	ALT1
	QSPI_B_DATA0	NAND_DATA04	ALT1
	QSPI_B_DATA1	NAND_DATA05	ALT1
	QSPI_B_DATA2	NAND_DATA06	ALT1
	QSPI_B_DATA3	NAND_DATA07	ALT1
	QSPI_B_DQS	NAND_RE_B	ALT1
	QSPI_B_SCLK	NAND_CLE	ALT1
	QSPI_B_SS0_B	NAND_CE2_B	ALT1
	QSPI_B_SS1_B	NAND_CE3_B	ALT1
SAI1	SAI1_MCLK	SAI1_MCLK	ALT0
	SAI1_RX_BCLK	SAI1_RXC	ALT0
	SAI1_RX_DATA0	SAI1_RXD0	ALT0
	SAI1_RX_DATA1	SAI1_RXD1	ALT0
	SAI1_RX_DATA2	SAI1_RXD2	ALT0
	SAI1_RX_DATA3	SAI1_RXD3	ALT0
	SAI1_RX_DATA4	SAI1_RXD4	ALT0
	SAI1_RX_DATA5	SAI1_RXD5	ALT0
	SAI1_RX_DATA6	SAI1_RXD6	ALT0
	SAI1_RX_DATA7	SAI1_RXD7	ALT0
	SAI1_RX_SYNC	SAI1_RXFS	ALT0
		SAI1_RXD5	ALT3
	SAI1_TX_BCLK	SAI1_TXC	ALT0
		SAI5_MCLK	ALT1
		SAI1_MCLK	ALT2
	SAI1_TX_DATA0	SAI1_TXD0	ALT0
		SAI5_RXFS	ALT1
	SAI1_TX_DATA1	SAI1_TXD1	ALT0
		SAI5_RXC	ALT1
		SAI1_RXD0	ALT2

Table continues on the next page...

Instance	Port	Pad	Mode
	SAI1_TX_DATA2	SAI1_TXD2	ALT0
		SAI5_RXD0	ALT1
	SAI1_TX_DATA3	SAI1_TXD3	ALT0
		SAI5_RXD1	ALT1
	SAI1_TX_DATA4	SAI1_TXD4	ALT0
		SAI5_RXD2	ALT1
		SAI1_RXD7	ALT3
	SAI1_TX_DATA5	SAI1_TXD5	ALT0
		SAI5_RXD3	ALT1
	SAI1_TX_DATA6	SAI1_TXD6	ALT0
	SAI1_TX_DATA7	SAI1_TXD7	ALT0
	SAI1_TX_SYNC	SAI1_TXFS	ALT0
		SAI5_RXD1	ALT2
		SAI5_RXD2	ALT2
		SAI5_RXD3	ALT2
		SAI1_RXD7	ALT2
SAI2	SAI2_MCLK	SAI2_MCLK	ALT0
	SAI2_RX_BCLK	SAI2_RXC	ALT0
	SAI2_RX_DATA0	SAI2_RXD0	ALT0
	SAI2_RX_DATA1	SAI3_RXFS	ALT1
		SAI2_RXFS	ALT3
	SAI2_RX_DATA2	SAI3_RXC	ALT1
	SAI2_RX_DATA3	SAI3_RXD	ALT1
	SAI2_RX_SYNC	SAI2_RXFS	ALT0
	SAI2_TX_BCLK	SAI2_TXC	ALT0
	SAI2_TX_DATA0	SAI2_TXD0	ALT0
	SAI2_TX_DATA1	SAI3_TXFS	ALT1
		SAI2_RXD0	ALT3
		SAI2_TXFS	ALT3
	SAI2_TX_DATA2	SAI3_TXC	ALT1
	SAI2_TX_DATA3	SAI3_TXD	ALT1
	SAI2_TX_SYNC	SAI2_TXFS	ALT0
SAI3	SAI3_MCLK	SAI3_MCLK	ALT0
		NAND_DQS	ALT2
		SAI2_MCLK	ALT6
	SAI3_RX_BCLK	SAI3_RXC	ALT0
	SAI3_RX_DATA0	SAI3_RXD	ALT0
		NAND_DATA00	ALT2
	SAI3_RX_DATA1	SAI3_RXFS	ALT3
	SAI3_RX_SYNC	SAI3_RXFS	ALT0
	SAI3_TX_BCLK	SAI3_TXC	ALT0

Table continues on the next page...

Instance	Port	Pad	Mode
		NAND_ALE	ALT2
	SAI3_TX_DATA0	SAI3_TXD	ALT0
		NAND_CE0_B	ALT2
	SAI3_TX_DATA1	SAI3_TXFS	ALT3
	SAI3_TX_SYNC	SAI3_TXFS	ALT0
		NAND_DATA01	ALT2
SAI5	SAI5_MCLK	SAI5_MCLK	ALT0
		SAI2_MCLK	ALT1
		SAI3_MCLK	ALT2
	SAI5_RX_BCLK	SAI5_RXC	ALT0
		SAI3_RXC	ALT2
	SAI5_RX_DATA0	SAI5_RXD0	ALT0
		SAI3_RXD	ALT2
	SAI5_RX_DATA1	SAI5_RXD1	ALT0
		SAI3_TXFS	ALT2
	SAI5_RX_DATA2	SAI5_RXD2	ALT0
		SAI3_TXC	ALT2
	SAI5_RX_DATA3	SAI5_RXD3	ALT0
		SAI3_TXD	ALT2
	SAI5_RX_SYNC	SAI5_RXFS	ALT0
		SAI3_RXFS	ALT2
	SAI5_TX_BCLK	SAI2_RXC	ALT1
		SAI5_RXD2	ALT3
	SAI5_TX_DATA0	SAI2_RXD0	ALT1
		SAI5_RXD3	ALT3
	SAI5_TX_DATA1	SAI2_TXFS	ALT1
		SAI2_RXFS	ALT2
	SAI5_TX_DATA2	SAI2_TXC	ALT1
	SAI5_TX_DATA3	SAI2_TXD0	ALT1
	SAI5_TX_SYNC	SAI2_RXFS	ALT1
		SAI5_RXD1	ALT3
SAI6	SAI6_MCLK	SAI1_RXD7	ALT1
		SAI1_TXD7	ALT1
		ENET_TX_CTL	ALT2
	SAI6_RX_BCLK	SAI1_TXD4	ALT1
		ENET_TD0	ALT2
		SAI1_RXD4	ALT2
	SAI6_RX_DATA0	SAI1_TXD5	ALT1
		ENET_TD2	ALT2
		SAI1_RXD5	ALT2
	SAI6_RX_SYNC	SAI1_TXD6	ALT1

Table continues on the next page...

Instance	Port	Pad	Mode
		ENET_TD1	ALT2
		SAI1_RXD6	ALT2
	SAI6_TX_BCLK	SAI1_RXD4	ALT1
		ENET_TD3	ALT2
		SAI1_TXD4	ALT2
	SAI6_TX_DATA0	SAI1_RXD5	ALT1
		ENET_MDC	ALT2
		SAI1_TXD5	ALT2
	SAI6_TX_SYNC	SAI1_RXD6	ALT1
		ENET_MDIO	ALT2
		SAI1_TXD6	ALT2
SAI7	SAI7_MCLK	ENET_RD3	ALT2
		ECSPI2_MISO	ALT3
	SAI7_RX_BCLK	ENET_RD2	ALT2
		ECSPI1_MOSI	ALT3
	SAI7_RX_DATA0	ENET_RD0	ALT2
		ECSPI1_MISO	ALT3
	SAI7_RX_SYNC	ENET_RD1	ALT2
		ECSPI1_SCLK	ALT3
	SAI7_TX_BCLK	ENET_RXC	ALT2
		ECSPI2_SCLK	ALT3
	SAI7_TX_DATA0	ENET_TXC	ALT2
		ECSPI2_MOSI	ALT3
	SAI7_TX_SYNC	ENET_RX_CTL	ALT2
		ECSPI1_SS0	ALT3
SDMA1	SDMA1_EXT_EVENT0	GPIO1_IO03	ALT5
	SDMA1_EXT_EVENT1	GPIO1_IO04	ALT5
SDMA2	SDMA2_EXT_EVENT0	GPIO1_IO09	ALT5
	SDMA2_EXT_EVENT1	GPIO1_IO12	ALT5
SJC	SJC_DE_B	GPIO1_IO02	ALT7
SNVS	SNVS_ONOFF	ONOFF	ALT0
	SNVS_PMIC_ON_REQ	PMIC_ON_REQ	ALT0
	SNVS_POR_B	POR_B	ALT0
	SNVS_RTC	RTC_XTALI	ALT0
SPDIF1	SPDIF1_EXT_CLK	SPDIF_EXT_CLK	ALT0
		SAI3_TXD	ALT4
	SPDIF1_IN	SPDIF_RX	ALT0
		ENET_RD3	ALT3
		SD2_DATA3	ALT3
		SAI3_RXFS	ALT4
		SAI3_MCLK	ALT6

Table continues on the next page...

Instance	Port	Pad	Mode
	SPDIF1_OUT	SPDIF_TX	ALT0
		ENET_TX_CTL	ALT3
		SD2_DATA2	ALT3
		SAI3_MCLK	ALT4
SRC	SRC_BOOT_MODE0	BOOT_MODE0	ALT0
	SRC_BOOT_MODE1	BOOT_MODE1	ALT0
	SRC_BOOT_MODE2	BOOT_MODE2	ALT0
	SRC_BOOT_MODE3	BOOT_MODE3	ALT0
UART1	UART1_CTS_B	UART3_RXD	ALT1
		SD1_DATA1	ALT4
		SAI2_TXFS	ALT4
	UART1_RTS_B	UART3_TXD	ALT1
		SD1_DATA0	ALT4
		SAI2_RXD0	ALT4
	UART1_RX	UART1_RXD	ALT0
		SD1_CMD	ALT4
		SAI2_RXC	ALT4
	UART1_TX	UART1_TXD	ALT0
		SD1_CLK	ALT4
		SAI2_RXFS	ALT4
UART2	UART2_CTS_B	UART4_RXD	ALT1
		SD1_DATA5	ALT4
		SAI3_RXC	ALT4
	UART2_RTS_B	UART4_TXD	ALT1
		SD1_DATA4	ALT4
		SAI3_RXD	ALT4
	UART2_RX	UART2_RXD	ALT0
		SD2_DATA0	ALT3
		SD1_DATA3	ALT4
		SAI3_TXFS	ALT4
	UART2_TX	UART2_TXD	ALT0
		SD2_DATA1	ALT3
		SD1_DATA2	ALT4
		SAI3_TXC	ALT4
UART3	UART3_CTS_B	ECSPI1_MISO	ALT1
		SD1_STROBE	ALT4
	UART3_RTS_B	ECSPI1_SS0	ALT1
		SD1_RESET_B	ALT4
	UART3_RX	UART3_RXD	ALT0
		ECSPI1_SCLK	ALT1
		SD1_DATA7	ALT4

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Instance	Port	Pad	Mode
		NAND_ALE	ALT4
	UART3_TX	UART3_TXD	ALT0
		ECSPI1_MOSI	ALT1
		SD1_DATA6	ALT4
		NAND_CE0_B	ALT4
UART4	UART4_CTS_B	ECSPI2_MISO	ALT1
		NAND_DATA02	ALT3
	UART4_RTS_B	ECSPI2_SS0	ALT1
		NAND_DATA03	ALT3
	UART4_RX	UART4_RXD	ALT0
		ECSPI2_SCLK	ALT1
		SD2_CLK	ALT3
		NAND_CLE	ALT4
		NAND_DATA00	ALT4
	UART4_TX	UART4_TXD	ALT0
		ECSPI2_MOSI	ALT1
		SD2_CMD	ALT3
		NAND_DATA01	ALT4
		NAND_RE_B	ALT4
USB1	USB1_ID	GPIO1_IO10	ALT1
	USB1_OC	GPIO1_IO13	ALT1
	USB1_PWR	GPIO1_IO12	ALT1
	USB1_DN	USB1_D_N	No muxing
	USB1_DP	USB1_D_P	No muxing
	USB1_RESREF	USB1_TXRTUNE	No muxing
	USB1_RX_N	USB1_RX_N	No muxing
	USB1_RX_P	USB1_RX_P	No muxing
	USB1_TX_N	USB1_TX_N	No muxing
	USB1_TX_P	USB1_TX_P	No muxing
	USB1_VBUS	USB1_VBUS	No muxing
USB2	USB2_ID	GPIO1_IO11	ALT1
	USB2_OC	GPIO1_IO15	ALT1
	USB2_PWR	GPIO1_IO14	ALT1
	USB2_DN	USB2_D_N	No muxing
	USB2_DP	USB2_D_P	No muxing
	USB2_RESREF	USB2_TXRTUNE	No muxing
	USB2_RX_N	USB2_RX_N	No muxing
	USB2_RX_P	USB2_RX_P	No muxing
	USB2_TX_N	USB2_TX_N	No muxing
	USB2_TX_P	USB2_TX_P	No muxing
	USB2_VBUS	USB2_VBUS	No muxing

Table continues on the next page...

Instance	Port	Pad	Mode
USDHC1	USDHC1_CD_B	GPIO1_IO06	ALT5
	USDHC1_CLK	SD1_CLK	ALT0
	USDHC1_CMD	SD1_CMD	ALT0
	USDHC1_DATA0	SD1_DATA0	ALT0
	USDHC1_DATA1	SD1_DATA1	ALT0
	USDHC1_DATA2	SD1_DATA2	ALT0
	USDHC1_DATA3	SD1_DATA3	ALT0
	USDHC1_DATA4	SD1_DATA4	ALT0
	USDHC1_DATA5	SD1_DATA5	ALT0
	USDHC1_DATA6	SD1_DATA6	ALT0
	USDHC1_DATA7	SD1_DATA7	ALT0
	USDHC1_RESET_B	SD1_RESET_B	ALT0
	USDHC1_STROBE	SD1_STROBE	ALT0
	USDHC1_VSELECT	GPIO1_IO03	ALT1
	USDHC1_WP	GPIO1_IO07	ALT5
USDHC2	USDHC2_CD_B	SD2_CD_B	ALT0
	USDHC2_CLK	SD2_CLK	ALT0
	USDHC2_CMD	SD2_CMD	ALT0
	USDHC2_DATA0	SD2_DATA0	ALT0
	USDHC2_DATA1	SD2_DATA1	ALT0
	USDHC2_DATA2	SD2_DATA2	ALT0
	USDHC2_DATA3	SD2_DATA3	ALT0
	USDHC2_RESET_B	SD2_RESET_B	ALT0
		GPIO1_IO08	ALT5
	USDHC2_VSELECT	GPIO1_IO04	ALT1
	USDHC2_WP	SD2_WP	ALT0
USDHC3	USDHC3_CD_B	NAND_DATA02	ALT2
		I2C2_SCL	ALT2
		GPIO1_IO14	ALT4
		ENET_TD1	ALT6
	USDHC3_CLK	NAND_WE_B	ALT2
		ENET_RD2	ALT6
	USDHC3_CMD	NAND_WP_B	ALT2
		ENET_RD3	ALT6
	USDHC3_DATA0	NAND_DATA04	ALT2
		ENET_TX_CTL	ALT6
	USDHC3_DATA1	NAND_DATA05	ALT2
		ENET_TXC	ALT6
	USDHC3_DATA2	NAND_DATA06	ALT2
		ENET_RX_CTL	ALT6
	USDHC3_DATA3	NAND_DATA07	ALT2

Table continues on the next page...

Instance	Port	Pad	Mode
		ENET_RXC	ALT6
	USDHC3_DATA4	NAND_RE_B	ALT2
		ENET_RD0	ALT6
	USDHC3_DATA5	NAND_CE2_B	ALT2
		ENET_MDIO	ALT6
	USDHC3_DATA6	NAND_CE3_B	ALT2
		ENET_TD3	ALT6
	USDHC3_DATA7	NAND_CLE	ALT2
		ENET_TD2	ALT6
	USDHC3_RESET_B	NAND_READY_B	ALT2
		UART3_RXD	ALT2
		GPIO1_IO09	ALT4
		ENET_RD1	ALT6
	USDHC3_STROBE	NAND_CE1_B	ALT2
		ENET_MDC	ALT6
	USDHC3_VSELECT	UART3_TXD	ALT2
		GPIO1_IO11	ALT4
	USDHC3_WP	NAND_DATA03	ALT2
		I2C2_SDA	ALT2
		GPIO1_IO15	ALT4
		ENET_TD0	ALT6
WDOG1	WDOG1_WDOG_ANY	GPIO1_IO02	ALT5
	WDOG1_WDOG_B	GPIO1_IO02	ALT1
XTALOSC	XTALI_24M	XTALI_24M	No Muxing
	XTALO_24M	XTALO_24M	No Muxing

8.2 IOMUX Controller (IOMUXC)

8.2.1 Overview

The IOMUX Controller (IOMUXC), together with the IOMUX, enables the IC to share one pad to several functional blocks. This sharing is done by multiplexing the pad's input and output signals.

Every module requires a specific pad setting (such as pull up or keeper), and for each pad, there are up to 8 muxing options (called ALT modes). The pad settings parameters are controlled by the IOMUXC.

The IOMUX consists only of combinatorial logic combined from several basic IOMUX cells. Each basic IOMUX cell handles only one pad signal's muxing.

Figure 8-1 illustrates the IOMUX/IOMUXC connectivity in the system.

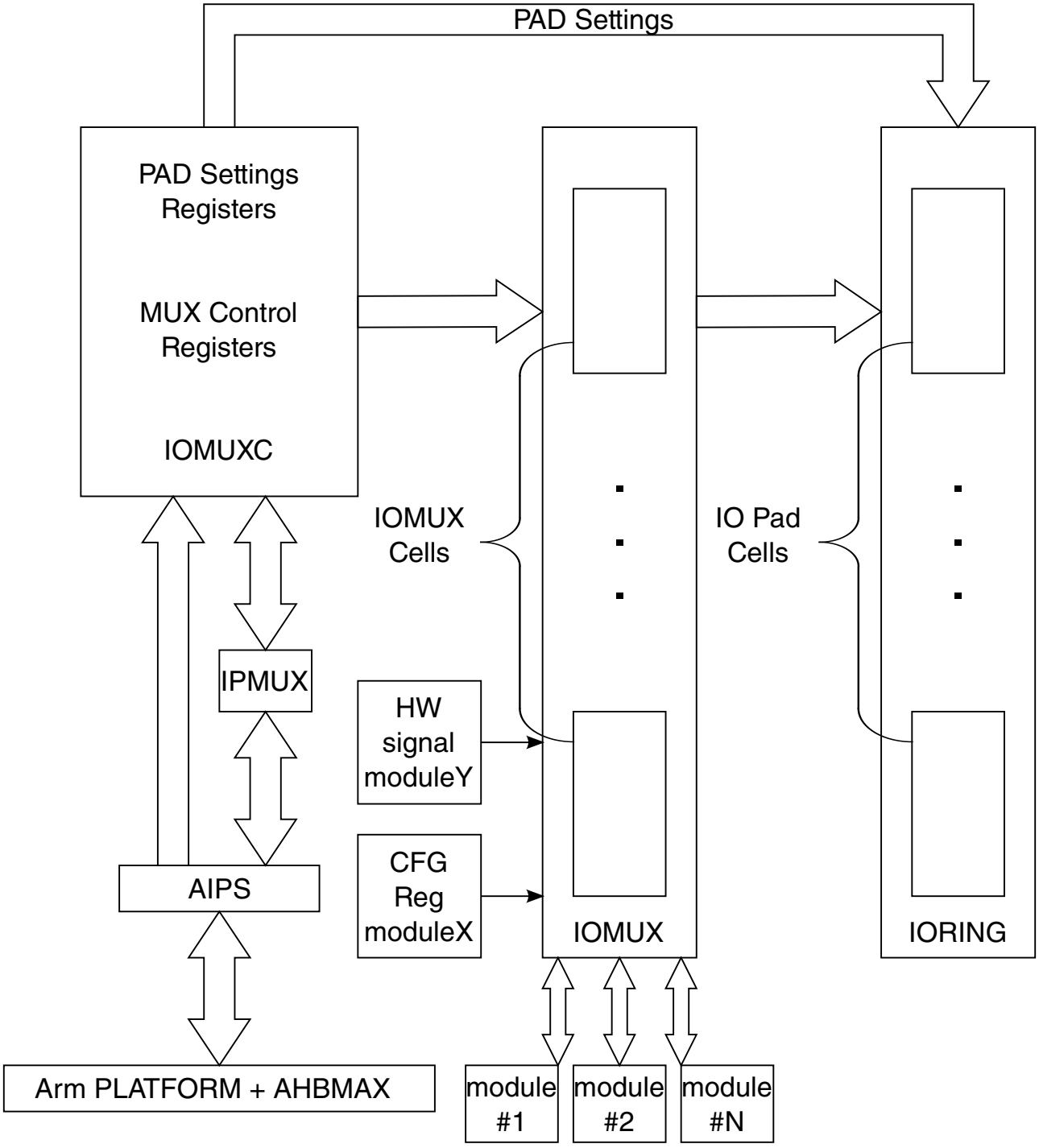

Figure 8-1. IOMUX SoC Level Block Diagram

8.2.1.1 Block Diagram

The high level illustration of the IO cells is shown in Figure 8-3

8.2.1.2 Features

The IOMUXC features include:

- 32-bit software mux control registers (IOMUXC_SW_MUX_CTL_PAD_<PAD NAME> or IOMUXC_SW_MUX_CTL_GRP_<GROUP NAME>) to configure 1 of 8 alternate (ALT) MUX_MODE fields of each pad or a predefined group of pads and to enable the forcing of an input path of the pad(s) (SION bit).
- 32-bit software pad control registers (IOMUXC_SW_PAD_CTL_PAD_<PAD_NAME> or IOMUXC_SW_PAD_CTL_GRP_<GROUP NAME>) to configure specific pad settings of each pad, or a predefined group of pads.
- 32-bit general purpose registers - several (GPR0 to GPR*n*) 32-bit registers according to SoC requirements for any usage.
- 32-bit input select control registers to control the input path to a module when more than one pad drives this module input.

Each SW MUX/PAD CTL IOMUXC register handles only one pad or one pad's group.

Only the minimum number of registers required by software are implemented by hardware. For example, if only ALT0 and ALT1 modes are used on Pad x then only one bit register will be generated as the MUX_MODE control field in the software mux control register of Pad x.

The software mux control registers may allow the forcing of pads to become input (input path enabled) regardless of the functional direction driven. This may be useful for loopback and GPIO data capture.

8.2.2 Functional description

This section provides a complete functional description of the block.

The IOMUXC consists of two sub-blocks:

- IOMUXC_REGISTERS includes all of the IOMUXC registers (see Features).
- IOMUXC_LOGIC includes all of the IOMUXC combinatorial logic (IP interface controls, address decoder, observability muxes).

The IOMUX consists of a number (about the number of pads in the SoC) of basic iomux_cell units. If only one functional mode is required for a specific pad, there is no need for IOMUX and the signals can be connected directly from the module to the I/O. The IOMUX cell is required whenever two or more functional modes are required for a specific pad or when one functional mode and the one test mode are required.

The basic iomux_cell design, which allows two levels of HW signal control (in ALT6 and ALT7 modes - ALT7 gets highest priority) is shown in Figure 8-2.

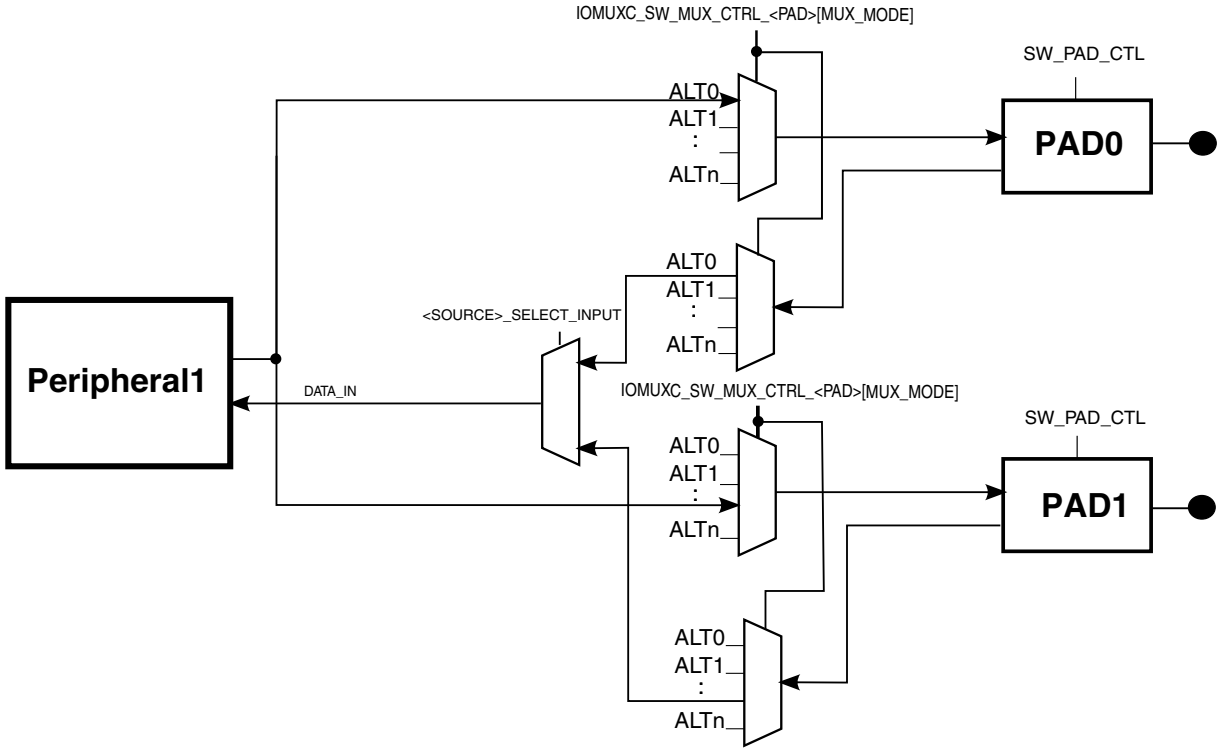

Figure 8-2. IOMUX Cell Block Diagram

8.2.2.1 GPIO pad features

The GPIO pad includes the following features:

- Wide-range voltage interface
  - 1.8V ~ 3.3V I/O interface
- CMOS input / Schmitt trigger Input
- 3-state and open-drain output
- Two slew rate control levels
- Programmable feature support
  - Controllable input enable

- Controllable CMOS/Schmitt trigger input
- Controllable pull-up/pull-down resistor
- Controllable output drive strength (x1 / x2 / x4 / x6)
- Controllable slew rate control (slow slew / fast slew)

8.2.2.1.1 Pull up/Pull down control

Pull up/Pull down function is controlled by the PE and PS pin.

Table 8-1. Pull up / Pull down control truth table

Mode	State	
	PE	PS
Disable	0	X
Pull-down enable	1	0
Pull-up enable	1	1

8.2.2.1.2 Input control

The IS pin selects CMOS and Schmitt trigger.

Table 8-2. Input control truth table

Mode	State	
	IE	IS
Disable	0	X
CMOS input	1	0
Schmitt trigger input	1	1

8.2.2.1.3 Output driver control

Output drive strength is controlled by the DS0, DS1 pin.

Table 8-3. Drive strength control truth table

State		Driver Strength
DS1	DS0	
0	0	X1
1	0	X2
0	1	X4
1	1	X6

The SR pin controls slew-rate of output driver.

Table 8-4. Slew-rate of output driver

State	Driver Slew
SR	
0	Fast Slew
1	Slow Slew

8.2.2.2 ALT6 and ALT7 extended muxing modes

The ALT7 and ALT6 extended muxing modes allow any signal in the system (such as fuse, pad input, JTAG, or software register) to override any software configuration and to force the ALT6/ALT7 muxing mode.

It also allows an IOMUX software register to control a group of pads.

8.2.2.3 SW Loopback through SION bit

A limited option exists to override the default pad functionality and force the input path to be active (ipp_ibe==1'b1) regardless of the value driven by the corresponding module. This can be done by setting the SION (Software Input On) bit in the IOMUXC_SW_MUX_CTL register (when available) to "1".

Uses include:

- LoopBack - Module x drives the pad and also receives pad value as an input.
- GPIO Capture - Module x drives the pad and the value is captured by GPIO.

8.2.2.4 Daisy chain - multi pads driving same module input pin

In some cases, more than one pad may drive a single module input pin. Such cases require the addition of one more level of IOMUXing; all of these input signals are muxed, and a dedicated software controlled register controls the mux in order to select the required input path.

A module port involved in "daisy chain" requires two software configuration commands, one for selecting the mode for this pad (programable via the IOMUXC_SW_MUX_CTL_<PAD> registers) and one for defining it as the input path (via the daisy chain registers).

This means that a module port involved in "daisy chain" requires two software configuration commands, one for selecting the mode for this pad (programable via the IOMUXC_SW_MUX_CTL_<PAD> registers) and one for defining it as the input path (via the daisy chain registers). The daisy chain is illustrated in the figure below.

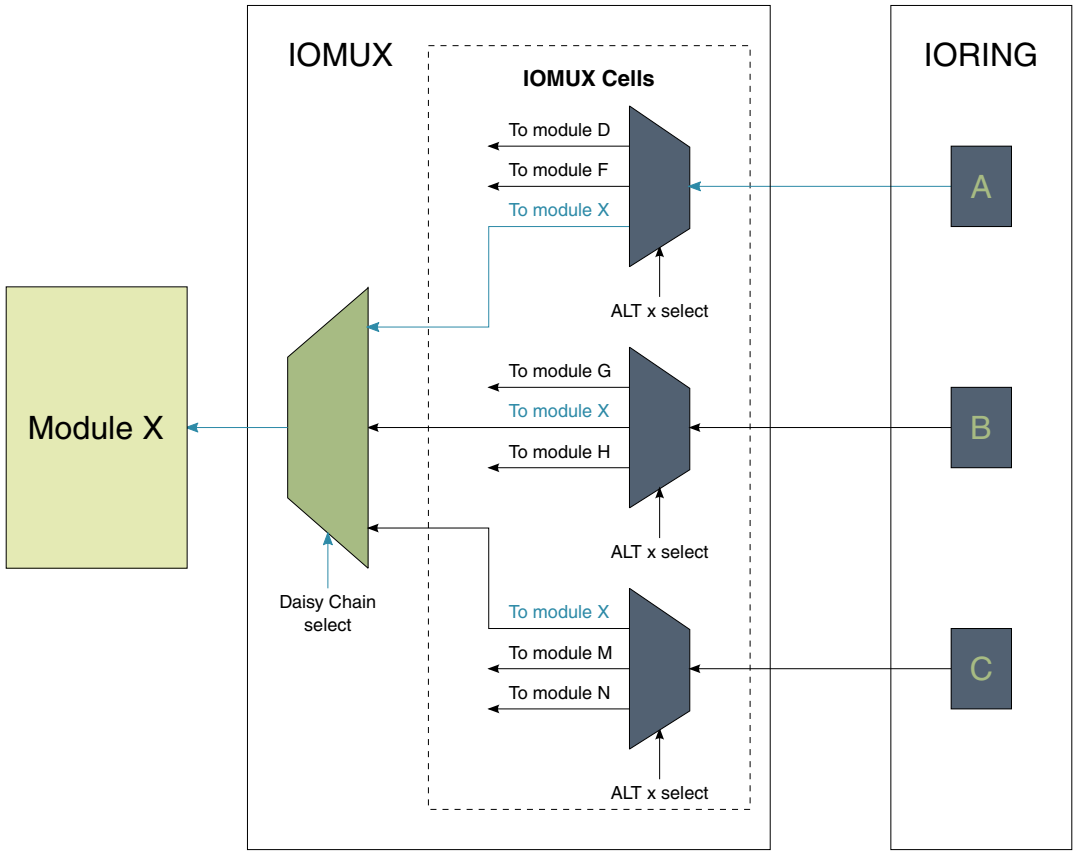

Figure 8-3. Daisy chain illustration

8.2.2.5 Clocks

The table found here describes the clock sources for IOMUXC.

Please see Clock Controller Module (CCM) for clock setting, configuration and gating information.

Table 8-5. IOMUXC Clocks

Clock name	Clock Root	Description
ipg_clk_s	ipg_clk_root	Peripheral access clock

8.2.3 IOMUXC GPR Memory Map/Register Definition

IOMUXC_GPR memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3034_0000	General Purpose Register 0 (IOMUXC_GPR_GPR0)	32	R/W	0000_0000h	8.2.3.1/ 1361
3034_0004	General Purpose Register 1 (IOMUXC_GPR_GPR1)	32	R/W	0001_0000h	8.2.3.2/ 1362
3034_0008	General Purpose Register 2 (IOMUXC_GPR_GPR2)	32	R/W	0000_0000h	8.2.3.3/ 1364
3034_000C	General Purpose Register 3 (IOMUXC_GPR_GPR3)	32	R/W	0000_0000h	8.2.3.4/ 1364
3034_0010	General Purpose Register 4 (IOMUXC_GPR_GPR4)	32	R/W	0000_0000h	8.2.3.5/ 1365
3034_0014	General Purpose Register 5 (IOMUXC_GPR_GPR5)	32	R/W	0000_0000h	8.2.3.6/ 1368
3034_0018	General Purpose Register 6 (IOMUXC_GPR_GPR6)	32	R/W	0000_0000h	8.2.3.7/ 1369
3034_001C	General Purpose Register 7 (IOMUXC_GPR_GPR7)	32	R/W	0000_0000h	8.2.3.8/ 1369
3034_0020	General Purpose Register 8 (IOMUXC_GPR_GPR8)	32	R/W	0000_0000h	8.2.3.9/ 1370
3034_0024	General Purpose Register 9 (IOMUXC_GPR_GPR9)	32	R/W	0000_0000h	8.2.3.10/ 1370
3034_0028	General Purpose Register 10 (IOMUXC_GPR_GPR10)	32	R/W	0000_0008h	8.2.3.11/ 1371
3034_002C	General Purpose Register 11 (IOMUXC_GPR_GPR11)	32	R/W	0000_0200h	8.2.3.12/ 1372
3034_0030	General Purpose Register 12 (IOMUXC_GPR_GPR12)	32	R/W	0000_4000h	8.2.3.13/ 1374

Table continues on the next page...

IOMUXC_GPR memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3034_0034	General Purpose Register 13 (IOMUXC_GPR_GPR13)	32	R/W	0000_0000h	8.2.3.14/ 1375
3034_0038	General Purpose Register 14 (IOMUXC_GPR_GPR14)	32	R/W	0349_4000h	8.2.3.15/ 1377
3034_003C	General Purpose Register 15 (IOMUXC_GPR_GPR15)	32	R/W	0000_0000h	8.2.3.16/ 1378
3034_0040	General Purpose Register 16 (IOMUXC_GPR_GPR16)	32	R/W	0000_0000h	8.2.3.17/ 1379
3034_0044	General Purpose Register 17 (IOMUXC_GPR_GPR17)	32	R/W	0000_0000h	8.2.3.18/ 1380
3034_0048	General Purpose Register 18 (IOMUXC_GPR_GPR18)	32	R/W	0000_0000h	8.2.3.19/ 1380
3034_004C	General Purpose Register 19 (IOMUXC_GPR_GPR19)	32	R	See section	8.2.3.20/ 1380
3034_0050	General Purpose Register 20 (IOMUXC_GPR_GPR20)	32	R/W	0000_0000h	8.2.3.21/ 1381
3034_0054	General Purpose Register 21 (IOMUXC_GPR_GPR21)	32	R/W	See section	8.2.3.22/ 1384
3034_0058	General Purpose Register 22 (IOMUXC_GPR_GPR22)	32	R/W	0000_0001h	8.2.3.23/ 1386
3034_005C	General Purpose Register 23 (IOMUXC_GPR_GPR23)	32	R/W	0000_0000h	8.2.3.24/ 1388
3034_0060	General Purpose Register 24 (IOMUXC_GPR_GPR24)	32	R	See section	8.2.3.25/ 1388

8.2.3.1 General Purpose Register 0 (IOMUXC_GPR_GPR0)

Address: 3034_0000h base + 0h offset = 3034_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

IOMUXC_GPR_GPR0 field descriptions

Field	Description
-	This field is reserved.