M.2 Key B Expansion Module

Features:

- 1 Lane PCIe (PExx0)
- USB 3.0 data multiplexed (USB2/Host, PExx1)
- USB 2.0 data multiplexed (USB2/Host)
- GNSS / Stem I2C (I2C3)
- MFG I2C (SYS I2C)
- AUDIO I2S MIC SAI5 4 channels (GPIO5..8 and COEX*)
- SPI (ANTCTL*)
- DAS/DSS broken out with activity LED + expander bit
- Additional signals via 16 bit I/O Expander
- Some are broken out with pads near connector (CONFIG 0/2/3, DPR)
- SIM pins are not connected, reserved for now
- 4 channel I2S stereo input
- 4 channel I2S stereo output

The USB2 data from the Systems Module is connected through the multiplexer to T-USB on boot. The multiplexer can switch it to the M.2 expansion USB pins. This is important as the USB 3.0 data pairs are connected to what can also be used for a second PCIe lane. The USB data signals from SoM are multiplexed between T-USB Host (USB2) and M.2 Key B based on MUX_USB2_SEL & MUX_USB3_SEL.

Be aware the current pin plan is not final. Input/Ouput such as DIN/DOUT RXD/TXD may be the wrong way around. It must be verified with reference hardware design/testing.

According to documentation: Type refers to the signal direction: • Type O means signal is an output from the MPU/MCU to the adapter. • Type I means signals is an input to the MPU/MCU from the adapter.

Control pins mapped by I/O Expander

Some extra M.2 pins are connected to I/O Expanders 4 and 6 to allow controlling the state of the inserted module. Muxing the USB2 signals between m.2 Key B and the T-USB Module is controlled by I/O Expander 0. Also, there will be no fastening screw for the m.2 board.

The system I/O expander controls mPCIe_PERST which resets PCIe. PCIE_CLKREQ_B is a direct pin on the SoM. PCIE_WAKE_B is a direct pin on the SoM.

(?) Consider bootup default state of I/O Expanders. USB must not connect M.2 by default

(?) A future revision may connect unallocated/GPIO pins from chipsets to M.2 module

Expander 4

This 919 EX4 Faceboard sensor I/O Expander is placed on faceboard and controlled via the Stem I2C.

- LED Controller
- Motion Sensor

- Sound Sensor
- Nighttime camera attached sensors
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The EX4 expander input triggers interrupt via STEM_INT.

Expander	Connected to
EX4.3	IMU_INTM - MC6470 INTM
EX4.4	IMU_IRQ - MC6470 INTA / Motion Controller
EX4.5	IMU_RESETN - Motion Controller
EX4.6	IMU_MODE - Motion Controller
EX4.7	LED_SHUTDOWN - SDB
EX4.8	MIC VM3011 DOUT
EX4.9	W_DISABLE2# on m.2 Key E
EX4.10	W_DISABLE1# on m.2 Key E
EX4.11	M2E_PWROFF on m.2 Key E
EX4.12	M2B_PWROFF on m.2 Key B
EX4.13	DEVSLP 3V3 on m.2 Key B
EX4.14	RIGHT_ATT_INT
EX4.15	RIGHT_ATT_XSHUT

I/O Expander to cover m.2 Expander (Stem I2C). Some sensor pins not connected.

Expander 6

The 919 EX6 expander is used for testing m.2 signals on Key B and Key E. It is on the SYS I2C bus. Pins on Key B are prefixed with B_. Pins on Key E are prefixed with E_.

The EX6 expander input triggers interrupt via EX0_nINT (GPIO4_IO19).

Expander	Connected to
EX6.0	E_COEX4
EX6.1	E_DEV_WLAN_WAKE
EX6.2	E_ALERT / I2C_IRQ
EX6.3	E_LED / DAS / DSS
EX6.4	E_UART WAKE
EX6.5	E_SDIO WAKE

Expander	Connected to
EX6.6	E_LED2#
EX6.8	B_RESET#
EX6.9	B_ALERT / I2C_IRQ
EX6.10	B_LED / DAS / DSS
EX6.11	B_CONFIG_1

I/O Expander to cover m.2 Expander (SYS I2C)

Key B - pinouts

M.2 Key B Pin allocations

Pin id.	Upper	Lower	Description	Counterpoint	Voltage Level
1	CONFIG_3		Defines Module Type	pad	
2		+3.3V	3.3 V power supply from main board		3.3V
3	GND		Ground		GND
4		+3.3V	3.3 V power supply from main board		3.3V
5	GND		Ground (available?)		GND
6		M2B_PWROFF	Card PWR OFF	EX2.5	1.8/3.3
7	USB D+		USB data pair positive USB D+	USB D+	
8		W_DIS1	Wireless disable 1	EXB.3	
9	USB D-		USB data pair negative USB D-	USB D-	
10		DAS/DSS	Device Actvty Signal	LED / EX2.9	3.3V
11	GND		Ground (available?)		GND
12 - 19					
20		M2_I2S_CLK	GPIO5 M2_I2S_CLK	MIC I2S	1.8V
21	CONFIG_0			pad	
22		M2_I2S_DIN	GPIO6 M2_I2S_DIN	MIC I2S DATA0	1.8V
23	GPIO11		NC	MIC I2S MCLK	1.8V

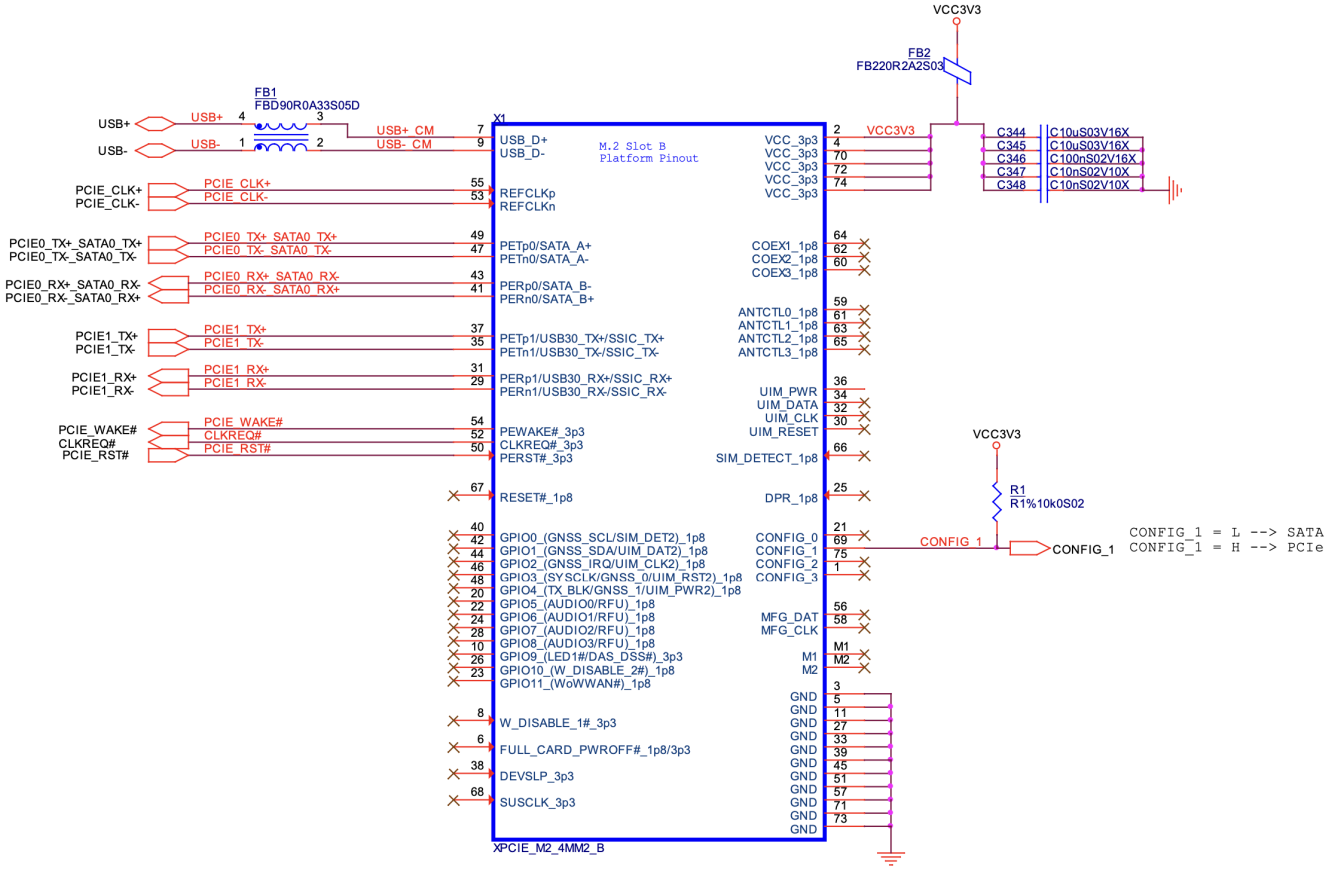
Pin id.	Upper	Lower	Description	Counterpoint	Voltage Level
24		M2_I2S_DOUT	GPIO7 M2_I2S_DOUT	SPK I2S DATA0	1.8V
25	DPR			pad	
26		GPIO10		EX2.10	1.8V
27	GND		Ground		GND
28		M2_I2S_WS	GPIO8 M2_I2S_WS	MIC I2S WS	1.8V
29	USB3 RX-		PER-1 / SSIC M2_USB3_SSRXN	M2_USB3_SSRX-	
30		SIM_RST	UIM RESET	-	
31	USB3 RX+		PER+1 / SSIC M2_USB3_SSRXP	M2_USB3_SSRX+	
32		SIM_CLK	UIM CLK	-	
33	GND		Ground		GND
34		SIM_DATA	UIM DATA	-	
35	USB3 TX-		PET-1 / SSIC M2_USB3_SSTX-	M2_USB3_SSTX-	
36		SIM_PWR	UIM PWR	-	
37	USB3 TX+		PET+2 / SSIC M2_USB3_SSTX+	M2_USB3_SSTX+	
38		DEVSLP	Device Sleep, input. high=sleep	EX2.12	3.3V
39	GND		Ground		GND
40		M2 SMB SCL	SMB_CLK M2 SMB SCL	I2C3 SCL	1.8V
41	PCIE RXN-		PCIE RXN- / PER-0 / SATA-B+	PCIE RXN-	
42		M2 SMB SDA	SMB_DATA M2 SMB SDA	I2C3 SDA	1.8V
43	PCIE RXN+		PCIE RXN+ / PER+0 / SATA-B-	PCIE RXN+	1.8V
44		GPIO2	GPIO2 / ALERT	EX2.7	1.8V
45	GND		Ground		GND
46		GPIO3		PWM2_OUT	1.8V
47	PCIE TXN-		PCIE TXN- / PET-0 / SATA-A-	PCIE TXN-	1.8V
48		GPIO4		PWM3_OUT	1.8V

Pin id.	Upper	Lower	Description	Counterpoint	Voltage Level
49	PCIE TXN+		PCIE TXN+ / PET-0 / SATA-A+	PCIE TXN+	1.8V
50		PERST	PCI Reset	mPCIe_PERST	
51	GND		Ground		GND
52		CLKREQ	Reference clock request	PCIE_CLKREQ_B	3.3V
53	PCIE REFCLK-		PCIE REFCLK-	REFCLK-	
54		WAKE	PCIe WAKE# Active Low.	PCIE_WAKE_B	
55	PCIE REFCLK+		PCIE REFCLK+	REFCLK+	
56		MFG_DAT	SDA	SYS I2C SDA	
57	GND		Ground		
58		MFG_CLK	SCL	SYS I2C SCL	
59	ANTCTL0			ECSPI2_MISO	
60		COEX3		MIC I2S DATA3	
61	ANTCTL1			ECSPI2_SS0	
62		COEX_TXD		MIC I2S DATA2	1.8V
63	ANTCTL2			ECSPI2_SCLK	
64		COEX_RXD		MIC I2S DATA1	1.8V
65	ANTCTL3			ECSPI2_MOSI	
66		SIM DETECT	SIM CD	-	
67	RESET#		RESET	EX2.6	1.8V
68		SUSCLK	32.768 kHz provided by Platform	-	
69	CONFIG_1		Defines module type +	EX2.14	
70		VRES	Power VRES		+3.3V
71	GND		Ground		GND
72		VRES	Power VRES		+3.3V
73	GND		Ground		GND
74		VRES	Power VRES		+3.3V
75	CONFIG_2		Defines Module Type NC		

I2C3 replaced with I2C6

Key B - Reference Design

3.2 Reference Design



Congatec reference design