Ziloo Expansion Connectors

Ziloo has an M.2 type B expansion port for SSD utility cards, and a type E expansion port for Wireless utility cards. Additional future expation ports are a 40 pin GPIO, uSIM / eSIM, Speakers, Microphones.

40 pins GPIO Header

The GPIO header is made to be compatible with RPi expansion hardware. It has fewer GND pins which are mapped to GPIO or receiving pins.

Features:

- Spare GPIOs
- SPI Image Boot
- Power 5V / 3V3 / 1V8 / RTC
- SPI / SAI7 I2S Out
- Stem and System I2C
- UART1 / UART3
- PWM1..3

Left side	**Function**	**Pin**	**Pin**	**Function**	**Right side**
	3V3	1	2	5V	
I2C3_SDA / GPIO5_IO19	SDA 3	3	4	5V	
I2C3_SCL / GPIO5_IO18	SCL 3	5	6	GND	
ETH0_MDI2P / SAI7_TX_SYNC	SAI7 SYNC	7	8	TxD	UART1 TxD / GPIO5_IO23
	GND	9	10	RxD	UART1 RxD / GPIO5_IO22
EX_H_nINT / GPIO1_IO0	GPIO1_IO0	11	12	GPIO1_01	GPIO1_01 / EX_O_nINT
EX0_nINT / GPIO4_IO19	GPIO4_IO19	13	14	GPIO2_IO19	
	GPIO2_IO8	15	16	GPIO4_IO16	
Powering suspended	VCC_RTC	17	18	GPIO4_IO17	
ECSPI2_MOSI / GPIO5_IO11	MOSI	19	20	GND	
ECSPI2_MISO / GPIO5_IO12	MISO	21	22	GPIO1_IO19	
ECSPI2_MOSI / GPIO5_IO10	SCLK	23	24	SPI CE0	ECSPI2_SS0 / GPIO5_IO13
	GPIO2_IO9	25	26	QSPI BOOT	QSPI_BOOT_EN_3P3
SYS I2C	SYS SDA	27	28	SYS SCL	SYS I2C

Left side	Function	Pin	Pin	Function	Right side
UART3_TXD / GPIO5_IO27	UART3_TXD	29	30	GPIO5_IO26	UART3_RXD / GPIO5_IO26
GPIO5_IO4	PWM2	31	32	PWM3	GPIO5_IO3
GPIO5_IO5	PWM1	33	34	CAN1_RX	GPIO4_IO25 (RPi GND)
UART2_RXD / GPIO5_IO24	GPIO5_IO24	35	36	CAN1_TX	GPIO4_IO22
UART2_TXD / GPIO5_IO25	GPIO5_IO25	37	38	CAN2_RX	GPIO4_IO27
	GND	39	40	CAN2_TX	GPIO4_IO26

Sound Connector

It is not yet defined if the signal level is 1.8V or 3.3V. It will depend on NVCC_SAI5 The pin layout wraps around aligning 1 and 20 close, but on opposite sides.

Two Connector components used are DF40HC(3.5)-20DS-0.4V(51). Socket @ Mouser

Pin	Code	Function	Description
1	GND		
2	SAI5_MCLK	SAI5_MCLK	Master Clock
3	SPK_BCLK	SAI5_TXC	I2S BCLK / SCK
4	SPK_LRCLK	SAI5_TXFS	I2S LRCLK
5	SPK_DATA0	SAI5_TXD0	I2S DATA
6	SPK_DATA1	SAI5_TXD1	I2S DATA
7	SPK_DATA2	SAI5_TXD2	I2S DATA
8	SPK_DATA3	SAI5_TXD3	I2S DATA
9	VIN	1V8 / 3V3	Power at signal level
10	3V3	3V3	Power
11	MIC_BCLK	SAI5_RXC	I2S BCLK / SCK
12	MIC_LRCLK	SAI5_RXFS	I2S LRCLK
13	MIC_DATA0	SAI5_RXD0	I2S DATA
14	MIC_DATA1	SAI5_RXD1	I2S DATA
15	MIC_DATA2	SAI5_RXD2	I2S DATA
16	MIC_DATA3	SAI5_RXD3	I2S DATA
17	SCL	I2C3_SCL	I2C

Pin	Code	Function	Description
18	SDA	I2C3_SDA	I2C
19	Reserved		
20	GND	GND	Power

M.2 Key B Expansion Module

Features:

- 1 Lane PCIe (PExx0)
- USB 3.0 data multiplexed (USB2/Host, PExx1)
- USB 2.0 data multiplexed (USB2/Host)
- GNSS / Stem I2C (I2C3)
- MFG I2C (SYS I2C)
- AUDIO I2S MIC SAI5 4 channels (GPIO5..8 and COEX*)
- SPI (ANTCTL*)
- DAS/DSS broken out with activity LED + expander bit
- Additional signals via 16 bit I/O Expander
- Some are broken out with pads near connector (CONFIG 0/2/3, DPR)
- SIM pins are not connected, reserved for now
- 4 channel I2S stereo input
- 4 channel I2S stereo output

The USB is connected to T-USB (not the M.2 expansions) on boot to support NVMe SSD expansions by default. The USB data signals from SoM are multiplexed between T-USB Host (USB2) and M.2 Key B based on MUX_USB2_SEL & MUX_USB3_SEL.

Be aware the current pin plan is not final. Input/Ouput such as DIN/DOUT RXD/TXD may be the wrong way around. It must be verified with reference hardware design/testing.

According to documentation: Type refers to the signal direction: • Type O means signal is an output from the MPU/MCU to the adapter. • Type I means signals is an input to the MPU/MCU from the adapter.

Control pins mapped by I/O Expander

The system I/O expander controls mPCIe_PERST which resets PCIe. PCIE_CLKREQ_B is a direct pin on the SoM. USB1_SS_SEL is a direct pin on the SoM.

TODO consider bootup default state of I/O Expanders. USB must not connect M.2 by default

TODO unallocated/GPIO pins from chipsets

A dedicated I/O Expander controls addition pins on Key B.

The development board uses a single Expander. The 909 and 801 uses 3x PCA9555 to control more states.

The EX2 expander input triggers interrupt via EX_H_nINT (GPIO1_IO0). The pins relate to USB2 Host and M.2 Key B.

The EX2 expander allows controlling T-USB maps,

Expander	Connected to
EX2.0	USB_H_ALT_EN
EX2.1	USB_H_ALT_POL
EX2.2	USB_H_ALT_AMSEL
EX2.3	MUX_USB2_SEL
EX2.4	MUX_USB3_SEL
EX2.5	M2B_PWROFF
EX2.6	RESET#
EX2.7	ALERT / I2C_IRQ
EX2.8	GPIO4 on 65988 (HPD2)
EX2.9	LED / DAS / DSS
EX2.10	W_DISABLE_2#
EX2.11	W_DISABLE#
EX2.12	DEVSLP 3V3
EX2.13	
EX2.14	CONFIG_1
EX2.15	

M.2 Key B Pin allocations

M.2 Key B Pin allocations

Pin id.	Upper	Lower	Description	Counterpoint	Voltage Level
1	CONFIG_3		Defines Module Type	pad	
2		+3.3V	3.3 V power supply from main board		3.3V
3	GND		Ground		GND
4		+3.3V	3.3 V power supply from main board		3.3V
5	GND		Ground (available?)		GND

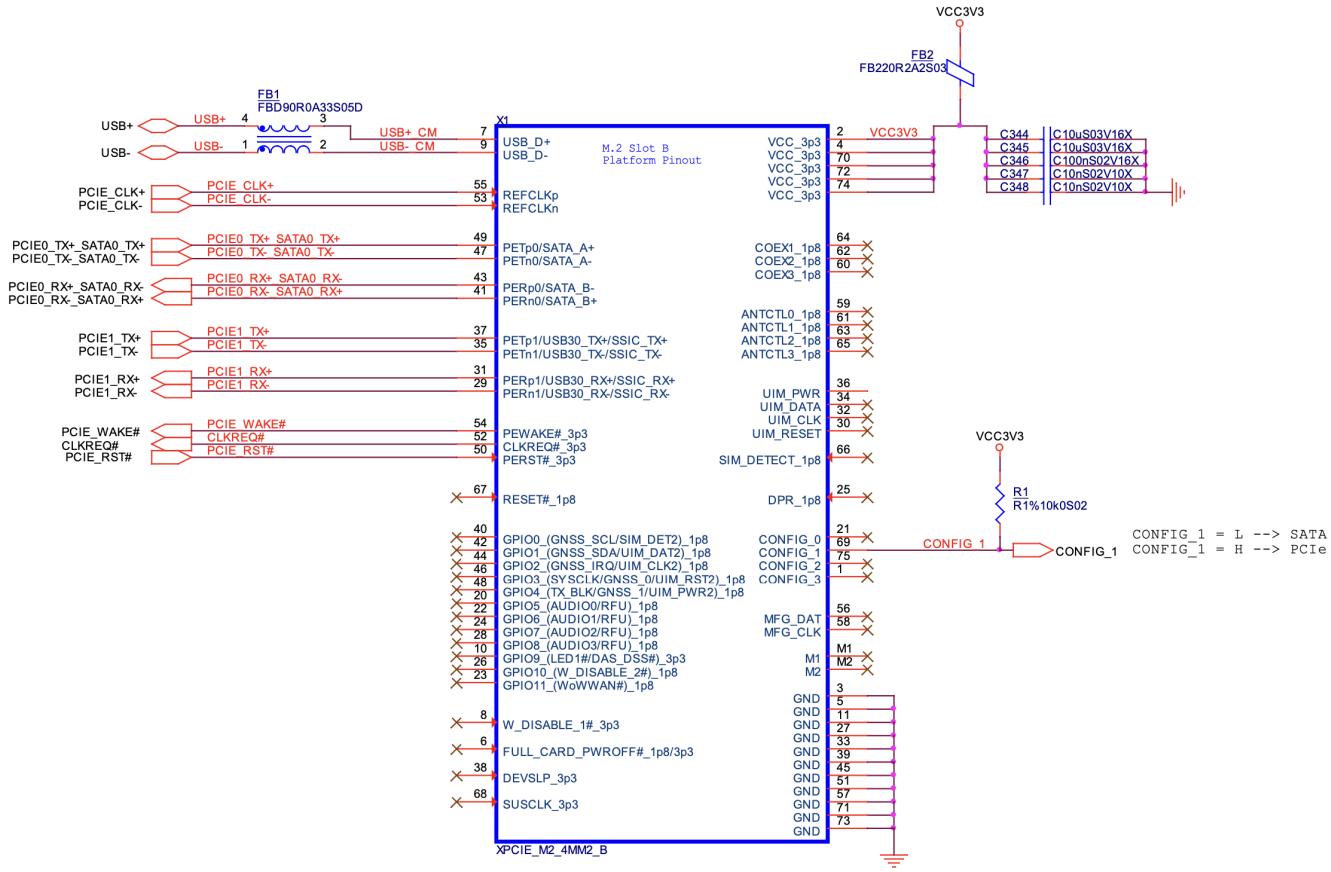
Pin id.	Upper	Lower	Description	Counterpoint	Voltage Level
6		M2B_PWROFF	Card PWR OFF	EX2.5	1.8/3.3
7	USB D+		USB data pair positive USB D+	USB D+	
8		W_DIS1	Wireless disable 1	EXB.3	
9	USB D-		USB data pair negative USB D-	USB D-	
10		DAS/DSS	Device Actvty Signal	LED / EX2.9	3.3V
11	GND		Ground (available?)		GND
12 - 19					
20		M2_I2S_CLK	GPIO5 M2_I2S_CLK	MIC I2S	1.8V
21	CONFIG_0			pad	
22		M2_I2S_DIN	GPIO6 M2_I2S_DIN	MIC I2S DATA0	1.8V
23	GPIO11		NC	MIC I2S MCLK	1.8V
24		M2_I2S_DOUT	GPIO7 M2_I2S_DOUT	PWM_OUT1	1.8V
25	DPR			pad	
26		GPIO10		EX2.10	1.8V
27	GND		Ground		GND
28		M2_I2S_WS	GPIO8 M2_I2S_WS	MIC I2S WS	1.8V
29	USB3 RX-		PER-1 / SSIC M2_USB3_SSRXN	M2_USB3_SSRX-	
30		SIM_RST	UIM RESET	-	
31	USB3 RX+		PER+1 / SSIC M2_USB3_SSRXP	M2_USB3_SSRX+	
32		SIM_CLK	UIM CLK	-	
33	GND		Ground		GND
34		SIM_DATA	UIM DATA	-	
35	USB3 TX-		PET-1 / SSIC M2_USB3_SSTX-	M2_USB3_SSTX-	
36		SIM_PWR	UIM PWR	-	

Pin id.	Upper	Lower	Description	Counterpoint	Voltage Level
37	USB3 TX+		PET+2 / SSIC M2_USB3_SSTX+	M2_USB3_SSTX+	
38		DEVSLP	Device Sleep, input. high=sleep	EX2.12	3.3V
39	GND		Ground		GND
40		M2 SMB SCL	SMB_CLK M2 SMB SCL	I2C3 SCL	1.8V
41	PCIE RXN-		PCIE RXN- / PER-0 / SATA-B+	PCIE RXN-	
42		M2 SMB SDA	SMB_DATA M2 SMB SDA	I2C3 SDA	1.8V
43	PCIE RXN+		PCIE RXN+ / PER+0 / SATA-B-	PCIE RXN+	1.8V
44		GPIO2	GPIO2 / ALERT	EX2.7	1.8V
45	GND		Ground		GND
46		GPIO3		PWM2_OUT	1.8V
47	PCIE TXN-		PCIE TXN- / PET-0 / SATA-A-	PCIE TXN-	1.8V
48		GPIO4		PWM3_OUT	1.8V
49	PCIE TXN+		PCIE TXN+ / PET-0 / SATA-A+	PCIE TXN+	1.8V
50		PERST	PCI Reset	mPCIe_PERST	
51	GND		Ground		GND
52		CLKREQ	Reference clock request	PCIE_CLKREQ_B	3.3V
53	PCIE REFCLK-		PCIE REFCLK-	REFCLK-	
54		WAKE	PCIe WAKE# Active Low.	USB1_SS_SEL	
55	PCIE REFCLK+		PCIE REFCLK+	REFCLK+	
56		MFG_DAT	SDA	SYS I2C SDA	
57	GND		Ground		
58		MFG_CLK	SCL	SYS I2C SCL	
59	ANTCTL0			ECSPI2_MISO	
60		COEX3		MIC I2S DATA3	
61	ANTCTL1			ECSPI2_SS0	
62		COEX_TXD		MIC I2S DATA2	1.8V

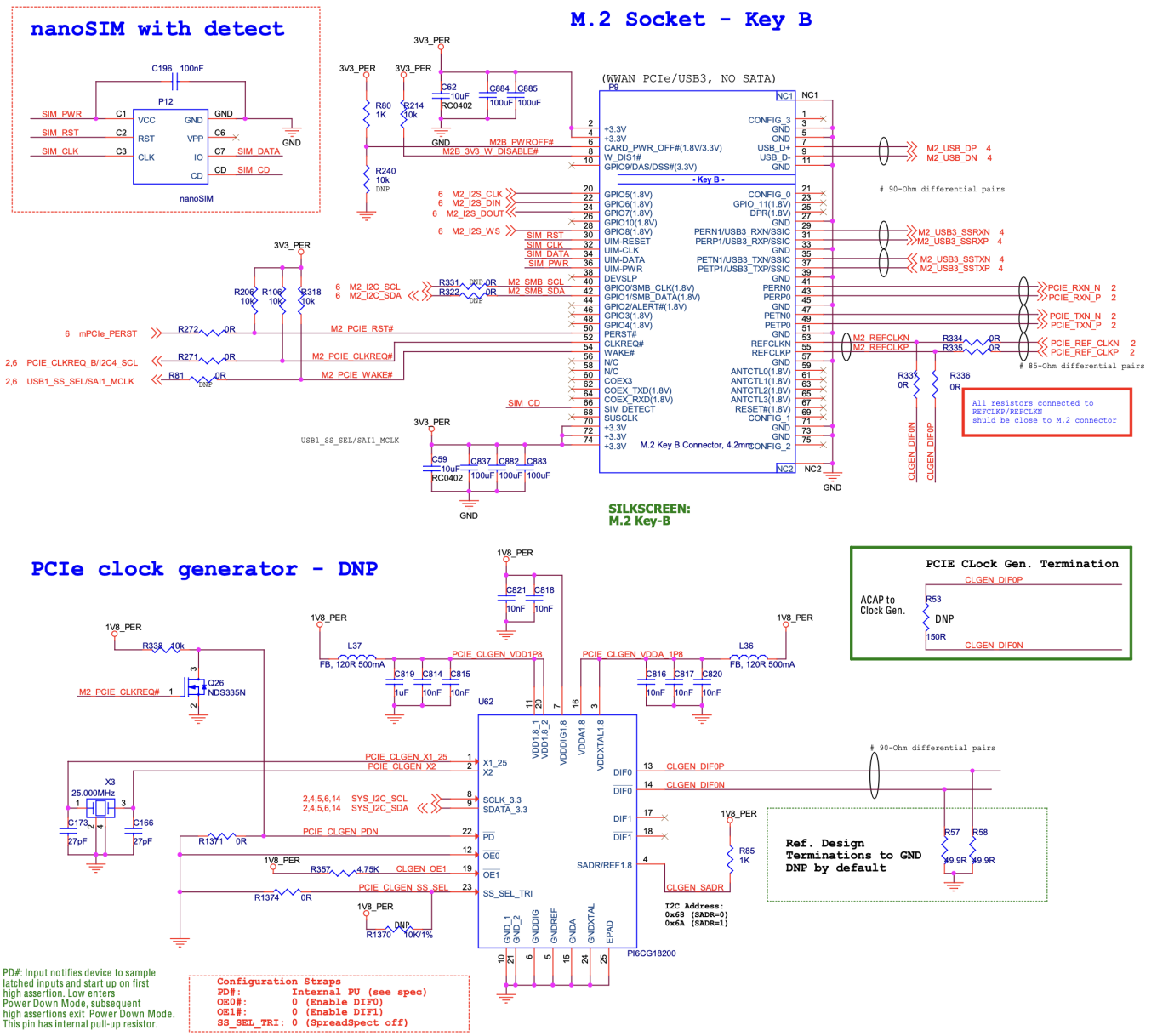
Pin id.	Upper	Lower	Description	Counterpoint	Voltage Level
63	ANTCTL2			ECSPI2_SCLK	
64		COEX_RXD		MIC I2S DATA1	1.8V
65	ANTCTL3			ECSPI2_MOSI	
66		SIM DETECT	SIM CD	-	
67	RESET#		RESET	EX2.6	1.8V
68		SUSCLK	32.768 kHz provided by Platform	-	
69	CONFIG_1		Defines module type +	EX2.14	
70		VRES	Power VRES		+3.3V
71	GND		Ground		GND
72		VRES	Power VRES		+3.3V
73	GND		Ground		GND
74		VRES	Power VRES		+3.3V
75	CONFIG_2		Defines Module Type NC		

Reference designs

3.2 Reference Design



Congatec reference design



Compulab reference design

M.2 Key E Expansion Module

Ziloo has an M.2 type E expansion port for Wireless/Bluetooth/GSM utility cards.

Features:

- UART2, UART4
- USB2/USB3 OTG data
- SD1 SDIO 4bit
- PCIe single lane reserved pins
- JTAG + debugging pins reserved (lay out pads)
- Speaker I2S
- Two LEDs next to connector
- SIM pins are not connected, reserved for now

Control pins mapped by I/O Expander

USB2_SS_SEL is a direct pin on the SoM.

TODO consider bootup default state of I/O Expanders. USB must not connect M.2 by default

TODO unallocated/GPIO pins from chipsets

A dedicated I/O Expander controls addition pins on Key E.

The development board uses a single Expander. The 909 and 801 uses 3x PCA9555 to control more states.

The EX1 expander input triggers interrupt via EX_O_nINT (GPIO1_IO1). The pins relate to USB1 Host and M.2 Key E.

The EX1 expander allows controlling T-USB maps,

Expander	Connected to
EX1.0	USB_O_ALT_EN
EX1.1	USB_O_ALT_POL
EX1.2	USB_O_ALT_AMSEL
EX1.3	MUX_USB2_SEL
EX1.4	MUX_USB3_SEL
EX1.5	COEX4
EX1.6	DEV_WLAN_WAKE
EX1.7	ALERT / I2C_IRQ
EX1.8	GPIO3 on 65988 (HPD1)
EX1.9	LED / DAS / DSS
EX1.10	W_DISABLE2#
EX1.11	W_DISABLE1#
EX1.12	UART WAKE
EX1.13	SDIO WAKE
EX1.14	LED2#
EX1.15	

M.2 Key E Pin allocations

Pin id.	Upper	Lower	Description	Counterpoint	Voltage Level
1	GND		Ground		

Pin id.	Upper	Lower	Description	Counterpoint	Voltage Level
2		+3.3V	3.3 V power supply from main board		3.3V
3	USB D+		USB data pair positive	USB D+	
4		+3.3V	3.3 V power supply from main board		3.3V
5	USB D-		USB data pair negative	USB D-	
6		M2B_PWROFF	Card PWR OFF	EX2.5	1.8/3.3
7	GND		Ground		GND
8		M2_I2S_CLK	GPIO5 M2_I2S_CLK	MIC I2S	1.8V
9	SDIO CLK		SDIO	SD1 CLK	1.8V
10		M2_I2S_WS	GPIO8 M2_I2S_WS	MIC I2S WS	1.8V
11	SDIO CMD		SDIO	SD1 CMD	1.8V
12		M2_I2S_DIN	GPIO6 M2_I2S_DIN SAI5	MIC I2S DATA0	1.8V
13	SDIO DATA0		SDIO	SD1 DATA0	1.8V
14		M2_I2S_DOUT	GPIO7 M2_I2S_DOUT SAI5	SAI5 TX DATA0	1.8V
15	SDIO DATA1		SDIO	SD1 DATA1	1.8V
16		LED2#			
17	SDIO DATA2		SDIO	SD1 DATA2	1.8V
18		GND	Ground		GND
19	SDIO DATA3		SDIO	SD1 DATA3	1.8V
20		UART WAKE#	Bluetooth uses to wake up platform	EX1.12	3.3V
21	SDIO WAKE#		WiFi uses to wake up platform	EX1.13	1.8V
22		UART RxD		UART2_RXD	1.8V
23	SDIO RESET#		Signal to independently reset WiFi	SD1_RESET_B	1.8V
24 - 31					

Pin id.	Upper	Lower	Description	Counterpoint	Voltage Level
32		UART TxD		UART2_TXD	1.8V
33	GND		Ground		GND
34		UART CTS		UART4_RXD	1.8V
35	PCIE TXN-		PCIE TXN- / PET-0 / SATA-A-	-	1.8V
36		UART RTS		UART4_TXD	1.8V
37	PCIE TXN+		PCIE TXN+ / PET-0 / SATA-A+	-	1.8V
38		JTAG_TDO	Debugging		1.8V
39	GND		Ground		GND
40		COEX4	Wake up the WiFi	EX1.5	1.8V
41	PCIE RXN-		PCIE RXN- / PER-0 / SATA-B+	-	
42		DEV_BT_WAKE	Wake up the Bluetooth	EX1.6	1.8V
43	PCIE RXN+		PCIE RXN+ / PER+0 / SATA-B-	-	1.8V
44		JTAG_TDI	Debugging		1.8V
45	GND		Ground		GND
46		JTAG_TCK	Debugging		1.8V
47	PCIE REFCLK+		PCIE REFCLK+	-	
48		JTAG_TMS	Debugging		1.8V
49	PCIE REFCLK-		PCIE REFCLK-	-	
50		SUSCLK	32.768 kHz provided by Platform	-	
51	GND		Ground		GND
52		PERST0#	PCI Reset	-	
53	CLKREQ0#		Reference clock request	-	3.3V
54		W_DISABLE2#	Independently reset the Bluetooth	EX1.10	1.8V
55	PE WAKE#		PCIe uses to wake up platform	-	1.8V

Pin id.	Upper	Lower	Description	Counterpoint	Voltage Level
56		W_DISABLE1#	Full power down Bluetooth + WiFi	EX1.11	1.8V
57	GND		Ground		GND
58		I2C_DATA	I2C DATA	I2C3 SDA	1.8V
59	USB3 TX+		PET+1 / SSIC M2_USB3_SSTX+	M2_USB3_SSTX+	
60		I2C_CLK	I2C CLK	I2C3 SCL	1.8V
61	USB3 TX-		PET-1 / SSIC M2_USB3_SSTX-	M2_USB3_SSTX-	
62		ALERT#		EX1.7	1.8V
63	GND		Ground		GND
64		Reserved			
65	USB3 RX+		PER+1 / SSIC M2_USB3_SSRXP	M2_USB3_SSRX+	
66		SIM_SWP	UIM SWP	-	
67	USB3 RX-		PER-1 / SSIC M2_USB3_SSRXN	M2_USB3_SSRX-	
68		SIM_PWR	UIM PWR	-	
69	GND		Ground		GND
70		SIM_PWR	UIM PWR / PEWAKE1#	-	
71	REFCLK+1			-	
72		VRES	Power VRES		+3.3V
73	Reserved				
74		VRES	Power VRES		+3.3V
75	GND		Ground		GND

Reference designs

2.2 Reference Design

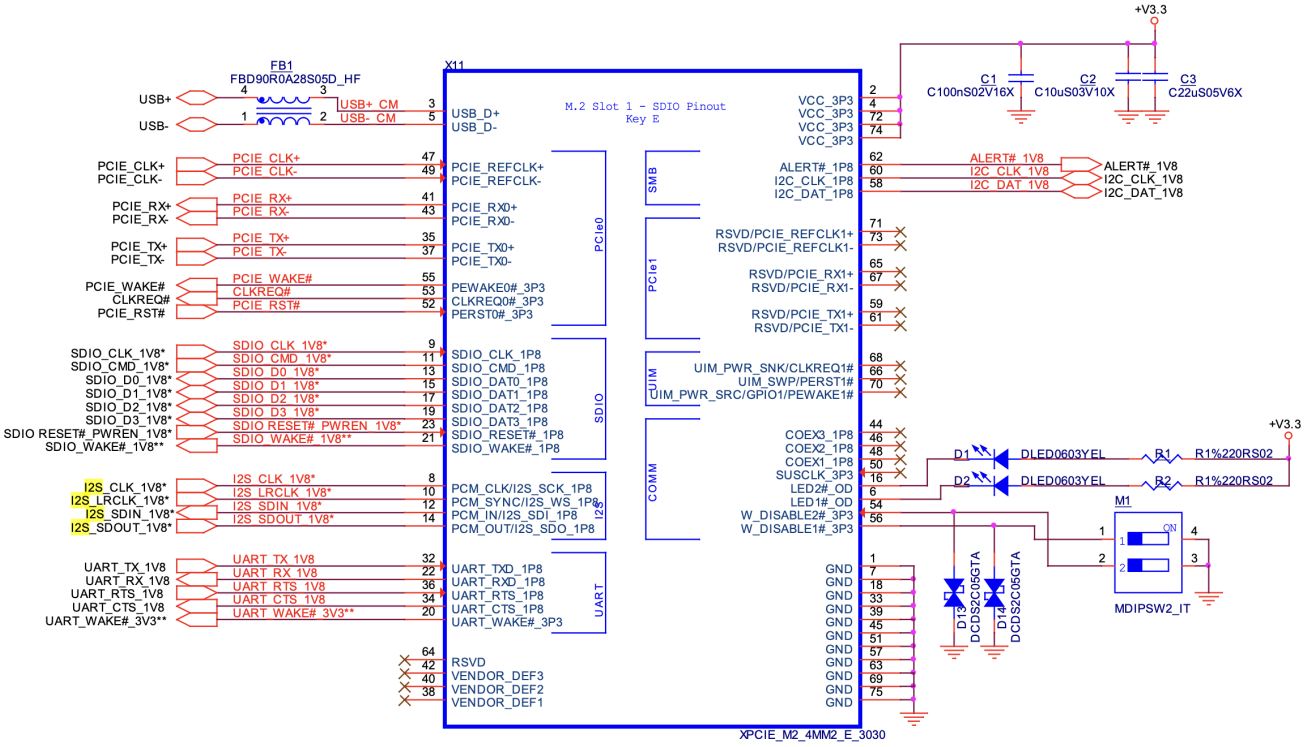


Figure 1: Socket 1 - Key E Reference Design

Congatec reference design

Future Expansion connection

UIM / SIM / eSIM

M.2 Connectors have pins reserved for SIM (UIM) cards. A connector or eSIM may be added in the future.

i.MX 8 only provides PCIe x1 so Key M is not relevant. This leaves A, B and E.

- B is good for USB3, Audio, SATA
- E is good for SDIO, UART and PCM
- ATP M.2 key info page
- Congatec AN43